2.25 MHz 400-mA Step Down Converter With Selectable VOUT

FEATURES

- **High Efficiency Step Down Converter**
- **Output Current up to 400 mA**
- **V_{IN} Range From 2V to 6V for Li-Ion Batteries With Extended Voltage Range**
- **2.25 MHz Fixed Frequency Operation**
- **Pin-Selectable Fixed Output Voltage**
- **Power Save Mode for Highest Efficiency**
- **Automatic transition between PFM and PWM Mode**
- **Voltage Positioning in PFM Mode**
- **Typical 15-µA Quiescent Current**
- **100% Duty Cycle for Lowest Dropout**
- **Available in 2×2×0,8 mm SON Package**
- **Allows <1 mm Solution Height**

APPLICATIONS

- **Low Power Processor Supply**
- **Cell Phones, Smart-phones**
- **Navigation Systems**
- **Low Power DSP Supply**
- **Portable Media Players**
- **Digital Cameras**

DESCRIPTION

The TPS62270 device is a high efficiency synchronous step down DC-DC converter optimized for battery powered portable applications. It provides up to 400 mA output current from a single Li-Ion cell.

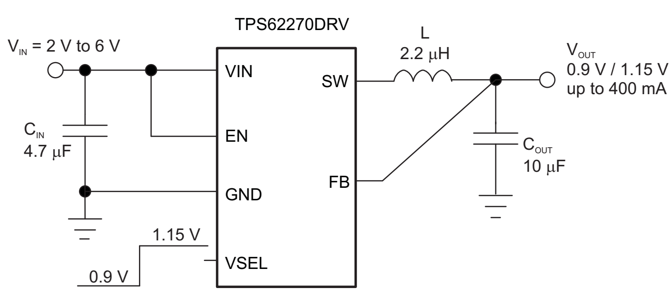
With an input voltage range of 2 V to 6 V the device supports Li-Ion batteries with extended voltage range, and is ideal to power portable applications like mobile phones and other portable equipment.

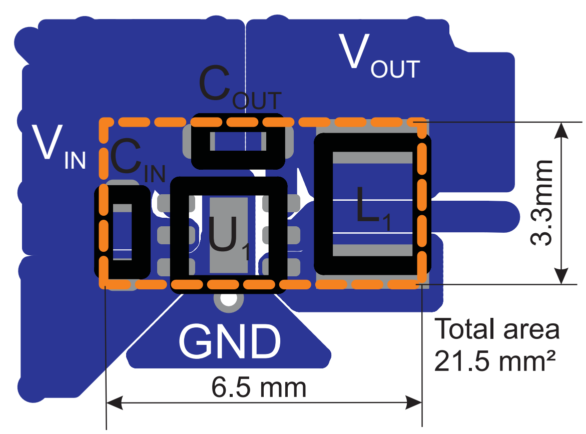
The TPS62270 operates at 2.25 MHz fixed switching frequency and enters Power Save Mode operation at light load currents to maintain high efficiency over the entire load current range. The Power Save Mode is optimized for low output voltage ripple.

With the VSEL pin, two different fixed output voltages can be selected. This function features a dynamic voltage scaling for low power processor cores.

In the shutdown mode, the current consumption is reduced to less than 1µA. TPS62270 allows the use of small inductors and capacitors to achieve a small solution size.

The TPS62270 is available in a 2 mm × 2 mm, 6-pin SON package.





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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

T_A	PART NUMBER(1)	OUTPUT VOLTAGE(2)		PACKAGE DESIGNATOR	ORDERING(1)	PACKAGE MARKING
		VSEL = 1	VSEL = 0			
–40°C to 85°C	TPS62270	1.15 V	0.9 V	DRV	TPS62270DRV	CCX
	TPS62272	3.3V	2.1V	DRV	TPS62272DRV	OAM
	TPS62273	3.3V	2.5V	DRV	TPS62273DRV	CGW

(1) The DRV (SON2x2) package is available in tape on reel. Add R suffix to order quantities of 3000 parts per reel, add T suffix to order quantities of 250 parts per reel.
(2) contact TI for other fixed output voltage options.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

			VALUE	UNIT
	Input voltage range(2)		–0.3 to 7	V
	Voltage range at EN, VSEL		–0.3 to VIN +0.3, ≤7	V
	Voltage on SW		–0.3 to 7	V
	Peak output current		Internally limited	A
	ESD rating(3)	HBM Human body model	2	kV
		CDM Charge device model	1	
		Machine model	200	V
T_J	Maximum operating junction temperature		–40 to 125	°C
T_{stg}	Storage temperature range		–65 to 150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) The human body model is a 100 pF capacitor discharged through a 1.5kΩ resistor into each pin. The machine model is a 200 pF capacitor discharged directly into each pin.

DISSIPATION RATINGS

PACKAGE	$R_{\theta JA}$	POWER RATING FOR T_A ≤ 25°C	DERATING FACTOR ABOVE T_A = 25°C
DRV	76°C/W	1300 mW	13 mW/°C

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Supply Voltage	2		6	V
T_A	Operating ambient temperature	–40		85	°C
T_J	Operating junction temperature	–40		125	°C

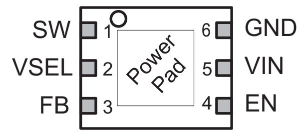
ELECTRICAL CHARACTERISTICS

Over full operating ambient temperature range, typical values are at T_A = 25°C. Unless otherwise noted, specifications apply for condition V_{IN} = EN = 3.6V. External components C_{IN} = 4.7µF 0603, C_{OUT} = 10µF 0603, L = 2µH, see the parameter measurement information.

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY								
V_{IN}	Input voltage range				2		6	V
I_{OUT}	Output current		2.5 V ≤ V_{IN} ≤ 6 V				400	mA
			2 V ≤ V_{IN} ≤ 2.5 V				150	
I_Q	Operating quiescent current		I_{OUT} = 0 mA, device not switching			15		µA
			I_{OUT} = 0 mA, device switching with no load, V_{OUT} = 1.15V			18		
I_{SD}	Shutdown current		EN = GND			0.1	1	µA
UVLO	Undervoltage lockout threshold		Falling			1.85		V
			Rising			1.95		
ENABLE, VSEL								
V_{IH}	High level input voltage, EN, VSEL		2 V ≤ V_{IN} ≤ 6 V		1		V_{IN}	V
V_{IL}	Low Level Input Voltage, EN, VSEL		2 V ≤ V_{IN} ≤ 6 V		0		0.4	V
I_{IN}	Input bias Current, EN, VSEL		EN, VSEL = GND or VIN			0.01	1.0	µA
POWER SWITCH								
$R_{DS(on)}$	High side MOSFET on-resistance		V_{IN} = V_{GS} = 3.6V, T_A = 25°C			240	480	mΩ
	Low side MOSFET on-resistance		V_{IN} = V_{GS} = 3.6V, T_A = 25°C			180	380	mΩ
I_{LIMF}	Forward current limit MOSFET high-side and low side		V_{IN} = V_{GS} = 3.6 V		0.56	0.7	0.84	A
T_{SD}	Thermal shutdown		Increasing junction temperature			140		°C
	Thermal shutdown hysteresis		Decreasing junction temperature			20		
OSCILLATOR								
f_{SW}	Oscillator frequency		2 V ≤ V_{IN} ≤ 6 V		2	2.25	2.5	MHz
OUTPUT								
V_{OUT}	Output voltage PWM	TPS62270	PWM operation, 2 V ≤ V_{IN} ≤ 6 V, FB pin connected to V_{OUT} (1)	VSEL = 1	1.13	1.15	1.167	V
				VSEL = 0	0.886	0.9	0.914	
		TPS62272	PWM operation, 2 V ≤ V_{IN} ≤ 6 V, FB pin connected to V_{OUT} (1)	VSEL = 1	3.23	3.3	3.37	
				VSEL = 0	2.06	2.1	2.14	
		TPS62273	PWM operation, FB pin connected to V_{OUT} (1)	VSEL = 1	3.23	3.3	3.37	
				VSEL = 0	2.45	2.5	2.55	
V_{OUT}	Output voltage in PFM mode, voltage positioning		TPS62270	VSEL = 1		1.16		V
				VSEL = 0		0.91		
			TS62272	VSEL = 1		3.34		
				VSEL = 0		2.12		
			TPS62273	VSEL = 1		3.34		
				VSEL = 0		2.53		
t_{Start}	Start-up time		Time from active EN to reach 95% of V_{OUT}			500		µs
t_{Ramp}	V_{OUT} ramp up time		Time to ramp from 5% to 95% of V_{OUT}			250		µs
I_{lkg}	Leakage Current into SW pin		V_{IN} = 3.6 V, V_{IN} = V_{OUT} = V_{SW}, EN = GND (2)			0.1	1	µA

(1) For V_{IN} = V_{OUT} + 0.6 V
(2) In fixed output voltage versions, the internal resistor divider network is disconnected from FB pin.

PIN ASSIGNMENTS

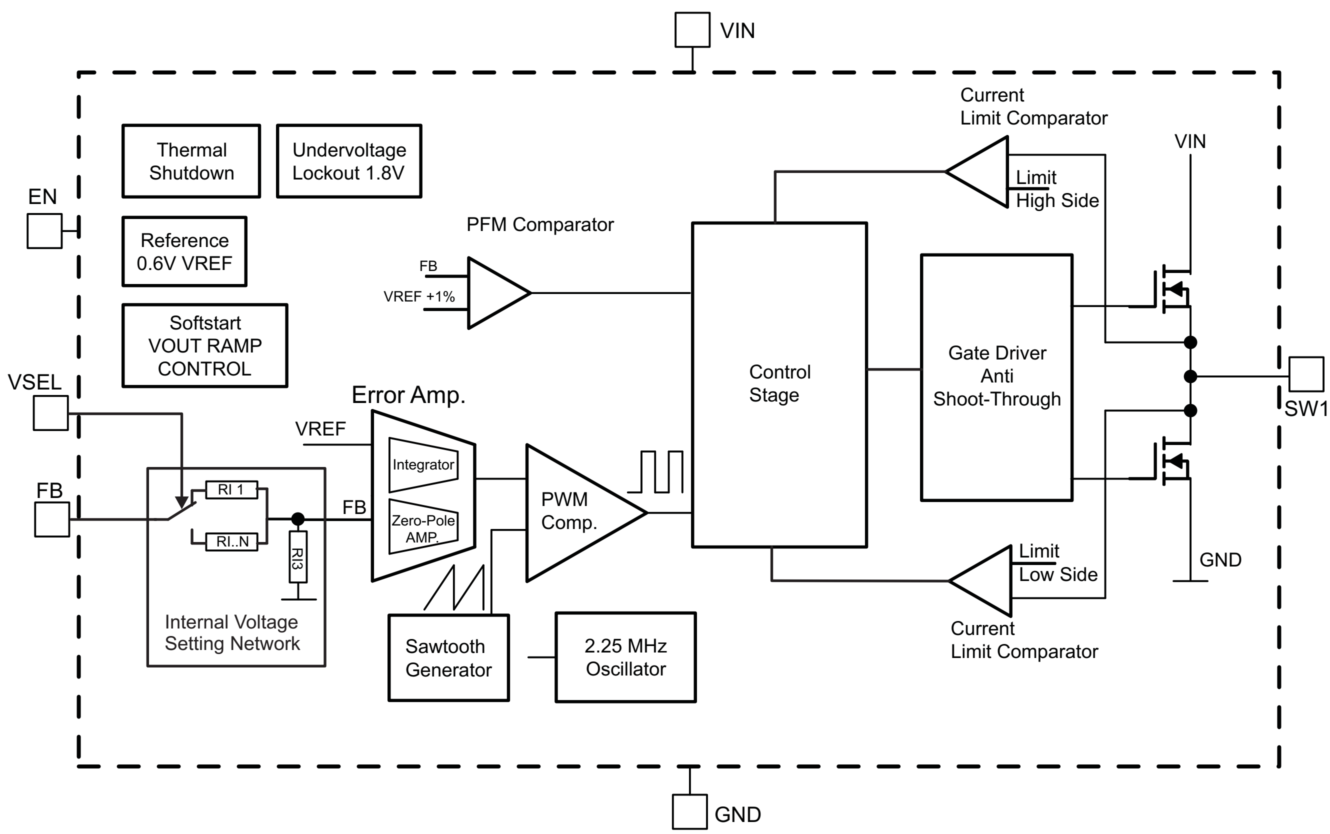


Top view DRV package

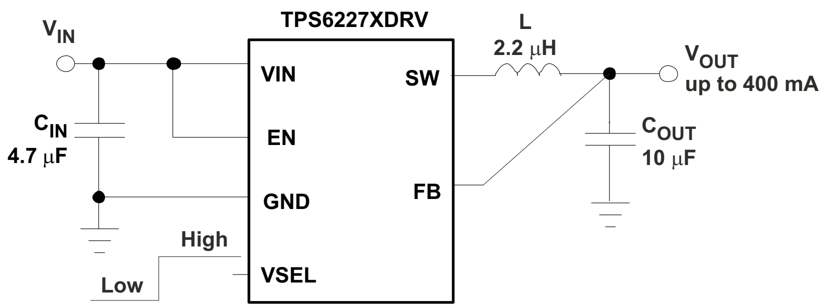
TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO. (SON)		
V_{IN}	5	PWR	VIN power supply pin.
GND	6	PWR	GND supply pin
EN	4	I	This is the enable pin of the device. Pulling this pin to low forces the device into shutdown mode. Pulling this pin to high enables the device. This pin must be terminated.
SW	1	OUT	This is the switch pin and is connected to the internal MOSFET switches. Connect the inductor to this terminal
FB	3	I	Feedback Pin for the internal regulation loop. Connect the external resistor divider to this pin. In case of fixed output voltage option, connect this pin directly to the output capacitor
VSEL	2	I	Voltage Select input. Please refer to table ordering information for available output voltage selections.

FUNCTIONAL BLOCK DIAGRAM



PARAMETER MEASUREMENT INFORMATION



L: MIPSA2520D2R2 2.0 µH
C_{IN}: GRM188R60J106M 4.7 µF
C_{OUT}: GRM188R60J106M 10 µF

TYPICAL CHARACTERISTICS

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Static Drain Source On-state Resistance	vs Input Voltage	Figure 22
Static Drain Source On-state Resistance	vs Input Voltage	Figure 23

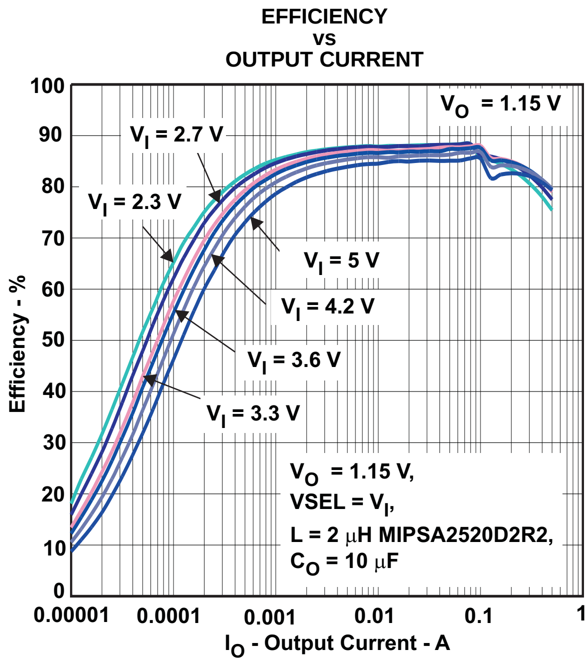

Figure 1.

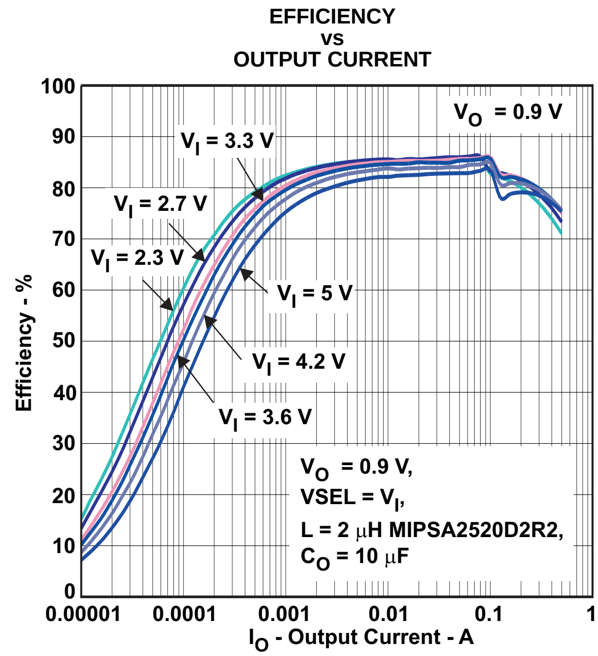

Figure 2.

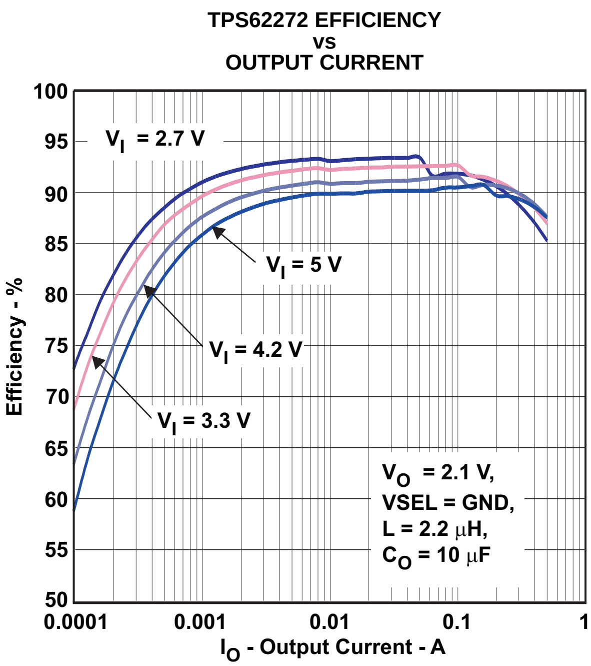

Figure 3.

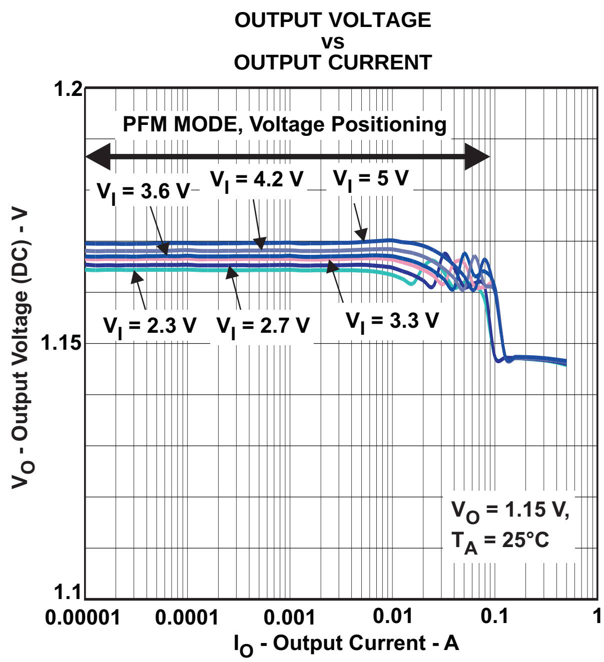

Figure 4.

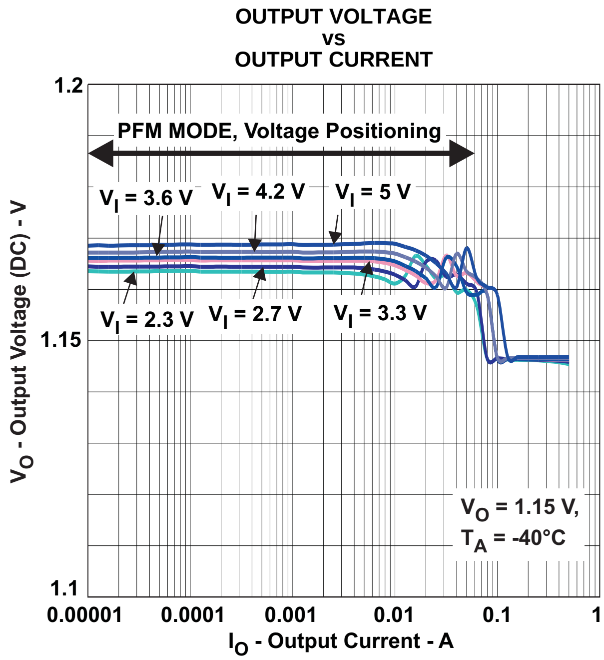

Figure 5.

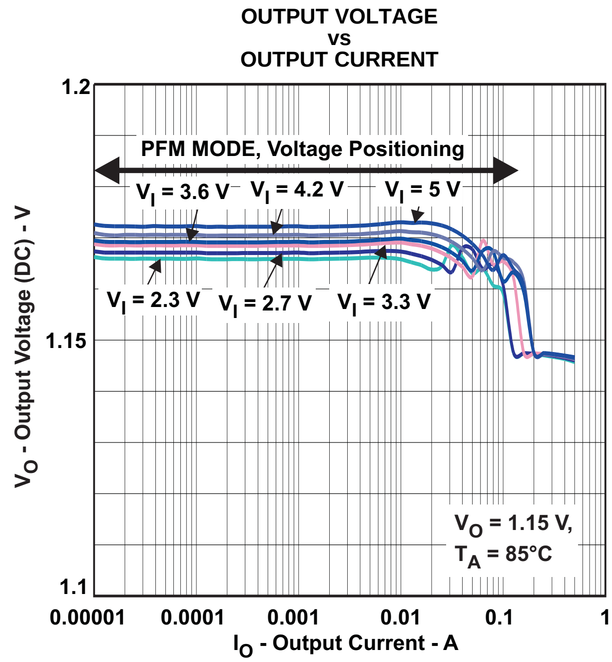

Figure 6.

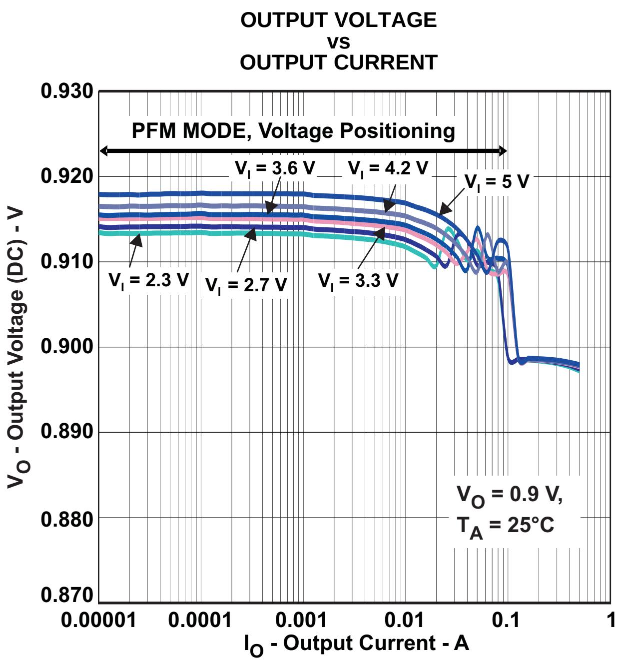

Figure 7.

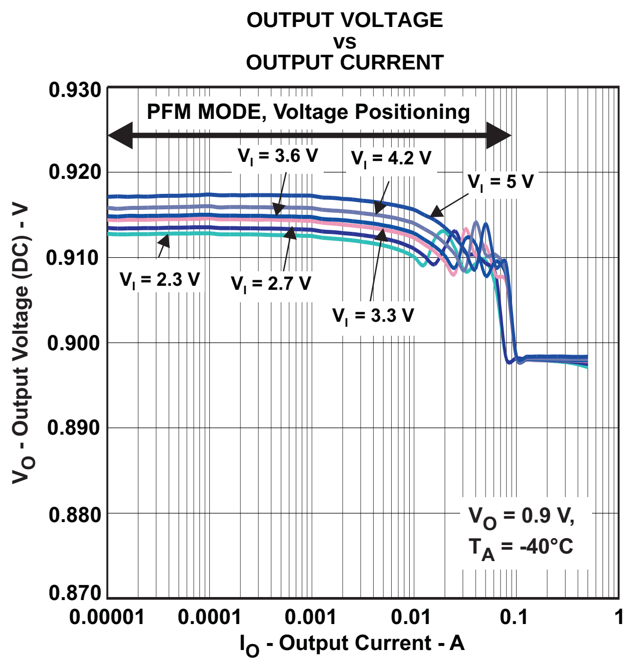

Figure 8.

OUTPUT VOLTAGE
vs
OUTPUT CURRENT

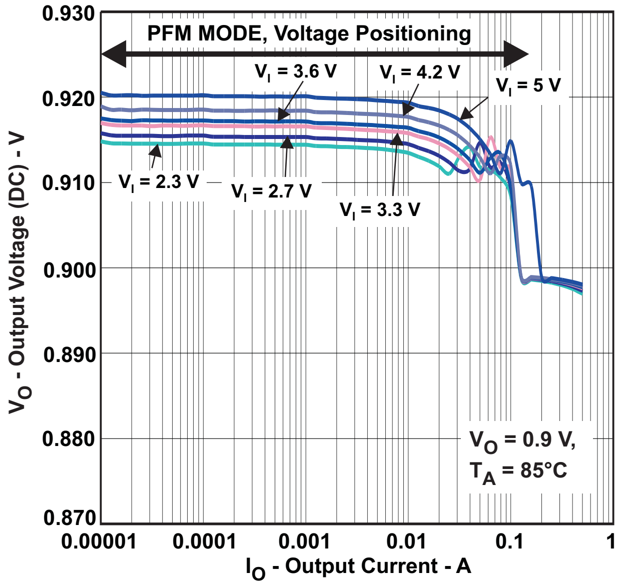

Figure 9.

PWM MODE OPERATION

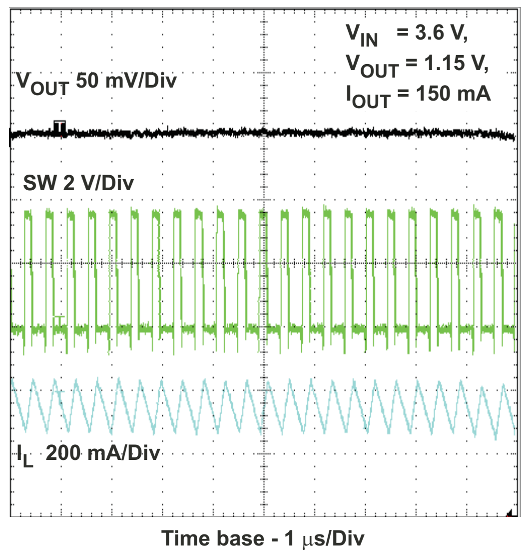

Figure 10.

PFM MODE OPERATION

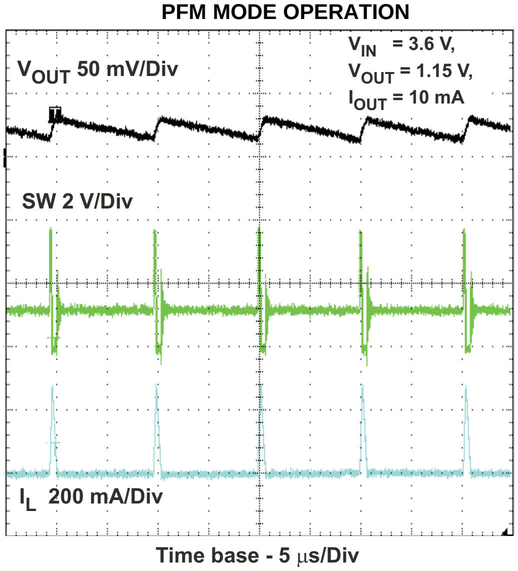

Figure 11.

LOAD TRANSIENT RESPONSE PFM MODE

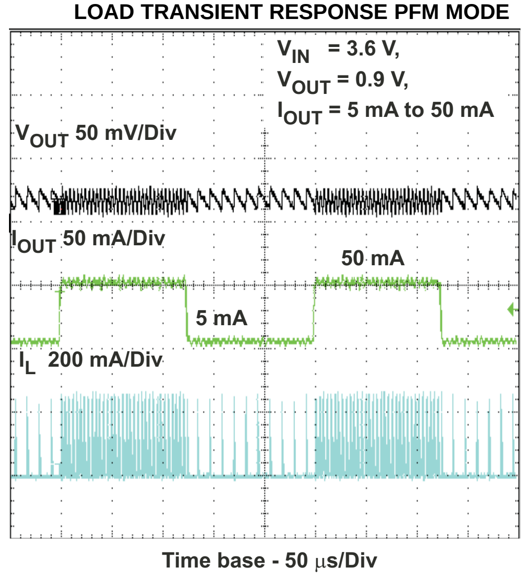

Figure 12.

LOAD TRANSIENT RESPONSE PFM/PWM MODE

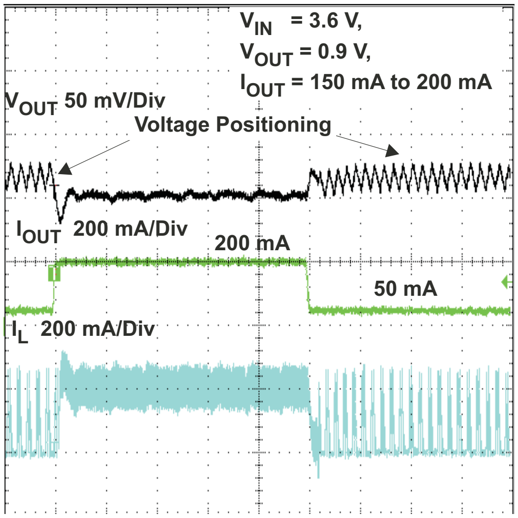

Figure 13.

LOAD TRANSIENT RESPONSE PFM/PWM MODE

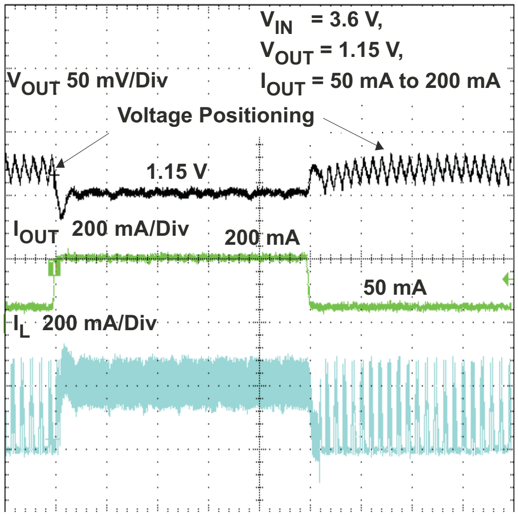

Figure 14.

VSEL OUTPUT VOLTAGE RESPONSE

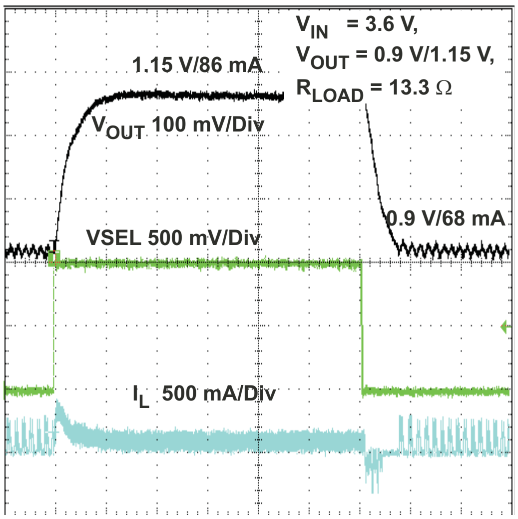

Figure 15.

STARTUP IN 10 Ω LOAD
AT 1.15 V OUTPUT VOLTAGE

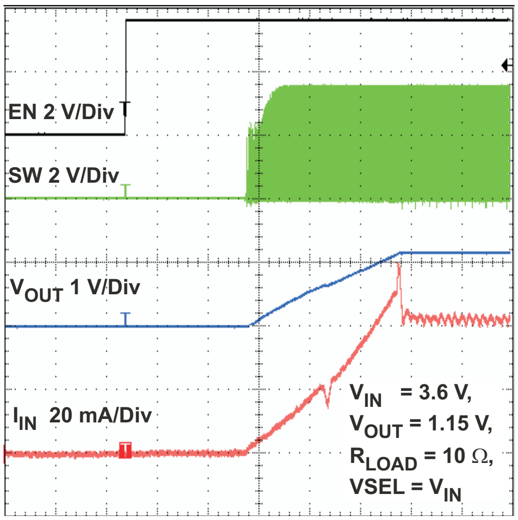

Figure 16.

STARTUP IN 100 Ω LOAD
AT 0.9 V OUTPUT VOLTAGE

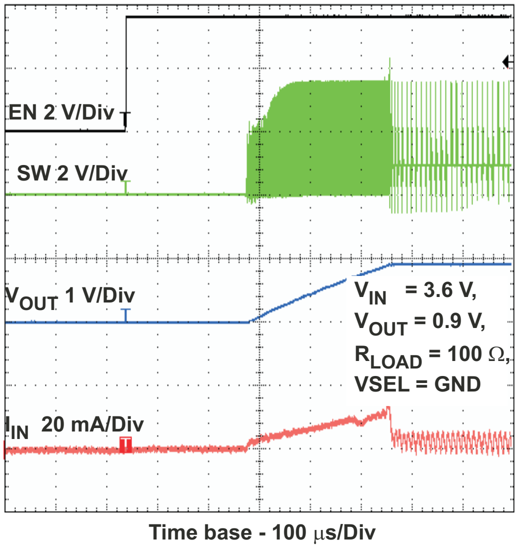

Figure 17.

STARTUP IN 220 Ω LOAD
AT 2.1 V OUTPUT VOLTAGE

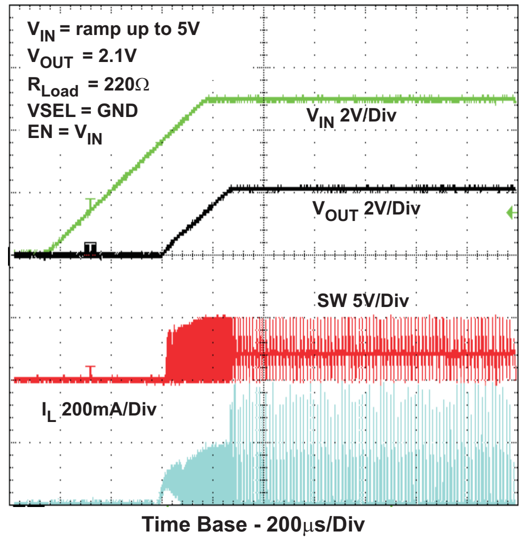

Figure 18.

STARTUP IN 220 Ω LOAD
AT 3.3 V OUTPUT VOLTAGE

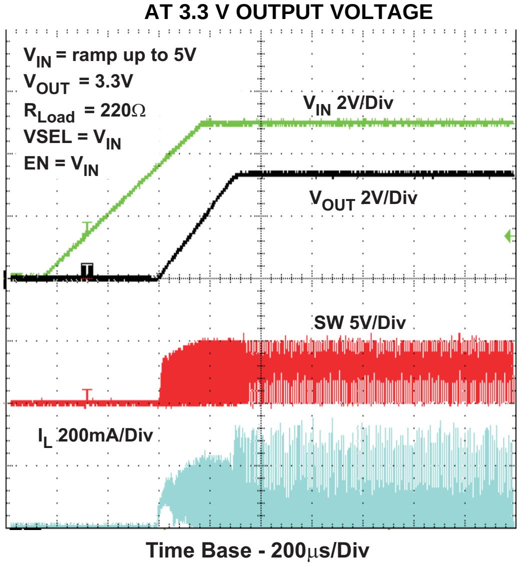

Figure 19.

QUIESCENT CURRENT
vs
INPUT VOLTAGE

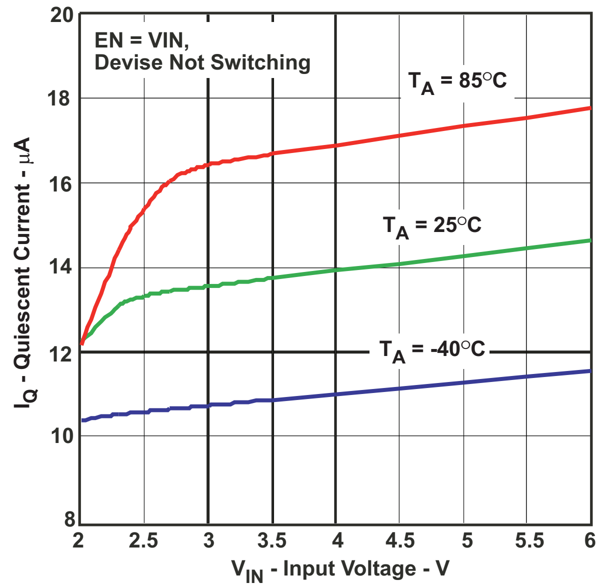

Figure 20.

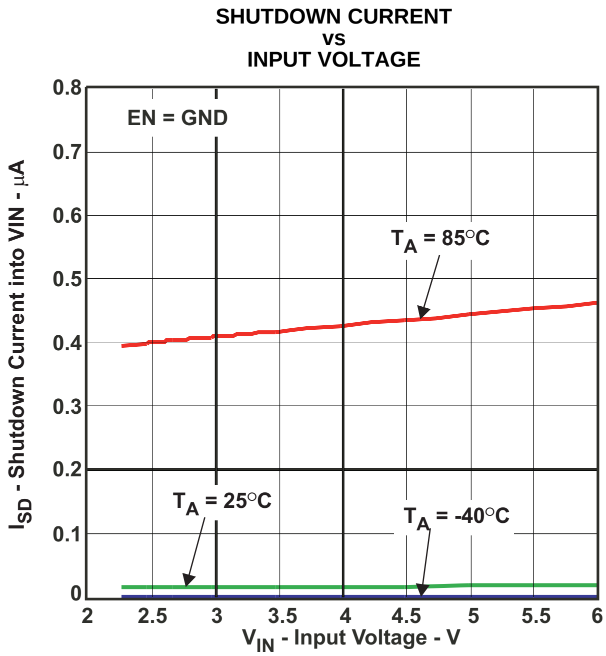

Figure 21.

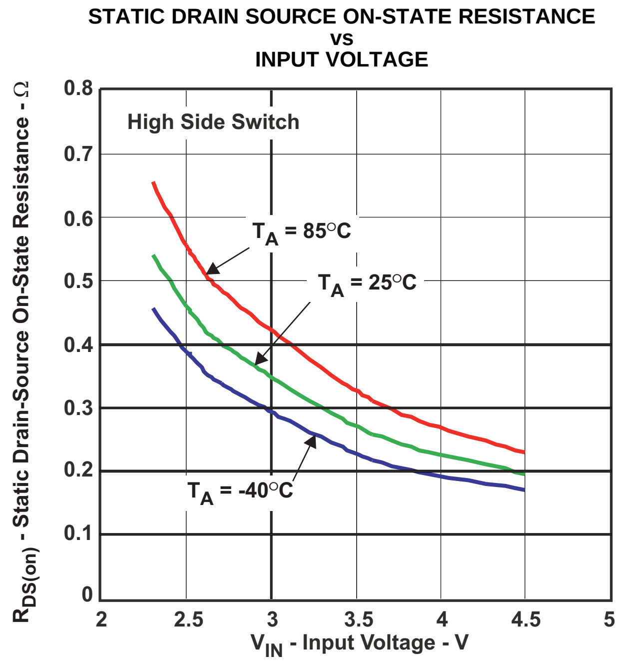

Figure 22.

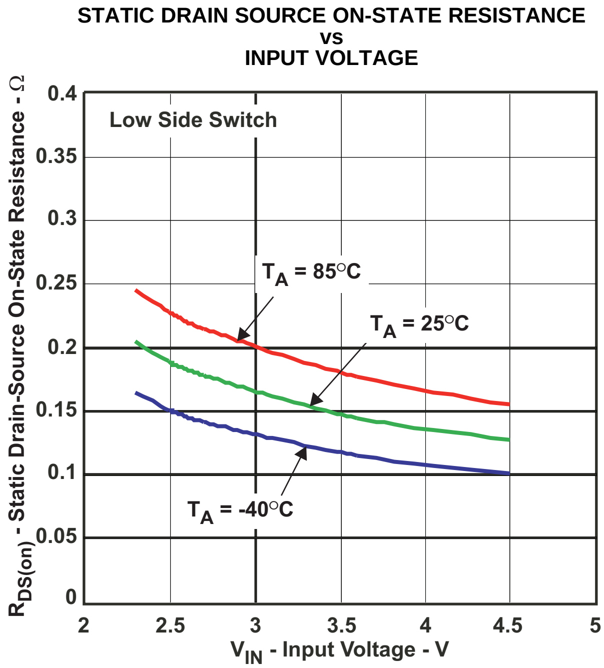

Figure 23.

DETAILED DESCRIPTION

OPERATION

The TPS62270 step down converter operates with typically 2.25 MHz fixed frequency pulse width modulation (PWM) at moderate to heavy load currents. At light load currents the converter automatically enters Power Save Mode and operates then in PFM mode.

During PWM operation the converter use a unique fast response voltage mode controller scheme with input voltage feed-forward to achieve good line and load regulation allowing the use of small ceramic input and output capacitors. At the beginning of each clock cycle initiated by the clock signal, the High Side MOSFET switch is turned on. The current flows now from the input capacitor via the High Side MOSFET switch through the inductor to the output capacitor and load. During this phase, the current ramps up until the PWM comparator trips and the control logic will turn off the switch. The current limit comparator will also turn off the switch in case the current limit of the High Side MOSFET switch is exceeded. After a dead time preventing shoot through current, the Low Side MOSFET rectifier is turned on and the inductor current will ramp down. The current flows now from the inductor to the output capacitor and to the load. It returns back to the inductor through the Low Side MOSFET rectifier.

The next cycle will be initiated by the clock signal again turning off the Low Side MOSFET rectifier and turning on the on the High Side MOSFET switch.

Power Save Mode

If the load current decreases, the converter will enter Power Save Mode operation automatically. During Power Save Mode the converter skips switching and operates with reduced frequency in PFM mode with a minimum quiescent current to maintain high efficiency.

The transition from PWM mode to PFM mode occurs once the inductor current in the Low Side MOSFET switch becomes zero, which indicates discontinuous conduction mode.

During the Power Save Mode the output voltage is monitored with a PFM comparator. As the output voltage falls below the PFM comparator threshold of VOUT +1%, the device starts a PFM current pulse. For this the High Side MOSFET switch will turn on and the inductor current ramps up. After the On-time expires the switch will be turned off and the Low Side MOSFET switch will be turned on until the inductor current becomes zero.

The converter effectively delivers a current to the output capacitor and the load. If the load is below the delivered current the output voltage will rise. If the output voltage is equal or higher than the PFM comparator threshold, the device stops switching and enters a sleep mode with typical 15µA current consumption.

In case the output voltage is still below the PFM comparator threshold, further PFM current pulses will be generated until the PFM comparator threshold is reached. The converter starts switching again once the output voltage drops below the PFM comparator threshold.

With a fast single threshold comparator, the output voltage ripple during PFM mode operation can be kept very small. The PFM Pulse is timing controlled, which allows to modify the charge transferred to the output capacitor by the value of the inductor. The resulting PFM output voltage ripple depends in first order on the size of the output capacitor and the inductor value. Increasing output capacitor values and/or inductor values will minimize the output ripple.

The PFM mode is left and PWM mode entered in case the output current can not longer be supported in PFM mode.

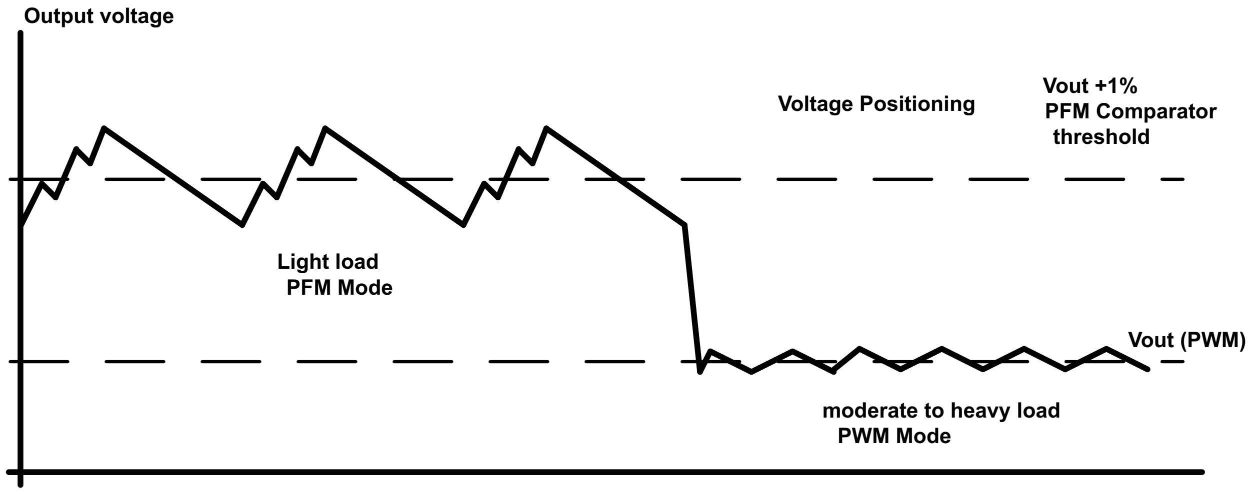

Figure 24. Power Save Mode

100% Duty Cycle Low Dropout Operation

The device starts to enter 100% duty cycle Mode once the input voltage comes close the nominal output voltage. In order to maintain the output voltage, the High Side MOSFET switch is turned on 100% for one or more cycles.

With further decreasing VIN the High Side MOSFET switch is turned on completely. In this case the converter offers a low input-to-output voltage difference. This is particularly useful in battery-powered applications to achieve longest operation time by taking full advantage of the whole battery voltage range.

The minimum input voltage to maintain regulation depends on the load current and output voltage, and can be calculated as:

$$Vin_{min} = Vout_{max} + Iout_{max} \times (R_{DS(on)}max + R_L)$$

With

$Iout_{max}$ = maximum output current plus inductor ripple current

$R_{DS(on)}max$ = maximum P-channel switch $R_{DS(on)}$.

R_L = DC resistance of the inductor

$Vout_{max}$ = nominal output voltage plus maximum output voltage tolerance

Undervoltage Lockout

The undervoltage lockout circuit prevents the device from malfunctioning at low input voltages and from excessive discharge of the battery and disables the output stage of the converter. The undervoltage lockout threshold is typically 1.85V with falling V_{IN}.

Output Voltage Selection VSEL

The VSEL pin features output voltage selection. The output voltages are set with an internal high precision feedback divider network. No further external components for output voltage setting or compensation are required. This features smallest solution size.

Connecting the VSEL pin to an external logic control signal allows simple dynamic voltage scaling for low power processors cores. During operation of the device, the output voltage can be changed with VSEL pin.

This allows setting the core voltage of an processor according to its operating mode and helps to optimize power consumption. Table 1 shows an overview of the selectable output voltages.

Table 1. VSEL Output Voltage Selection

DEVICE	OUTPUT VOLTAGE VOUT	
	VSEL = low	VSEL = high
TPS62270	0.9 V	1.15 V
TPS62272	2.1V	3.3V
TPS62273	2.5V	3.3V

Enable

The device is enabled setting EN pin to high. During the start up time $t_{Start\ up}$ the internal circuits are settled. Afterwards the device activates the soft start circuit. The EN input can be used to control power sequencing in a system with various DC/DC converters. The EN pin can be connected to the output of another converter, to drive the EN pin high and getting a sequencing of supply rails.

Soft Start

The TPS62270 has an internal soft start circuit that controls the ramp up of the output voltage. The output voltage ramps up from 5% to 95% of its nominal value within typ. 250µs. This limits the inrush current in the converter during start up and prevents possible input voltage drops when a battery or high impedance power source is used. The Soft start circuit is enabled after the start up time $t_{Start\ up}$ has expired.

Short-Circuit Protection

The High Side and Low Side MOSFET switches are short-circuit protected with maximum output current = I_{LIMF}. Once the High Side MOSFET switch reaches its current limit, it is turned off and the Low Side MOSFET switch is turned on. The High Side MOSFET switch can only turn on again, once the current in the Low Side MOSFET switch decreases below its current limit.

Thermal Shutdown

As soon as the junction temperature, T_J, exceeds 150°C (typical) the device goes into thermal shutdown. In this mode, the High Side and Low Side MOSFETs are turned-off. The device continues its operation when the junction temperature falls below the thermal shutdown hysteresis.

APPLICATION INFORMATION

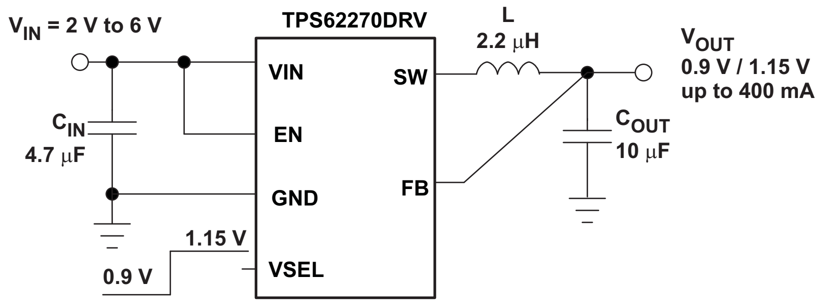

Figure 25. TPS62270DRV Application Circuit

OUTPUT FILTER DESIGN (INDUCTOR AND OUTPUT CAPACITOR)

The TPS62270 is designed to operate with inductors in the range of 1.5µH to 4.7µH and with output capacitors in the range of 4.7µF to 22µF. The part is optimized for operation with a 2.2µH inductor and 10µF output capacitor. Larger or smaller inductor values can be used to optimize the performance of the device for specific operation conditions. For stable operation, the L and C values of the output filter may not fall below 1µH effective inductance and 3.5µF effective capacitance.

Inductor Selection

The inductor value has a direct effect on the ripple current. The selected inductor has to be rated for its dc resistance and saturation current. The inductor ripple current (ΔI_L) decreases with higher inductance and increases with higher V_I or V_O.

The inductor selection has also impact on the output voltage ripple in PFM mode. Higher inductor values will lead to lower output voltage ripple and higher PFM frequency, lower inductor values will lead to a higher output voltage ripple but lower PFM frequency.

Equation 1 calculates the maximum inductor current under static load conditions. The saturation current of the inductor should be rated higher than the maximum inductor current as calculated with Equation 2. This is recommended because during heavy load transient the inductor current will rise above the calculated value.

$$\Delta I_L = Vout \times \frac{1 - \frac{Vout}{Vin}}{L \times f} \tag{1}$$

$$I_{Lmax} = I_{outmax} + \frac{\Delta I_L}{2} \tag{2}$$

With:

f = Switching Frequency (2.25 MHz typical)
L = Inductor Value
ΔI_L = Peak to Peak inductor ripple current
I_{Lmax} = Maximum Inductor current

A more conservative approach is to select the inductor current rating just for the maximum switch current of the corresponding converter.

Accepting larger values of ripple current allows the use of low inductance values, but results in higher output voltage ripple, greater core losses, and lower output current capability.

The total losses of the coil have a strong impact on the efficiency of the DC/DC conversion and consist of both the losses in the dc resistance ($R_{(DC)}$) and the following frequency-dependent components:

- The losses in the core material (magnetic hysteresis loss, especially at high switching frequencies)
- Additional losses in the conductor from the skin effect (current displacement at high frequencies)
- Magnetic field losses of the neighboring windings (proximity effect)
- Radiation losses

Table 2. List of Inductors

DIMENSIONS [mm^3]	INDUCTOR TYPE	SUPPLIER
2.5 × 2.0 × 1.0	MIPS2520	FDK
2.5 × 2.0 × 1.2	MIPSA2520	FDK
2.5 × 2.0 × 1.0	KSLI-252010AG2R2	Hitachi Metals
2.5 × 2.0 × 1.2	LQM2HPN2R2MJ0L	Murata

Output Capacitor Selection

The advanced fast-response voltage mode control scheme of the TPS62270 allows the use of tiny ceramic capacitors. Ceramic capacitors with low ESR values have the lowest output voltage ripple and are recommended. The output capacitor requires either an X7R or X5R dielectric. Y5V and Z5U dielectric capacitors, aside from their wide variation in capacitance over temperature, become resistive at high frequencies.

At nominal load current, the device operates in PWM mode and the RMS ripple current is calculated as:

$$I_{RMSCout} = Vout \times \frac{1 - \frac{Vout}{Vin}}{L \times f} \times \frac{1}{2 \times \sqrt{3}} \tag{3}$$

At nominal load current, the device operates in PWM mode and the overall output voltage ripple is the sum of the voltage spike caused by the output capacitor ESR plus the voltage ripple caused by charging and discharging the output capacitor:

$$\Delta Vout = Vout \times \frac{1 - \frac{Vout}{Vin}}{L \times f} \times \left(\frac{1}{8 \times Cout \times f} + ESR\right) \tag{4}$$

At light load currents the converter operates in Power Save Mode and the output voltage ripple is dependent on the output capacitor and inductor value. Larger output capacitor and inductor values minimize the voltage ripple in PFM mode and tighten DC output accuracy in PFM mode.

Input Capacitor Selection

An input capacitor is required for best input voltage filtering, and minimizing the interference with other circuits caused by high input voltage spikes. For most applications, a 4.7µF to 10µF ceramic capacitor is recommended. Because ceramic capacitor loses up to 80% of its initial capacitance at 5 V, it is recommended that 10µF input capacitors be used for input voltages >4.5V. The input capacitor can be increased without any limit for better input voltage filtering. Take care when using only small ceramic input capacitors. When a ceramic capacitor is used at the input and the power is being supplied through long wires, such as from a wall adapter, a load step at the output or VIN step on the input can induce ringing at the VIN pin. This ringing can couple to the output and be mistaken as loop instability or could even damage the part by exceeding the maximum ratings.

Table 3. List of Capacitors

CAPACITANCE	TYPE	SIZE mm^3	SUPPLIER
4.7 µF	GRM188R60J475K	0603: 1.6 × 0.8 × 0.8 mm^3	Murata
10 µF	GRM188R60J106M69D	0603: 1.6 × 0.8 × 0.8 mm^3	Murata

LAYOUT CONSIDERATIONS

As for all switching power supplies, the layout is an important step in the design. Proper function of the device demands careful attention to PCB layout. Care must be taken in board layout to get the specified performance. If the layout is not carefully done, the regulator could show poor line and/or load regulation, stability issues as well as EMI problems. It is critical to provide a low inductance, impedance ground path. Therefore, use wide and short traces for the main current paths. The input capacitor should be placed as close as possible to the IC pins as well as the inductor and output capacitor.

Connect the GND Pin of the device to the PowerPad™ of the PCB and use this pad as a star point. Use a common Power GND node and a different node for the Signal GND to minimize the effects of ground noise. Connect these ground nodes together to the PowerPad™ (star point) underneath the IC. Keep the common path to the GND PIN, which returns the small signal components and the high current of the output capacitors as short as possible to avoid ground noise. The FB line should be connected right to the output capacitor and routed away from noisy components and traces (e.g., SW line).

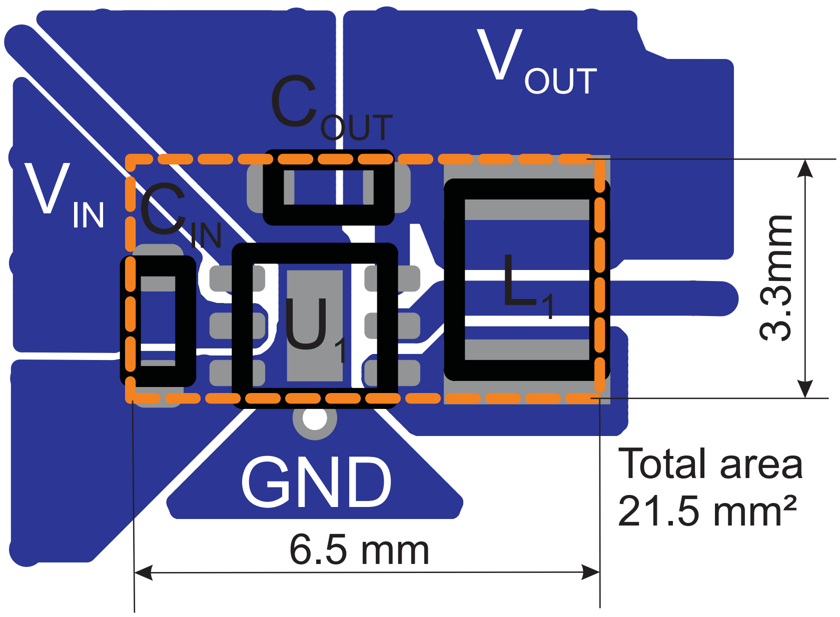

Figure 26. Suggested Board Layout

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS62270DRVR	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CCX	Samples
TPS62270DRVT	ACTIVE	WSON	DRV	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CCX	Samples
TPS62272DRVR	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	OAM	Samples
TPS62272DRVT	ACTIVE	WSON	DRV	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	OAM	Samples
TPS62273DRVR	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CGW	Samples
TPS62273DRVT	ACTIVE	WSON	DRV	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CGW	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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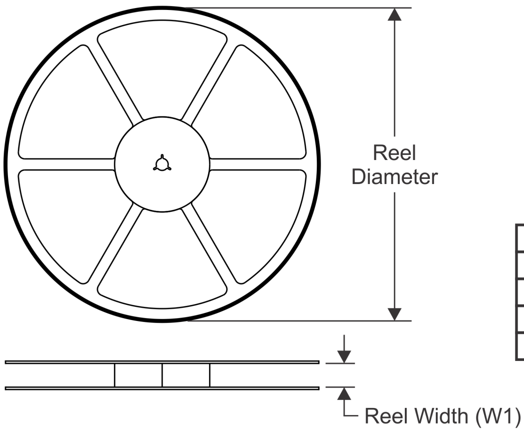
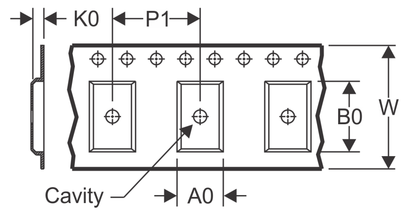
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

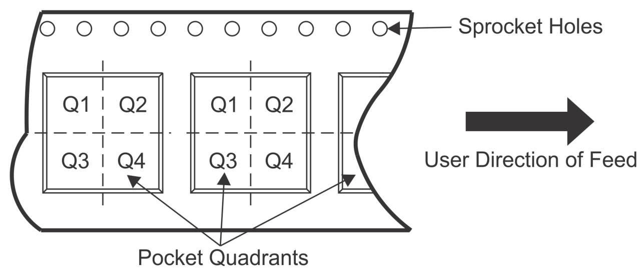


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

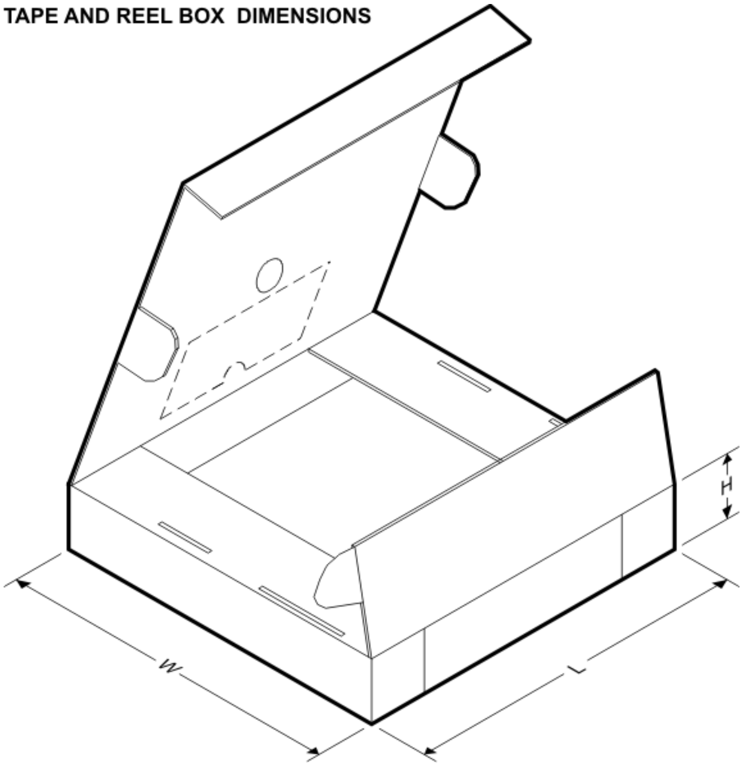
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

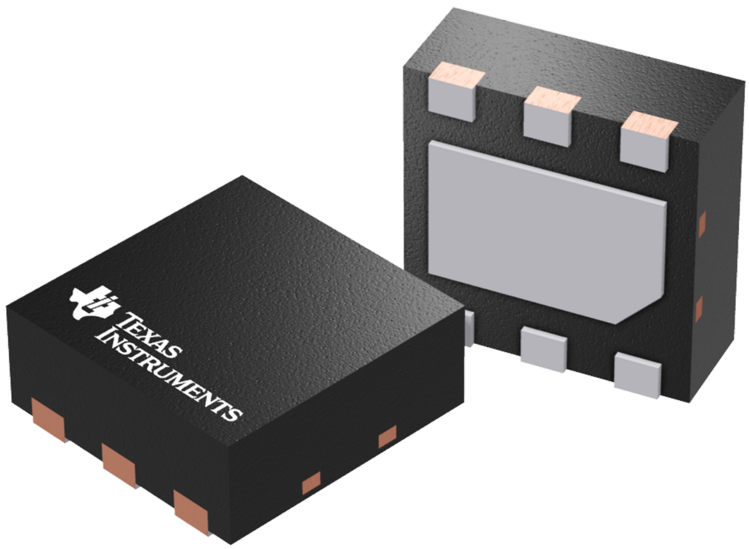
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS62270DRVR	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS62272DRVR	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS62272DRVT	WSON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS62273DRVR	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS62273DRVT	WSON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



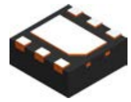
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS62270DRVR	WSON	DRV	6	3000	200.0	183.0	25.0
TPS62272DRVR	WSON	DRV	6	3000	200.0	183.0	25.0
TPS62272DRVT	WSON	DRV	6	250	203.0	203.0	35.0
TPS62273DRVR	WSON	DRV	6	3000	200.0	183.0	25.0
TPS62273DRVT	WSON	DRV	6	250	203.0	203.0	35.0



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

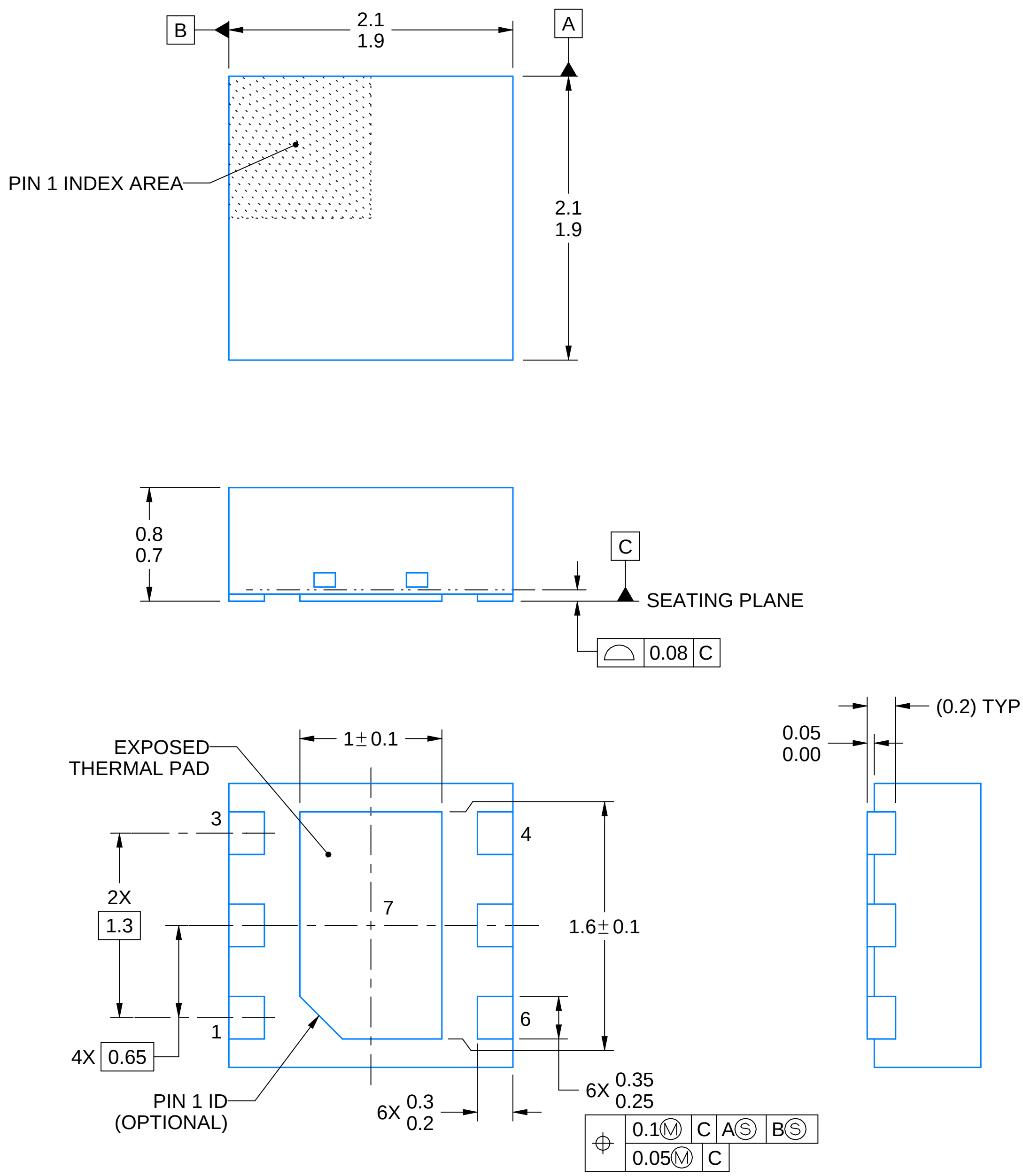
4206925/F



PACKAGE OUTLINE

WSON - 0.8 mm max height

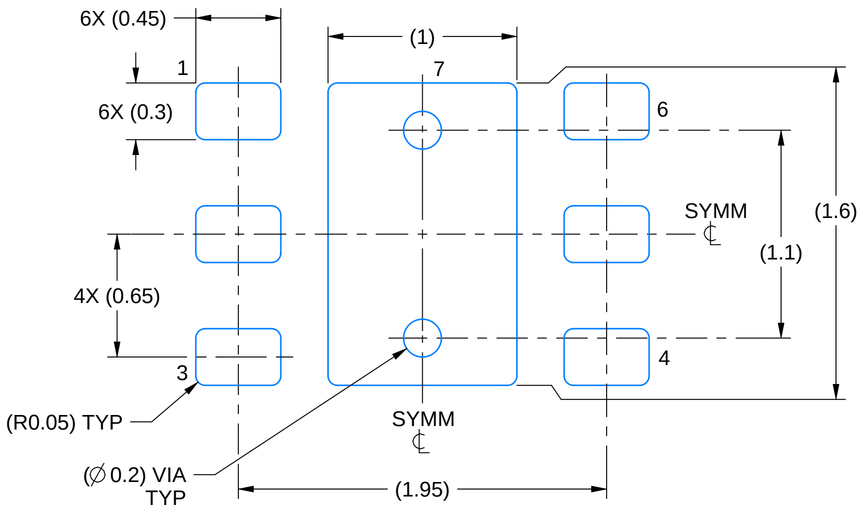
PLASTIC SMALL OUTLINE - NO LEAD



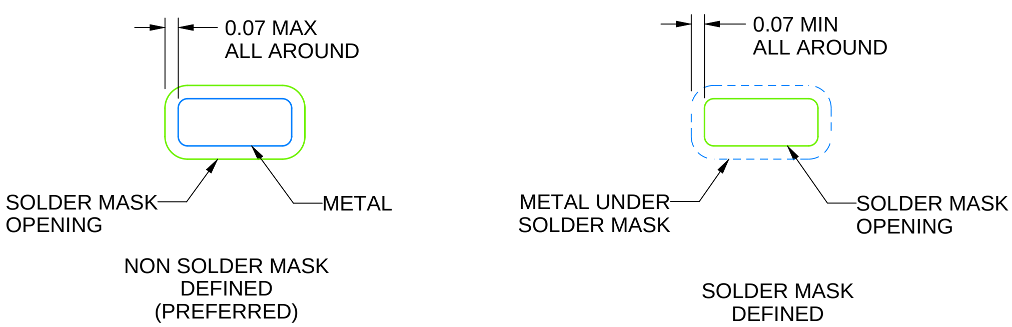
4222173/B 04/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:25X

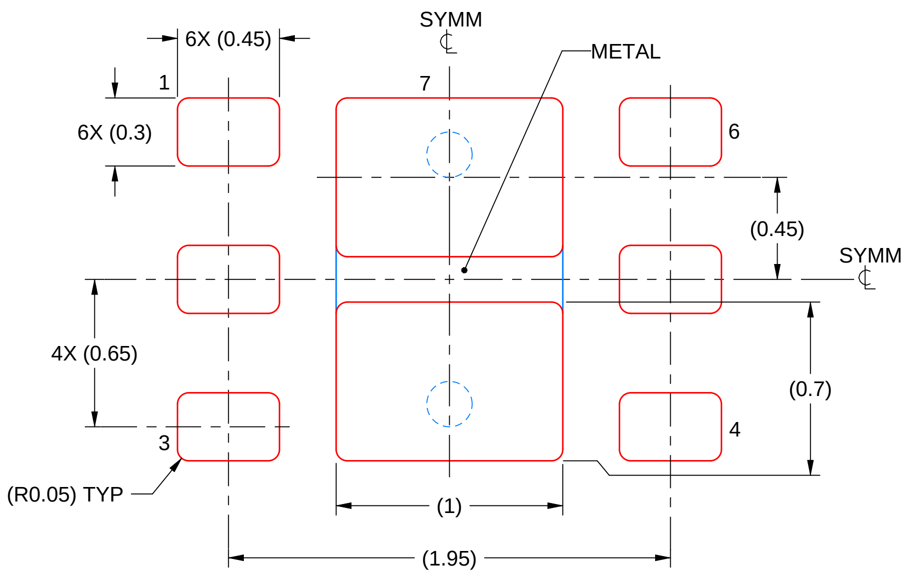


SOLDER MASK DETAILS

4222173/B 04/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



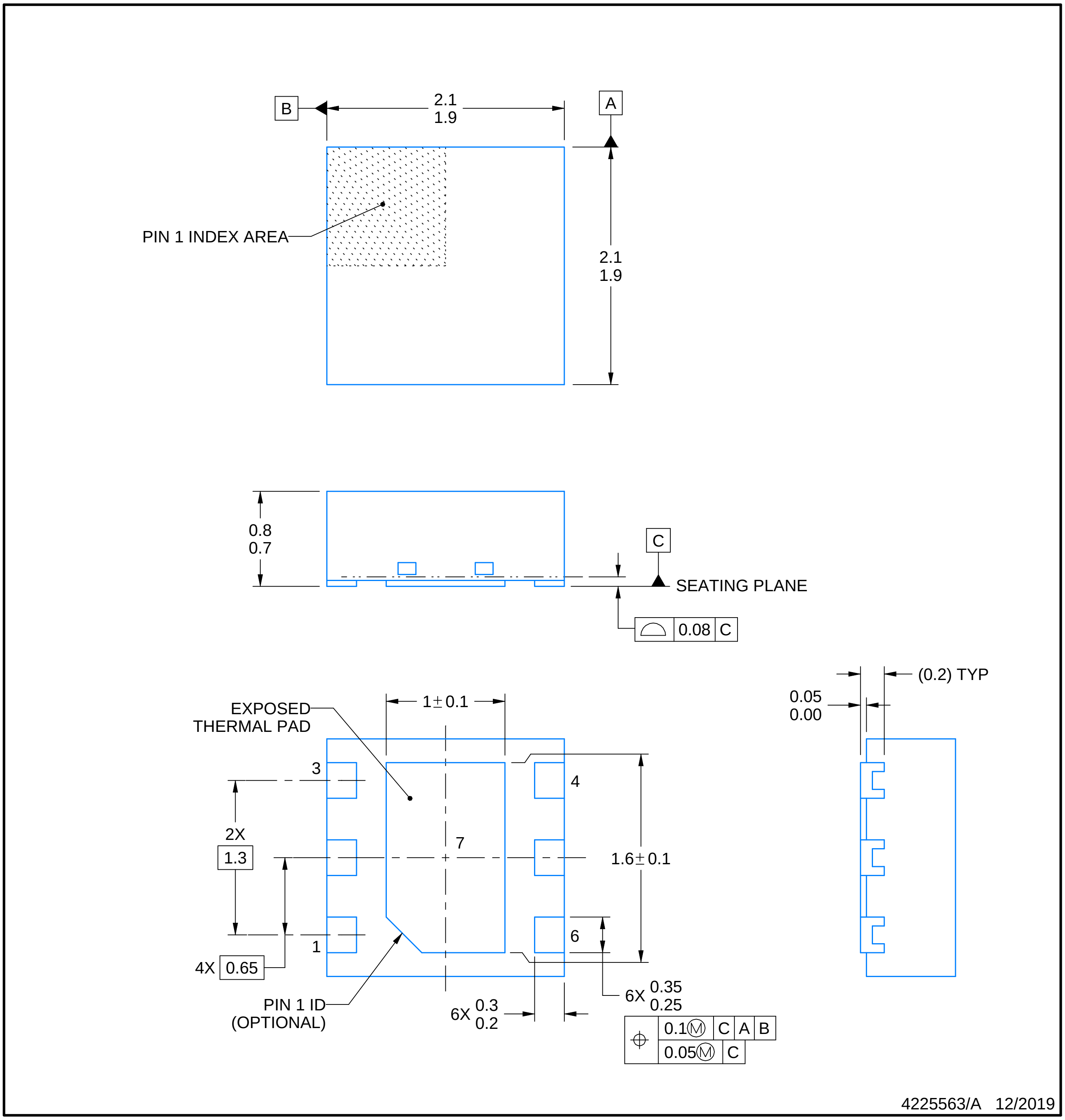
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

4222173/B 04/2018

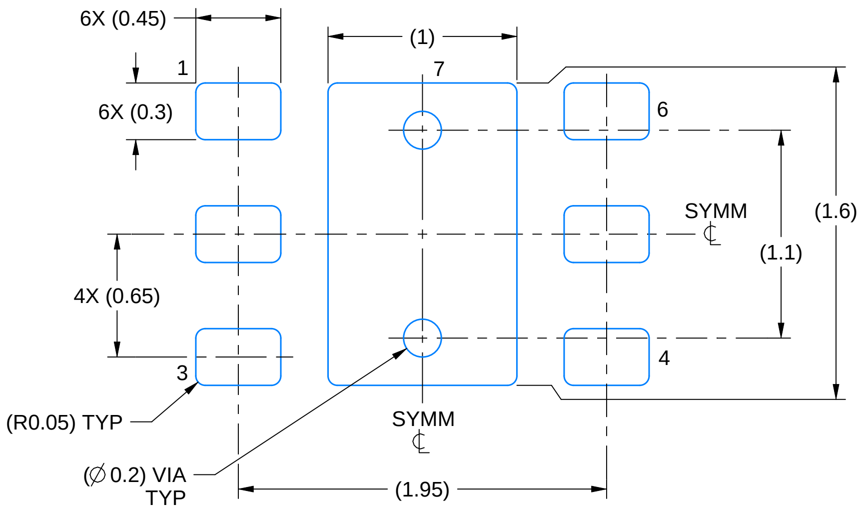
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

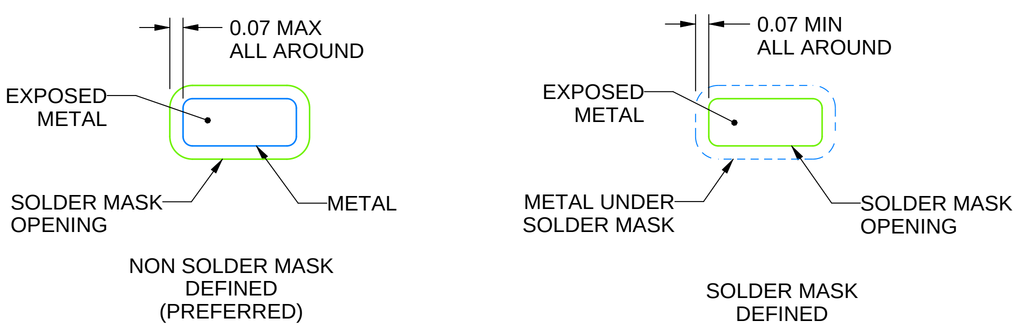


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:25X

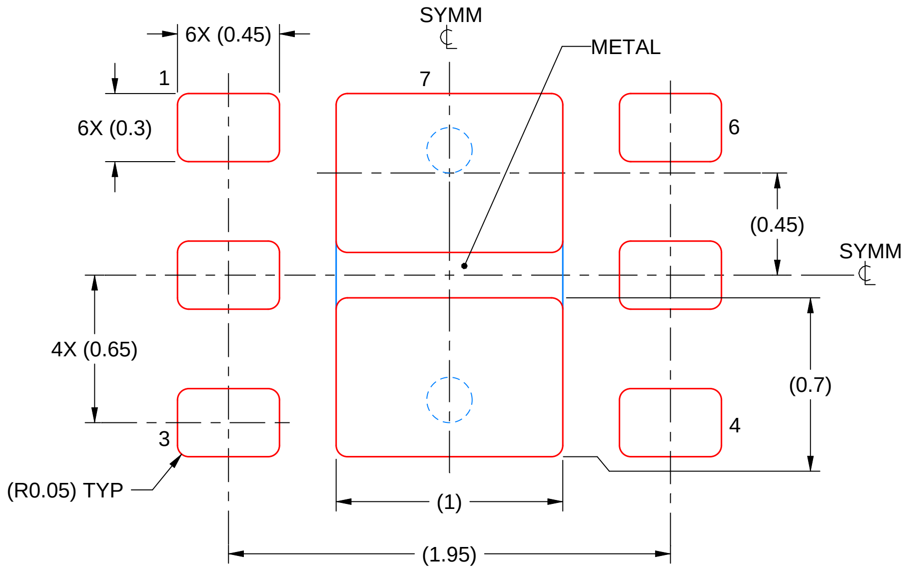


SOLDER MASK DETAILS

4225563/A 12/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

4225563/A 12/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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