

# SN54ALS534A, SN74ALS534A, SN74AS534 OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

SDAS168B – APRIL 1982 – REVISED JULY 1996

- 3-State Bus Driving Inverting Outputs
- Buffered Control Inputs
- Package Options Include Plastic Small-Outline (DW), Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

## description

These octal D-type edge-triggered flip-flops feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

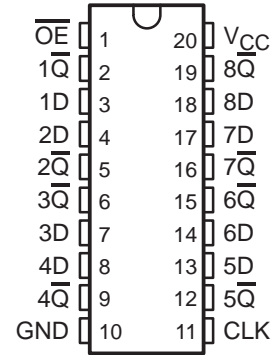
On the positive transition of the clock (CLK) input, the  $\bar{Q}$  outputs are set to the complement of the logic states set up at the data (D) inputs. The 'ALS534A and SN74AS534 have inverted outputs, but otherwise are functionally equivalent to the 'ALS374A and SN74AS374.

A buffered output-enable ( $\overline{OE}$ ) input places the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

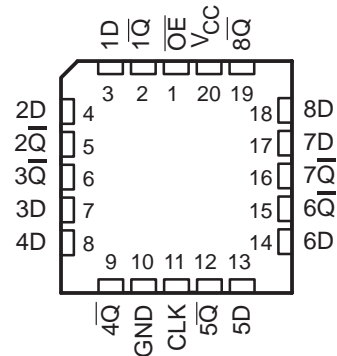
$\overline{OE}$  does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are off.

The SN54ALS534A is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74ALS534A and SN74AS534 are characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

SN54ALS534A . . . J PACKAGE  
SN74ALS534A, SN74AS534 . . . DW OR N PACKAGE  
(TOP VIEW)



SN54ALS534A . . . FK PACKAGE  
(TOP VIEW)



FUNCTION TABLE  
(each flip-flop)

INPUTS			OUTPUT
$\overline{OE}$	CLK	D	$\bar{Q}$
L	$\uparrow$	H	L
L	$\uparrow$	L	H
L	H or L	X	$\bar{Q}_0$
H	X	X	Z



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 **TEXAS  
INSTRUMENTS**

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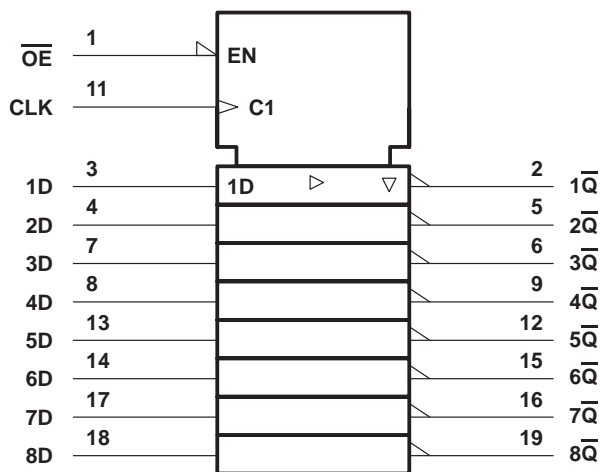
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# SN54ALS534A, SN74ALS534A, SN74AS534

## OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

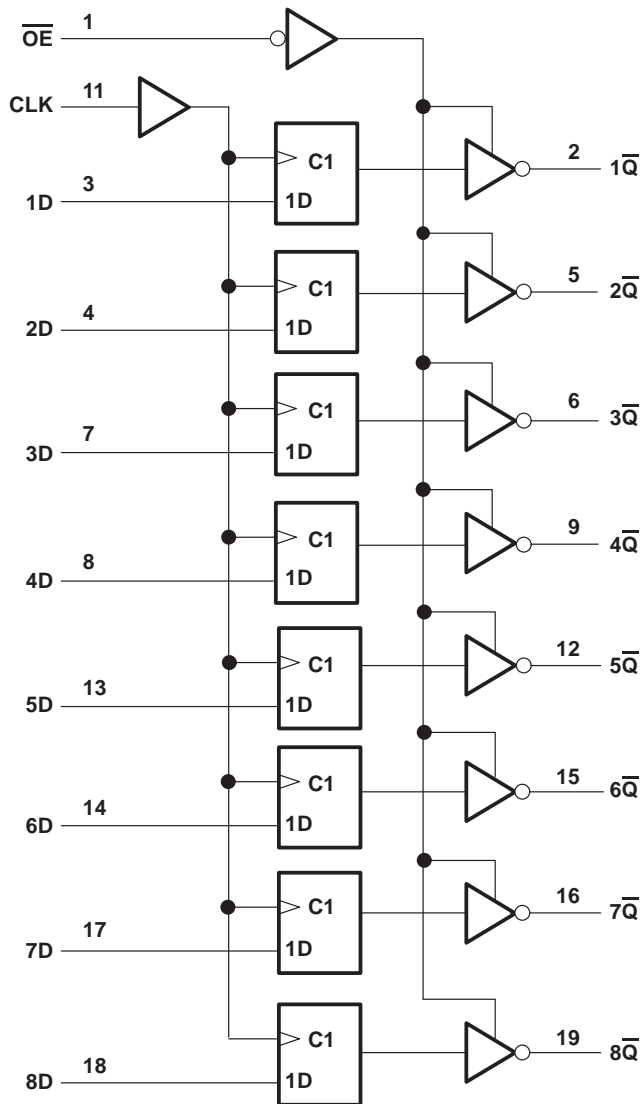
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### logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

### logic diagram (positive logic)



# SN54ALS534A, SN74ALS534A, SN74AS534 OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

SDAS168B – APRIL 1982 – REVISED JULY 1996

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, $V_{CC}$ .....	7 V
Input voltage, $V_I$ .....	7 V
Voltage applied to a disabled 3-state output .....	5.5 V
Operating free-air temperature range, $T_A$ : SN54ALS534A .....	–55°C to 125°C
SN74ALS534A .....	0°C to 70°C
Storage temperature range, $T_{stg}$ .....	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## recommended operating conditions

		SN54ALS534A			SN74ALS534A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
$V_{IH}$	High-level input voltage	2			2			V
$V_{IL}$	Low-level input voltage			0.7			0.8	V
$I_{OH}$	High-level output current			–1			–2.6	mA
$I_{OL}$	Low-level output current			12			24	mA
$f_{clock}$	Clock frequency	0		30	0		35	MHz
$t_w$	Pulse duration, CLK high or low	16.5			14			ns
$t_{su}$	Setup time, data before CLK↑	10			10			ns
$t_h$	Hold time, data after CLK↑	0			0			ns
$T_A$	Operating free-air temperature	–55		125	0		70	°C

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS534A			SN74ALS534A			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
$V_{IK}$		$V_{CC} = 4.5\text{ V}$ ,	$I_I = -18\text{ mA}$			–1.5		–1.5	V	
$V_{OH}$		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$ ,	$I_{OH} = -0.4\text{ mA}$	$V_{CC} - 2$		$V_{CC} - 2$			V	
		$V_{CC} = 4.5\text{ V}$	$I_{OH} = -1\text{ mA}$	2.4	3.3					
			$I_{OH} = -2.6\text{ mA}$			2.4	3.2			
$V_{OL}$		$V_{CC} = 4.5\text{ V}$	$I_{OL} = 12\text{ mA}$	0.25	0.4	0.25	0.4	V		
			$I_{OL} = 24\text{ mA}$			0.35	0.5			
$I_{OZH}$		$V_{CC} = 5.5\text{ V}$ ,	$V_O = 2.7\text{ V}$			20		20	μA	
$I_{OZL}$		$V_{CC} = 5.5\text{ V}$ ,	$V_O = 0.4\text{ V}$			–20		–20	μA	
$I_I$		$V_{CC} = 5.5\text{ V}$ ,	$V_I = 7\text{ V}$			0.1		0.1	mA	
$I_{IH}$		$V_{CC} = 5.5\text{ V}$ ,	$V_I = 2.7\text{ V}$			20		20	μA	
$I_{IL}$	CLK, $\overline{OE}$	$V_{CC} = 5.5\text{ V}$ ,	$V_I = 0.4\text{ V}$			–0.1		–0.1	mA	
	D					–0.2		–0.2		
$I_{OS}§$		$V_{CC} = 5.5\text{ V}$ ,	$V_O = 2.25\text{ V}$	–20	–112	–30	–112	mA		
$I_{CC}$		$V_{CC} = 5.5\text{ V}$	Outputs high	11	19	11	19	mA		
			Outputs low	19	28	19	28			
			Outputs disabled	10	31	20	31			

‡ All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current,  $I_{OS}$ .



# SN54ALS534A, SN74ALS534A, SN74AS534

## OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS

### WITH 3-STATE OUTPUTS

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#### switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 4.5 V to 5.5 V, C <sub>L</sub> = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T <sub>A</sub> = MIN to MAX†				UNIT
			SN54ALS534A		SN74ALS534A		
			MIN	MAX	MIN	MAX	
f <sub>max</sub>			30		35		MHz
t <sub>PLH</sub>	CLK	Any $\bar{Q}$	3	17	3	12	ns
t <sub>PHL</sub>			4	18	4	16	
t <sub>PZH</sub>	$\overline{OE}$	Any $\bar{Q}$	3	19	3	17	ns
t <sub>PZL</sub>			4	20	4	18	
t <sub>PHZ</sub>	$\overline{OE}$	Any $\bar{Q}$	1	12	1	10	ns
t <sub>PLZ</sub>			1	25	2	14	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V <sub>CC</sub>	7 V
Input voltage, V <sub>I</sub>	7 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range, T <sub>A</sub> : SN74AS534	0°C to 70°C
Storage temperature range, T <sub>stg</sub>	-65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

#### recommended operating conditions

		SN74AS534			UNIT
		MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5	5.5	V
V <sub>IH</sub>	High-level input voltage	2			V
V <sub>IL</sub>	Low-level input voltage			0.8	V
I <sub>OH</sub>	High-level output current			-15	mA
I <sub>OL</sub>	Low-level output current			48	mA
f <sub>clock</sub>	Clock frequency	0		125	MHz
t <sub>w</sub>	Pulse duration	CLK high		4	ns
		CLK low		3	
t <sub>su</sub>	Setup time, data before CLK↑	2			ns
t <sub>h</sub>	Hold time, data after CLK↑	2			ns
T <sub>A</sub>	Operating free-air temperature	0		70	°C



# SN54ALS534A, SN74ALS534A, SN74AS534 OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

SDAS168B – APRIL 1982 – REVISED JULY 1996

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	SN74AS534		UNIT		
		MIN	TYP†		MAX	
$V_{IK}$	$V_{CC} = 4.5\text{ V}$ , $I_I = -18\text{ mA}$			-1.2	V	
$V_{OH}$	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$ , $I_{OH} = -2\text{ mA}$	$V_{CC} - 2$			V	
	$V_{CC} = 4.5\text{ V}$ , $I_{OH} = -15\text{ mA}$	2.4	3.3			
$V_{OL}$	$V_{CC} = 4.5\text{ V}$ , $I_{OL} = 48\text{ mA}$	0.34	0.5		V	
$I_{OZH}$	$V_{CC} = 5.5\text{ V}$ , $V_O = 2.7\text{ V}$			50	$\mu\text{A}$	
$I_{OZL}$	$V_{CC} = 5.5\text{ V}$ , $V_I = 0.4\text{ V}$			-50	$\mu\text{A}$	
$I_I$	$V_{CC} = 5.5\text{ V}$ , $V_I = 7\text{ V}$			0.1	mA	
$I_{IH}$	$V_{CC} = 5.5\text{ V}$ , $V_I = 2.7\text{ V}$			20	$\mu\text{A}$	
$I_{IL}$	$\overline{OE}$ , CLK	$V_{CC} = 5.5\text{ V}$ , $V_I = 0.4\text{ V}$		-0.5	mA	
	D			-2		
$I_{O\ddagger}$	$V_{CC} = 5.5\text{ V}$ , $V_O = 2.25\text{ V}$			-30	-112	mA
$I_{CC}$	$V_{CC} = 5.5\text{ V}$	Outputs high	77	120	mA	
		Outputs low	84	128		
		Outputs disabled	84	128		

† All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current,  $I_{OS}$ .

## switching characteristics (see Figure 1)

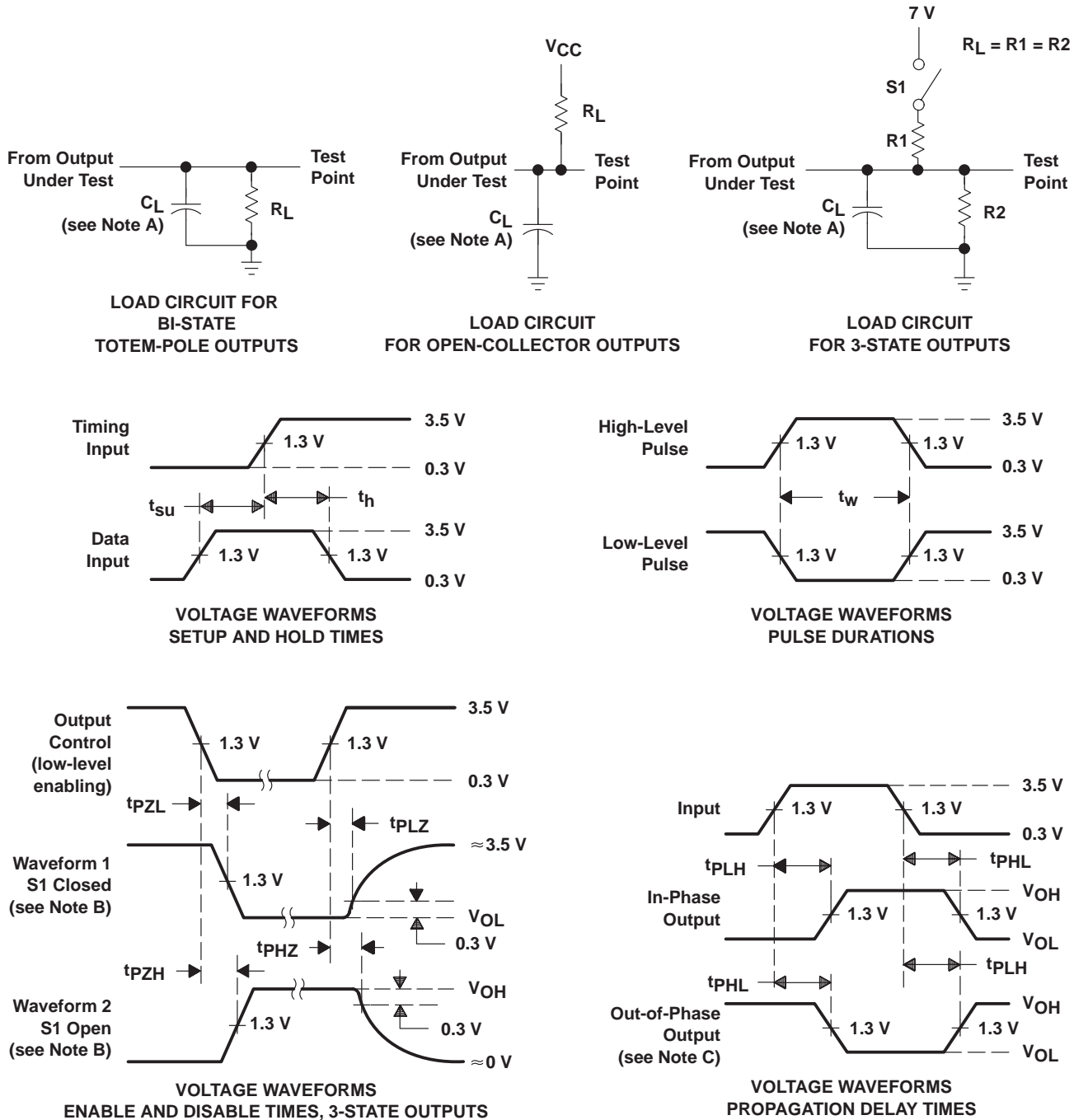
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$ , $C_L = 50\text{ pF}$ , $R_1 = 500\ \Omega$ , $R_2 = 500\ \Omega$ , $T_A = \text{MIN to MAX}\S$		UNIT
			SN74AS534		
			MIN	MAX	
$f_{\text{max}}$			125		MHz
$t_{PLH}$	CLK	Any $\overline{Q}$	3	8	ns
$t_{PHL}$			4	9	
$t_{PZH}$	$\overline{OE}$	Any $\overline{Q}$	2	6	ns
$t_{PZL}$			3	10	
$t_{PHZ}$	$\overline{OE}$	Any $\overline{Q}$	2	6	ns
$t_{PLZ}$			2	6	

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

**SN54ALS534A, SN74ALS534A, SN74AS534**  
**OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS**  
**WITH 3-STATE OUTPUTS**

SDAS168B – APRIL 1982 – REVISED JULY 1996

**PARAMETER MEASUREMENT INFORMATION**  
**SERIES 54ALS/74ALS AND 54AS/74AS DEVICES**



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.  
 D. All input pulses have the following characteristics:  $PRR \leq 1$  MHz,  $t_r = t_f = 2$  ns, duty cycle = 50%.  
 E. The outputs are measured one at a time with one transition per measurement.

**Figure 1. Load Circuits and Voltage Waveforms**

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74ALS534ADWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS534A	<a href="#">Samples</a>
SN74ALS534AN	ACTIVE	PDIP	N	20	20	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74ALS534AN	<a href="#">Samples</a>
SN74ALS534ANSR	ACTIVE	SO	NS	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS534A	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALS534ADWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74ALS534ANSR	SO	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALS534ADWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74ALS534ANSR	SO	NS	20	2000	367.0	367.0	45.0

**TUBE**



\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74ALS534AN	N	PDIP	20	20	506	13.97	11230	4.32

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - $\triangle D$  The 20 pin end lead shoulder width is a vendor option, either half or full width.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

# DW0020A



# PACKAGE OUTLINE

## SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

**NOTES:**

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



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