SN65HVD11-HT 3.3-V RS-485 Transceiver

1 Features

- Operates With a 3.3-V Supply
- Bus-Pin ESD Protection Exceeds 16-kV Human-Body Model (HBM)
- 1/8 Unit-Load Option Available (up to 256 Nodes on Bus)
- Optional Driver Output Transition Times for Signaling Rates (1) of 1 Mbps, 10 Mbps, and 32 Mbps
- Based on ANSI TIA/EIA-485-A
- Bus-Pin Short Circuit Protection From –7 V to 12 V
- Open-Circuit, Idle-Bus, and Shorted-Bus Fail-Safe Receiver
- Glitch-Free Power-Up and Power-Down Protection for Hot-Plugging Applications
- SN75176 Footprint
- Supports Extreme Temperature Applications:
  - Controlled Baselines
  - One Assembly and Test Sites
  - One Fabrication Sites
  - Available in Extreme (–55°C/210°C) Temperature Range (2)
  - Extended Product Life Cycles
  - Extended Product-Change Notifications
  - Product Traceability
  - Texas Instruments' High Temperature Products Use Highly Optimized Silicon (Die) Solutions With Design and Process Enhancements to Maximize Performance Over Extended Temperatures.

(1) The signaling rate of a line is the number of voltage transitions that are made per second expressed in the units bits per second (bps).
(2) Custom temperature ranges available

2 Applications

- Down-Hole Drilling
- High Temperature Environments
- Digital Motor Controls
- Utility Meters
- Chassis-to-Chassis Interconnects
- Electronic Security Stations
- Industrial Process Controls
- Building Automation
- Point-of-Sale (POS) Terminals and Networks

3 Description

The SN65HVD11-HT device combines a 3-state differential line driver and differential input line receiver that operates with a single 3.3-V power supply. It is designed for balanced transmission lines and meets or exceeds ANSI TIA/EIA-485-A and ISO 8482:1993, with the exception that the thermal shutdown is removed. This differential bus transceiver is a monolithic integrated circuit designed for bidirectional data communication on multipoint bus-transmission lines. The driver and receiver have active-high and active-low enables, respectively, that can be externally connected together to function as direction control.

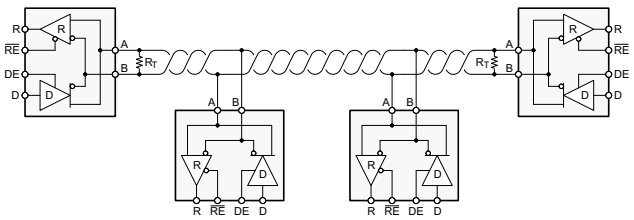
The driver differential outputs and receiver differential inputs connect internally to form a differential input/output (I/O) bus port that is designed to offer minimum loading to the bus when the driver is disabled or V_{CC} = 0.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN65HVD11-HT	SOIC (8)	4.90 mm × 3.91 mm
	CFP (8) (2)	6.90 mm × 5.65 mm
	CFP (8) (3)	6.90 mm × 5.65 mm
	CDIP SB (8)	11.81 mm × 7.49 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) HKJ Package
(3) HKQ Package

Typical Application Diagram



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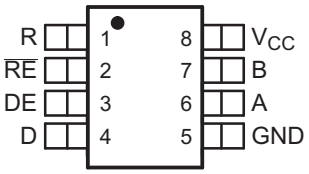
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

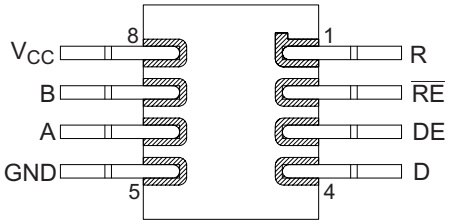
Changes from Revision E (June 2012) to Revision F	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

5 Pin Configuration and Functions

D, JD, or HKJ Package
8-Pin SOIC, PDIP, or CFP
Top View



HKQ Package
8-Pin CFP
Top View



Pin Functions

PIN			TYPE	DESCRIPTION
NAME	SOIC, PDIP	HKQ		
A	6	6	Bus input/output	Driver output or receiver input (complementary to B)
B	7	7	Bus input/output	Driver output or receiver input (complementary to A)
D	4	4	Digital input	Driver data input
DE	3	3	Digital input	Active-high driver enable
GND	5	5	Reference potential	Local device ground
R	1	1	Digital output	Receive data output
$\overline{RE}$	2	2	Digital input	Active-low receiver enable
V_{CC}	8	8	Supply	3-V to 3.6-V supply

Bare Die Information

DIE THICKNESS	BACKSIDE FINISH	BACKSIDE POTENTIAL	BOND PAD METALLIZATION COMPOSITION
15 mils.	Silicon with backgrind	GND	Cu-Ni-Pd

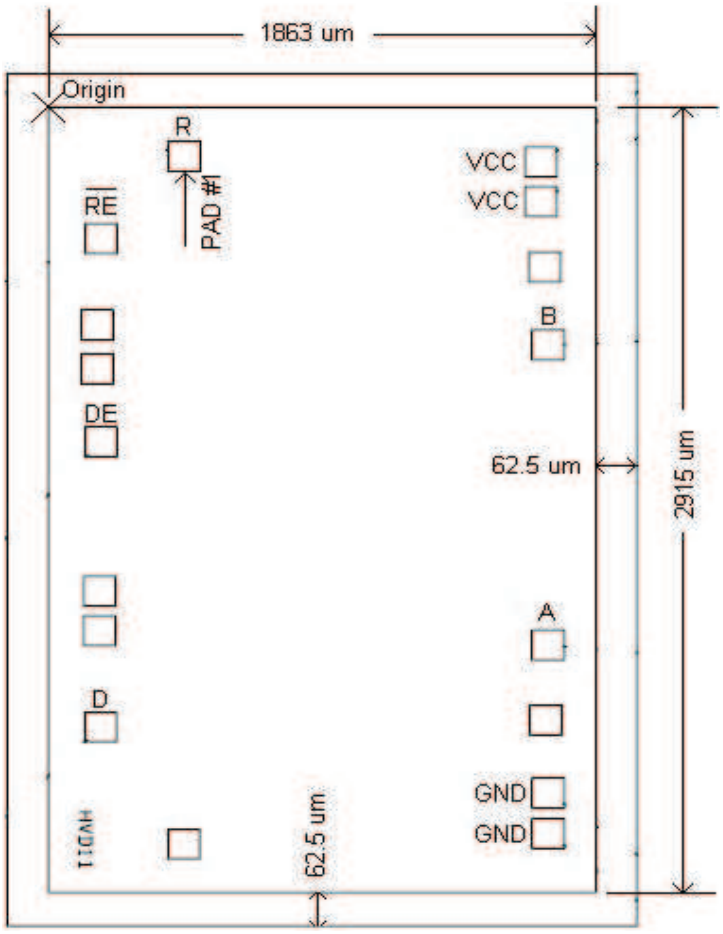
Bond Pad Coordinates in Microns - Rev A

DESCRIPTION(1)	PAD NUMBER	a	b	c	d
R	1	69.3	372.15	185.3	489.15
~RE	2	388.75	71.5	503.75	186.5
DNC	3	722.4	55.4	839.4	172.4
DNC	4	891.4	55.4	1008.4	172.4
DE	5	1174.8	71.5	1289.8	186.5
DNC	6	1754.35	65.4	1869.35	180.4
DNC	7	1907.35	65.4	2022.35	180.4
D	8	2280.55	69.5	2395.55	184.5
DNC	9	2733.5	371.5	2848.5	486.5
GND	10	2691	1693.1	2808	1810.1
GND	11	2535	1693.1	2652	1810.1
DNC	12	2253.45	1685.65	2368.45	1800.65
A	13	1961.55	1693.1	2078.55	1810.1
B	14	799.55	1693.1	916.55	1810.1
DNC	15	498.35	1681.2	613.35	1796.2
VCC	16	244.8	1668.5	359.8	1783.5

(1) DNC = Do Not Connect

Bond Pad Coordinates in Microns - Rev A (continued)

DESCRIPTION(1)	PAD NUMBER	a	b	c	d
VCC	17	91.8	1668.5	206.8	1783.5



6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	–0.3	6	V
	Voltage at A or B	–9	14	V
	Input voltage at D, DE, R, or $\overline{RE}$	–0.5	V_{CC} + 0.5	V
	Voltage input, transient pulse, A and B, through 100 Ω (see Figure 20)	–50	50	V
I_O	Receiver output current	–11	11	mA
	Continuous total power dissipation	See *Thermal Information*		

(1) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	A, B, and GND	±16000	V
			All pins	±4000	
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)		±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3		3.6	V
V_I or V_{IC}	Voltage at any bus terminal (separately or common-mode)		–7 (1)		12	V
V_{IH}	High-level input voltage	D, DE, $\overline{RE}$	2		V_{CC}	V
V_{IL}	Low-level input voltage	D, DE, $\overline{RE}$	0		0.8	V
V_{ID}	Differential input voltage	Figure 16	–12		12	V
I_{OH}	High-level output current	Driver	–60			mA
		Receiver	–8			
I_{OL}	Low-level output current	Driver			60	mA
		Receiver			8	
R_L	Differential load resistance		54	60		Ω
C_L	Differential load capacitance			50		pF
	Signaling rate				10	Mbps
T_J (2)	Operating junction temperature	T_A = –55°C to 125°C		129		°C
		T_A = 175°C		179		
		T_A = 210°C		214		

(1) The algebraic convention, in which the least-positive (most-negative) limit is designated as minimum, is used in this data sheet.
(2) See *Thermal Information* table for information regarding this specification.

6.4 Thermal Information

THERMAL METRIC (1)		SN65HVD11-HT				UNIT
		D (SOIC)	JD (CDIP SB)	HKJ (CFP)	HKQ (CFP)	
		8 PINS	8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	101.5	73.9	N/A	170	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	53.6	N/A	N/A	6.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	45.1	39.8	N/A	195	°C/W
ψ_{JT}	Junction-to-top characterization parameter	4.8	6.9	N/A	3.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	41.8	49.2	N/A	146.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	9.1	6.2	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Driver Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{IK}	Input clamp voltage		I_I = –18 mA			–1.5			V
$\lvert V_{OD}\rvert$	Differential output voltage		I_O = 0			2		V_{CC}	V
			R_L = 54 Ω, See Figure 10			1			
			V_{test} = –7 V to 12 V, See Figure 11			1			
$\Delta\lvert V_{OD}\rvert$	Change in magnitude of differential output voltage		V_{test} = –7 V to 12 V, See Figure 10 and Figure 11			–0.2		0.2	V
$V_{OC(PP)}$	Peak-to-peak common mode output voltage		See Figure 12				400		mV
$V_{OC(SS)}$	Steady-state common mode output voltage		See Figure 12			1.4		2.5	V
$\Delta V_{OC(SS)}$	Change in steady-state common mode output voltage		See Figure 12			–0.06		0.06	V
I_{OZ}	High-impedance output current		See receiver input currents						
I_I	Input current	D		T_A = –55°C to 125°C		–100		0	μA
				T_A = 175°C(1)		–100		3	
				T_A = 210°C(2)		–100		3	
		DE				0		100	
I_{OS}	Short circuit output current		–7 V ≤ V_O ≤ 12 V			–250		250	mA
$C_{(OD)}$	Differential output capacitance		V_{OD} = 0.4 sin (4E6πt) + 0.5 V, DE = 0 V				18		pF
I_{CC}	Supply current		$\overline{RE}$ = V_{CC}, D and DE = V_{CC}, No load	Receiver disabled and driver enabled	T_A = –55°C to 125°C		11	15.5	mA
					T_A = 175°C(1)		11.5	17.5	
					T_A = 210°C(2)		14	18	
			$\overline{RE}$ = V_{CC}, D = V_{CC}, DE = 0 V, No load	Receiver disabled and driver disabled (standby)	T_A = –55°C to 125°C		2.5	20	μA
					T_A = 175°C(1)		20	150	
					T_A = 210°C(2)		175	450	
			$\overline{RE}$ = 0 V, D and DE = V_{CC}, No load	Receiver enabled and driver enabled	T_A = –55°C to 125°C		11	15.5	mA
					T_A = 175°C(1)		11	17.5	
					T_A = 210°C(2)		11	18	

(1) Minimum and maximum parameters are characterized for operation at T_A = 175°C but may not be production tested at that temperature. Production test limits with statistical guardbands are used to ensure high temperature performance.
(2) Minimum and maximum parameters are characterized for operation at T_A = 210°C but may not be production tested at that temperature. Production test limits with statistical guardbands are used to ensure high temperature performance.

6.6 Receiver Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	I_O = –8 mA					–0.01	V
V_{IT-}	Negative-going input threshold voltage	I_O = 8 mA			–0.2			V
V_{hys}	Hysteresis voltage (V_{IT+} – V_{IT-})		T_A = –55°C to 125°C			35		mV
			T_A = 175°C(1)			41		
			T_A = 210°C(2)			41		
V_{IK}	Enable-input clamp voltage	I_I = –18 mA			–1.5			V
V_{OH}	High-level output voltage	V_{ID} = 200 mV, I_{OH} = –8 mA, See Figure 16			2.4			V
V_{OL}	Low-level output voltage	V_{ID} = –200 mV, I_{OL} = 8 mA, See Figure 16					0.4	V
I_{OZ}	High-impedance state output current	V_O = 0 or V_{CC}, $\overline{RE}$ = V_{CC}			–1		1	µA
I_I	Bus input current	V_A or V_B = 12 V	Other input at 0 V	T_A = –55°C to 125°C		0.075	0.11	mA
				T_A = 175°C(1)		0.1	0.15	
				T_A = 210°C(2)		0.1	0.15	
		V_A or V_B = 12 V, V_{CC} = 0 V		T_A = –55°C to 125°C		0.085	0.13	
				T_A = 175°C(1)		0.12	0.16	
				T_A = 210°C(2)		0.12	0.16	
		V_A or V_B = –7 V		T_A = –55°C to 125°C	–0.1	–0.05		
				T_A = 175°C(1)	–0.3	–0.15		
				T_A = 210°C(2)	–0.3	–0.15		
		V_A or V_B = –7 V, V_{CC} = 0 V		T_A = –55°C to 125°C	–0.1	–0.05		
				T_A = 175°C(1)	–0.3	–0.15		
				T_A = 210°C(2)	–0.3	–0.15		
I_{IH}	High-level input current, $\overline{RE}$	V_{IH} = 2 V		T_A = –55°C to 125°C	–30		0	µA
				T_A = 175°C(1)	–30		3	
				T_A = 210°C(2)	–30		3	
I_{IL}	Low-level input current, $\overline{RE}$	V_{IL} = 0.8 V			–30		0	µA
C_{ID}	Differential input capacitance	V_{ID} = 0.4 sin (4E6πt) + 0.5 V, DE at 0 V		T_A = –55°C to 125°C		15		pF
				T_A = 175°C(1)		18		
				T_A = 210°C(2)		18		
I_{CC}	Supply current	$\overline{RE}$ = 0 V, D and DE = 0 V, No load	Receiver enabled and driver disabled	T_A = –55°C to 125°C		5	8	mA
				T_A = 175°C(1)		7.5	8.5	
				T_A = 210°C(2)		7.5	10	
		$\overline{RE}$ = V_{CC}, D = V_{CC}, DE = 0 V, No load	Receiver disabled and driver disabled (standby)	T_A = –55°C to 125°C		2.5	20	µA
				T_A = 175°C(1)		12.5	200	
				T_A = 210°C(2)		175	450	
		$\overline{RE}$ = 0 V, D and DE = V_{CC}, No load	Receiver enabled and driver enabled	T_A = –55°C to 125°C		11	15.5	mA
				T_A = 175°C(1)		11.5	17.5	
				T_A = 210°C(2)		14	18	

(1) Minimum and maximum parameters are characterized for operation at T_A = 175°C but may not be production tested at that temperature. Production test limits with statistical guardbands are used to ensure high temperature performance.
(2) Minimum and maximum parameters are characterized for operation at T_A = 210°C but may not be production tested at that temperature. Production test limits with statistical guardbands are used to ensure high temperature performance.

6.7 Driver Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 54 Ω, C_L = 50 pF, See Figure 13		18	25	40	ns
t_{PHL}	Propagation delay time, high-to-low-level output			18	25	40	ns
t_r	Differential output signal rise time		T_A = –55°C to 125°C	10	21	30	ns
			T_A = 175°C(1)	10	22	30	
			T_A = 210°C(2)	10	22	30	
t_f	Differential output signal fall time		T_A = –55°C to 125°C	10	21	30	ns
			T_A = 175°C(1)	10	22	30	
			T_A = 210°C(2)	10	22	30	
$t_{sk(p)}$	Pulse skew ($\lvert t_{PHL} - t_{PLH} \rvert$)					2.5	ns
$t_{sk(pp)}$(3)	Part-to-part skew (t_{PHL} or t_{PLH})					11	ns
t_{PZH}	Propagation delay time, high-impedance to high-level output	R_L = 110 Ω, $\overline{RE}$ = 0 V, See Figure 14				55	ns
t_{PHZ}	Propagation delay time, high-level to high-impedance output					55	ns
t_{PZL}	Propagation delay time, high-impedance to low-level output	R_L = 110 Ω, $\overline{RE}$ = 0 V, See Figure 15				55	ns
t_{PLZ}	Propagation delay time, low-level to high-impedance output					75	ns
t_{PZH}	Propagation delay time, standby to high-level output	R_L = 110 Ω, $\overline{RE}$ = 3 V, See Figure 14				6	µs
t_{PZL}	Propagation delay time, standby to low-level output	R_L = 110 Ω, $\overline{RE}$ = 3 V, See Figure 15				6	µs

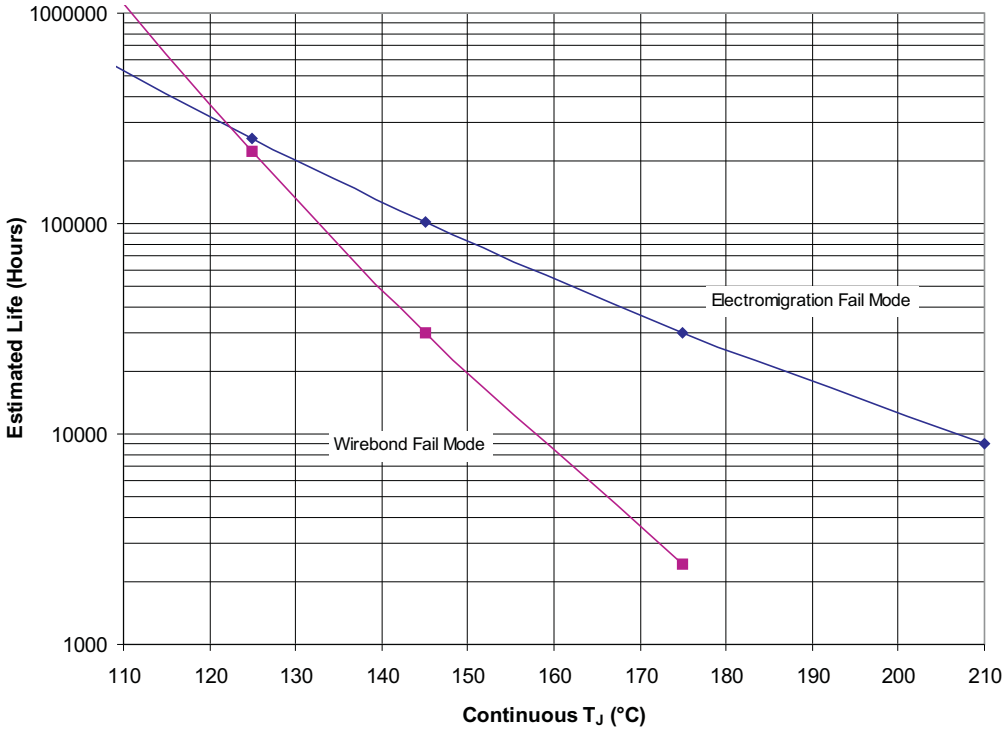
(1) Minimum and maximum parameters are characterized for operation at T_A = 175°C but may not be production tested at that temperature. Production test limits with statistical guardbands are used to ensure high temperature performance.
(2) Minimum and maximum parameters are characterized for operation at T_A = 210°C but may not be production tested at that temperature. Production test limits with statistical guardbands are used to ensure high temperature performance.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

6.8 Receiver Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	V_{ID} = –1.5 V to 1.5 V, C_L = 15 pF, See Figure 17		30	55	70	ns
t_{PHL}	Propagation delay time, high-to-low-level output			30	55	70	ns
$t_{sk(p)}$	Pulse skew ($\lvert t_{PHL} - t_{PLH} \rvert$)					4	ns
$t_{sk(pp)}$ (1)	Part-to-part skew					15	ns
t_r	Output signal rise time	C_L = 15 pF, See Figure 17	T_A = –55°C to 125°C	1	3	5	ns
			T_A = 175°C (2)	1	4	5	
			T_A = 210°C (3)	1	4	5	
t_f	Output signal fall time		T_A = –55°C to 125°C	1	3	5	ns
			T_A = 175°C (2)	1	4	5	
			T_A = 210°C (3)	1	4	5	
t_{PZH} (3)	Output enable time to high level	C_L = 15 pF, DE = 3 V, See Figure 18				15	ns
t_{PZL} (3)	Output enable time to low level					15	ns
t_{PHZ}	Output disable time from high level					20	ns
t_{PLZ}	Output disable time from low level					15	ns
t_{PZH} (1)	Propagation delay time, standby-to-high-level output	C_L = 15 pF, DE = 0, See Figure 19				6	µs
t_{PZL} (1)	Propagation delay time, standby-to-low-level output					6	µs

(1) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(2) Minimum and maximum parameters are characterized for operation at T_A = 175°C but may not be production tested at that temperature. Production test limits with statistical guardbands are used to ensure high temperature performance.
(3) Minimum and maximum parameters are characterized for operation at T_A = 210°C but may not be production tested at that temperature. Production test limits with statistical guardbands are used to ensure high temperature performance.



(1) See data sheet for absolute maximum and minimum recommended operating conditions.

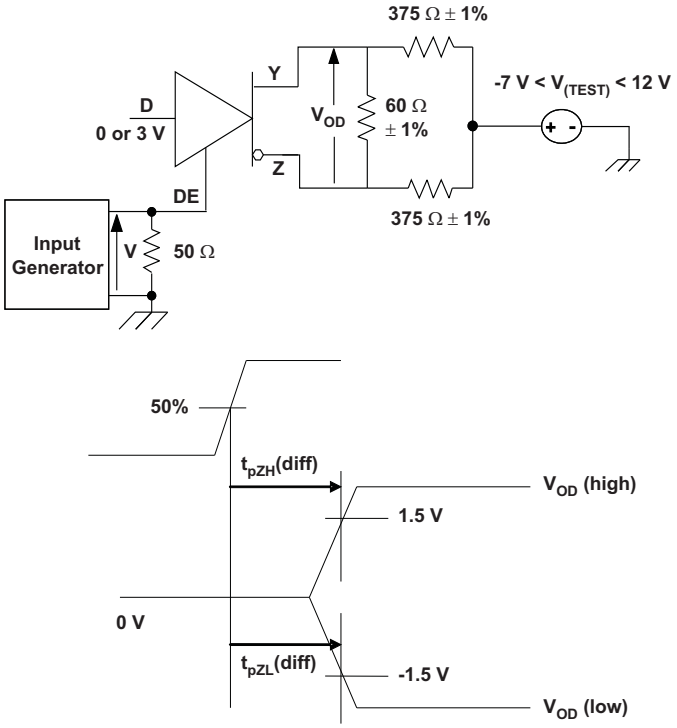
(2) Silicon operating life design goal is 10 years at 105°C junction temperature (does not include package interconnect life).

(3) The predicted operating lifetime vs. junction temperature is based on reliability modeling using electromigration as the dominant failure mechanism affecting device wearout for the specific device process and design characteristics.

(4) Wirebond fail mode applicable for D package only.

(5) Wirebond life approaches 0 hours < 200°C which is only true of the HD device.

Figure 1. SN65HVD11SJD/SKGDA/SHKJ/SHKQ/HD Operating Life Derating Chart



Note: The time $t_{pZL}(x)$ is the measure from DE to $V_{OD}(x)$. V_{OD} is valid when it is greater than 1.5 V.

Figure 2. Driver Enable Time From De to V_{OD}

6.9 Typical Characteristics

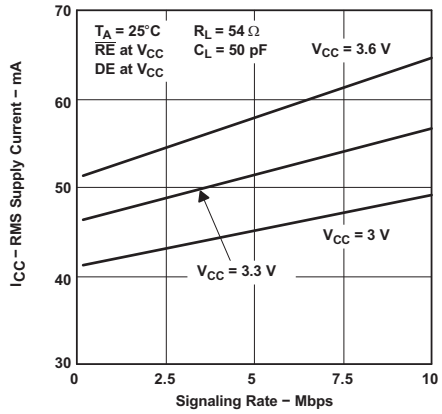


Figure 3. RMS Supply Current vs Signaling Rate

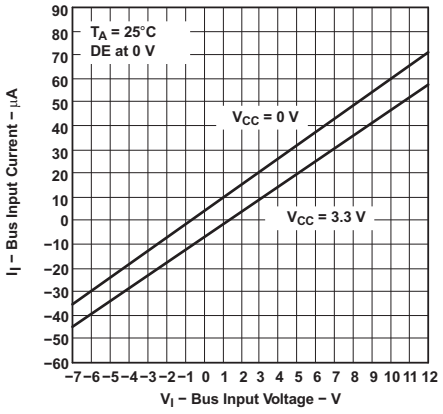


Figure 4. Bus Input Current vs Bus Input Voltage

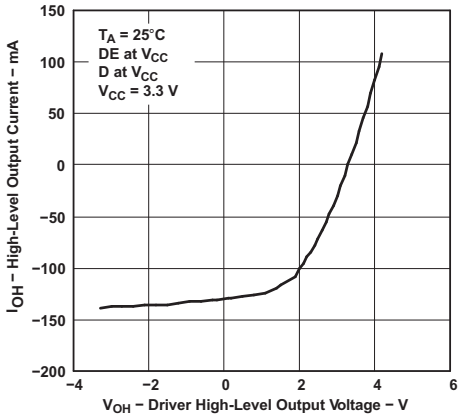


Figure 5. High-Level Output Current vs Driver High-Level Output Voltage

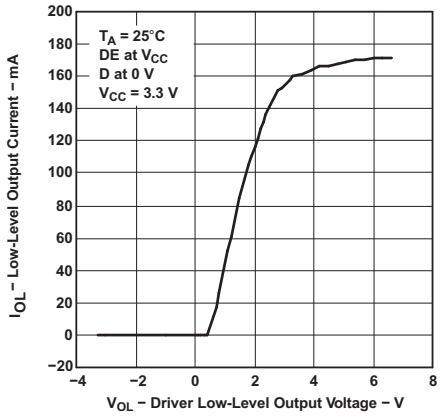


Figure 6. Low-Level Output Current vs Driver Low-Level Output Voltage

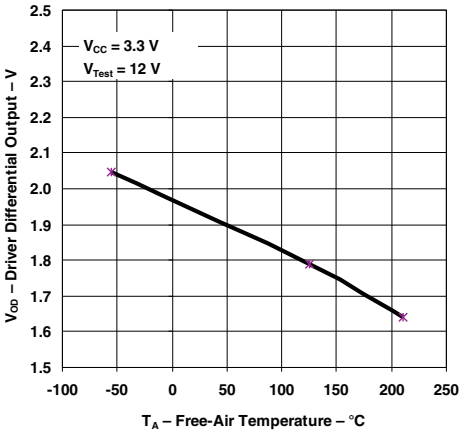


Figure 7. Driver Differential Output vs Free-Air Temperature

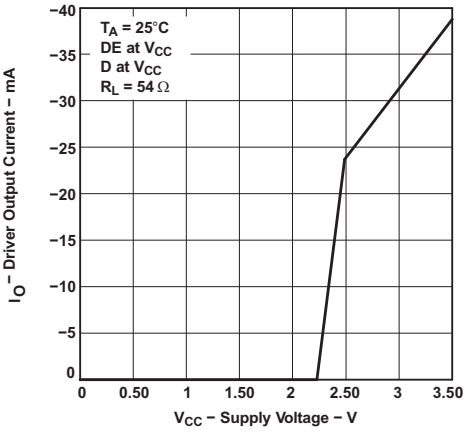


Figure 8. Driver Output Current vs Supply Voltage

Typical Characteristics (continued)

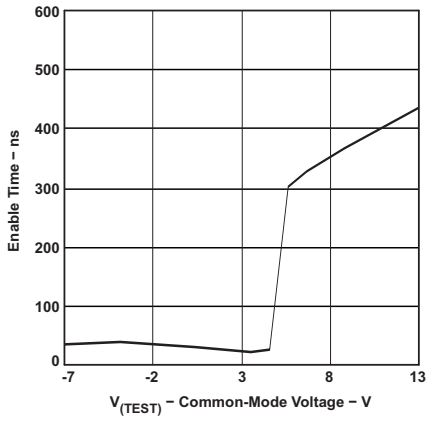


Figure 9. Enable Time vs Common Mode Voltage (See Figure 2)

7 Parameter Measurement Information

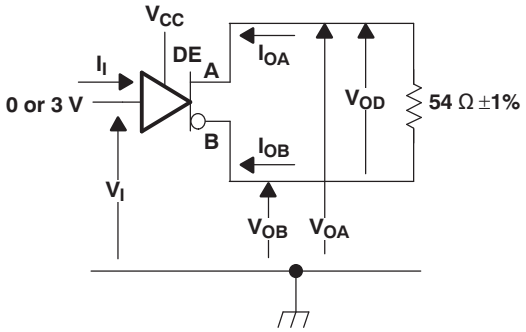


Figure 10. Driver V_{OD} Test Circuit and Voltage and Current Definitions

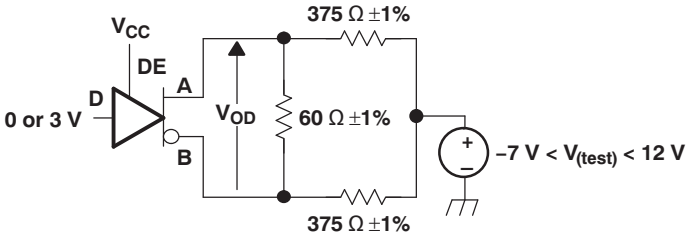
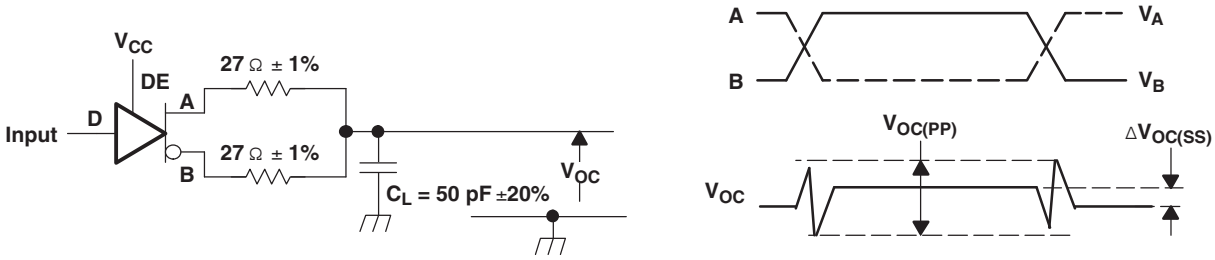
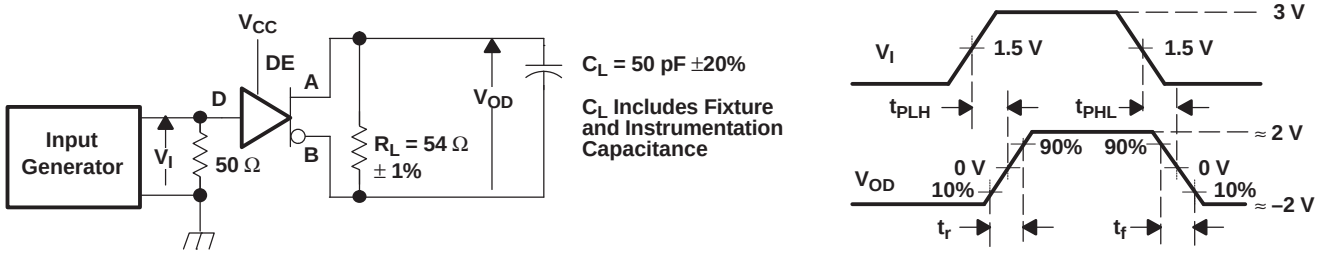


Figure 11. Driver V_{OD} With Common Mode Loading Test Circuit



A. Input: PRR = 500 kHz, 50% Duty Cycle, t_r<6ns, t_f<6ns, Z_O = 50 Ω
B. C_L Includes fixture and instrumentation capacitance

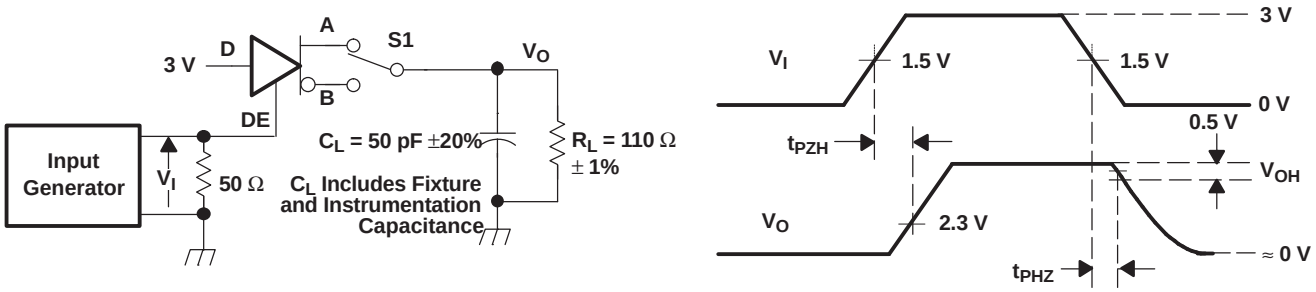
Figure 12. Test Circuit and Definitions for Driver Common Mode Output Voltage



Generator: PRR = 500 kHz, 50% Duty Cycle, t_r <6 ns, t_f <6 ns, Z_o = 50 Ω

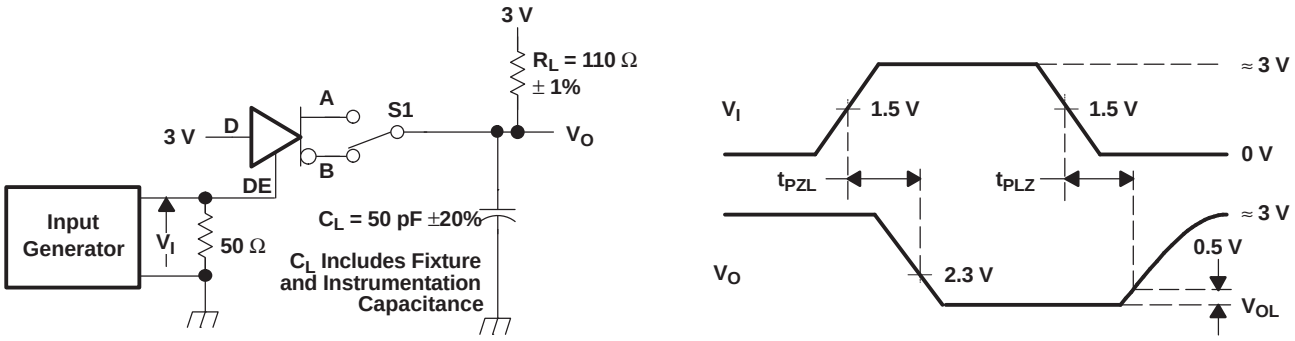
Figure 13. Driver Switching Test Circuit and Voltage Waveforms

Parameter Measurement Information (continued)



Generator: PRR = 500 kHz, 50% Duty Cycle, t_r <6 ns, t_f <6 ns, Z_o = 50 Ω

Figure 14. Driver High-Level Enable and Disable Time Test Circuit and Voltage Waveforms



Generator: PRR = 500 kHz, 50% Duty Cycle, t_r <6 ns, t_f <6 ns, Z_o = 50 Ω

Figure 15. Driver Low-Level Output Enable and Disable Time Test Circuit and Voltage Waveforms

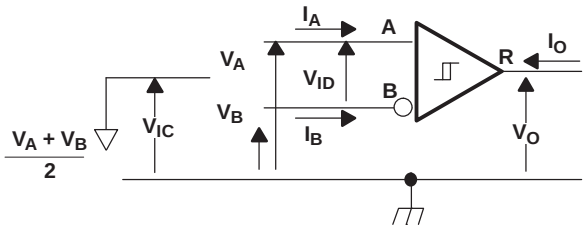


Figure 16. Receiver Voltage and Current Definitions

Parameter Measurement Information (continued)

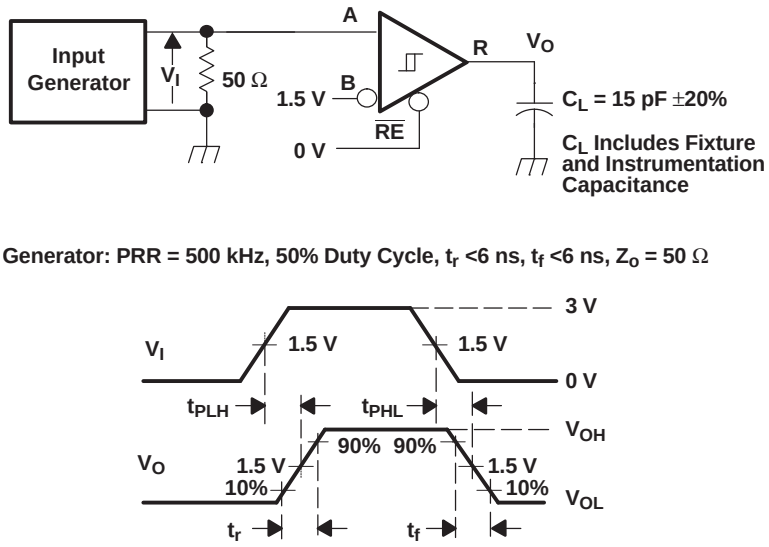
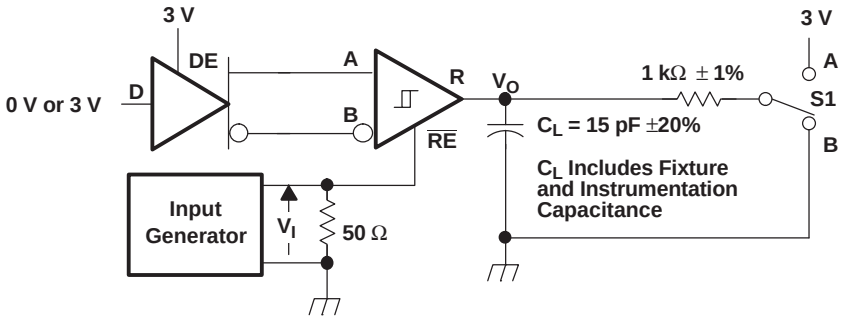


Figure 17. Receiver Switching Test Circuit and Voltage Waveforms



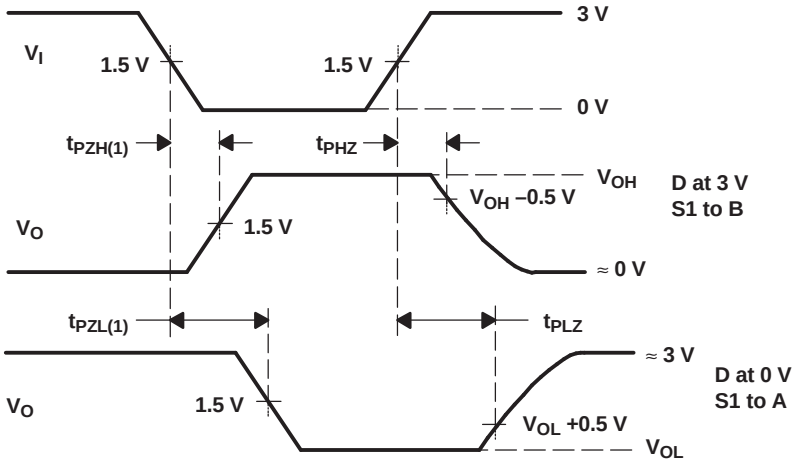


Figure 18. Receiver Enable and Disable Time Test Circuit and Voltage Waveforms With Drivers Enabled

Parameter Measurement Information (continued)

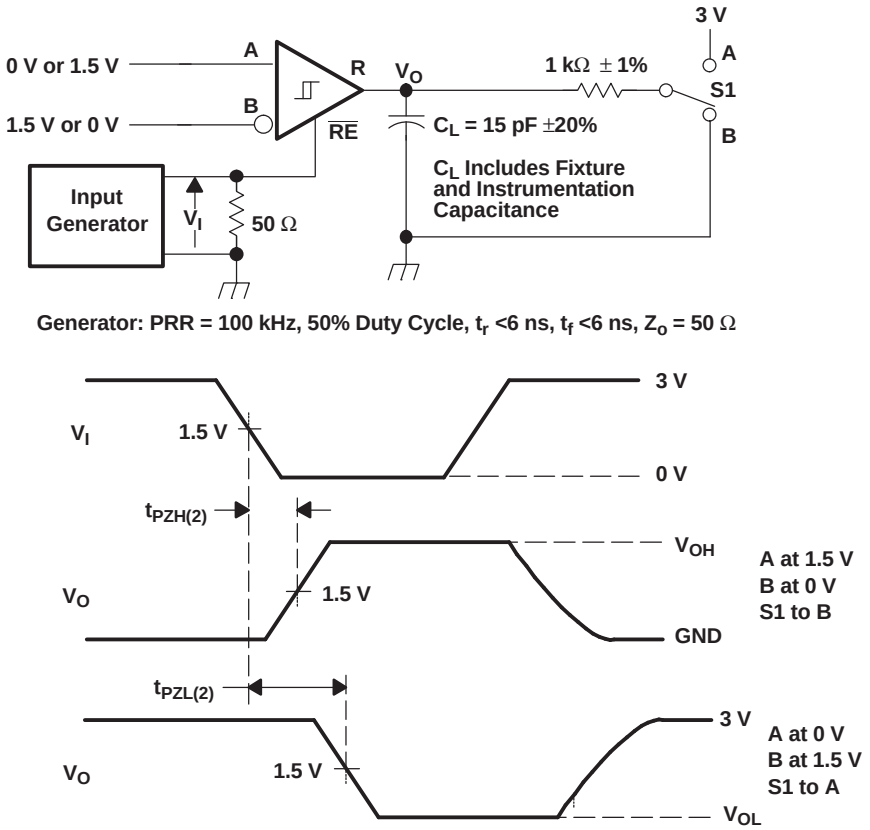
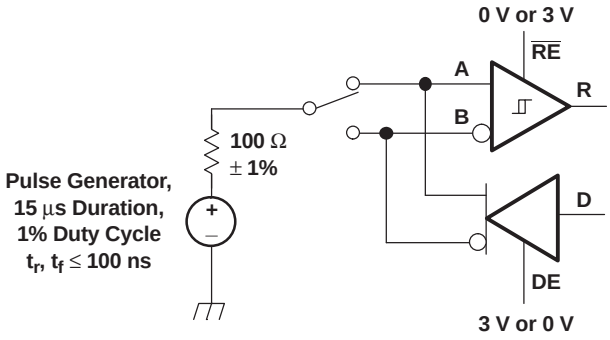


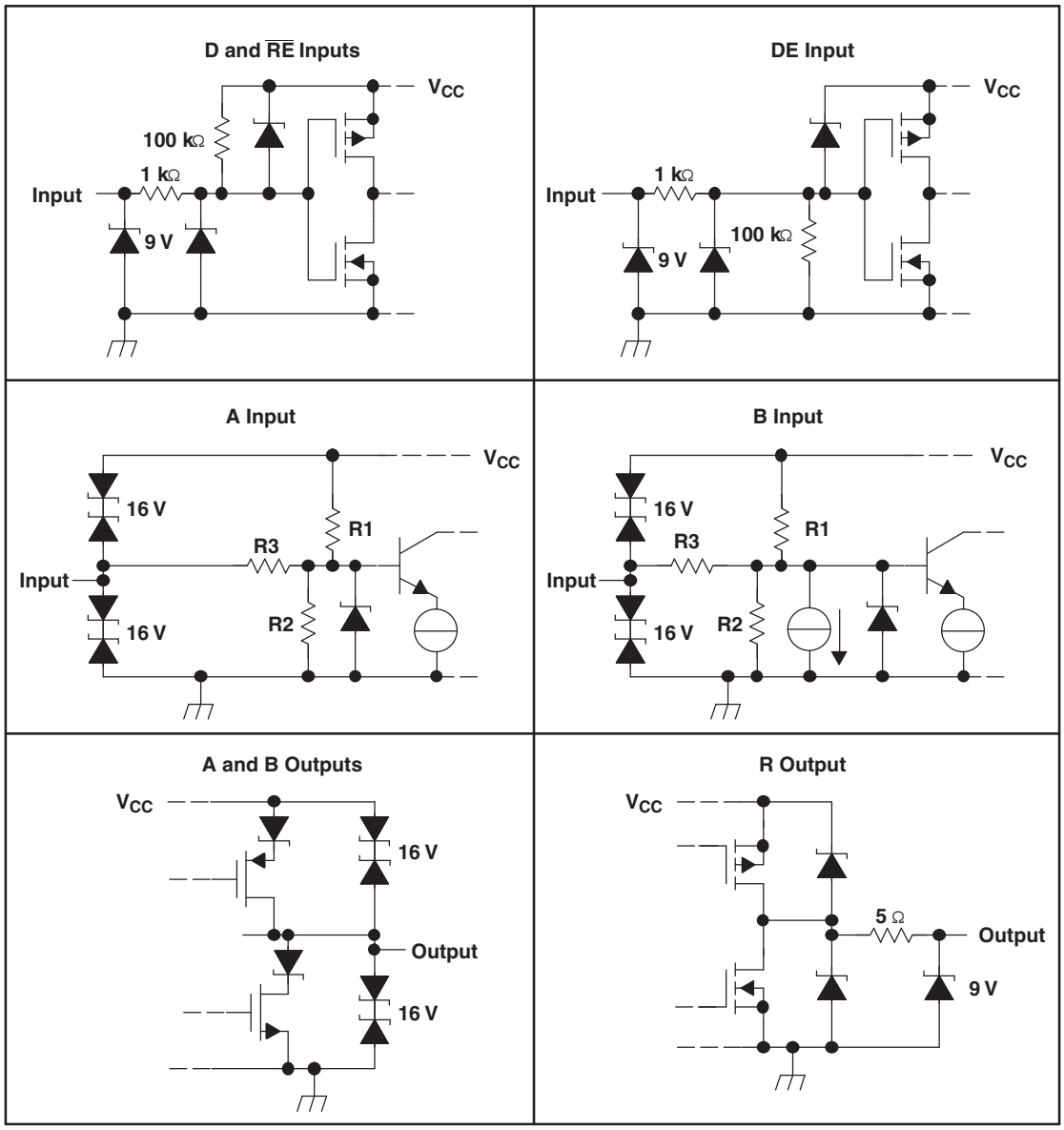
Figure 19. Receiver Enable Time From Standby (Driver Disabled)



NOTE: This test is conducted to test survivability only. Data stability at the R output is not specified.

Figure 20. Test Circuit, Transient Overvoltage Test

Parameter Measurement Information (continued)



R1/R2 = 36 kΩ

R3 = 180 kΩ

Figure 21. Equivalent Input and Output Schematic Diagrams

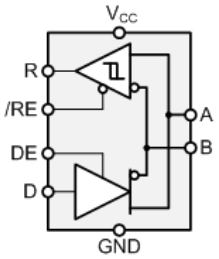
8 Detailed Description

8.1 Overview

The SN65HVD11-HT device is a 3.3 V, half-duplex, RS-485 transceiver available in 3 speed grades suitable for data transmission up to 32 Mbps, 10 Mbps, and 1 Mbps, respectively.

The device has active-high driver enables and active-low receiver enables. A standby current of less than 5 µA can be achieved by disabling both driver and receiver.

8.2 Functional Block Diagram



8.3 Feature Description

Internal ESD protection circuits protect the transceiver bus terminals against ±16-kV Human Body Model (HBM) electrostatic discharges and ±4-kV electrical fast transients (EFT) according to IEC61000-4-4.

The SN65HVD11-HT half-duplex device provides internal biasing of the receiver input thresholds for open-circuit, bus-idle, or short circuit failsafe conditions, and a typical receiver hysteresis of 35 mV.

8.4 Device Functional Modes

When the driver enable pin, DE, is logic high, the differential outputs A and B follow the logic states at data input D. A logic high at D causes A to turn high and B to turn low. In this case the differential output voltage defined as $V_{OD} = V_A – V_B$ is positive. When D is low, the output states reverse, B turns high, A becomes low, and V_{OD} is negative.

When DE is low, both outputs turn high-impedance. In this condition the logic state at D is irrelevant. The DE pin has an internal pulldown resistor to ground; thus, when left open, the driver is disabled (high-impedance) by default. The D pin has an internal pullup resistor to V_{CC}; thus, when left open while the driver is enabled, output A turns high and B turns low.

Table 1. Driver Functions(1)

INPUT	ENABLE	OUTPUTS		FUNCTION
D	DE	A	B	
H	H	H	L	Actively drive bus High
L	H	L	H	Actively drive bus Low
X	L	Z	Z	Driver disabled
X	OPEN	Z	Z	Driver disabled by default
OPEN	H	H	L	Actively drive bus High by default

(1) H = high level; L = low level; Z = high impedance; X = irrelevant; ? = indeterminate

When the receiver enable pin, $\overline{RE}$, is logic low, the receiver is enabled. When the differential input voltage defined as $V_{ID} = V_A - V_B$ is positive and higher than the positive input threshold, V_{IT+}, the receiver output, R, turns high. When V_{ID} is negative and lower than the negative input threshold, V_{IT-}, the receiver output, R, turns low. If V_{ID} is between V_{IT+} and V_{IT-}, the output is indeterminate.

When $\overline{RE}$ is logic high or left open, the receiver output is high-impedance and the magnitude and polarity of V_{ID} are irrelevant. Internal biasing of the receiver inputs causes the output to go failsafe-high when the transceiver is disconnected from the bus (open-circuit), the bus lines are shorted (short-circuit), or the bus is not actively driven (idle bus).

Table 2. Receiver Functions(1)

DIFFERENTIAL INPUT $V_{ID} = V_A - V_B$	ENABLE $\overline{RE}$	OUTPUT R	FUNCTION
$V_{ID} > V_{IT+}$	L	H	Receive valid bus High
$V_{IT-} < V_{ID} < V_{IT+}$	L	?	Indeterminate bus state
$V_{ID} < V_{IT-}$	L	L	Receive valid bus Low
X	H	Z	Receiver disabled
X	OPEN	Z	Receiver disabled by default
Open-circuit bus	L	H	Fail-safe high output
Short circuit bus	L	H	Fail-safe high output

(1) H = high level; L = low level; Z = high impedance; X = irrelevant; ? = indeterminate

8.4.1 Low-Power Standby Mode

When both the driver and receiver are disabled (DE low and $\overline{RE}$ high) the device is in standby mode. If the enable inputs are in this state for less than 60 ns, the device does not enter standby mode. This guards against inadvertently entering standby mode during driver or receiver enabling. Only when the enable inputs are held in this state for 300 ns or more, the device is assured to be in standby mode. In this low-power standby mode, most internal circuitry is powered down, and the supply current is typically less than 1 µA. When either the driver or the receiver is reenabled, the internal circuitry becomes active.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN65HVD11-HT is a half-duplex RS-485 transceiver commonly used for asynchronous data transmissions. The driver and receiver enable pins allow for the configuration of different operating modes.

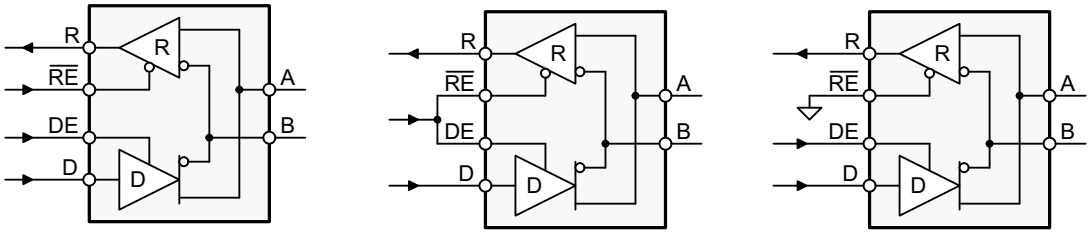


Figure 22. Half-Duplex Transceiver Configurations

a. Using independent enable lines provides the most flexible control as it allows for the driver and the receiver to be turned on and off individually. While this configuration requires two control lines, it allows for selective listening into the bus traffic, whether the driver is transmitting data or not.

b. Combining the enable signals simplifies the interface to the controller by forming a single direction-control signal. In this configuration, the transceiver operates as a driver when the direction-control line is high, and as a receiver when the direction-control line is low.

c. Only one line is required when connecting the receiver-enable input to ground and controlling only the driver-enable input. In this configuration, a node not only receives the data from the bus, but also the data it sends and can verify that the correct data have been transmitted.

9.2 Typical Application

An RS-485 bus consists of multiple transceivers connected in parallel to a bus cable. To eliminate line reflections, each cable end is terminated with a termination resistor, R_T, whose value matches the characteristic impedance, Z_0, of the cable. This method, known as parallel termination, allows for higher data rates over a longer cable length.

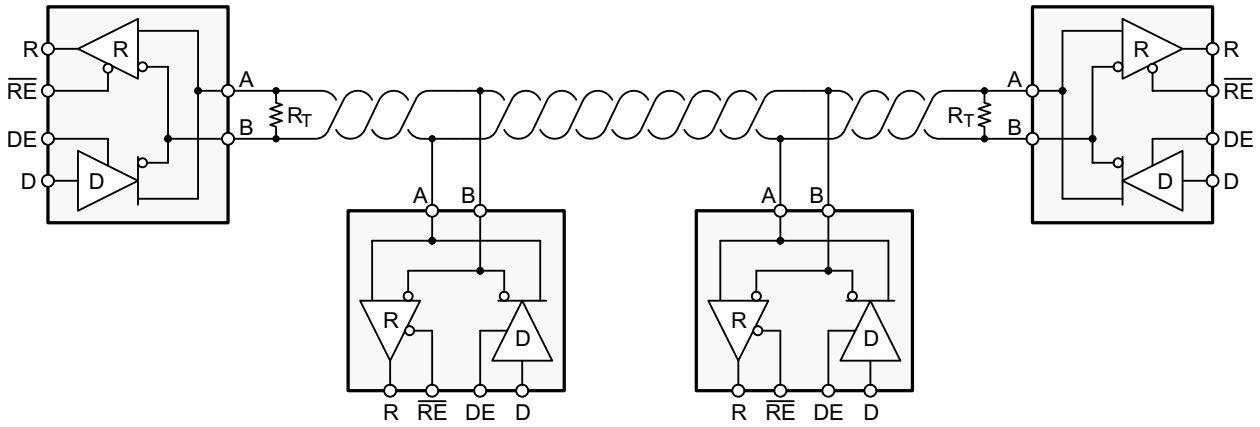


Figure 23. Typical RS-485 Network With Half-Duplex Transceivers

9.2.1 Design Requirements

RS-485 is a robust electrical standard suitable for long-distance networking that may be used in a wide range of applications with varying requirements, such as distance, data rate, and number of nodes.

9.2.1.1 Data Rate and Bus Length

There is an inverse relationship between data rate and bus length, meaning the higher the data rate, the shorter the cable length; and conversely, the lower the data rate, the longer the cable may be without introducing data errors. While most RS-485 systems use data rates between 10 kbps and 100 kbps, some applications require data rates up to 250 kbps at distances of 4000 feet and longer. Longer distances are possible by allowing for small signal jitter of up to 5 or 10%.

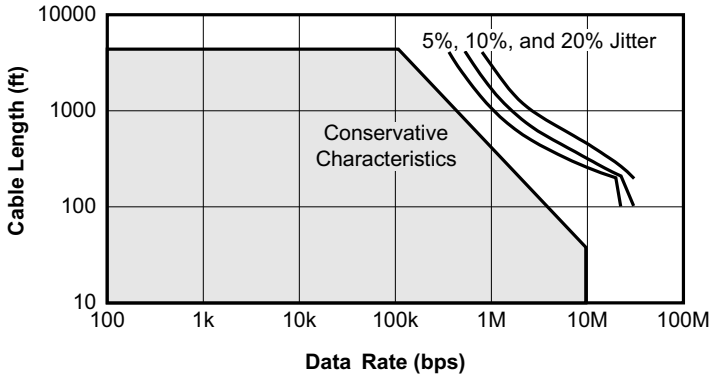


Figure 24. Cable Length vs Data Rate Characteristic

Typical Application (continued)

9.2.1.2 Stub Length

When connecting a node to the bus, the distance between the transceiver inputs and the cable trunk, known as the stub, should be as short as possible. Stubs present a nonterminated piece of bus line which can introduce reflections as the length of the stub increases. As a general guideline, the electrical length, or round-trip delay, of a stub should be less than one-tenth of the rise time of the driver, thus giving a maximum physical stub length as shown in Equation 1.

$$L_{(STUB)} \leq 0.1 \times t_r \times v \times c \quad (1)$$

where

- t_r is the 10/90 rise time of the driver
- v is the signal velocity of the cable or trace as a factor of c
- c is the speed of light (3×10^8 m/s)

Per Equation 1, Table 3 lists the maximum cable-stub lengths for the minimum-driver output rise-times of the SN65HVD1x full-duplex family of transceivers for a signal velocity of 78%.

Table 3. Maximum Stub Length

DEVICE	MINIMUM DRIVER OUTPUT RISE TIME (ns)	MAXIMUM STUB LENGTH	
		(m)	(ft)
SN65HVD11-HT	10	0.23	0.75

9.2.1.3 Bus Loading

The RS-485 standard specifies that a compliant driver must be able to driver 32 unit loads (UL), where 1 unit load represents a load impedance of approximately 12 kΩ. Because the SN65HVD11-HT and HVD12 are each 1/8 UL transceivers, it is possible to connect up to 256 receivers to the bus. The SN65HVD11-HT is a 1/4 UL transceiver, and up to 64 receivers may be connected to the bus.

9.2.1.4 Receiver Failsafe

The differential receivers of the SN65HVD11-HT are failsafe to invalid bus states caused by:

- Open bus conditions, such as a disconnected connector
- Shorted bus conditions, such as cable damage shorting the twisted-pair together
- Idle bus conditions that occur when no driver on the bus is actively driving.

In any of these cases, the differential receiver will output a failsafe logic High state so that the output of the receiver is not indeterminate.

Receiver failsafe is accomplished by offsetting the receiver thresholds such that the input indeterminate range does not include zero volts differential. To comply with the RS-422 and RS-485 standards, the receiver output must output a High when the differential input V_{ID} is more positive than 200 mV, and must output a Low when V_{ID} is more negative than –200 mV. The receiver parameters which determine the failsafe performance are $V_{IT(+)}$ and $V_{IT(–)}$. As shown in *Receiver Electrical Characteristics*, differential signals more negative than –200 mV will always cause a Low receiver output, and differential signals more positive than 200 mV will always cause a High receiver output.

When the differential input signal is close to zero, it is still above the maximum $V_{IT(+)}$ threshold of –10 mV, and the receiver output will be High.

9.2.2 Detailed Design Procedure

To protect bus nodes against high-energy transients, the implementation of external transient protection devices is therefore necessary. Figure 25 shows a protection circuit against 10-kV ESD (IEC 61000-4-2), 4-kV EFT (IEC 61000-4-4), and 1-kV surge (IEC 61000-4-5) transients.

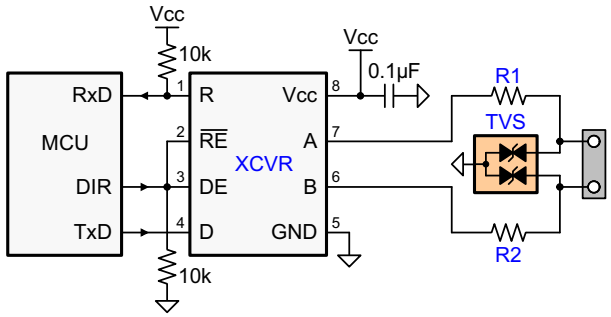


Figure 25. Transient Protection Against ESD, EFT, and Surge Transients

Table 4. Bill of Materials

DEVICE	FUNCTION	ORDER NUMBER	MANUFACTURER
XCVR	3.3-V, full-duplex RS-485 transceiver	SN65HVD11-HT	TI
R1, R2	10-Ω, pulse-proof, thick-film resistor	CRCW0603010RJNEAHP	Vishay
TVS	Bidirectional 400-W transient suppressor	CDSOT23-SM712	Bourns

9.2.3 Application Curve

Figure 26 demonstrates operation of the SN65HVD11-HT at a signaling rate of 250 kbps. Two SN65HVD11-HT transceivers are used to transmit data through a 2000 foot (600 m) segment of Commscope 5524 category 5e+ twisted pair cable. The bus is terminated at each end by a 100-Ω resistor, matching the cable characteristic impedance.

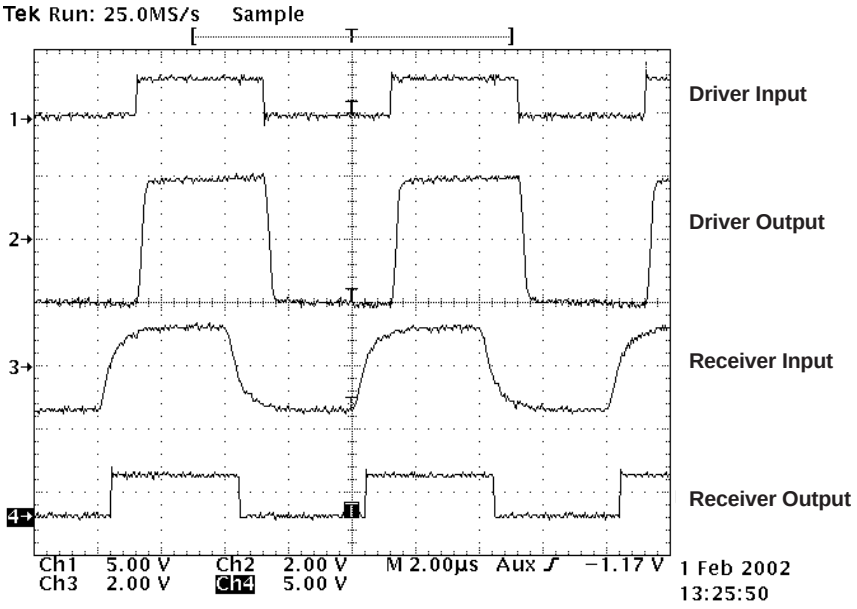


Figure 26. SN65HVD11-HT Input and Output Through 2000 Feet of Cable

10 Power Supply Recommendations

To assure reliable operation at all data rates and supply voltages, each supply must be buffered with a 100-nF ceramic capacitor located as close to the supply pins as possible. The TPS76333 linear voltage regulator is suitable for the 3.3-V supply.

11 Layout

11.1 Layout Guidelines

On-chip IEC-ESD protection is sufficient for laboratory and portable equipment but never sufficient for EFT and surge transients occurring in industrial environments. Therefore, robust and reliable bus node design requires the use of external transient protection devices.

Because ESD and EFT transients have a wide frequency bandwidth from approximately 3 MHz to 3 GHz, high-frequency layout techniques must be applied during PCB design.

1. Place the protection circuitry close to the bus connector to prevent noise transients from entering the board.
2. Use V_{CC} and ground planes to provide low-inductance. High-frequency currents follow the path of least inductance and not the path of least impedance.
3. Design the protection components into the direction of the signal path. Do not force the transient currents to divert from the signal path to reach the protection device.
4. Apply 100-nF to 220-nF bypass capacitors as close as possible to the V_{CC} pins of transceiver, UART, and controller ICs on the board.
5. Use at least two vias for V_{CC} and ground connections of bypass capacitors and protection devices to minimize effective via-inductance.
6. Use 1-kΩ to 10-kΩ pullup or pulldown resistors for enable lines to limit noise currents in these lines during transient events.
7. Insert pulse-proof series resistors into the A and B bus lines if the TVS clamping voltage is higher than the specified maximum voltage of the transceiver bus terminals. These resistors limit the residual clamping current into the transceiver and prevent it from latching up.
8. While pure TVS protection is sufficient for surge transients up to 1 kV, higher transients require metal-oxide varistors (MOVs) which reduce the transients to a few hundred volts of clamping voltage, and transient blocking units (TBUs) that limit transient current to less than 1 mA.

11.2 Layout Example

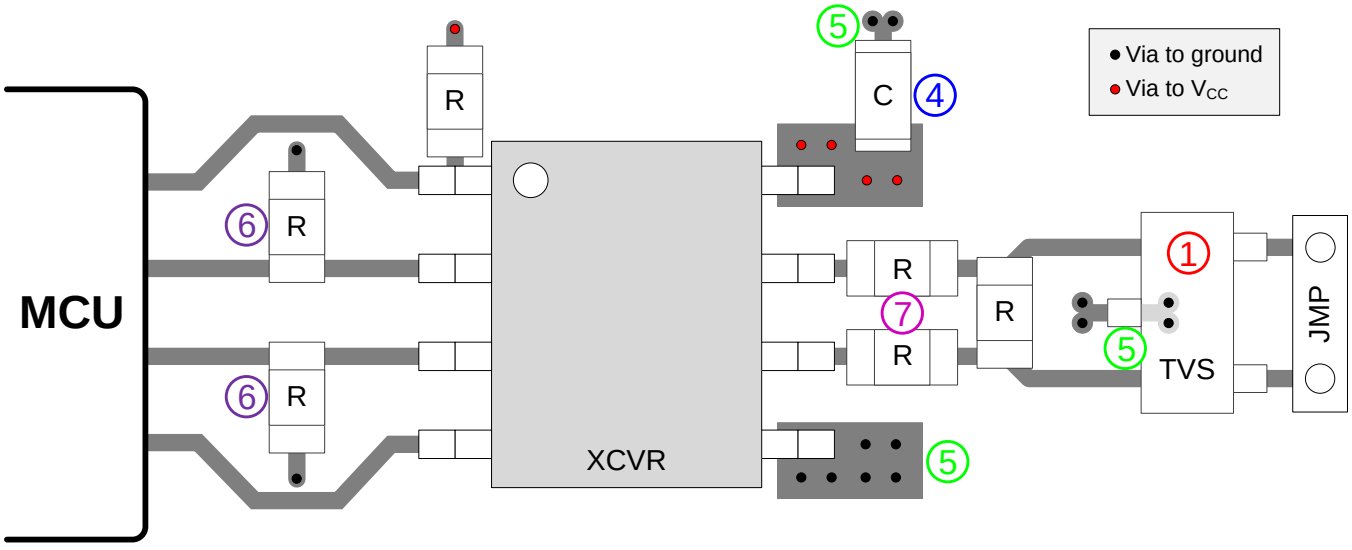


Figure 27. SN65HVD11-HT Layout Example

11.3 Thermal Considerations

$R_{\theta JA}$ (Junction-to-Ambient Thermal Resistance) is defined as the difference in junction temperature to ambient temperature divided by the operating power.

$R_{\theta JA}$ is *not* a constant and is a strong function of:

- the PCB design (50% variation)
- altitude (20% variation)
- device power (5% variation)

$R_{\theta JA}$ can be used to compare the thermal performance of packages if the specific test conditions are defined and used. Standardized testing includes specification of PCB construction, test chamber volume, sensor locations, and the thermal characteristics of holding fixtures. θ_{JA} is often misused when it is used to calculate junction temperatures for other installations.

TI uses two test PCBs as defined by JEDEC specifications. The low-k board gives *average* in-use condition thermal performance, and it consists of a single copper trace layer 25-mm long and 2-oz thick. The high-k board gives best *case* in-use condition, and it consists of two 1-oz buried power planes with a single copper trace layer 25-mm long and 2-oz thick. A 4% to 50% difference in θ_{JA} can be measured between these two test cards.

$R_{\theta JC}$ (Junction-to-Case Thermal Resistance) is defined as difference in junction temperature to case divided by the operating power. It is measured by putting the mounted package up against a copper block cold plate to force heat to flow from die, through the mold compound into the copper block.

$R_{\theta JC}$ is a useful thermal characteristic when a heatsink is applied to package. It is *not* a useful characteristic to predict junction temperature because it provides pessimistic numbers if the case temperature is measured in a nonstandard system and junction temperatures are backed out. It can be used with θ_{JB} in 1-dimensional thermal simulation of a package system.

$R_{\theta JB}$ (Junction-to-Board Thermal Resistance) is defined as the difference in the junction temperature and the PCB temperature at the center of the package (closest to the die) when the PCB is clamped in a cold-plate structure. θ_{JB} is only defined for the high-k test card.

$R_{\theta JB}$ provides an overall thermal resistance between the die and the PCB. It includes a bit of the PCB thermal resistance (especially for BGA's with thermal balls) and can be used for simple 1-dimensional network analysis of package system, see Figure 28.

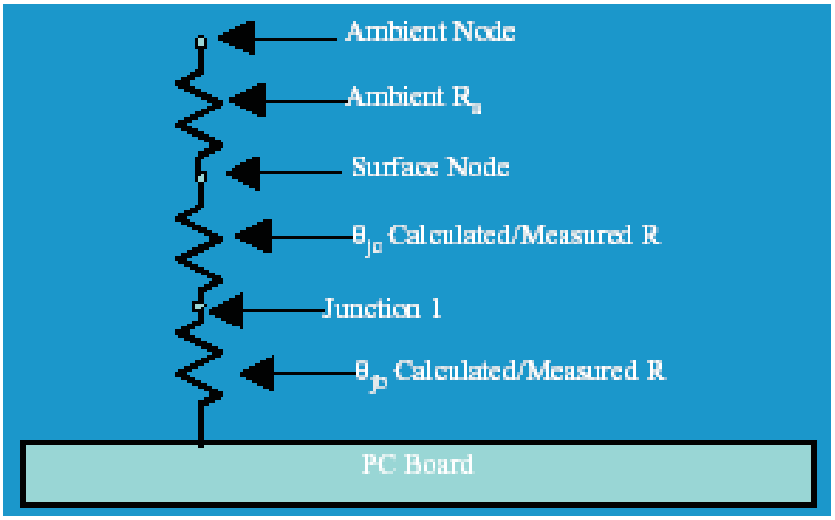


Figure 28. Thermal Resistance

12 Device and Documentation Support

12.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65HVD11HD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 175	HD11	Samples
SN65HVD11SHKJ	ACTIVE	CFP	HKJ	8	25	RoHS & Green	Call TI	N / A for Pkg Type	-55 to 210	SN65HVD11S HKJ	Samples
SN65HVD11SHKQ	ACTIVE	CFP	HKQ	8	25	RoHS & Green	AU	N / A for Pkg Type	-55 to 210	HVD11S HKQ	Samples
SN65HVD11SJD	ACTIVE	CDIP SB	JDJ	8	1	RoHS & Green	Call TI	N / A for Pkg Type	-55 to 210	SN65HVD11SJD	Samples
SN65HVD11SKGDA	ACTIVE	XCEPT	KGD	0	130	RoHS & Green	Call TI	N / A for Pkg Type	-55 to 210		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

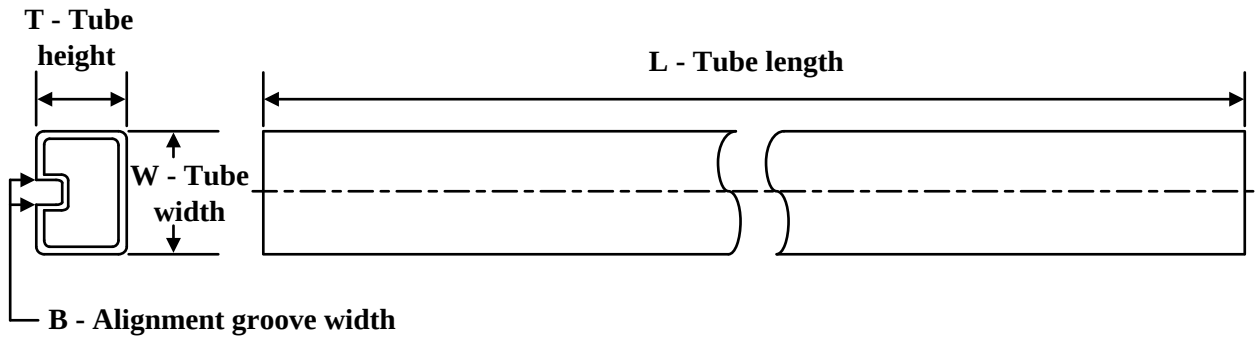
OTHER QUALIFIED VERSIONS OF SN65HVD11-HT :

- Catalog : SN65HVD11

NOTE: Qualified Version Definitions:

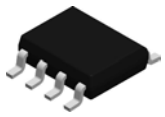
- Catalog - TI's standard catalog product

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN65HVD11HD	D	SOIC	8	75	507	8	3940	4.32
SN65HVD11SHKJ	HKJ	CFP	8	25	506.98	26.16	6220	NA
SN65HVD11SHKQ	HKQ	CFP	8	25	506.98	26.16	6220	NA

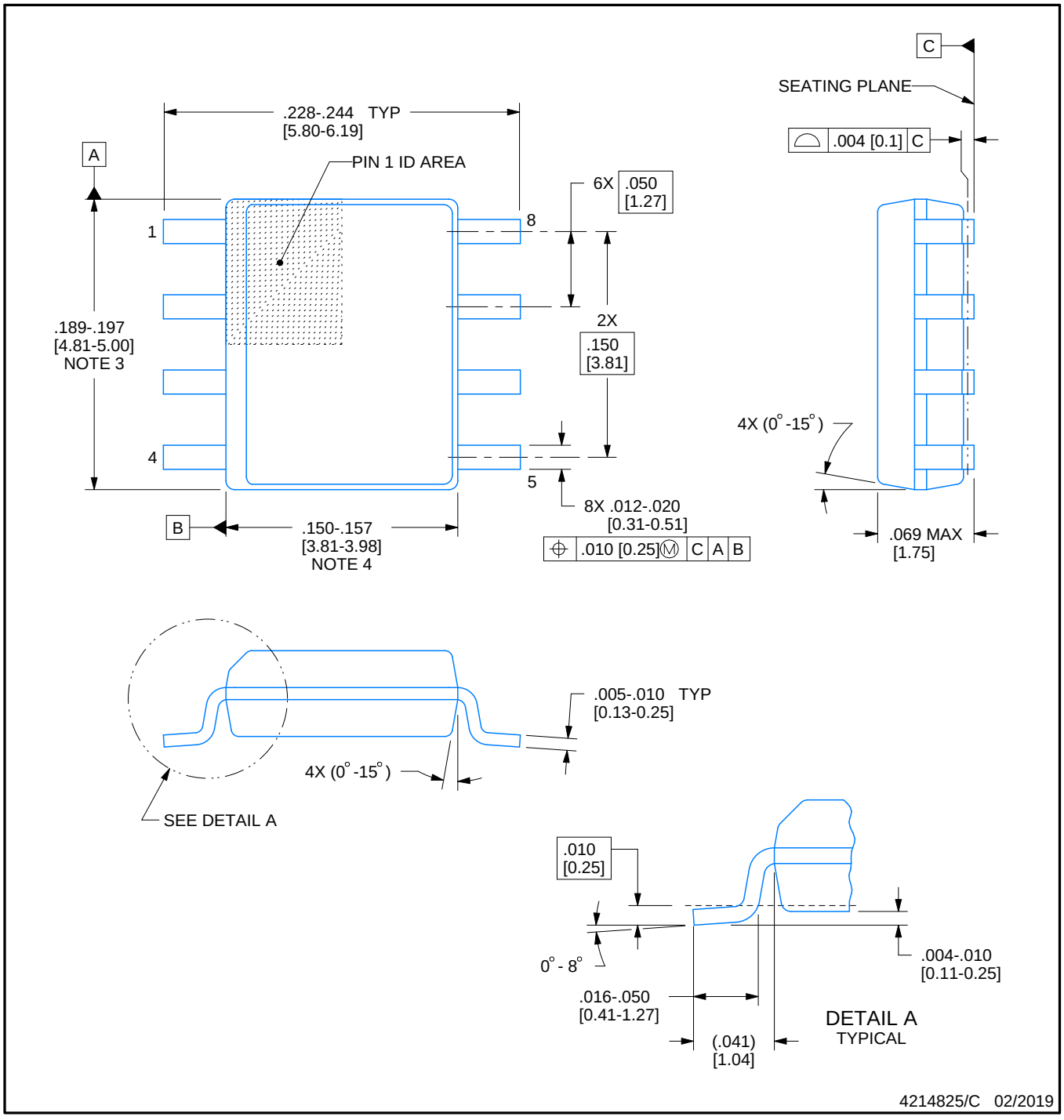


PACKAGE OUTLINE

D0008A

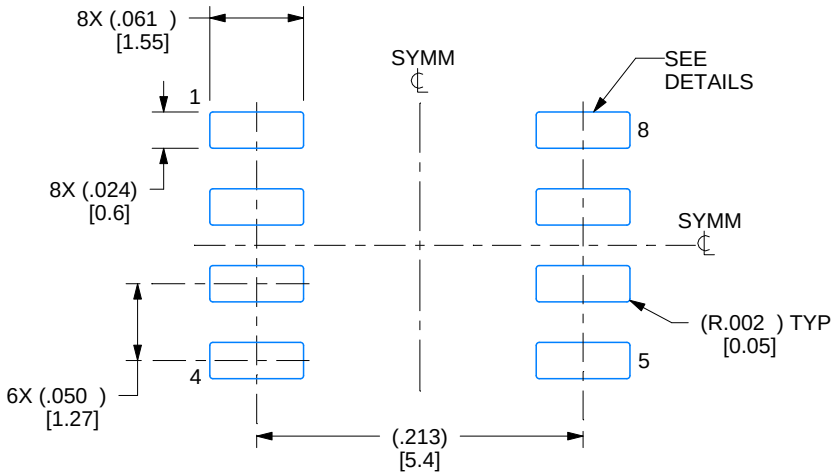
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

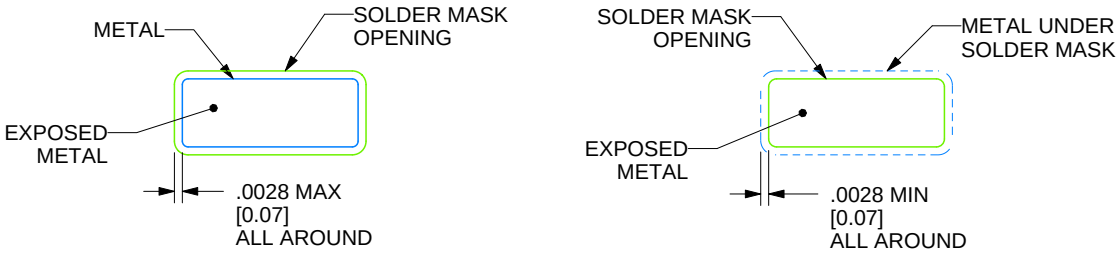


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

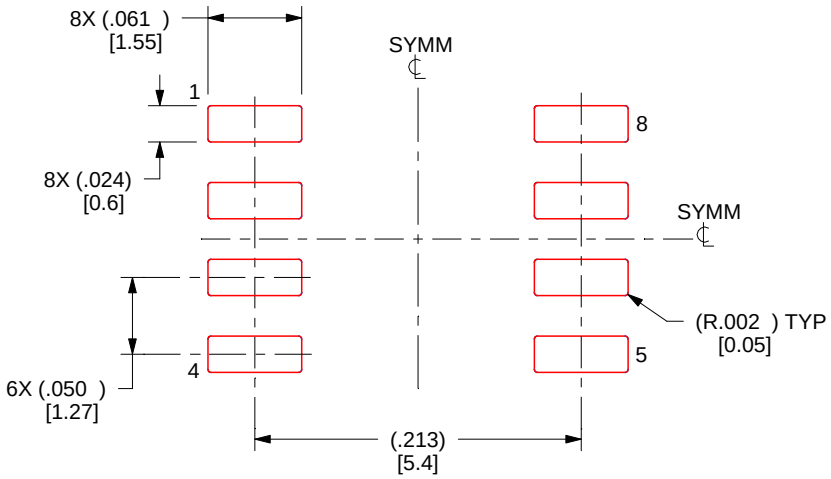
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



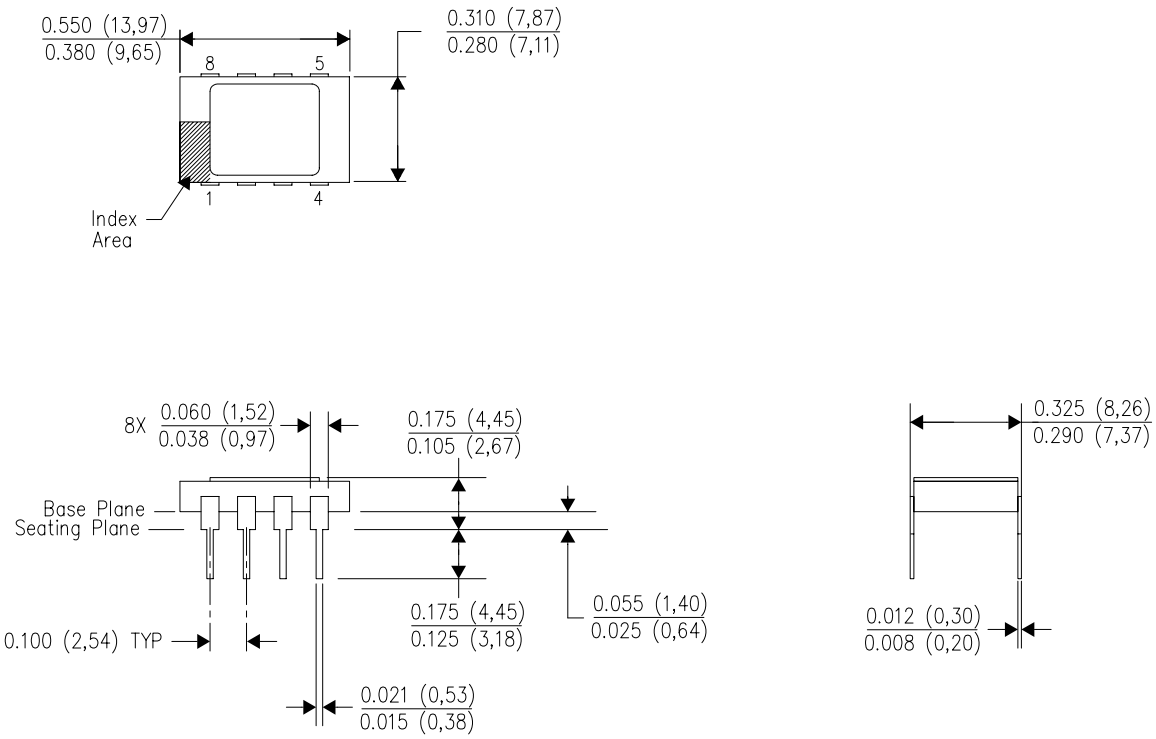
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

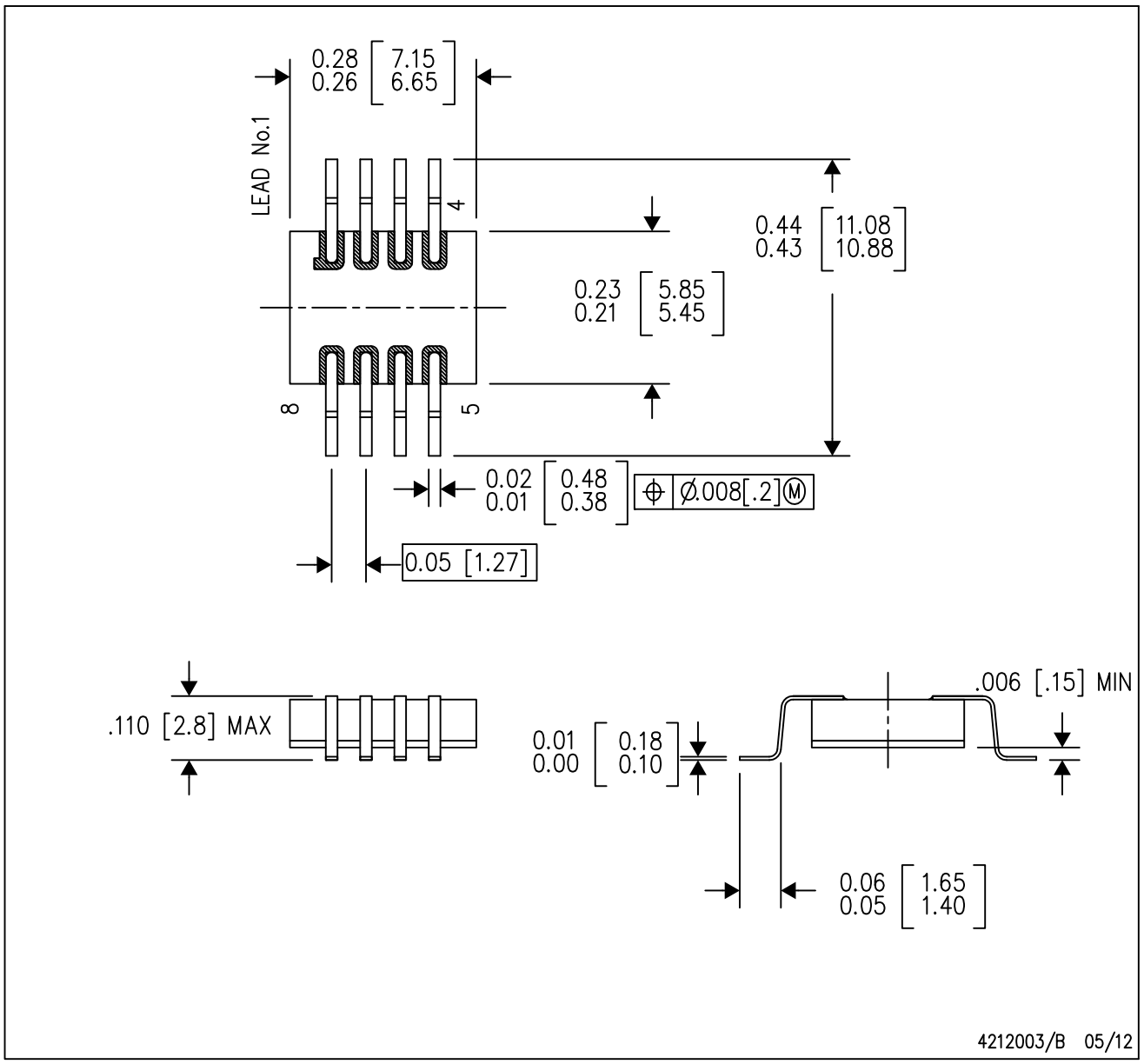
JDJ (R–CDIP–T8) CERAMIC DUAL IN–LINE PACKAGE



4202646–2/B 07/10

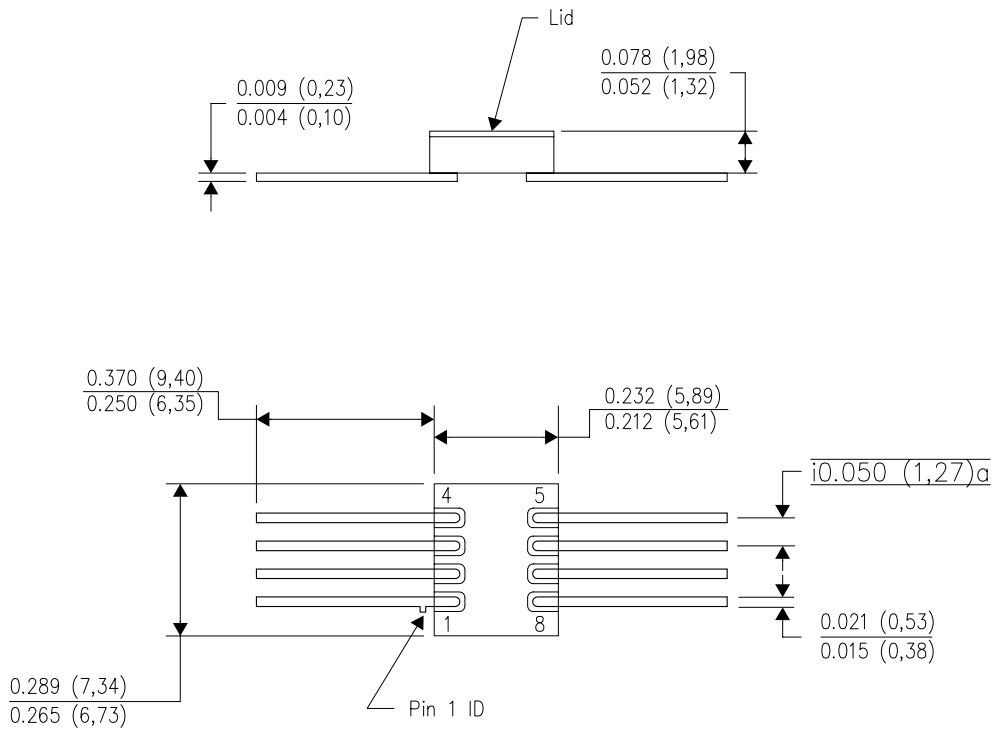
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Ceramic quad flatpack with flat leads brazed to non–conductive tie bar carrier.
D. This package is hermetically sealed with a metal lid.
E. The leads are gold plated and can be solderdipped.
F. Leads not shown for clarity purposes.
G. Lid and heat sink are connected to GND leads.

HKQ (R–CDFP–G8) CERAMIC GULL WING



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals will be gold plated.
E. Lid is not connected to any lead.

HKJ (R–CDFP–F8) CERAMIC DUAL FLATPACK



4209892/A 10/08

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals will be gold plated.

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