PRODUCT/PROCESS CHANGE NOTIFICATION

PCN IPG-IPC/14/8696
Dated 23 Sep 2014

New DIE for Darlington Array ULQ2003 and ULN2003

Table 1. Change Implementation Schedule

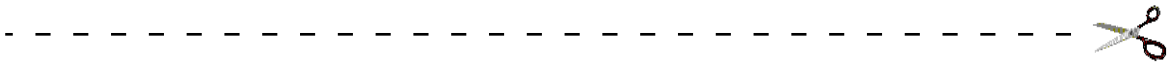
Forecasted implementation date for change	15-Dec-2014
Forecasted availability date of samples for customer	16-Sep-2014
Forecasted date for **STMicroelectronics** change Qualification Plan results availability	16-Sep-2014
Estimated date of changed product first shipment	23-Dec-2014

Table 2. Change Identification

Product Identification (Product Family/Commercial Product)	see attached list
Type of change	Product design change
Reason for change	New equipment utilization, capacity optimization, better performance
Description of the change	Following Divisional Commitments towards a continuous improvement philosophy, a new DIE for Darlington Array ULQ2003 and ULN2003 has been introduced. Same diffusion, assembly and testing location are maintained. No process change. Quality and electrical performances are guaranteed
Change Product Identification	QA number
Manufacturing Location(s)	

Table 3. List of Attachments

Customer Part numbers list	
Qualification Plan results	



Customer Acknowledgement of Receipt	**PCN IPG-IPC/14/8696**
Please sign and return to STMicroelectronics Sales Office	**Dated 23 Sep 2014**

☐ Qualification Plan Denied	Name:
☐ Qualification Plan Approved	Title:
	Company:
☐ Change Denied	Date:
☐ Change Approved	Signature:

Remark

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DOCUMENT APPROVAL

Name	Function
Riviera, Antonio	Marketing Manager
Naso, Lorenzo	Product Manager
Moretti, Paolo	Q.A. Manager

WHAT:

Following Divisional Commitments towards a continuous improvement philosophy, a new DIE for Darlington Array ULQ2003 and ULN2003 has been introduced.
Same diffusion, assembly and testing location are maintained. No process change. Quality and electrical performances are guaranteed.

For the complete list of the part numbers affected by the change, please refer to the attached Products list.

WHY:
New equipment utilization, capacity optimization, better performance.
This manufacturing change will improve service to ST Customers.

HOW:
The qualification program mainly consist of reliability tests and comparative electrical characterizations.
The related reliability report is annexed to this document.

WHEN:

The implementation will be finalized within Week 50-14

Marking and traceability:

Unless otherwise stated by customer specific requirement, the traceability of the parts assembled with the new die will be ensured by the Q.A. number.

The changed here reported will not affect the electrical, dimensional and thermal parameters keeping unchanged all information reported on the relevant datasheets.
There is as well no change in the packing process or in the standard delivery quantities.

Lack of acknowledgement of the PCN within 30 days will constitute acceptance of the change. After acknowledgement, lack of additional response within the 90 day period will constitute acceptance of the change (Jedec Standard No. 46-C).
In any case, first shipments may start earlier with customer’s written agreement.

Reliability Report

Reliability Qualification on

T.V.:ULQ2003D1013TR

New die with layout optimization

General Information	
Product Line	L20303
Product Description	SEVEN DARLINGTON ARRAYS
P/N	ULQ2003D1013TR
Product Group	IPG
Product division	IND.& POWER CONV.
Packages	SO16
Silicon Process technology	BIPOLAR

Locations	
Wafer fab	*Ang Mo Kio*
Assembly plant	*SHENZHEN*
Reliability Lab	*ST Catania*

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comment
1.0	August 2014	8	Angelo Basile	Giovanni Presti	Final Report

TABLE OF CONTENTS

1 APPLICABLE AND REFERENCE DOCUMENTS 3
2 GLOSSARY 3
3 RELIABILITY EVALUATION OVERVIEW 3
3.1 OBJECTIVES 3
3.2 CONCLUSION 3
4 DEVICE CHARACTERISTICS 4
4.1 DEVICE DESCRIPTION 4
4.2 CONSTRUCTION NOTE 4
5 TESTS RESULTS SUMMARY 5
5.1 TEST VEHICLE 5
5.2 TEST PLAN AND RESULTS SUMMARY 5
6 ANNEXES 6
6.1 DEVICE DETAILS 6

1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits

2 GLOSSARY

DUT	Device Under Test
SS	Sample Size

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

Qualifications of the New die *with layout optimization*

3.2 Conclusion

Qualification Plan requirements have been fulfilled without exception. It is stressed that reliability tests have shown that the devices behave correctly against environmental tests (no failure)

The present reliability final report is positive

4 DEVICE CHARACTERISTICS

4.1 Device description

The ULQ2001A, ULQ2002A, ULQ2003 andULQ2004A are high voltage, high current darlington arrays each containing seven open collector darlington pairs with common emitters. Each channel is rated at 500 mA and can withstand peak currents of600 mA. Suppression diodes are included for inductive load driving and the inputs are pinned opposite the outputs to simplify board layout. The four versions interface to all common logic These versatile devices are useful for driving a wide range of loads including solenoids, relays DC motors,LED displays filament lamps, thermal printheads and high power buffers.The ULQ2001A/2002A/2003A and 2004A are supplied in 16 pin plastic DIP packages with a copper leadframe to reduce thermal resistance. They are available also in small outline package (SO-16) as ULQ2001D1/2002D1/2003D1/2004D1.

4.2 Construction note

P/N	***ULQ2003D1013TR***
Wafer/Die fab. information	
Wafer fab manufacturing location	Ang Mo Kio
Technology	BiP > 6um
Die finishing back side	CHROMIUM/NICKEL/GOLD
Die size	2280, 1200 micron
Passivation type	SiN (nitride)
Prod. Mask Set Rev.	CL203D REV A for DIE CODE : PL
Wafer Testing (EWS) information	
Electrical testing manufacturing location	Ang Mo Kio EWS
Tester	ASL1000
Test program	CL203CB6_0200.ZIP
Assembly information	
Assembly site	SHENZHEN
Package description	SO 16
Molding compound	Epoxy
Frame material	FRAME SO 16L 94x150 SHD OpC 8fus 4Layers
Die attach material	Epoxy
Wires bonding materials/diameters	WIRE Cu D1.0
Final testing information	
Testing location	SHENZHEN
Tester	ASL 1000
Test program	L203_STS_FA_01.prg

5 TESTS RESULTS SUMMARY

5.1 Test vehicle

Lot #	Diffusion Lot	Assy Lot	Thecn code	Process/ Package	Product Line	Comments
1	641107HD#25	GK420TV01	PZQ7*L203DA6	SO16	L20303	

5.2 Test plan and results summary

P/N

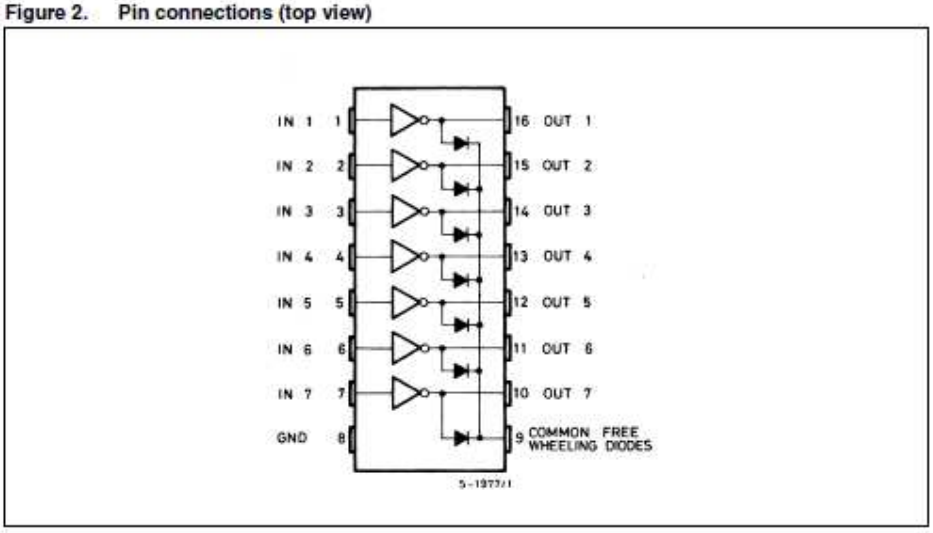
Test	PC	Std ref.	Conditions	SS	Steps h=hours cy=cycles	Failure/SS LOT 1	Note
Die Oriented Tests							
HTOL	N	JESD22 A-108	Tj = 125° C BIAS= Vin=+ 50V	77	168h	0/77	
					500h	0/77	
					1000h	0/77	
HTSL	N	JESD22 A-103	Ta = 150°C	45	168h	0/45	
					500h	0/45	
					1000h	0/45	
Package Oriented Tests							
PC	Y	JESD22 A-113	Drying 24 H@ 125° C Store 168H @ Ta=85°C Rh=85% Over Reflow @ Tpeak=260° C 3 times	231	168H	PASS	
AC	Y	JESD22 A-102	Pa=2Atm / Ta=121°C	77	168h	0/77	
THB	Y	JESD22 A-101	Ta = 85°C, Rh=85% Vbias +35V	77	168h	0/77	
					500h	0/77	
					1000h	0/77	
TC	Y	JESD22 A-104	Ta = -65°C to 150°C	77	100cy	0/77	
					300cy	0/77	
					500cy	077	
Other Tests							
ESD	N	JEDEC JS001	HBM	3	+/- 3KV	Pass	
		JESD22-C101	CDM	3	+/- 500V	Pass	

6 ANNEXES

6.1 Device details

6.1.1 Pin connection

Figure 2. Pin connections (top view)

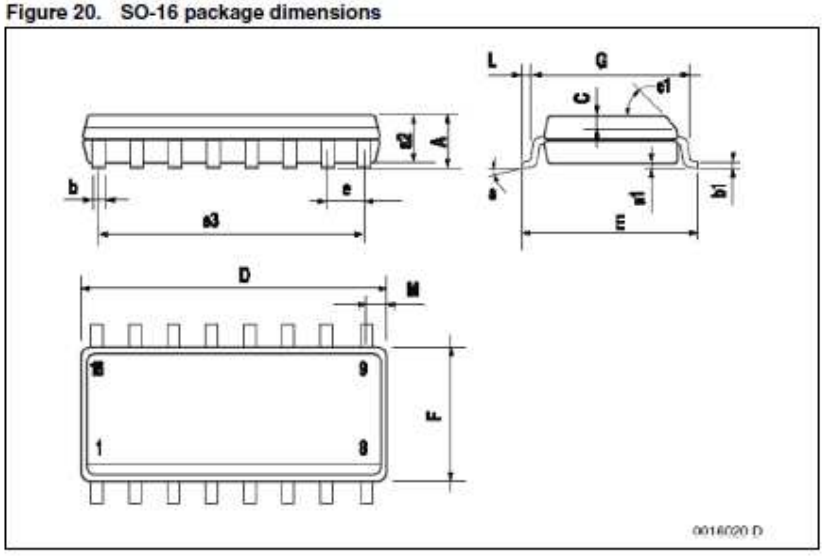


6.1.2 Package information

Table 6. SO-16 narrow mechanical data

Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
a1	0.1		0.25	0.004		0.009
a2			1.6			0.063
b	0.35		0.46	0.014		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.020	
c1			45°	(typ.)		
D(1)	9.8		10	0.386		0.394
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F(1)	3.8		4.0	0.150		0.157
G	4.60		5.30	0.181		0.208
L	0.4		1.27	0.150		0.050
M			0.62			0.024
S	8° (max.)					

Figure 20. SO-16 package dimensions



6.1.3 Test description

Test name	Description	Purpose
Die Oriented		
HTOL High Temperature Operative Life	The device is stressed in static or dynamic configuration, approaching the operative max. absolute ratings in terms of junction temperature and bias condition.	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. The typical failure modes are related to, silicon degradation, wire-bonds degradation, oxide faults.
HTSL High Temperature Storage Life	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
Package Oriented		
PC Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	As stand-alone test: to investigate the moisture sensitivity level. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.
AC Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
THB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
ESD Electro Static Discharge	The device is submitted to a high voltage peak on all his pins simulating ESD stress according to different simulation models. **HBM**: Human Body Model **CBM**: Charged Device Model	To classify the device according to his susceptibility to damage or degradation by exposure to electrostatic discharge.

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