APPLICATION NOTE

1   Introduction

This application note describes hardware and system design guidelines for incorporating precision power monitoring of better than 1% accuracy into AC/DC power supplies using the 78M6610+PSU. For real-time embedded measurement of the AC input power in a power supply, there are three possible sensor locations:

1. Measuring behind the EMI filtering circuit (recommended).
   - Balanced approach to component cost and calibration cost made possible by real-time XY capacitor compensation and data processing included with the 78M6610+PSU.
2. Measuring right at the AC inlet (supported).
   - Size (and cost) of isolated sensors often prohibitive.
3. Measuring the half-wave rectified signal after the bridge (not covered).
   - Not recommended for precision accuracy across entire operating range due to extensive offset and gain calibration times.

The following topics are discussed in more detail:

- Recommended Sensor Configuration
    - Powering the 78M6610+PSU
    - Line Voltage Resistor Dividers
    - Current Shunt Selection
- Alternative Sensor Configuration
    - Current Transformers
- Device Configuration
    - Clock Circuitry
    - Reset Circuitry
    - Connecting 5V Devices
    - Driving External Loads
    - Serial Interfaces
- PCB Layout Guidelines

2   Recommended Configuration

Resistive current shunts and voltage dividers are commonly used to meet system limitations on size and cost. When using a shunt current sensor, the measurement IC and its power domain are directly connected to AC mains. In this case, the 78M6610+PSU measurement device is typically powered through an auxiliary winding of the SMPS transformer (generally the stand-by channel). To protect the auxiliary winding from surge events and avoid switching noise from being conducted onto AC mains, the resistive sensors are located behind the EMI filter.

The system communicates with the 78M6610+PSU across data isolators (i.e. opto-couplers or digital isolators) as the host controller is located on the secondary side and often referenced to earth ground. The UART interface is suggested for lowest cost of data isolation.
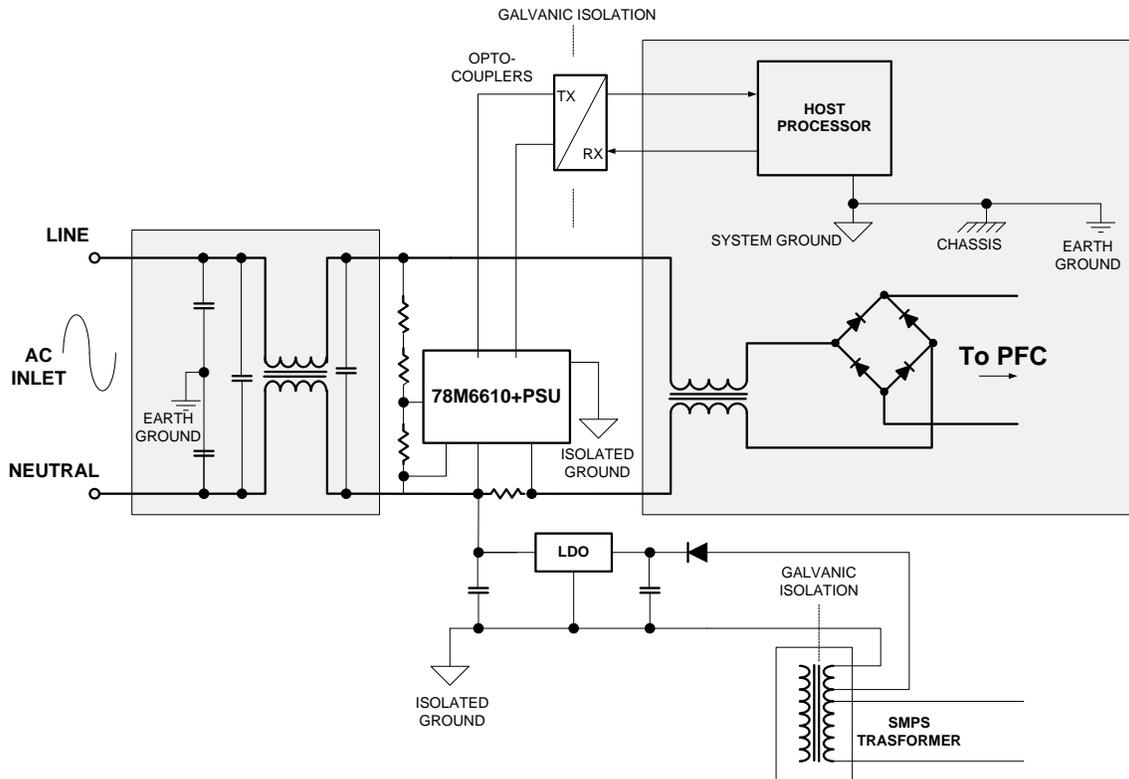

Figure 1: Typical Implementation of 78M6610+PSU

2.1 Sensor Connections

The basic connections for a shunt-based system are represented below.
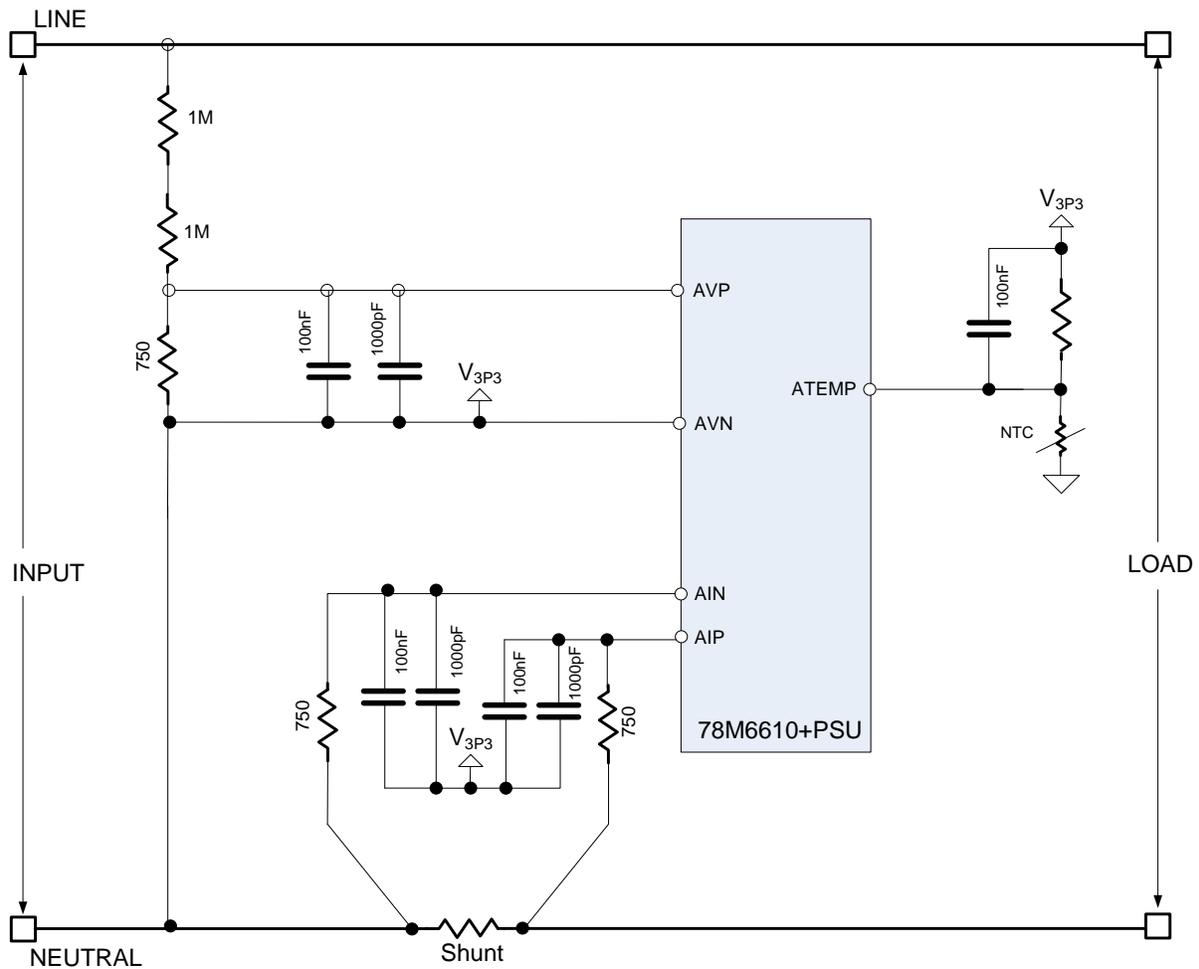

Figure 2: Basic Connection Diagram on Shunt-Based Systems

The 78M6610+PSU makes use of a single 3.3 VDC supply (V_{3P3}) that also represents the reference potential for the following analog inputs:

- AVP/AVN used to measure the line voltage.
- AIP/AIN used to measure the current.
- ATEMP1 and ATEMP2 used to measure external temperature.

> CAUTION
>
> Do not tie the ground of the 78M6610+PSU directly to earth ground when using shunts. See the Safety Precautions section.

2.1.1   Line Voltage Resistor Divider Selection

The input AC line voltage is scaled down to match the 78M6610+PSU's ADC input signal range of ±176.78 mVrms (+/-250mV pk-pk). To support most 2-wire AC voltages with enough overhead for surges, a peak RMS voltage of 471 VAC is recommended. Using the circuit in the previous figure, the line voltage is scaled down as follows:

$$VADC = \frac{VLINE * 750}{1M + 1M + 750} = VLINE * 3.7486 * 10^{-4}$$

The use of two 1 MΩ resistors instead of a single 2 MΩ resistor is suggested to meet the maximum voltage rating of the resistor and to provided adequate breakdown and arcing clearance. A series of 2 or more resistors may be needed in order to meet the safety standards requirements (UL, IEC etc.) for the intended system.

A couple of important aspects to consider in the selection of the voltage divider resistors are the tolerance and temperature coefficient (TCR in Ωppm/°C).

Component tolerance can easily be compensated for during calibration. Depending on the system accuracy requirements, however, the incremental cost of higher precision resistors (i. e. 0.1% versus 5%) may justify lower production costs (shorter calibration time). If 0.1% tolerance resistors are sufficient for the system accuracy targets, the nominal voltage calibration coefficient obtained from a few calibrated units can be used for production units saving time calibration time in the manufacturing cycle. The measurement accuracy variation from board to board would be within the tolerance of the resistors used in the divider.

More importantly, higher precision resistors will often have a smaller temperature coefficient. This eliminates the source of error that can arise from changes in resistance caused by temperature changes. TCR of 50 ppm/°C or lower (preferably 25 ppm/°C) is recommended. To maintain a consistent temperature coefficient, it is recommended to use similar resistive types in the divider.

2.1.2   Shunt Resistor Selection

The value of the shunt to be used is a tradeoff between a higher shunt value that utilizes the full analog sensor input range of the IC and the lowest possible value that minimizes the power loss in the shunt.

For best utilization of the device's input range (+/-250 mVpp) and performance at lower currents, a larger shunt value that supports the maximum input current without clipping peak currents should be used. The maximum shunt value should be calculated at the lowest operating voltage and at maximum input power (accounting for max output power ratings, conversion efficiency, and standby power consumption of the PSU). As an example, with 90 VAC as a minimum operating voltage and a maximum input power of 1.0 KW, the maximum RMS input current is:

$$Imax(rms) = \frac{PINmax}{VACmin} = \frac{1.0KW}{90VAC} = 11.11 \ A$$

Using the maximum supported current as input full scale, the maximum shunt value would be:

$$Rshunt = \frac{VADCmax}{Imax(peak)} = \frac{250 \ mVpk}{\sqrt{2} * 11.12 \ Arms} = 15 \ m\Omega$$

While a 15 mΩ shunt value may fully utilizes the ADC input range, this shunt value produces a dissipated power of 1.85 W at maximum load. In order to ensure more ADC signal margin due to higher crest factors and to lower the power dissipation in the shunt resistor, the lowest possible shunt resistance is often desirable. To find the minimum shunt value, the minimum current to be accurately measured should be considered. As an example, with 265 VAC as a maximum operating voltage and a minimum input power of 5W, the minimum RMS input current to be measured is:

$$Imin(rms) = \frac{PINmin}{VACmax} = \frac{5W}{265VAC} = 18.87 \ mA(\text{rms})$$

Using this minimum supported current as the 2000:1 limit for current accuracy, the minimum shunt resistance value would be:

$$Rshunt = \frac{VADCmax}{2000 * Imin(peak)} = \frac{250 \ mVpk}{2000 * \sqrt{2} * 18.87 \ mA(rms)} = 4 \ m\Omega$$

Other considerations involved in the shunt resistor selection include the power dissipation in the shunt and the device's temperature coefficient. In the case of a 4mΩ shunt, the power dissipated in the shunt at maximum load current is 0.5 W. A 2 W rated device package is recommended for good long-term reliability and minimize the self heating of the resistor. The initial shunt tolerance is often compensated during calibration. The temperature coefficient, however, plays an important role in the overall accuracy and cannot be easily compensated. For example, a temperature coefficient of 100 ppm/°C causes a resistance variation of 1% over the 100 °C operating temperature environment.

## 2.2   Safety Precautions

CAUTION

With V_{3P3} directly connected to NEUTRAL, the 78M6610+PSU's Ground signal can be -3.3 V below earth ground. Any external test equipment attached to the 78M6610+PSU will be subject to this -3.3 V ground reference disparity. External test equipment **must** be disconnected from earth ground to avoid equipment damage due to this ground reference disparity.

A more serious safety issue may arise due to mis-wiring of the AC circuit. If the LINE and NEUTRAL wire connections at the AC plug are reversed between the 78M6610+PSU and the external test equipment, the 78M6610+PSU and external test equipment will see a 120/240 VAC voltage difference rather than -3.3 V. This scenario can occur when the 78M6610+PSU and external test equipment are powered from different wall outlets or power strips, one of which is mis-wired. With proper earth grounding, the external equipment is always referenced to earth ground via their enclosures.

2.3   Powering the 78M6610+PSU

The 78M6610+PSU requires a single 3.3VDC supply. The supply circuit should provide about 10 mA to power the 78M6610+PSU. Additionally, power is required for the surrounding circuitry (i.e. opto-couplers). In the following diagrams, circuit protections such as Metal-Oxide Varistors (MOV), chokes, etc. are omitted.

Commonly power supplies have a main (SMPS) channel that powers the DC loads (servers, storage, communication equipment etc.) and a stand-by (SMPS) channel that powers the controllers and supervisory circuits. The most common way to power the 78M6610+PSU in a power supply is to use an auxiliary winding (tap) of the transformer used in the stand-by channel.   The advantage is that the winding is isolated and the circuitry requires a minimal number of components.
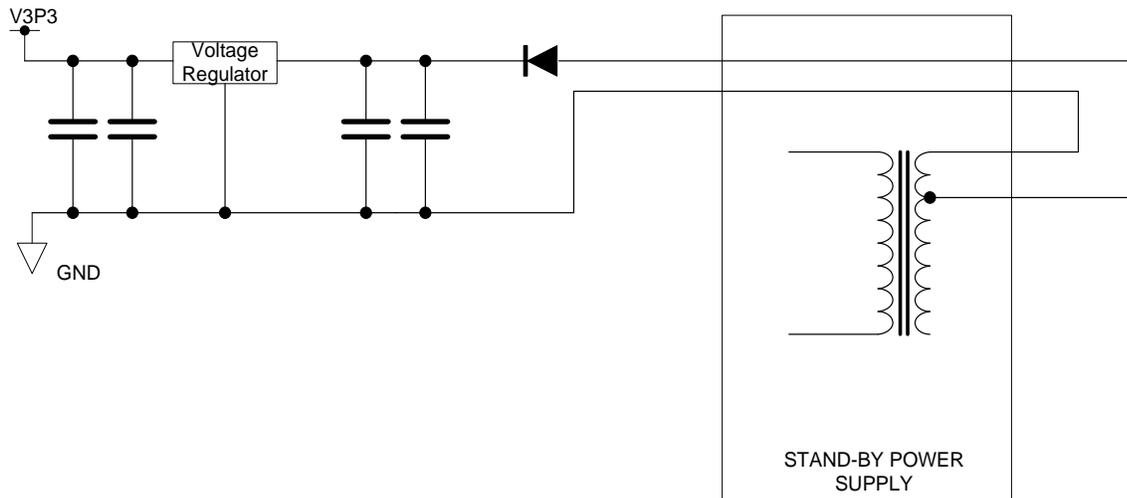
3   Alternate Configuration

Voltage and current sensors can alternatively be located right at the AC inlet in front of the EMI filters if using a current transformer (CT).   In this configuration, the measurement device is powered using the same auxiliary winding from the standby channel, but with a high impedance path between 78M6610+PSU circuitry and AC mains.
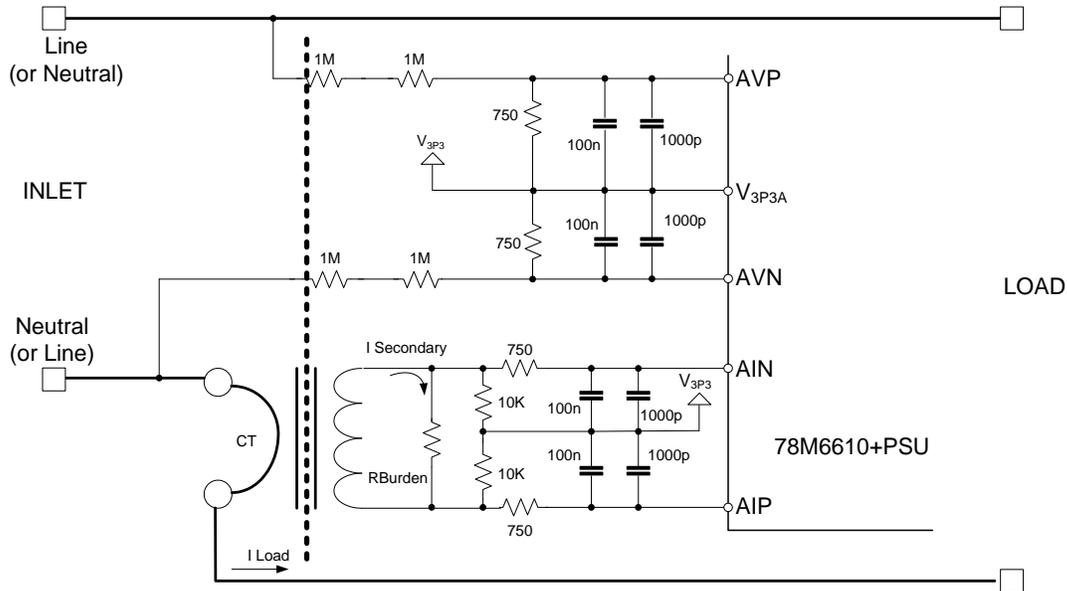

Figure 3: Pseudo-Isolated Configuration Example

It is highly recommended to use high-tolerance resistors in the voltage divider to minimize measurement error caused by divider ratio mis-matching.

3.1   Current Transformer Selection

The consideration for selecting a current transformer should include measurement accuracy, line frequency (and harmonics), current range and the CT's turns ratio. The load current range should also be considered. Subjecting a current transformer to load currents above the manufacturer's rated current specification may saturate the CT and cause winding failures due to excessive temperature rise. On the other hand, a current transformer that is rated much higher than the target load current might be restrictively too large and expensive for its purpose.
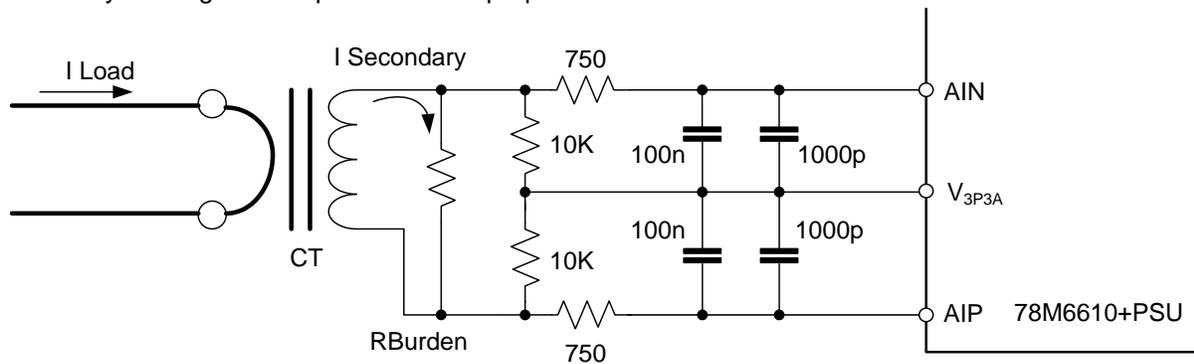

Figure 4: Current Transformer (CT) Basic Connections

Usually, current transformers have turns ratios ranging from 10:1 to 2500:1. The higher the turns ratio (TurnRatio = Nsecondary/Nprimary), the higher the resolution of the current measurement. A too high turns ratio increases distributed capacitance and leakage inductance. These characteristics may decrease the CT's accuracy and capability to operate at higher frequencies. However, if the number of turns is too low, the output signal may distort or "droop" (for positively sloped unipolar input signals). Such distortion may cause measurement inaccuracies. We recommend a minimum turns ratio of 1000:1.

The next step towards selecting a current transformer is the calculation of the burden resistor's value (RBurden). The 78M6610+PSU signal input range is ±176.78 mVrms (±250 mVpk). Therefore, the CT's secondary output voltage (Vout) must operate within this range. Assuming the maximum load current is 20 Arms (28.284A pk), a 1000:1 ratio current transformer will produce a secondary current of 20 mA rms (28.284 mA pk). Per Figure 4, the burden resistor's value is calculated as follows:

$$RBurden = \frac{Vout}{Iout}$$

Using the values in the above example, the value of the burden resistor is:

$$RBurden = \frac{0.250}{0.028284} = 8.85 \ \Omega$$

A standard value 8.2 Ω resistor is recommended. Always consult the CT's manufacturer for proper usage of their CT and burden resistor recommendations.

The use of a CT allows for the 78M6610+PSU's V_{3P3} to be isolated from the plant NEUTRAL wiring. This topology eliminates the safety issues stated earlier regarding shunt-based current sensing.

The V_{3P3} reference point critical to multi-shunt measurement performance is not an issue with CTs. The output currents generated by the CT's secondary winding is small enough that the sheet resistance of the 1 oz. copper plating does not present measurement errors from adjacent CTs. Shield the CTs secondary pins, burden resistor and filter components with top and bottom printed circuit board layer V_{3P3} plane surfaces. Insert multiple V_{3P3} vias to interconnect the top and bottom V_{3P3} structures for a low impedance shield.

4   Device Configuration

The following section covers the rest of the hardware interfaces found on the 78M6610+PSU.

4.1   VDC Supply (V$_{3P3D}$, V$_{3P3A}$) and Decoupling

The 78M6610+PSU requires a single 3.3VDC supply. In order to minimize the effect of digital output switching on the analog circuitry, the 78M6610+PSU has separate supply pins for analog (V$_{3P3A}$/GNDA) and digital circuitry (V$_{3P3D}$/GNDD). The two supply inputs can be tied to a common voltage node externally. A ferrite bead connecting the two power domains is not typically needed.

As in every design, particular attention must be paid to the supply voltage ripple noise and proper decoupling must be provided. Minimizing power supply noise is necessary for reliable operation of the processors and the various peripherals.

The 78M6610+PSU supply ranges (for both V$_{3P3A}$ and V$_{3P3D}$) from 3.0V to 3.6V (or 3.3VDC +/-9%). These limits include both the DC supply voltage error and the peak amplitude of any noise. Therefore it is necessary to account for deviation in the regulator output voltage and reduce the peak noise voltage. For example, given a voltage regulator precision of ±2.5%, the peak noise should never exceed ±2.1 V.

The 78M6610+PSU provides a high PSRR (Power Supply Ripple Rejection). However, it is necessary to limit the ripple and its frequency components. It is preferable to limit the ripple amplitude to 100 mV (pk-pk) and its frequency components to100 KHz. In these conditions the effect of the ripple noise on the A/D Converter accuracy, clock jitter and other peripherals is greatly minimized.

Voltage regulators have a tolerance typically between 1% and 2.5%. The voltage regulator output and the noise component should not exceed the 3.6 V to 3.0 V supply range (see Figure 5).
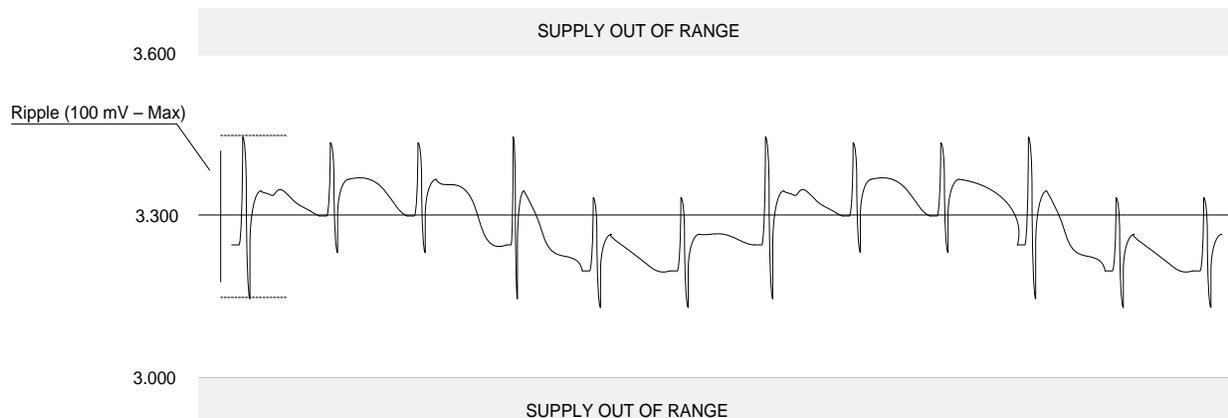
Figure 5: Supply Range

The basic power supply filter connections are shown in Figure 6, showing also the required decoupling capacitors. 3.3 VDC bypassing incorporates the combination of three different capacitor values. A 1000 pF in parallel with a 0.1 µF ceramic capacitor must be placed as close as possible to the 78M6610+PSU V_{3P3A} pin. Place the 1000 pF capacitor closest to the V_{3P3A} pin of the 78M6610+PSU. An additional 22 µF bulk capacitor is placed in the vicinity of the V_{3P3D} pin to provide decoupling for the external DIO circuitry. These three capacitor values provide decoupling over a wide frequency spectrum.
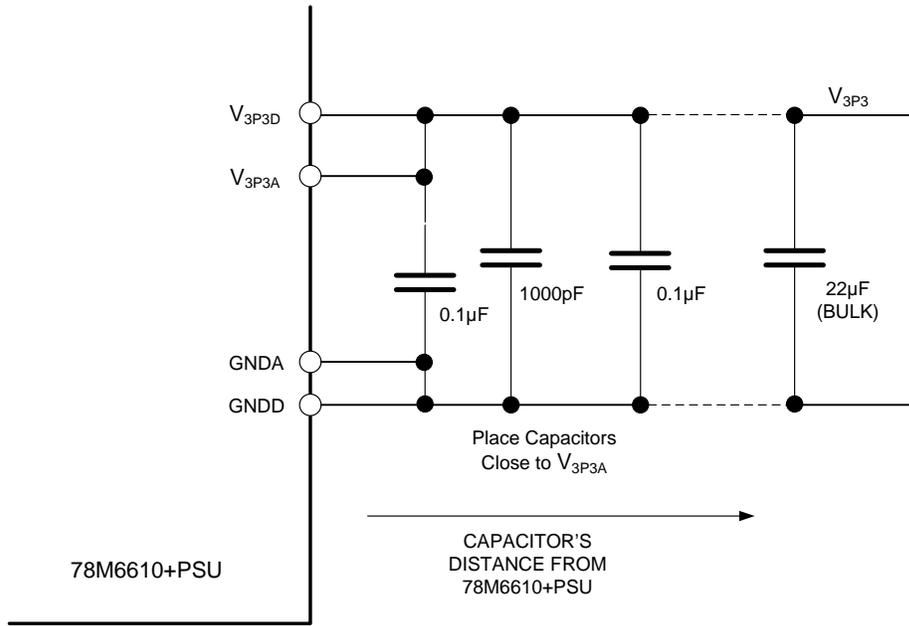
Figure 6: Power Supply Decoupling

4.2   Clock Circuitry

The 78M6610+PSU can utilize an external 20.000 MHz crystal for optimum performance. The circuitry includes two ceramic capacitors. The selected crystal must have a specified 18 pF load capacitance.

The oscillator is specifically designed for these types of crystals which have high impedance and limited power handling capability. The oscillator design minimizes power dissipation.

Minimize the printed circuit board capacitance for XIN to XOUT. Encase XIN and XOUT with a ground shield to minimize external noise interference of the low power oscillator.

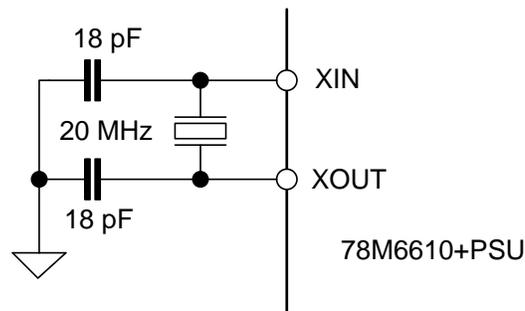The oscillator is self-biasing. Do not connect an external resistor across the crystal.

Figure 7: Crystal Connections

An external clock signal can be utilized instead of the crystal. In this case the external clock should be connected to the XOUT pin while the XIN pin should be connected to GNDD.

If the external crystal is not utilized (not mounted), the internal oscillator is selected automatically. In this case the XOUT pin should be connected to GNDD and the XIN pin left unconnected. Refer to the *78M6610+PSU Data Sheet* for parametric data relating to internal oscillator operation.

4.3   Reset Circuitry

The 78M6610+PSU employs an active low Reset input pin. Figure 8 shows the external circuit configuration using a pushbutton switch to generate the reset signal. If an external reset is not required, connect the Reset pin to V_{3P3}. An external reset is typically only used during the development phase of a project. The $\overline{RESET}$ pin can be tied high for the production version of the PCB.
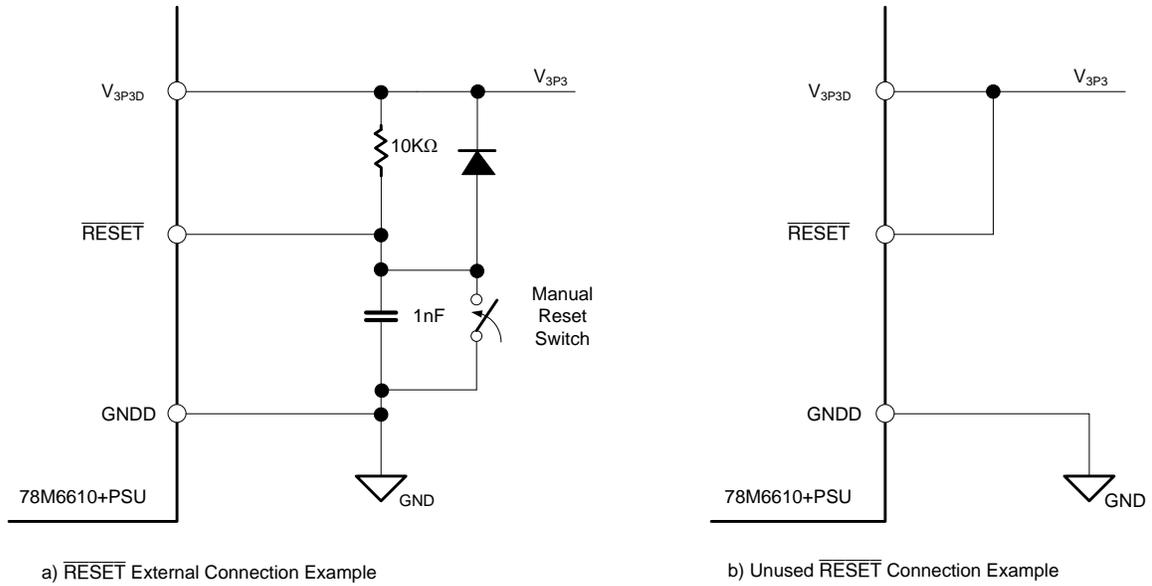

a) $\overline{RESET}$ External Connection Example   b) Unused $\overline{RESET}$ Connection Example

Figure 8: Reset Pin Connections

4.4   Connecting 5 V Devices

All digital input pins (DIO pins) of the 78M6610+PSU are 5 V tolerant allowing connection to external 5 V devices. I/O pins configured as inputs do not require current-limiting resistors when they are connected to external 5 V devices.

4.5   Driving External Loads

Even though the current output for the 78M6610+ PSU are similar driving high or low, if current is sourced by the &8M6610+PSU, the digital power supply current to V3P3D will be increased by that amount. See Figure 9 for our preferred connection. Sourcing current when the output is high is allowed but will add to the apparent V3P3D current for the part.

NOT RECOMMENDED   RECOMMENDED
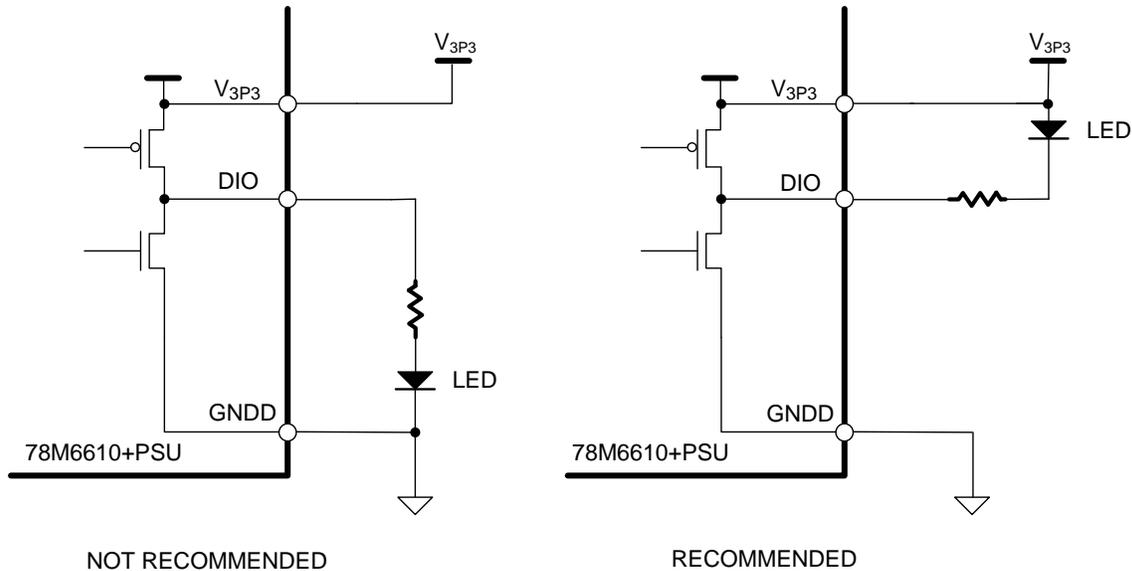
Figure 9: Connecting an External Load to a Digital Output

4.6   Serial Interfaces

The 78M6610+PSU has on-chip UART, I^2C, and SPI serial interfaces selectable through the configuration of the pins IFCONFIG and SSB/DIR/SCL according to the following table. The status of these pins is sampled at power-on or reset. Both the SSB/DIR/SCL and IFCONFIG pins contain internal 50-200K pull-up resistors so unconnected pins default to 1.

Selected Interface	SSB/DIR/SCL	IFCONFIG
SPI	X (don't care)	0
UART	0	1
I^2C	1	1

For I^2C operation, it is assumed that the I^2C master does not activate the clock (SCL) until after the 78M6610+PSU has completed its startup.

For UART operation, the RS-485 driver enable pin will be monetarily low until the 73M6610+PSU completes its startup.

5   Printed Circuit Board Layout Guidelines

The 78M6610+PSU minimizes the external component count and reduces the complexity of the printed circuit board layout design. However, some elements of the board design require consideration for optimum measurement accuracy and reliability. This section discusses these topics for the Maxim device:

- Printed Circuit Board Stack-up
- Crystal Oscillator Components
- LINE Voltage Resistor Network
- Shunt Current Sensor
- V_{3P3} Decoupling Capacitors
- System Communication Interface

This application note does not discuss creepage and clearance requirements described in UL 60950-1.

5.1   Printed Circuit Board Stack-up

The 78M6610+PSU can achieve excellent measurement accuracy using a 2-layer printed circuit board. If the component density becomes too high resulting in insufficient plane flooding surface area, a 4-layer stack-up must be employed. The plane flooding surface area is insufficient when the critical components presented in this application note are not properly shielded and isolated from external noise or each other. Additionally, there must be multiple redundant connection paths across the board's surface area to present low impedance paths for the various power and ground connections. The power and ground planes should mirror each other as much as possible since the ground return current tends to travel directly beneath the supply current across the board. This minimizes current loops and radiated emissions.

The following section regarding the respective critical components uses the 78M6610+PSU Evaluation Board as an example. The board has a 2-layer plane assignment.

5.2   Crystal Oscillator Components

The 78M6610+PSU Evaluation Board has the crystal and its two load capacitors located on the bottom layer. Place a GND trace between the two terminals of the crystal to minimize oscillator startup problems.
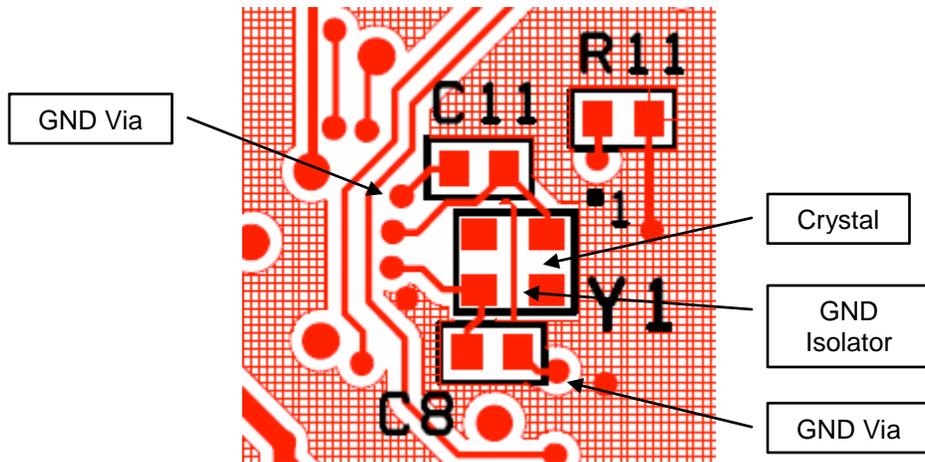

Figure 10: Crystal Y1 and Capacitors C8/ C11

The 78M6610+PSU can operate without an external crystal. Attach the XOUT pin to GND when the external crystal is not used.

5.3   LINE Voltage Resistor Network

The LINE voltage resistor network can be split between a 78M6610+PSU (daughter) board and the host board. The 750 Ω termination resistor and anti-aliasing capacitors should be placed near the 78M6610+PSU's analog input pin.
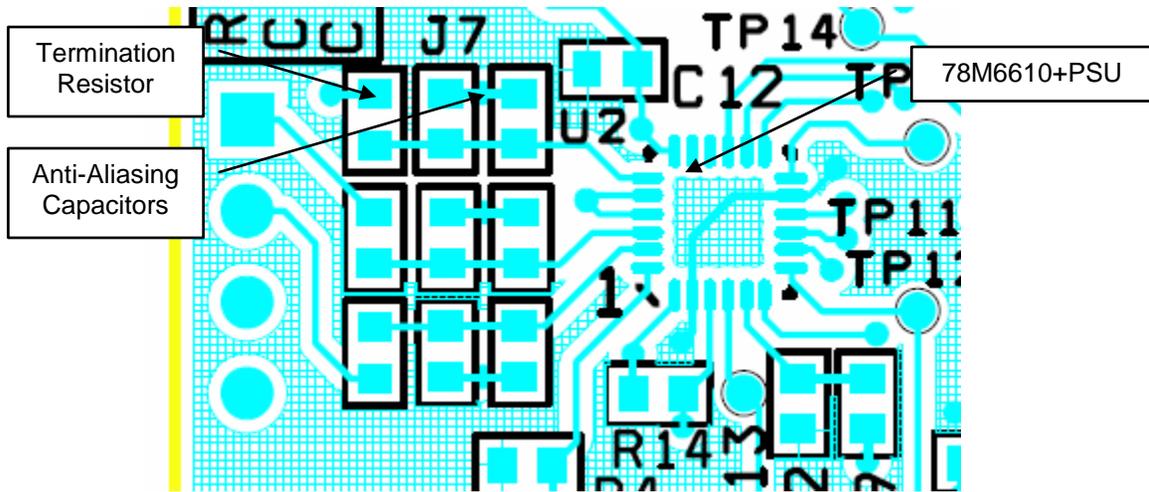
Figure 11: LINE Voltage Filter Network

The high voltage 1 MΩ resistors can be placed remotely on the host board.
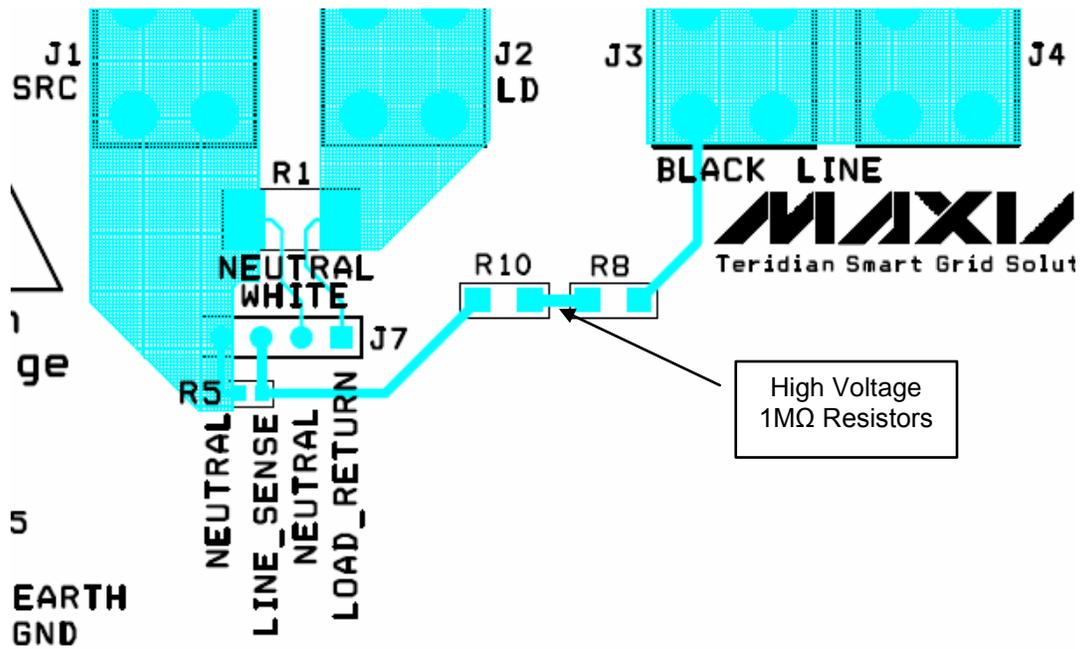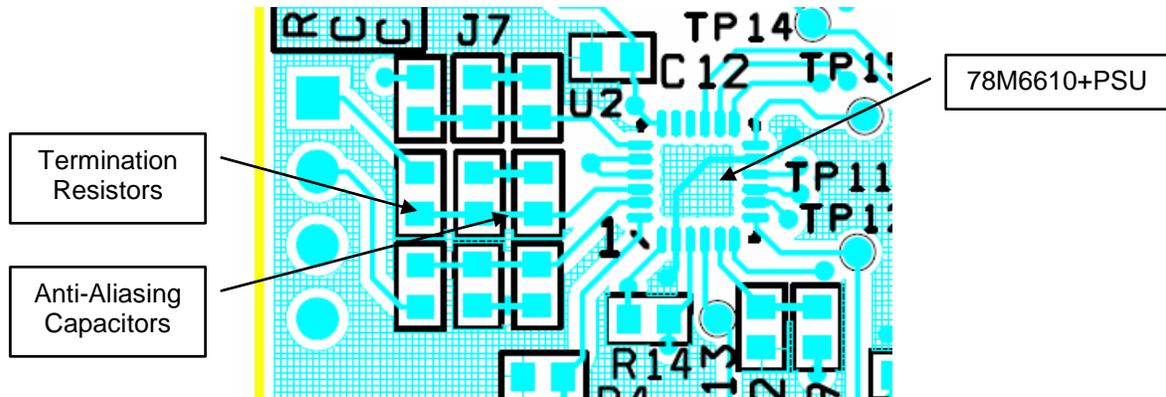

Figure 12: High Voltage Resistors

5.4   Shunt Current Sensor

The current shunt network can also be split between the 78M6610+PSU (daughter) board and the host board. The 750 Ω termination resistors and anti-aliasing capacitors should be placed near the 78M6610+PSU's analog input pins.

Figure 13: AIP and AIN Filter Network

The resistive current shunt can be placed remotely on the host board. It is important to provide a wide, heavy copper path between the current shunt and its connections to high current AC wiring.
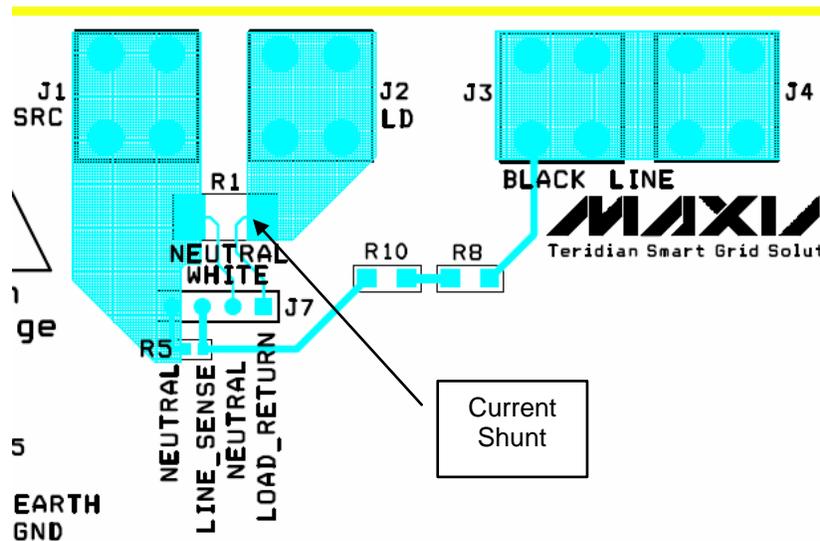

Figure 14: Current Shunt Sensor

5.6 V$_{3P3}$ Decoupling Capacitors

Place the V$_{3P3}$ decoupling capacitors close to the 3.3V regulator and 78M6610+PSU. Provide adequate V$_{3P3}$ copper plane from the voltage regulator and decoupling capacitors to the V$_{3P3D}$ and V$_{3P3D}$ pins of the 78M6610+PSU. Two separate V3P3A and V3P3D planes are recommended, but they should be electrically connected via either a zero ohm resistor or inductor if needed.
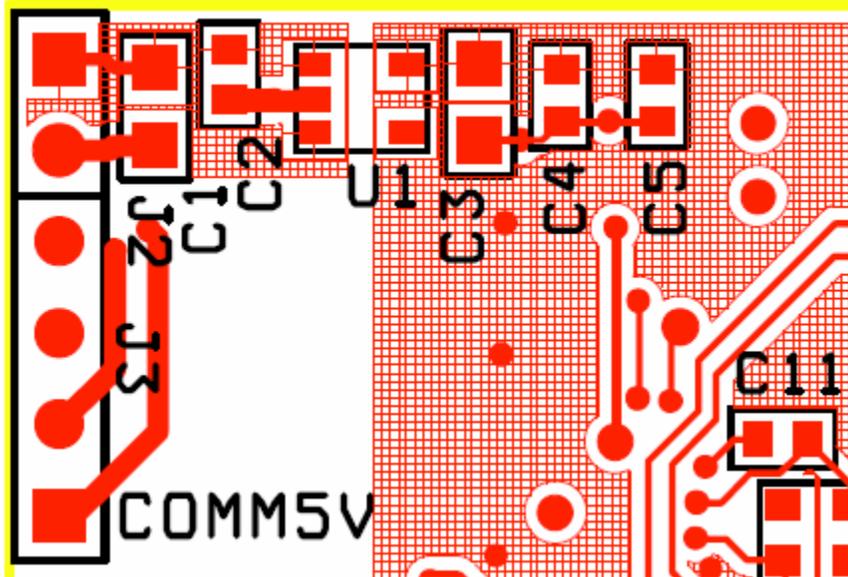

Figure 15: V$_{3P3}$ C3, C4, C5 Decoupling Capacitors

5.7 Systems Communication Interface

In most cases, the systems communication interface (UART, SPI, I^{2}C) between the 78M6610+PSU and external circuitry must be isolated to accommodate the -3.3V disparity in their GND pins (or, in the event of a LINE reversal). Depending on various requirements, a minimum clearance barrier must exist under the isolating components. A gap of 3 mm is the minimum requirement. Verify the isolating component's maximum barrier voltage meets your system requirements.

The supply for the 78M6610+PSU power domain should allow for powering the digital isolators. A low baud rate serial UART interface is recommended for lowest power and cost associated with the digital isolation.

6   Revision History

Revision	Date	Description
0	7/27/2012	First publication.