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## PIC18F27/47/57Q83 Silicon Errata and Data Sheet Clarifications

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The PIC18F27/47/57Q83 devices that you have received conform functionally to the current device data sheet (DS40002265A), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in the table below.

The errata described in this document will be addressed in future revisions of the PIC18F27/47/57Q83 silicon.

**Note:** This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current.

**Table 1. Silicon Device Identification**

Part Number	Device ID	Revision ID
		B3
PIC18F27Q83	0x9909	0xA043
PIC18F47Q83	0x990A	0xA043
PIC18F57Q83	0x990B	0xA043



**Important:** Refer to the **Device/Revision ID** section in the current “**PIC18FXXQ84 Family Programming Specification**” (DS40002137) for more detailed information on Device Identification and Revision IDs for a specific device.

**Table 2. Silicon Issue Summary**

Module	Feature	Item No.	Issue Summary	Affected Revisions
				B3
UTMR	Hardware Reset Condition	1.1.1	Reset does not happen at period match when prescaler > 0	X
	Level-triggered ERS Start/Reset Condition	1.1.2	Dead zone exists in level-triggered Start/Reset condition when ERS signal is generated due to an SFR access	X

**Note:** Only those issues indicated in the last column apply to the current silicon revision.

# 1. Silicon Errata Issues



**Notice:** This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the bold font in the following tables apply to the current silicon revision.

## 1.1 Module: Universal Timer (UTMR) Module

### 1.1.1 Reset Does Not Happen at Period Match When the Prescaler > 0

When the prescaler > 0 and a hardware-based Reset event is selected (RESET = `b01 or `b10 or `b11), the timer does not reset at period match.

**Work around**

1. Use prescaler = 0, or
2. When using prescaler > 0, clear the timer in software using CLR command at every PR match interrupt.

**Affected Silicon Revisions**

B3
X

### 1.1.2 Dead Zone Exists in Level-Triggered Start/Reset Condition When an ERS Signal Is Generated Due to an SFR Access

When a level-triggered Start/Reset condition (START = `b11 or RESET = `b01) is triggered by an ERS signal generated by an SFR access like TUxyPRL\_Write or TUxyTMRL\_Read or TUxyCRL\_Read (TUxyERS = 0x3E or 0x3F), there exists a dead zone in which subsequent SFR accesses will be missed. This dead zone is the period between the ZIF flag being set and the timer starting to count again. This can be monitored by either checking the RUN status bit or the level output of the timer.

**Work around**

The user must wait for the timer to start counting before accessing the period, counter and capture registers again.

**Affected Silicon Revisions**

B3
X

## **2. Data Sheet Clarifications**

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS40002265A):

**Note:** Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

### **2.1 None**

There are no known data sheet clarifications as of this publication date.

**3. Appendix A: Revision History**

Doc Rev.	Date	Comments
A	11/2020	Initial document release.

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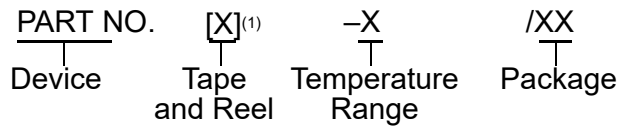
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	E	= -40°C to +125°C (Extended)
Package: <sup>(2)</sup>	JQ	= UQFN
	P	= PDIP
	ST	= TSSOP
	SL	= SOIC-14
	SN	= SOIC-8
	RF	= UDFN
Pattern:	QTP, SQTP <sup>SM</sup> (Serial Quick Turn Programming capability), Code or Special Requirements (blank otherwise)	

- Device A - I/P Industrial temperature, PDIP package
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