TPS37xx-Q1
Dual-Channel, Low-Power, High-Accuracy Voltage Detectors

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1: –40°C to 125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level H2
  - Device CDM ESD Classification Level C4B
- Two-Channel Detectors in Small Packages
- High-Accuracy Threshold and Hysteresis: 1.0%
- Low Quiescent Current: 2 µA (typ)
- Adjustable Detection Voltage Down to 1.2 V
- 5% and 10% Hysteresis Options
- Temperature Range: –40°C to +125°C
- Push-Pull (TPS3779-Q1) and Open-Drain (TPS3780-Q1) Output Options
- Available in an SOT-23 Package

2 Applications

- DSPs, Microcontrollers, and Microprocessors
- Advanced Driver Assistance Systems (ADAS)
- Infotainment and Clusters
- Power-Supply Sequencing Applications

3 Description

The TPS3779-Q1 and TPS3780-Q1 are a family of high-accuracy, two-channel voltage detectors featuring low power and small solution size. The SENSE1 and SENSE2 inputs include hysteresis to reject brief glitches, thus ensuring stable output operation without false triggering. This device family offers different factory-set hysteresis options of 5% or 10%.

The TPS3779-Q1 and TPS3780-Q1 have adjustable SENSEx inputs that can be configured by an external resistor divider. When the voltage at the SENSE1 or SENSE2 input goes below the falling threshold, OUT1 or OUT2 is driven low, respectively. When SENSE1 or SENSE2 rises above the rising threshold, OUT1 or OUT2 goes high, respectively.

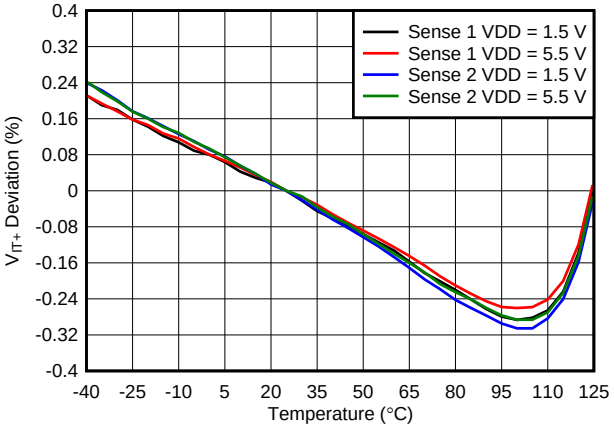
The devices have a very low quiescent current of 2 µA (typical) and provide a precise, space-conscious solution for voltage detection suitable for low-power, system-monitoring, and portable applications. The TPS3779-Q1 and TPS3780-Q1 operate from 1.5 V to 5.5 V, over the –40°C to +125°C temperature range.

Device Information(1)

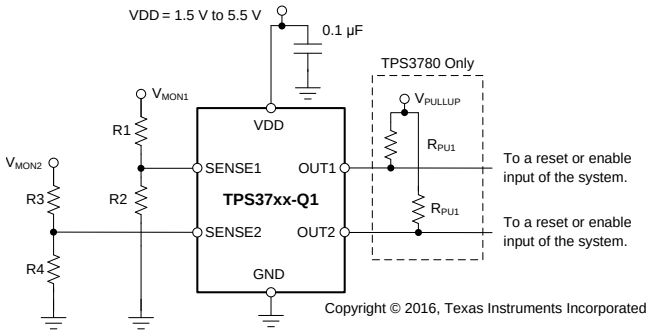
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS37xx-Q1	SOT-23 (6)	2.90 mm × 1.60 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Sense Threshold (V_{IT+}) Deviation versus Temperature



Typical Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

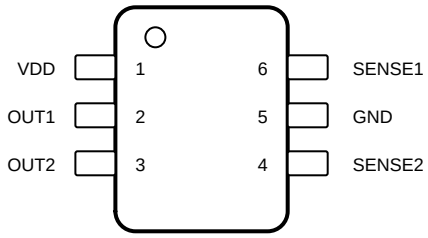
Changes from Original (June 2016) to Revision A	Page
• Added TPS3780A-Q1 row to *Device Comparison Table*	3
• Added TPS37xxA-Q1 row to V_{IT-} parameter in *Electrical Characteristics* table	5

5 Device Comparison Table

PRODUCT	HYSTERESIS (%)	OUTPUT
TPS3779B-Q1	5	Push-pull
TPS3779C-Q1	10	Push-pull
TPS3780A-Q1	0.5	Open-drain
TPS3780B-Q1	5	Open-drain
TPS3780C-Q1	10	Open-drain

6 Pin Configuration and Functions

DBV Package
6-Pin SOT-23
Top View



Not to scale

Pin Functions

NAME	NO.	I/O	DESCRIPTION
GND	5	—	Ground
OUT1	2	O	OUT1 is the output for SENSE1. OUT1 is asserted (driven low) when the voltage at SENSE1 falls below V_{IT-}. OUT1 is deasserted (goes high) after SENSE1 rises higher than V_{IT+}. OUT1 is a push-pull output for the TPS3779-Q1 and an open-drain output for the TPS3780-Q1. The open-drain device (TPS3780-Q1) can be pulled up to 5.5 V independent of VDD; a pullup resistor is required for this device.
OUT2	3	O	OUT2 is the output for SENSE2. OUT2 is asserted (driven low) when the voltage at SENSE2 falls below V_{IT-}. OUT2 is deasserted (goes high) after SENSE2 rises higher than V_{IT+}. OUT2 is a push-pull output for the TPS3779-Q1 and an open-drain output for the TPS3780-Q1. The open-drain device (TPS3780-Q1) can be pulled up to 5.5 V independent of VDD; a pullup resistor is required for this device.
SENSE1	6	I	This pin is connected to the voltage to be monitored with the use of an external resistor divider. When the voltage at this pin drops below the threshold voltage (V_{IT-}), OUT1 is asserted.
SENSE2	4	I	This pin is connected to the voltage to be monitored with the use of an external resistor divider. When the voltage at this pin drops below the threshold voltage (V_{IT-}), OUT2 is asserted.
VDD	1	I	Supply voltage input. Connect a 1.5-V to 5.5-V supply to VDD in order to power the device. Good analog design practice is to place a 0.1-µF ceramic capacitor close to this pin (required for VDD < 1.5 V).

7 Specifications

7.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	VDD	–0.3	7	V
	OUT1, OUT2 (TPS3779-Q1 only)	–0.3	VDD + 0.3	
	OUT1, OUT2 (TPS3780-Q1 only)	–0.3	7	
	SENSE1, SENSE2	–0.3	7	
Current	OUT1, OUT2		±20	mA
Temperature	Operating junction, T_J(2)	–40	125	°C
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) For low-power devices, the junction temperature rise above the ambient temperature is negligible; therefore, the junction temperature is considered equal to the ambient temperature ($T_J = T_A$).

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
	Power-supply voltage		1.5		5.5	V
	Sense voltage	SENSE1, SENSE2	0		5.5	V
	Output voltage (TPS3779-Q1 only)	OUT1, OUT2	0		VDD + 0.3	V
	Output voltage (TPS3780-Q1 only)	OUT1, OUT2	0		5.5	V
R_{PU}	Pullup resistor (TPS3780-Q1 only)		1.5		10,000	kΩ
	Current	OUT1, OUT2	–5		5	mA
C_{IN}	Input capacitor			0.1		µF
T_J	Junction temperature		–40	25	125	°C

7.4 Thermal Information

THERMAL METRIC(1)		TPS3779-Q1, TPS3780-Q1 DBV (SOT-23) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	193.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	134.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	39.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	30.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	38.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

all specifications are over the operating temperature range of –40°C < T_J < +125°C and 1.5 V ≤ VDD ≤ 5.5 V (unless otherwise noted); typical values are at T_J = 25°C and VDD = 3.3 V

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
VDD	Input supply range			1.5		5.5	V
$V_{(POR)}$	Power-on-reset voltage(1)	V_{OL} (max) = 0.2 V, I_{OL} = 15 µA				0.8	V
I_{DD}	Supply current (into VDD pin)	VDD = 3.3 V, no load			2.09	5.80	µA
		VDD = 5.5 V, no load			2.29	6.50	
V_{IT+}	Positive-going input threshold voltage	$V_{(SENSEx)}$ rising			1.194		V
				–1%		1%	
$V_{IT–}$	Negative-going input threshold voltage	$V_{(SENSEx)}$ falling	TPS37xxA-Q1 (0.5% hysteresis)		1.188		V
			TPS37xxB-Q1 (5% hysteresis)		1.134		
			TPS37xxC-Q1 (10% hysteresis)		1.074		
		$V_{(SENSEx)}$ falling		–1%		1%	
$I_{(SENSEx)}$	Input current	$V_{(SENSEx)}$ = 0 V or VDD		–15		15	nA
V_{OL}	Low-level output voltage	VDD ≥ 1.5 V, I_{SINK} = 0.4 mA				0.25	V
		VDD ≥ 2.7 V, I_{SINK} = 2 mA				0.25	
		VDD ≥ 4.5 V, I_{SINK} = 3.2 mA				0.30	
V_{OH}	High-level output voltage (TPS3779-Q1 only)	VDD ≥ 1.5 V, I_{SOURCE} = 0.4 mA		0.8 VDD			V
		VDD ≥ 2.7 V, I_{SOURCE} = 1 mA		0.8 VDD			
		VDD ≥ 4.5 V, I_{SOURCE} = 2.5 mA		0.8 VDD			
$I_{lkg(OD)}$	Open-drain output leakage current (TPS3780-Q1 only)	High impedance, $V_{(SENSEx)}$ = $V_{(OUTx)}$ = 5.5 V		–250		250	nA

(1) Outputs are undetermined below $V_{(POR)}$.

7.6 Timing Requirements

typical values are at T_J = 25°C and VDD = 3.3 V; SENSEx transitions between 0 V and 1.3 V

		MIN	NOM	MAX	UNIT
$t_{PD(r)}$	SENSEx (rising) to OUTx propagation delay		5.5		µs
$t_{PD(f)}$	SENSEx (falling) to OUTx propagation delay		10		µs
t_{SD}	Startup delay(1)		570		µs

(1) During power-on or when a VDD transient is below VDD(min), the outputs reflect the input conditions 570 µs after VDD transitions through VDD(min).

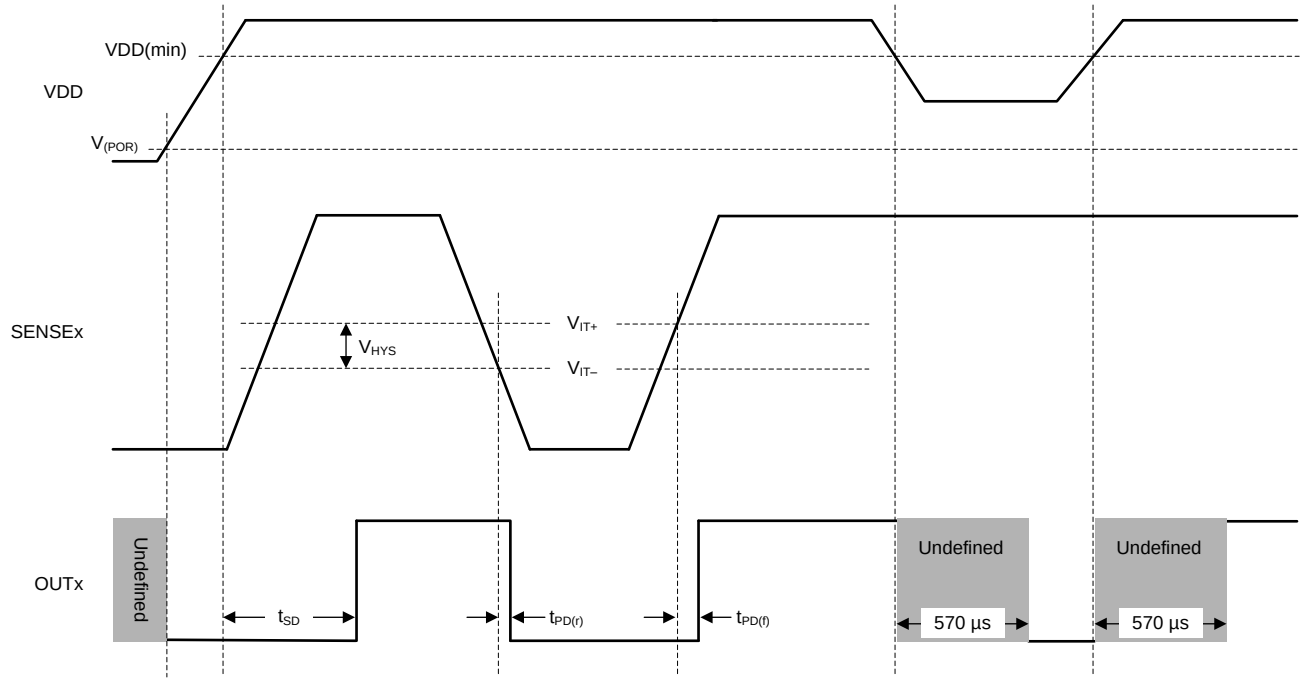


Figure 1. Timing Diagram

7.7 Typical Characteristics

at T_J = 25°C with a 0.1-µF capacitor close to VDD (unless otherwise noted)

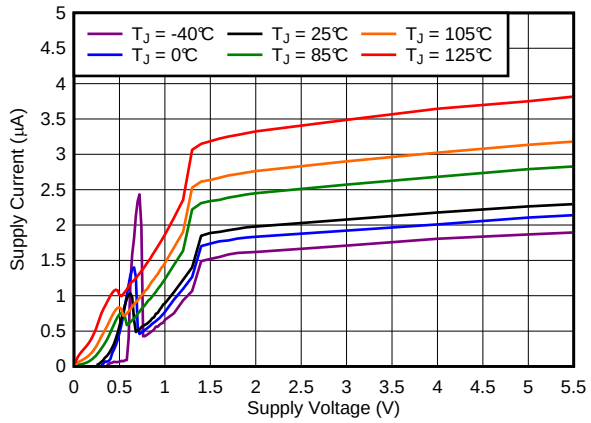


Figure 2. Supply Current vs Supply Voltage

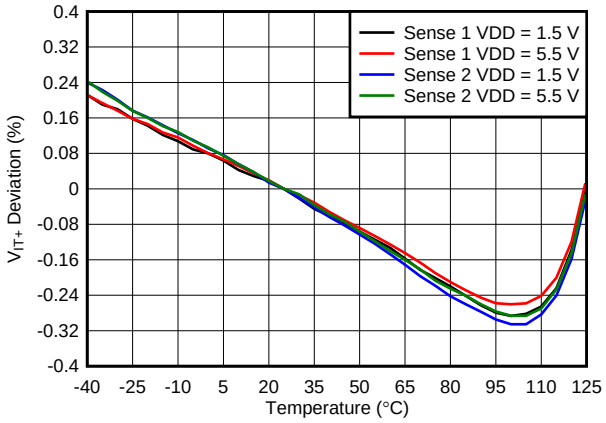


Figure 3. Sense Threshold (V_{IT+}) Deviation vs Temperature

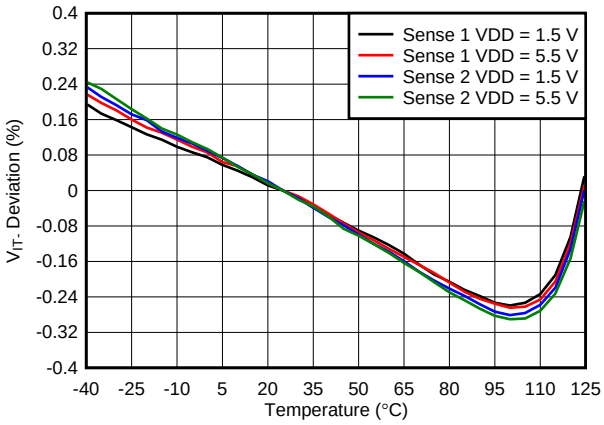


Figure 4. Sense Threshold (V_{IT-}) Deviation vs Temperature

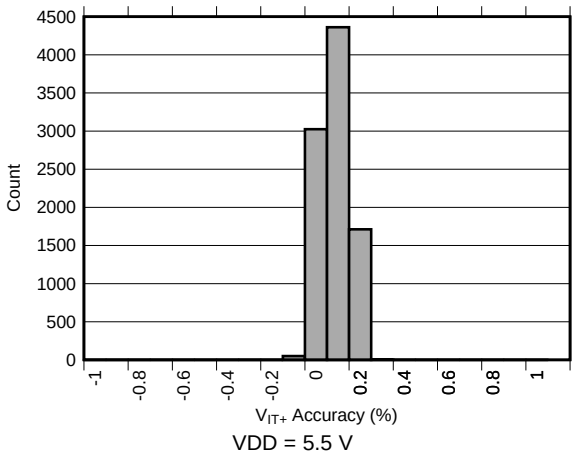


Figure 5. Sense Threshold (V_{IT+})

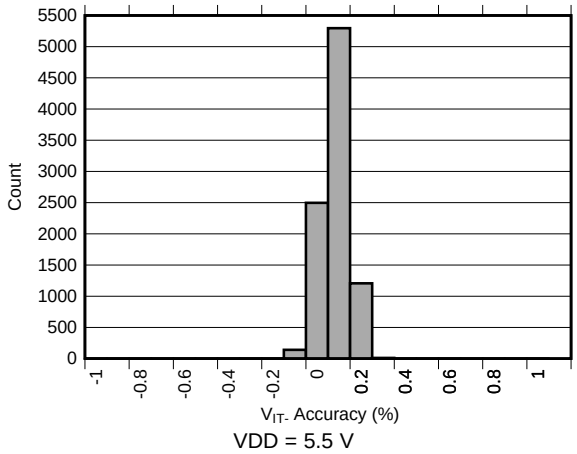


Figure 6. Sense Threshold (V_{IT-})

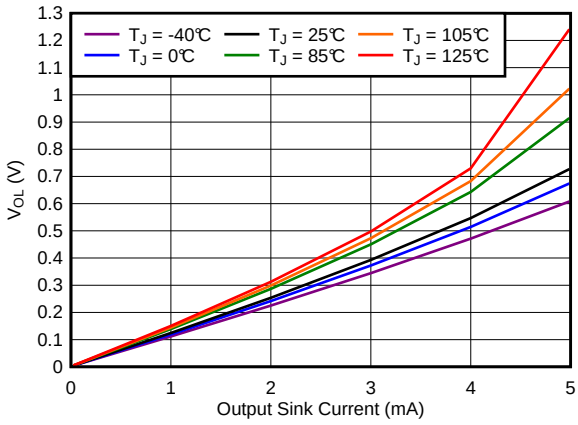


Figure 7. Output Voltage Low vs Output Current (VDD = 1.5 V)

Typical Characteristics (continued)

at T_J = 25°C with a 0.1-µF capacitor close to VDD (unless otherwise noted)

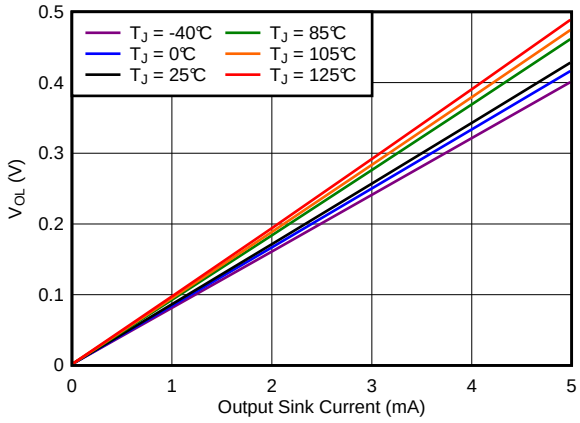


Figure 8. Output Voltage Low vs Output Current (VDD = 3.3 V)

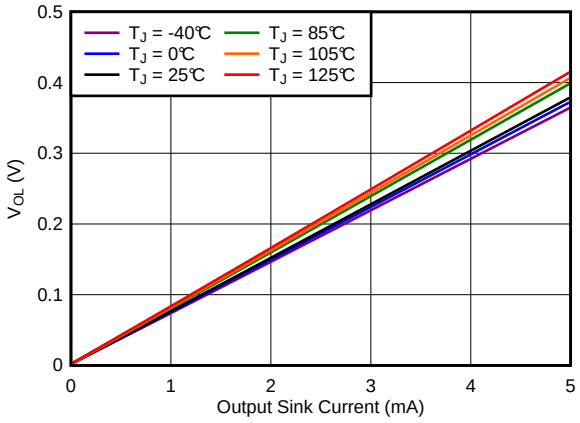


Figure 9. Output Voltage Low vs Output Current (VDD = 5.5 V)

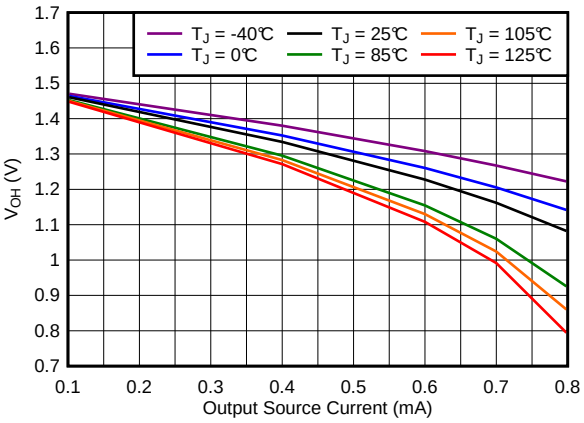


Figure 10. Output Voltage High vs Output Current (VDD = 1.5 V)

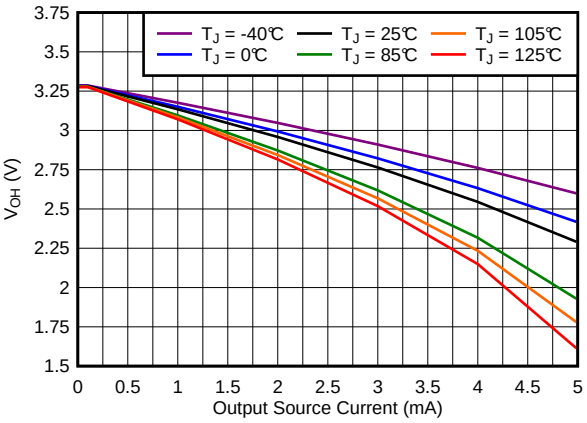


Figure 11. Output Voltage High vs Output Current (VDD = 3.3 V)

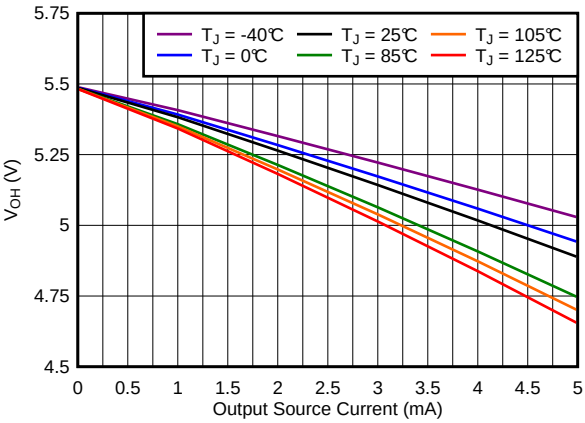
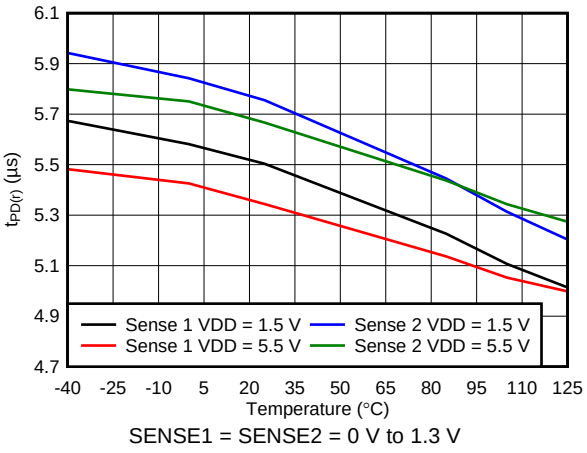


Figure 12. Output Voltage High vs Output Current (VDD = 5.5 V)

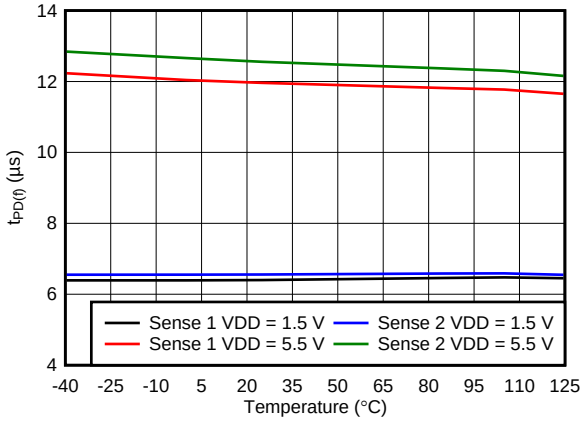


SENSE1 = SENSE2 = 0 V to 1.3 V

Figure 13. Propagation Delay from SENSEx High to Output High

Typical Characteristics (continued)

at T_J = 25°C with a 0.1-µF capacitor close to VDD (unless otherwise noted)



SENSE1 = SENSE2 = 1.3 V to 0 V

Figure 14. Propagation Delay from SENSEx Low to Output Low

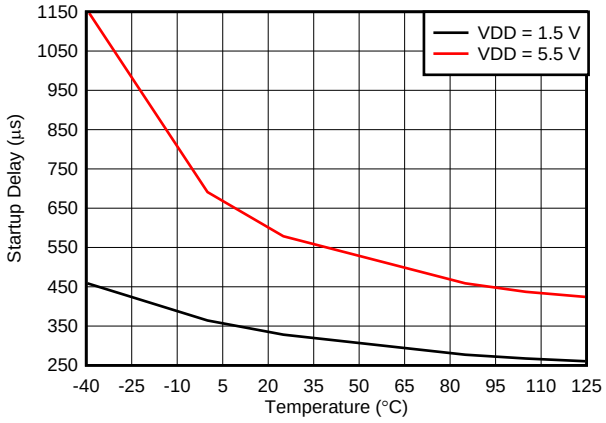
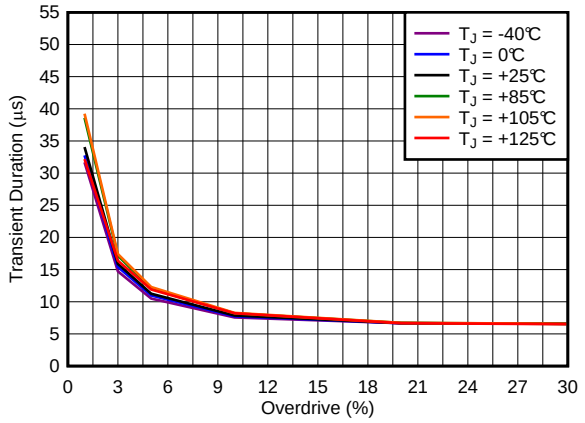
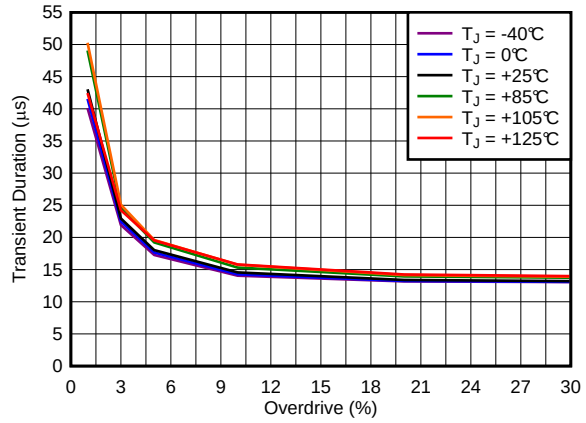


Figure 15. Startup Delay



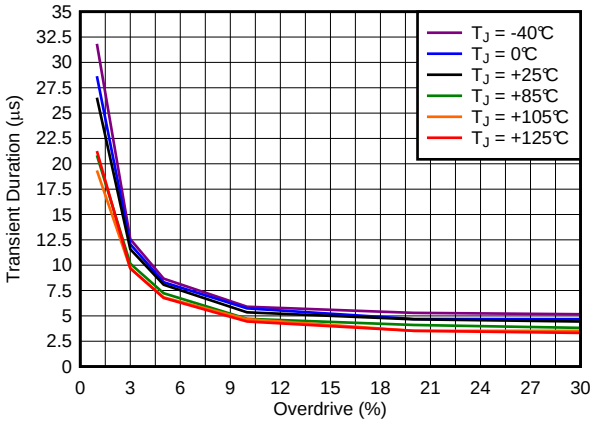
High-to-low transition occurs above the curve

Figure 16. Minimum Transient Duration vs Overdrive (VDD = 1.5 V)



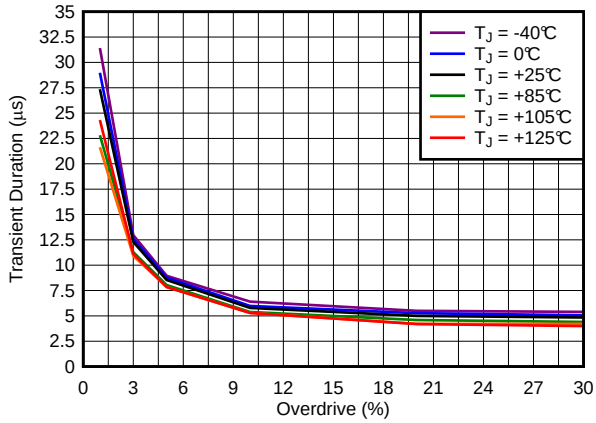
High-to-low transition occurs above the curve

Figure 17. Minimum Transient Duration vs Overdrive (VDD = 5.5 V)



Low-to-high transition occurs above the curve

Figure 18. Minimum Transient Duration vs Overdrive (VDD = 1.5 V)



Low-to-high transition occurs above the curve

Figure 19. Minimum Transient Duration vs Overdrive (VDD = 5.5 V)

8 Detailed Description

8.1 Overview

The TPS3779-Q1 and TPS3780-Q1 are small, low quiescent current (I_{DD}), dual-channel voltage detectors. These devices have high-accuracy rising and falling input thresholds, and assert the output as shown in Table 1. The output (OUTx pin) goes low when the SENSEx pin is less than V_{IT-} and goes high when the pin is greater than V_{IT+}. The TPS3779-Q1 and TPS3780-Q1 offer two hysteresis options (5% and 10%) for use in a wide variety of applications. These devices have two independent voltage-detection channels that can be used in systems where multiple voltage rails are required to be monitored, or where one channel can be used as an early warning signal and the other channel can be used as the system reset signal.

Table 1. TPS3779-Q1, TPS3780-Q1 Truth Table

CONDITIONS	OUTPUT
SENSE1 < V_{IT-}	OUT1 = low
SENSE2 < V_{IT-}	OUT2 = low
SENSE1 > V_{IT+}	OUT1 = high
SENSE2 > V_{IT+}	OUT2 = high

8.2 Functional Block Diagrams

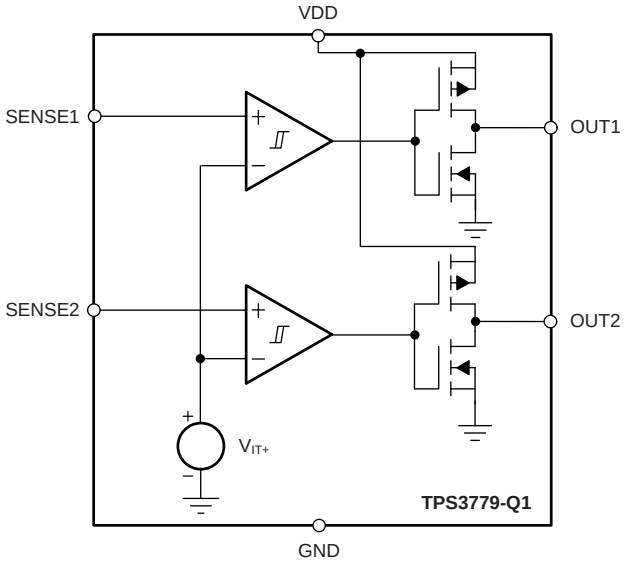


Figure 20. TPS3779-Q1 Block Diagram

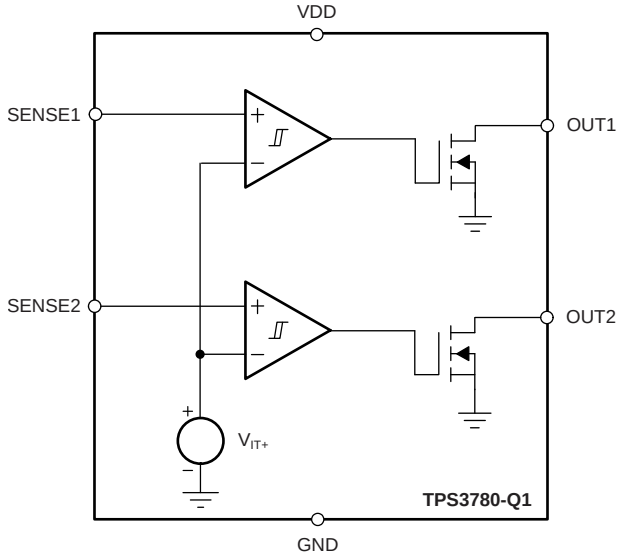


Figure 21. TPS3780-Q1 Block Diagram

8.3 Feature Description

8.3.1 Inputs (SENSE1, SENSE2)

The TPS3779-Q1 and TPS3780-Q1 each have two comparators for voltage detection. Each comparator has one external input; the other input is connected to the internal reference. The comparator rising threshold is designed and trimmed to be equal to V_{IT+}, and the falling threshold is trimmed to be equal to $V_{IT–}$. The built-in falling hysteresis options make the devices immune to supply rail noise and ensure stable operation.

The comparator inputs can swing from ground to 5.5 V, regardless of the device supply voltage used. Although not required in most cases, for extremely noisy applications, good analog design practice is to place a 1-nF to 10-nF bypass capacitor at the comparator input in order to reduce sensitivity to transients and layout parasitic.

For each SENSEx input, the corresponding output (OUTx) is driven to logic low when the input voltage drops below $V_{IT–}$. When the voltage exceeds V_{IT+}, the output (OUTx) is driven high; see Figure 1.

8.3.2 Outputs (OUT1, OUT2)

In a typical device application, the outputs are connected to a reset or enable input of another device, such as a digital signal processor (DSP), central processing unit (CPU), field-programmable gate array (FPGA), or application-specific integrated circuit (ASIC); or the outputs are connected to the enable input of a voltage regulator, such as a dc-dc or low-dropout (LDO) regulator.

The TPS3779-Q1 provides two push-pull outputs. The logic high level of the outputs is determined by the VDD pin voltage. Pullup resistors are not required with this configuration, thus saving board space. However, all interface logic levels must be examined. All OUTx connections must be compatible with the VDD pin logic level.

The TPS3780-Q1 provides two open-drain outputs (OUT1 and OUT2); pullup resistors must be used to hold these lines high when the output goes to a high-impedance condition (not asserted). By connecting pullup resistors to the proper voltage rails, the outputs can be connected to other devices at correct interface voltage levels. The outputs can be pulled up to 5.5 V, independent of the device supply voltage. To ensure proper voltage levels, make sure to choose the correct pullup resistor values. The pullup resistor value is determined by V_{OL}, the sink current capability, and the output leakage current ($I_{lkg(OD)}$). These values are specified in the *Electrical Characteristics* table. By using wired-AND logic, OUT1 and OUT2 can be combined into one logic signal. The *Inputs (SENSE1, SENSE2)* section describes how the outputs are asserted or deasserted. See Figure 1 for a description of the relationship between threshold voltages and the respective output.

8.4 Device Functional Modes

8.4.1 Normal Operation (VDD ≥ VDD(min))

When the voltage on VDD is greater than VDD(min) for t_{SD}, the output signals react to the present state of the corresponding SENSEx pins.

8.4.2 Power-On-Reset (VDD < $V_{(POR)}$)

When the voltage on VDD is lower than the required voltage to internally pull the logic low output to GND ($V_{(POR)}$), both outputs are undefined and are not to be relied upon for proper system function.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS3779-Q1 and TPS3780-Q1 are used as precision, dual-voltage detectors. The monitored voltage, VDD voltage, and output pullup voltage (TPS3780-Q1 only) can be independent voltages or connected in any configuration.

9.1.1 Threshold Overdrive

Threshold overdrive is how much V_{SENSE1} or V_{SENSE2} exceeds the specified threshold, and is important to know because a smaller overdrive results in a slower OUTx response. Threshold overdrive is calculated as a percent of the threshold in question, as shown in Equation 1:

$$\text{Overdrive} = | (V_{SENSE1,2} / V_{IT} - 1) \times 100\% | \quad (1)$$

where

- V_{IT} is either V_{IT-} or V_{IT+}, depending on whether calculating the overdrive for the negative-going threshold or the positive-going threshold, respectively
- $V_{SENSE1,2}$ is the voltage at the SENSE1 or SENSE2 input

Figure 16 illustrates the minimum detectable pulse on the SENSEx inputs versus overdrive, and is used to visualize the relationship that overdrive has on $t_{PD(f)}$ for negative-going events.

9.1.2 Sense Resistor Divider

The resistor divider values and target threshold voltage can be calculated by using Equation 2 and Equation 3 to determine $V_{MON(UV)}$ and $V_{MON(PG)}$, respectively.

$$V_{MON(UV)} = \left(1 + \frac{R1}{R2}\right) \times V_{IT-} \quad (2)$$

$$V_{MON(PG)} = \left(1 + \frac{R1}{R2}\right) \times V_{IT+} \quad (3)$$

where

- R1 and R2 are the resistor values for the resistor divider on the SENSEx pins
- $V_{MON(UV)}$ is the target voltage at which an undervoltage condition is detected
- $V_{MON(PG)}$ is the target voltage at which the output goes high when V_{MONx} rises

Choose R_{TOTAL} (equal to R1 + R2) so that the current through the divider is approximately 100 times higher than the input current at the SENSEx pins. The resistors can have high values to minimize current consumption as a result of low input bias current without adding significant error to the resistive divider. For details on sizing input resistors, see the *Optimizing Resistor Dividers at a Comparator Input* application report (SLVA450), available for download from www.ti.com.

9.2 Typical Applications

9.2.1 Monitoring Two Separate Rails

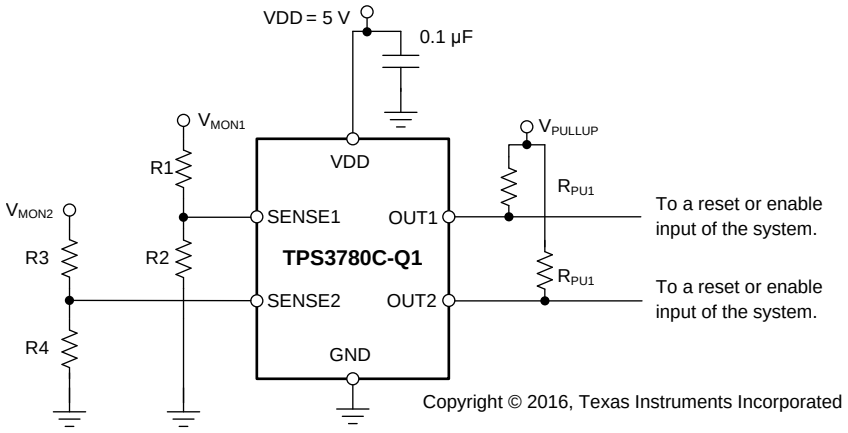


Figure 22. Monitoring Two Separate Rails Schematic

9.2.1.1 Design Requirements

Table 2. Design Parameters

PARAMETER	DESIGN REQUIREMENT	DESIGN RESULT
VDD	5 V	5 V
Hysteresis	10%	10%
Monitored voltage 1	3.3 V nominal, $V_{MON(PG)}$ = 2.9 V, $V_{MON(UV)}$ = 2.6 V	$V_{MON(PG)}$ = 2.908 V, $V_{MON(UV)}$ = 2.618 V
Monitored voltage 2	3 V nominal, $V_{MON(PG)}$ = 2.6 V, $V_{MON(UV)}$ = 2.4 V	$V_{MON(PG)}$ = 2.606 V, $V_{MON(UV)}$ = 2.371 V
Output logic voltage	3.3-V CMOS	3.3-V CMOS

9.2.1.2 Detailed Design Procedure

1. Select the TPS3780C-Q1. The C version is selected to satisfy the hysteresis requirement. The TPS3780-Q1 is selected for the output logic requirement. An open-drain output allows for the output to be pulled up to a voltage other than VDD.
2. The resistor divider values are calculated by using Equation 2 and Equation 3. For SENSE1, R1 = 1.13 MΩ and R2 = 787 kΩ. For SENSE2, R3 (R1) = 681 kΩ and R4 (R2) = 576 kΩ.

9.2.1.3 Application Curve

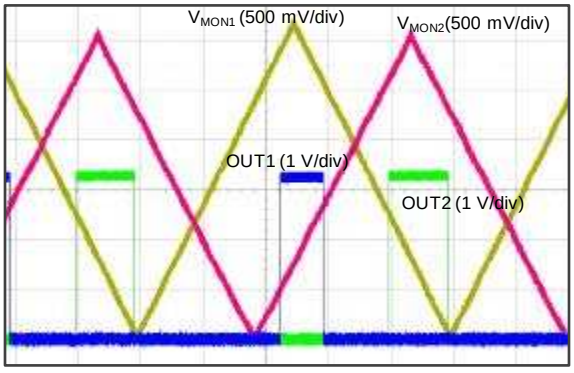


Figure 23. Monitoring Two Separate Rails Curve

9.2.2 Early Warning Detection

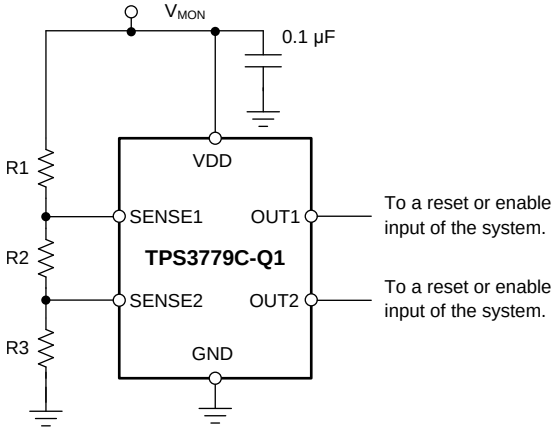


Figure 24. Early Warning Detection Schematic

9.2.2.1 Design Requirements

Table 3. Design Parameters

PARAMETER	DESIGN REQUIREMENT	DESIGN RESULT
VDD	V_{MON}	V_{MON}
Hysteresis	10%	10%
Monitored voltage 1	$V_{MON(PG)}$ = 3.3 V, $V_{MON(UV)}$ = 3 V	$V_{MON(PG)}$ = 3.330 V, $V_{MON(UV)}$ = 2.997 V
Monitored voltage 2	$V_{MON(PG)}$ = 3.9 V, $V_{MON(UV)}$ = 3.5 V	$V_{MON(PG)}$ = 3.921 V, $V_{MON(UV)}$ = 3.529 V

9.2.2.2 Detailed Design Procedure

1. Select the TPS3779C-Q1. The C version is selected to satisfy the hysteresis requirement. The TPS3779-Q1 is selected to save on component count and board space.
2. Use Equation 4 to calculate the total resistance for the resistor divider. Determine the minimum total resistance of the resistor network necessary to achieve the current consumption specification. For this example, the current flow through the resistor network is chosen to be 1.41 µA. Use the key transition point for V_{MON2}. For this example, the low-to-high transition, $V_{MON(PG)}$, is considered more important.

$$R_{TOTAL} = \frac{V_{MON(PG\_2)}}{I} = \frac{3.9\ V}{1.41\ \mu A} = 2.78\ M\Omega \quad (4)$$

   where
   - $V_{MON(PG\_2)}$ is the target voltage at which OUT2 goes high when V_{MON} rises
   - I is the current flowing through the resistor network

3. After R_{TOTAL} is determined, R3 can be calculated using Equation 5. Select the nearest 1% resistor value for R3. In this case, 845 kΩ is the closest value.

$$R3 = \frac{V_{IT+}}{I} = \frac{1.194\ V}{1.41\ \mu A} = 846\ k\Omega \quad (5)$$

4. Use Equation 6 to calculate R2. Select the nearest 1% resistor value for R2. In this case, 150 kΩ is the closest value. Use the key transition point for V_{MON1}. For this example, the high-to-low transition, $V_{MON(UV)}$, is considered more important.

$$R2 = \frac{R_{TOTAL}}{V_{MON(UV\_1)}} \bullet V_{IT-} - R3 = \frac{2.78\ M\Omega}{3\ V} \bullet 1.074\ V - 845\ k\Omega = 149\ k\Omega \quad (6)$$

   where
   - $V_{MON(UV\_1)}$ is the target voltage at which OUT1 goes low when V_{MON} falls

5. Use Equation 7 to calculate R1. Select the nearest 1% resistor value for R1. In this case, 1.78 MΩ is a 1% resistor.

$$R1 = R_{TOTAL} - R2 - R3 = 2.78\ M\Omega - 150\ k\Omega - 845\ k\Omega = 1.78\ M\Omega \quad (7)$$

9.2.2.3 Application Curve

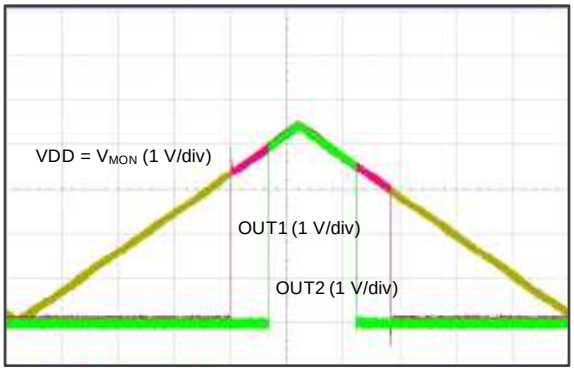


Figure 25. Early Warning Detection Curve

10 Power-Supply Recommendations

The TPS3779-Q1 and TPS3780-Q1 are designed to operate from an input voltage supply range between 1.5 V and 5.5 V. An input supply capacitor is not required for this device; however, good analog practice is to place a 0.1-µF or greater capacitor between the VDD pin and the GND pin. This device has a 7-V absolute maximum rating on the VDD pin. If the voltage supply providing power to VDD is susceptible to any large voltage transient that can exceed 7 V, additional precautions must be taken.

For applications where SENSEx is greater than 0 V before VDD, and is subject to a startup slew rate of less than 200 mV per 1 ms, the output can be driven to logic high in error. To correct the output, cycle the SENSEx lines below V_{IT-} or sequence SENSEx after VDD.

11 Layout

11.1 Layout Guidelines

Place the VDD decoupling capacitor close to the device.

Avoid using long traces for the VDD supply node. The VDD capacitor, along with parasitic inductance from the supply to the capacitor, can form an LC tank circuit that creates ringing with peak voltages above the maximum VDD voltage.

11.2 Layout Example

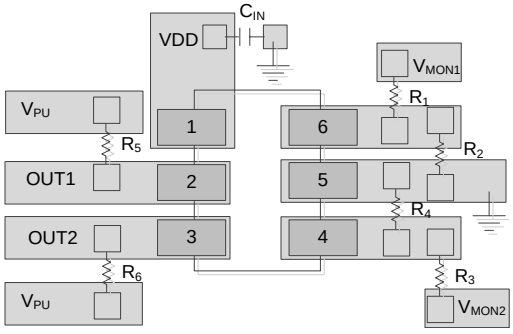


Figure 26. Example SOT-23 Layout

12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

12.1.1.1 Evaluation Modules

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the TPS3779-Q1 and TPS3780-Q1. The *TPS3780EVM-154 Evaluation Module* details the design kits and evaluation modules for the TPS3780EVM-154.

The EVM can be requested at Texas Instruments through the TPS3779-Q1 and TPS3780-Q1 product folders, or purchased directly from the TI eStore.

12.1.1.2 Spice Models

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. A SPICE model for the TPS3779-Q1 and TPS3780-Q1 is available through the respective device product folders under *Simulation Models*.

12.1.2 Device Nomenclature

The TPS3779xQyyyzQ1 and TPS3780xQyyyzQ1 are the generic naming conventions for these devices. The TPS3779-Q1 and TPS3780-Q1 represent the family of these devices; x is used to display the hysteresis version, yyy is reserved for the package designator, and z is the package quantity.

- Example: TPS3780CDBVRQ1
- Family: TPS3780-Q1 (open-drain)
- Hysteresis: 10%
- DBV package: 6-pin SOT-23
- Package quantity: R is for 3000 pieces

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation see the following:

- *TPS3780EVM-154 Evaluation Module* (SLVU796)
- *Optimizing Resistor Dividers at a Comparator Input* Application Report (SLVA450)

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 4. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS3779-Q1	Click here	Click here	Click here	Click here	Click here
TPS3780-Q1	Click here	Click here	Click here	Click here	Click here

12.5 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.6 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.7 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.8 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS3779BQDBVRQ1	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	12OE	Samples
TPS3779CQDBVRQ1	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	12PE	Samples
TPS3780AQDBVRQ1	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	12FE	Samples
TPS3780BQDBVRQ1	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	12GE	Samples
TPS3780CQDBVRQ1	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	12HE	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TPS3779-Q1, TPS3780-Q1 :

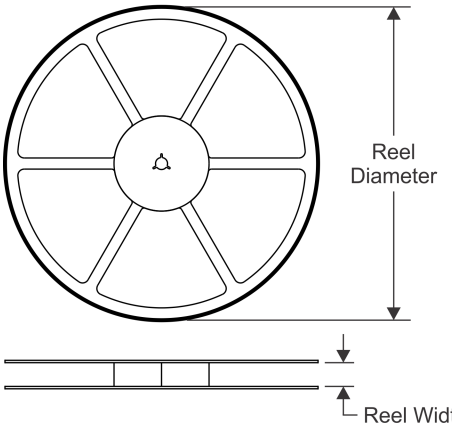
- Catalog: TPS3779, TPS3780

NOTE: Qualified Version Definitions:

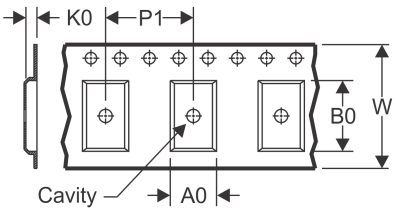
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

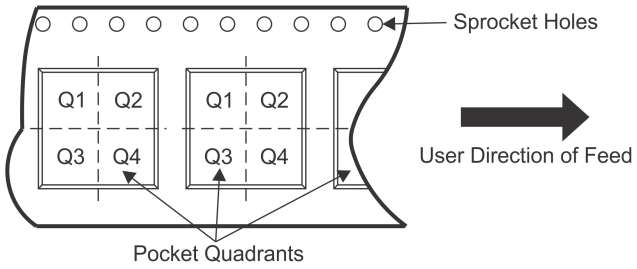


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

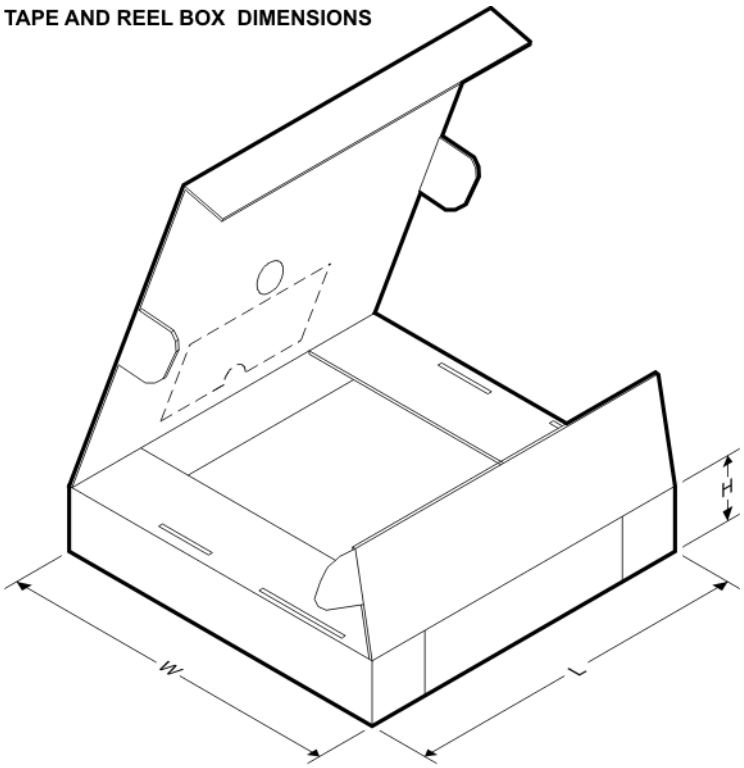
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3779BQDBVRQ1	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3779CQDBVRQ1	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3780AQDBVRQ1	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3780BQDBVRQ1	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3780CQDBVRQ1	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

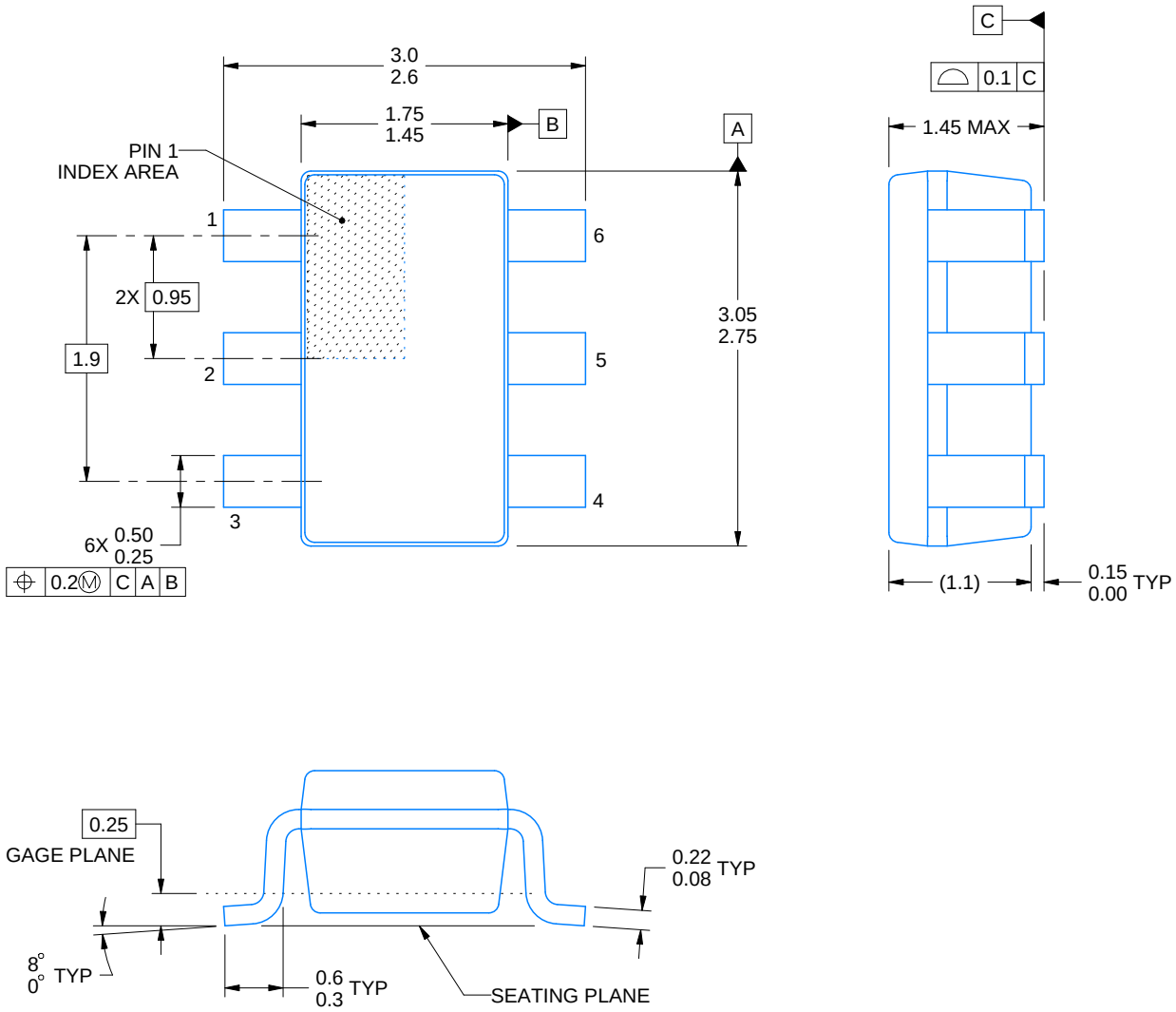
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3779BQDBVRQ1	SOT-23	DBV	6	3000	180.0	180.0	18.0
TPS3779CQDBVRQ1	SOT-23	DBV	6	3000	180.0	180.0	18.0
TPS3780AQDBVRQ1	SOT-23	DBV	6	3000	180.0	180.0	18.0
TPS3780BQDBVRQ1	SOT-23	DBV	6	3000	180.0	180.0	18.0
TPS3780CQDBVRQ1	SOT-23	DBV	6	3000	180.0	180.0	18.0

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



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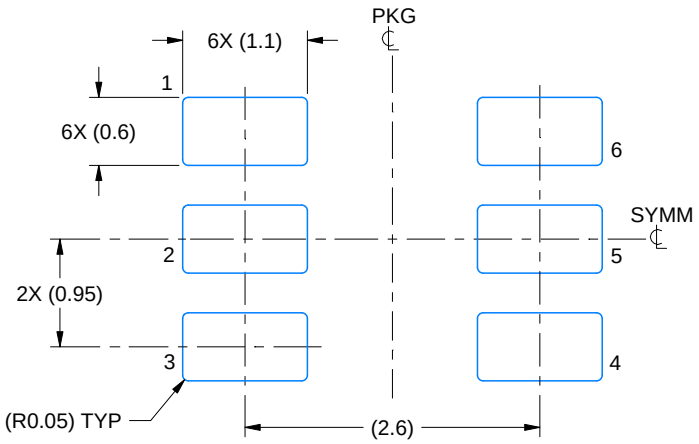
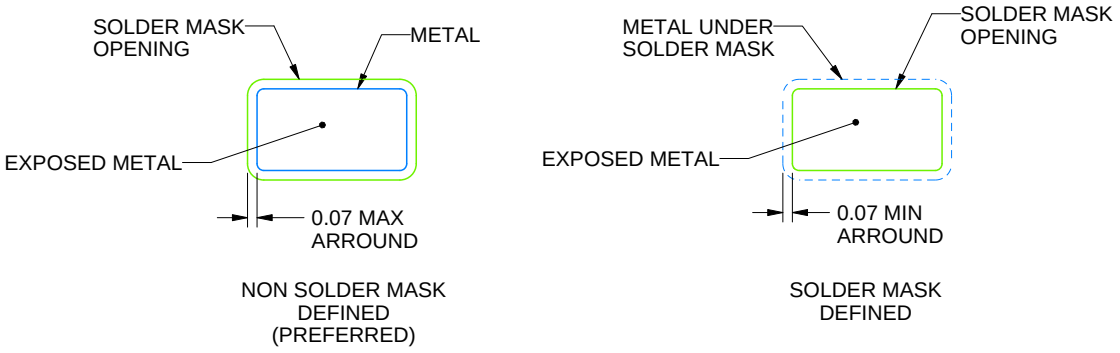
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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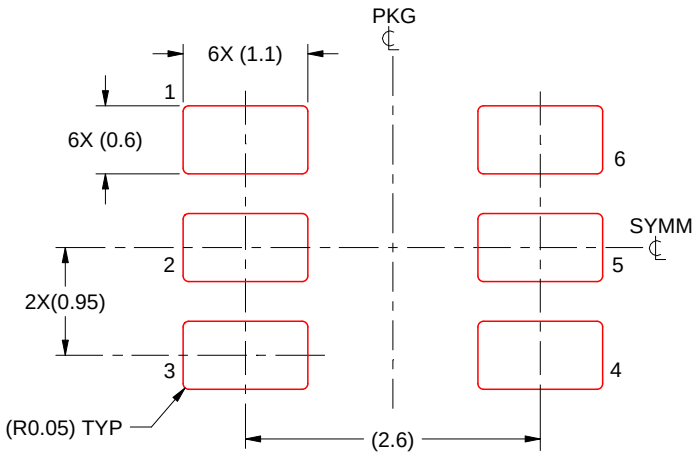
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/C 06/2021

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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