NX3L4051-Q100

Single low-ohmic 8-channel analog switch

Rev. 1 — 7 August 2012 Product data sheet

1. General description

The NX3L4051-Q100 is a low-ohmic 8-channel analog switch, suitable for use as an analog or digital multiplexer/demultiplexer. The NX3L4051-Q100 has three digital select inputs (S1 to S3), eight independent inputs/outputs (Y0 to Y7) and a common input/output (Z). All eight switches share an enable input ($\overline{E}$). A HIGH on $\overline{E}$ causes all switches into the high impedance OFF-state, independent of Sn.

Schmitt trigger action at the digital inputs makes the circuit tolerant to slower input rise and fall times. Low threshold digital inputs allows this device to be driven by 1.8 V logic levels in 3.3 V applications without significant increase in supply current I_{CC}. This makes it possible for the NX3L4051-Q100 to switch 4.3 V signals with a 1.8 V digital controller, eliminating the need for logic level translation. The NX3L4051-Q100 allows signals with amplitude up to V_{CC} to be transmitted from Z to Yn or from Yn to Z. The low ON resistance (0.5 Ω) and flatness (0.13 Ω), ensures minimal attenuation and distortion of transmitted signals.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
  - Specified from −40 °C to +85 °C and from −40 °C to +125 °C
- Wide supply voltage range from 1.4 V to 4.3 V
- Very low ON resistance (peak):
  - 1.7 Ω (typical) at V_{CC} = 1.4 V
  - 1.0 Ω (typical) at V_{CC} = 1.65 V
  - 0.6 Ω (typical) at V_{CC} = 2.3 V
  - 0.5 Ω (typical) at V_{CC} = 2.7 V
  - 0.5 Ω (typical) at V_{CC} = 4.3 V
- Break-before-make switching
- High noise immunity
- ESD protection:
  - MIL-STD-883, method 3015 Class 3A exceeds 7500 V
  - HBM JESD22-A114F Class 3A exceeds 7500 V
  - MM JESD22-A115-A exceeds 200 V (C = 200 pF, R = 0 Ω)
  - CDM AEC-Q100-011 revision B exceeds 1000 V
  - IEC61000-4-2 contact discharge exceeds 8000 V for switch ports
- CMOS low-power consumption

- Latch-up performance exceeds 100 mA per JESD 78B Class II Level A
- 1.8 V control logic at V_{CC} = 3.6 V
- Control input accepts voltages above supply voltage
- Very low supply current, even when input is below V_{CC}
- High current handling capability (350 mA continuous current under 3.3 V supply)

3. Applications

- Cell phone
- PDA
- Portable media player
- Analog multiplexing and demultiplexing
- Digital multiplexing and demultiplexing
- Signal gating

4. Ordering information

Table 1. Ordering information

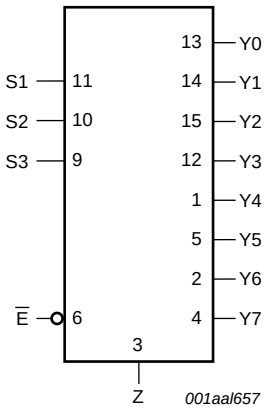
Type number	Package			
	Temperature range	Name	Description	Version
NX3L4051HR-Q100	–40 °C to +125 °C	HXQFN16	plastic thermal enhanced extremely thin quad flat package; no leads; 16 terminals; body 3 × 3 × 0.5 mm	SOT1039-2
NX3L4051PW-Q100	–40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

5. Marking

Table 2. Marking codes

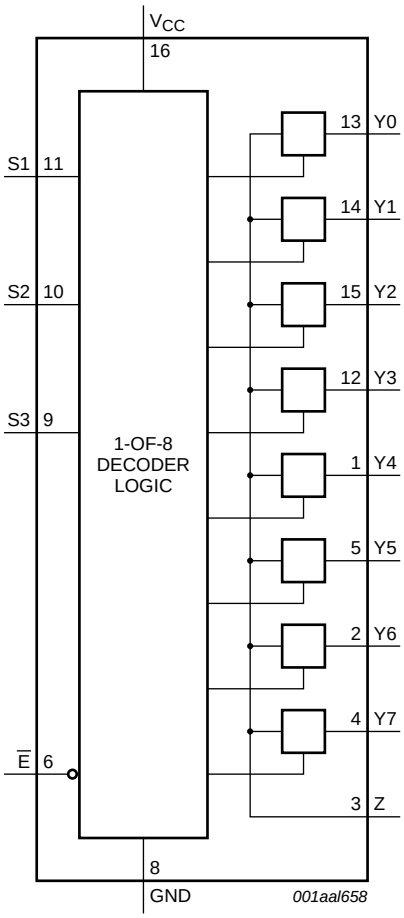
Type number	Marking code
NX3L4051HR-Q100	M41
NX3L4051PW-Q100	X3L4051

6. Functional diagram



Pin numbers are shown for TSSOP16 package only.

Fig 1. Logic symbol

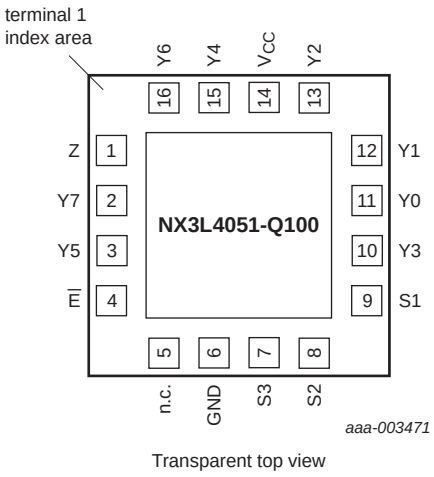


Pin numbers are shown for TSSOP16 package only.

Fig 2. Functional diagram

7. Pinning information

7.1 Pinning



Transparent top view

Fig 3. Pin configuration SOT1039-2 (HXQFN16)

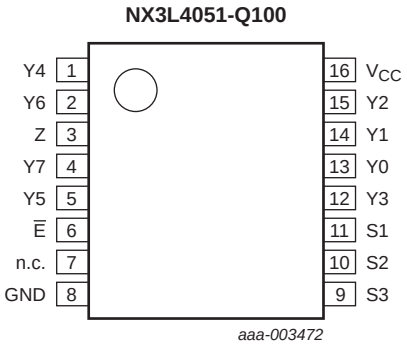


Fig 4. Pin configuration SOT403-1 (TSSOP16)

7.2 Pin description

Table 3. Pin description

Symbol	Pin		Description
	SOT1039-2	SOT403-1	
Y0, Y1, Y2, Y3, Y4, Y5, Y6, Y7	11, 12, 13, 10, 15, 3, 16, 2	13, 14, 15, 12, 1, 5, 2, 4	independent input or output
Z	1	3	independent output or input
$\overline{E}$	4	6	enable input (active LOW)
n.c.	5	7	not connected
GND	6	8	ground (0 V)
S1, S2, S3	9, 8, 7	11, 10, 9	select input
V_{CC}	14	16	supply voltage

8. Functional description

Table 4. Function table[1]

Input				Channel ON
$\overline{E}$	S3	S2	S1	
L	L	L	L	Y0 = Z
L	L	L	H	Y1 = Z
L	L	H	L	Y2 = Z
L	L	H	H	Y3 = Z
L	H	L	L	Y4 = Z
L	H	L	H	Y5 = Z
L	H	H	L	Y6 = Z
L	H	H	H	Y7 = Z
H	X	X	X	switches off

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care.

9. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+4.6	V
V_I	input voltage	Sn and $\overline{E}$	[1]	–0.5	+4.6	V
V_{SW}	switch voltage		[2]	–0.5	V_{CC} + 0.5	V
I_{IK}	input clamping current	V_I < –0.5 V		–50	-	mA
I_{SK}	switch clamping current	V_I < –0.5 V or V_I > V_{CC} + 0.5 V		-	±50	mA
I_{SW}	switch current	V_{SW} > –0.5 V or V_{SW} < V_{CC} + 0.5 V; source or sink current		-	±350	mA
		V_{SW} > –0.5 V or V_{SW} < V_{CC} + 0.5 V; pulsed at 1 ms duration, < 10 % duty cycle; peak current		-	±500	mA
T_{stg}	storage temperature			–65	+150	°C
P_{tot}	total power dissipation	T_{amb} = –40 °C to +125 °C				
		HXQFN16	[3]	-	250	mW
		TSSOP16	[4]	-	500	mW

[1] The minimum input voltage rating may be exceeded if the input current rating is observed.

[2] The minimum and maximum switch voltage ratings may be exceeded if the switch clamping current rating is observed but may not exceed 4.6 V.

[3] For HXQFN16 package: above 135 °C the value of P_{tot} derates linearly with 16.9 mW/K.

[4] For TSSOP16 package: above 60 °C the value of P_{tot} derates linearly with 5.5 mW/K.

10. Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			1.4	4.3	V
V_I	input voltage	Sn and $\overline{E}$		0	4.3	V
V_{SW}	switch voltage		[1]	0	V_{CC}	V
T_{amb}	ambient temperature			–40	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	Sn and $\overline{E}$; V_{CC} = 1.4 V to 4.3 V		-	200	ns/V

[1] To avoid sinking GND current from terminal Z when switch current flows in terminal Yn, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminal Z, no GND current flows from terminal Yn. In this case, there is no limit for the voltage drop across the switch.

11. Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground 0 V).

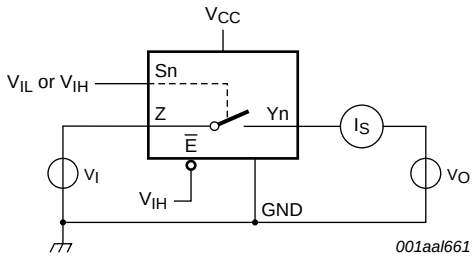
Symbol	Parameter	Conditions	T_{amb} = 25 °C			T_{amb} = –40 °C to +125 °C			Unit
			Min	Typ	Max	Min	Max (85 °C)	Max (125 °C)	
V_{IH}	HIGH-level input voltage	V_{CC} = 1.4 V to 1.6 V	0.9	-	-	0.9	-	-	V
		V_{CC} = 1.65 V to 1.95 V	0.9	-	-	0.9	-	-	V
		V_{CC} = 2.3 V to 2.7 V	1.1	-	-	1.1	-	-	V
		V_{CC} = 2.7 V to 3.6 V	1.3	-	-	1.3	-	-	V
		V_{CC} = 3.6 V to 4.3 V	1.4	-	-	1.4	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 1.4 V to 1.6 V	-	-	0.3	-	0.3	0.3	V
		V_{CC} = 1.65 V to 1.95 V	-	-	0.4	-	0.4	0.3	V
		V_{CC} = 2.3 V to 2.7 V	-	-	0.4	-	0.4	0.4	V
		V_{CC} = 2.7 V to 3.6 V	-	-	0.5	-	0.5	0.5	V
		V_{CC} = 3.6 V to 4.3 V	-	-	0.6	-	0.6	0.6	V
I_I	input leakage current	Sn and $\overline{E}$; V_I = GND to 4.3 V; V_{CC} = 1.4 V to 4.3 V	-	-	-	-	±0.5	±1	µA
$I_{S(OFF)}$	OFF-state leakage current	Yn ports; see Figure 5							
		V_{CC} = 1.4 V to 3.6 V	-	-	±5	-	±50	±500	nA
		V_{CC} = 3.6 V to 4.3 V	-	-	±10	-	±50	±500	nA
$I_{S(ON)}$	ON-state leakage current	Z port; V_{CC} = 1.4 V to 3.6 V; see Figure 6							
		V_{CC} = 1.4 V to 3.6 V	-	-	±20	-	±200	±2000	nA
		V_{CC} = 3.6 V to 4.3 V	-	-	±40	-	±200	±2000	nA
I_{CC}	supply current	V_I = V_{CC} or GND; V_{SW} = GND or V_{CC}							
		V_{CC} = 3.6 V	-	-	100	-	500	5000	nA
		V_{CC} = 4.3 V	-	-	150	-	800	6000	nA

Table 7. Static characteristics *...continued*

At recommended operating conditions; voltages are referenced to GND (ground 0 V).

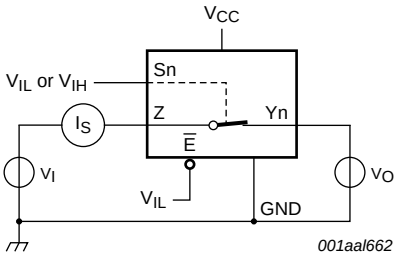
Symbol	Parameter	Conditions	T_{amb} = 25 °C			T_{amb} = –40 °C to +125 °C			Unit
			Min	Typ	Max	Min	Max (85 °C)	Max (125 °C)	
ΔI_{CC}	additional supply current	V_{SW} = GND or V_{CC}							
		V_I = 2.6 V; V_{CC} = 4.3 V	-	2.0	4.0	-	7	7	µA
		V_I = 2.6 V; V_{CC} = 3.6 V	-	0.35	0.7	-	1	1	µA
		V_I = 1.8 V; V_{CC} = 4.3 V	-	7.0	10.0	-	15	15	µA
		V_I = 1.8 V; V_{CC} = 3.6 V	-	2.5	4.0	-	5	5	µA
		V_I = 1.8 V; V_{CC} = 2.5 V	-	50	200	-	300	500	nA
C_I	input capacitance	Sn and $\overline{E}$	-	1.0	-	-	-	-	pF
$C_{S(OFF)}$	OFF-state capacitance		-	35	-	-	-	-	pF
$C_{S(ON)}$	ON-state capacitance		-	350	-	-	-	-	pF

11.1 Test circuits



V_I = 0.3 V or V_{CC} – 0.3 V; V_O = V_{CC} – 0.3 V or 0.3 V.

Fig 5. Test circuit for measuring OFF-state leakage current



V_I = 0.3 V or V_{CC} – 0.3 V; V_O = V_{CC} – 0.3 V or 0.3 V.

Fig 6. Test circuit for measuring ON-state leakage current

11.2 ON resistance

Table 8. ON resistance[1]

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for graphs see Figure 8 to Figure 14.

Symbol	Parameter	Conditions	T_{amb} = –40 °C to +85 °C			T_{amb} = –40 °C to +125 °C		Unit
			Min	Typ[2]	Max	Min	Max	
$R_{ON(peak)}$	ON resistance (peak)	V_I = GND to V_{CC}; I_{SW} = 100 mA; see Figure 7						
		V_{CC} = 1.4 V	-	1.7	3.7	-	4.1	Ω
		V_{CC} = 1.65 V	-	1.0	1.6	-	1.7	Ω
		V_{CC} = 2.3 V	-	0.6	0.8	-	0.9	Ω
		V_{CC} = 2.7 V	-	0.5	0.75	-	0.9	Ω
		V_{CC} = 4.3 V	-	0.5	0.75	-	0.9	Ω
ΔR_{ON}	ON resistance mismatch between channels	V_I = GND to V_{CC}; I_{SW} = 100 mA [3]						
		V_{CC} = 1.4 V; V_{SW} = 0.4 V	-	0.18	0.30	-	0.30	Ω
		V_{CC} = 1.65 V; V_{SW} = 0.5 V	-	0.18	0.20	-	0.30	Ω
		V_{CC} = 2.3 V; V_{SW} = 0.7 V	-	0.07	0.10	-	0.13	Ω
		V_{CC} = 2.7 V; V_{SW} = 0.8 V	-	0.07	0.10	-	0.13	Ω
		V_{CC} = 4.3 V; V_{SW} = 0.8 V	-	0.07	0.10	-	0.13	Ω
$R_{ON(flat)}$	ON resistance (flatness)	V_I = GND to V_{CC}; I_{SW} = 100 mA [4]						
		V_{CC} = 1.4 V	-	1.0	3.3	-	3.6	Ω
		V_{CC} = 1.65 V	-	0.5	1.2	-	1.3	Ω
		V_{CC} = 2.3 V	-	0.15	0.3	-	0.35	Ω
		V_{CC} = 2.7 V	-	0.13	0.3	-	0.35	Ω
		V_{CC} = 4.3 V	-	0.2	0.4	-	0.45	Ω

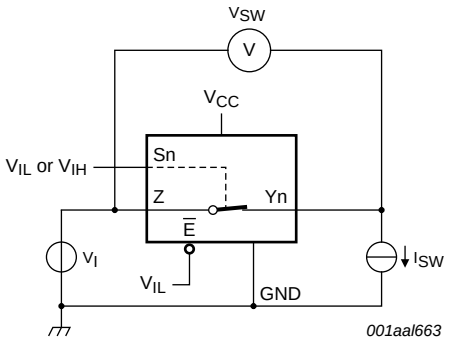
[1] For NX3L4051PW-Q100 (TSSOP16 package), all ON resistance values are up to 0.05 Ω higher.

[2] Typical values are measured at T_{amb} = 25 °C.

[3] Measured at identical V_{CC}, temperature and input voltage.

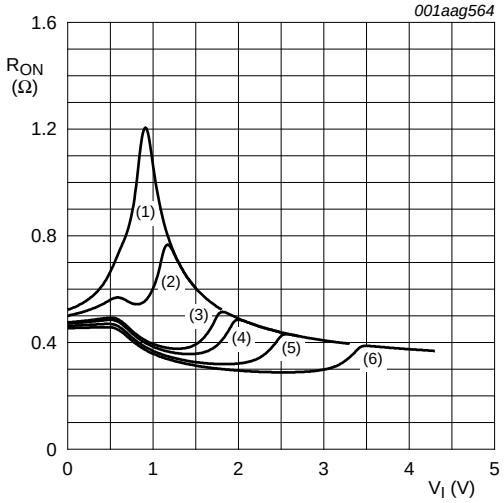
[4] Flatness is defined as the difference between the maximum and minimum value of ON resistance measured at identical V_{CC} and temperature.

11.3 ON resistance test circuit and graphs



$R_{ON} = V_{SW} / I_{SW}$.

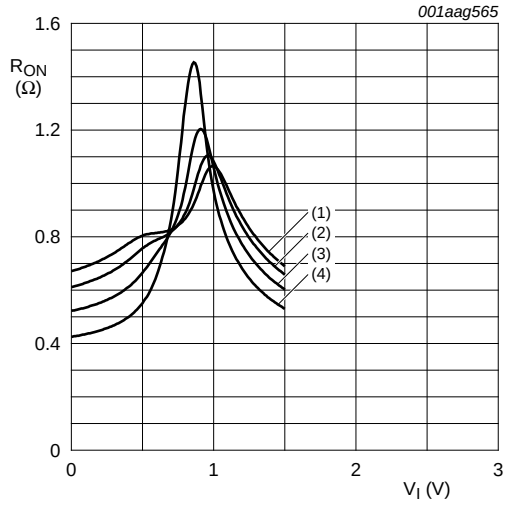
Fig 7. Test circuit for measuring ON resistance



(1) V_{CC} = 1.5 V.
(2) V_{CC} = 1.8 V.
(3) V_{CC} = 2.5 V.
(4) V_{CC} = 2.7 V.
(5) V_{CC} = 3.3 V.
(6) V_{CC} = 4.3 V.

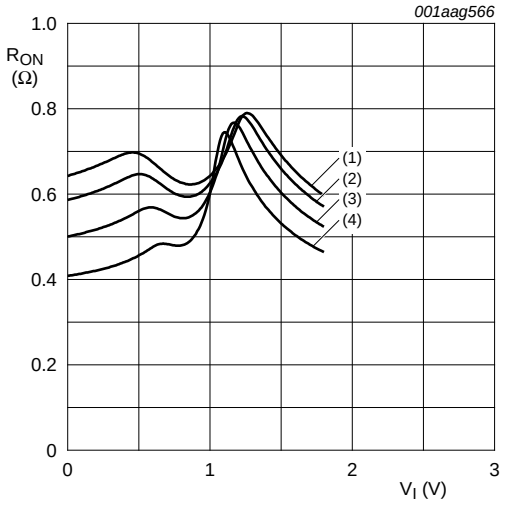
Measured at T_{amb} = 25 °C.

Fig 8. Typical ON resistance as a function of input voltage



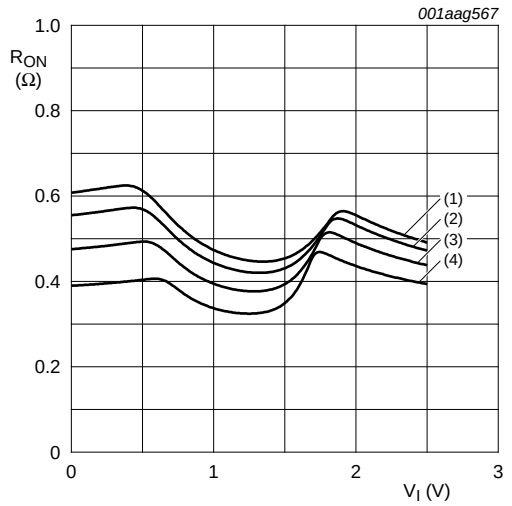
(1) T_{amb} = 125 °C.
(2) T_{amb} = 85 °C.
(3) T_{amb} = 25 °C.
(4) T_{amb} = −40 °C.

Fig 9. ON resistance as a function of input voltage; V_{CC} = 1.5 V



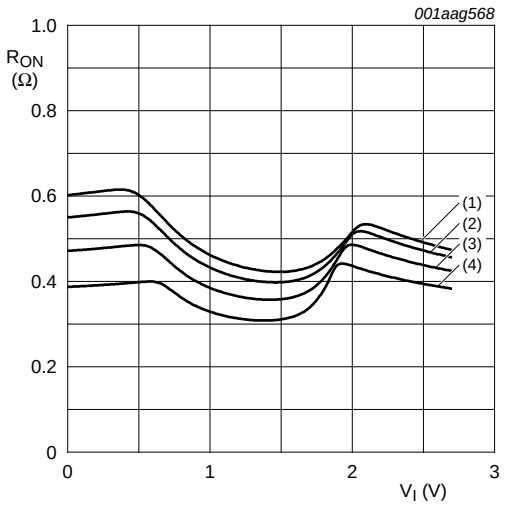
(1) T_{amb} = 125 °C.
(2) T_{amb} = 85 °C.
(3) T_{amb} = 25 °C.
(4) T_{amb} = −40 °C.

Fig 10. ON resistance as a function of input voltage; V_{CC} = 1.8 V



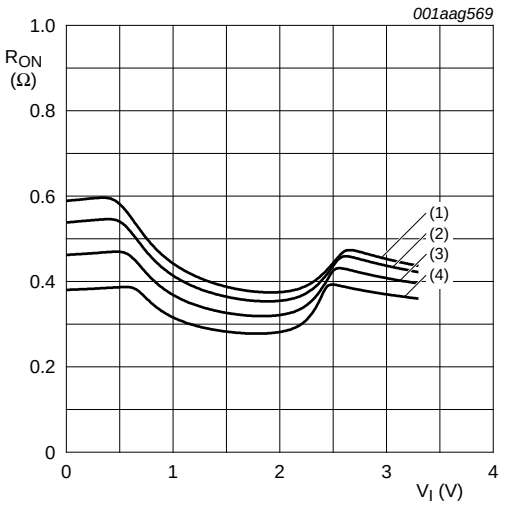
(1) T_{amb} = 125 °C.
(2) T_{amb} = 85 °C.
(3) T_{amb} = 25 °C.
(4) T_{amb} = −40 °C.

Fig 11. ON resistance as a function of input voltage; V_{CC} = 2.5 V



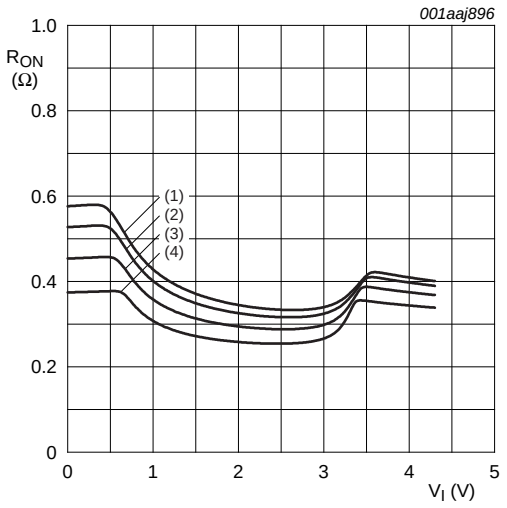
(1) T_{amb} = 125 °C.
(2) T_{amb} = 85 °C.
(3) T_{amb} = 25 °C.
(4) T_{amb} = −40 °C.

Fig 12. ON resistance as a function of input voltage; V_{CC} = 2.7 V



(1) T_{amb} = 125 °C.
(2) T_{amb} = 85 °C.
(3) T_{amb} = 25 °C.
(4) T_{amb} = –40 °C.

Fig 13. ON resistance as a function of input voltage; V_{CC} = 3.3 V



(1) T_{amb} = 125 °C.
(2) T_{amb} = 85 °C.
(3) T_{amb} = 25 °C.
(4) T_{amb} = –40 °C.

Fig 14. ON resistance as a function of input voltage; V_{CC} = 4.3 V

12. Dynamic characteristics

Table 9. Dynamic characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for load circuit see Figure 17.

Symbol	Parameter	Conditions	T_{amb} = 25 °C			T_{amb} = –40 °C to +125 °C			Unit
			Min	Typ[1]	Max	Min	Max (85 °C)	Max (125 °C)	
t_{en}	enable time	$\overline{E}$, Sn to Z or Yn; see Figure 15							
		V_{CC} = 1.4 V to 1.6 V	-	45	100	-	120	125	ns
		V_{CC} = 1.65 V to 1.95 V	-	32	75	-	85	95	ns
		V_{CC} = 2.3 V to 2.7 V	-	21	50	-	55	60	ns
		V_{CC} = 2.7 V to 3.6 V	-	19	45	-	45	50	ns
		V_{CC} = 3.6 V to 4.3 V	-	19	45	-	45	50	ns
t_{dis}	disable time	$\overline{E}$, Sn to Z or Yn; see Figure 15							
		V_{CC} = 1.4 V to 1.6 V	-	25	80	-	90	105	ns
		V_{CC} = 1.65 V to 1.95 V	-	15	65	-	70	75	ns
		V_{CC} = 2.3 V to 2.7 V	-	9	30	-	35	40	ns
		V_{CC} = 2.7 V to 3.6 V	-	8	25	-	30	35	ns
		V_{CC} = 3.6 V to 4.3 V	-	8	25	-	30	35	ns

Table 9. Dynamic characteristics *...continued*

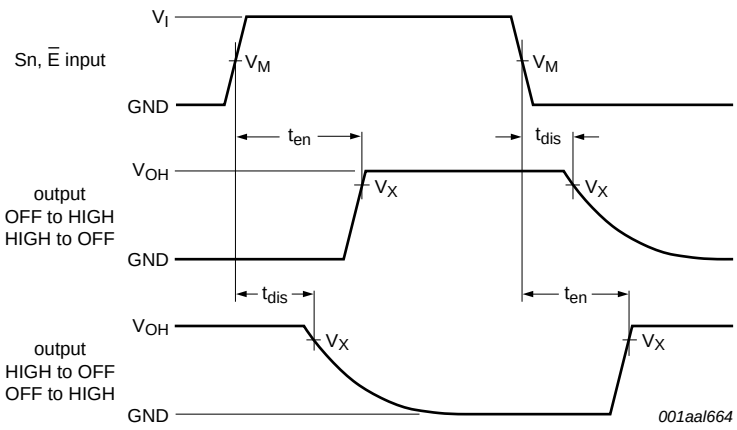
At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for load circuit see Figure 17.

Symbol	Parameter	Conditions	T_{amb} = 25 °C			T_{amb} = –40 °C to +125 °C			Unit
			Min	Typ[1]	Max	Min	Max (85 °C)	Max (125 °C)	
t_{b-m}	break-before-make time	see Figure 16 [2]							
		V_{CC} = 1.4 V to 1.6 V	-	19	-	9	-	-	ns
		V_{CC} = 1.65 V to 1.95 V	-	17	-	7	-	-	ns
		V_{CC} = 2.3 V to 2.7 V	-	12	-	4	-	-	ns
		V_{CC} = 2.7 V to 3.6 V	-	10	-	3	-	-	ns
		V_{CC} = 3.6 V to 4.3 V	-	9	-	2	-	-	ns

[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.5 V, 1.8 V, 2.5 V, 3.3 V and 4.3 V respectively.

[2] Break-before-make guaranteed by design.

12.1 Waveform and test circuits



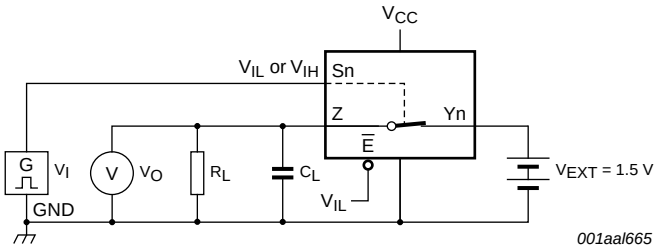
Measurement points are given in Table 10.

Logic level: V_{OH} is typical output voltage level that occurs with the output load.

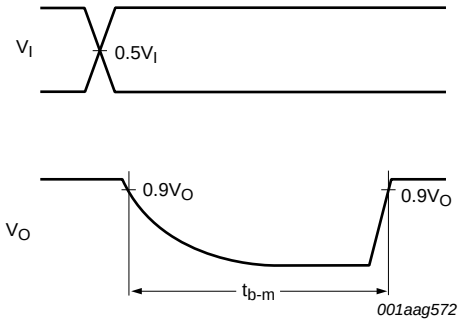
Fig 15. Enable and disable times

Table 10. Measurement points

Supply voltage	Input	Output
V_{CC}	V_M	V_X
1.4 V to 4.3 V	$0.5V_{CC}$	$0.9V_{OH}$

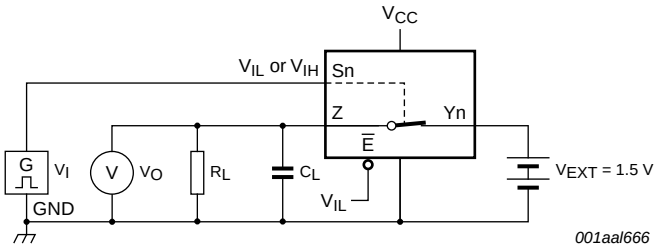


a. Test circuit



b. Input and output measurement points

Fig 16. Test circuit for measuring break-before-make timing



Test data is given in Table 11.

Definitions test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

V_{EXT} = External voltage for measuring switching times.

V_I may be connected to Sn or $\overline{E}$.

Fig 17. Test circuit for measuring switching times

Table 11. Test data

Supply voltage	Input		Load	
V_{CC}	V_I	t_r, t_f	C_L	R_L
1.4 V to 4.3 V	V_{CC}	≤ 2.5 ns	35 pF	50 Ω

12.2 Additional dynamic characteristics

Table 12. Additional dynamic characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); V_I = GND or V_{CC} (unless otherwise specified); $t_r = t_f \leq 2.5$ ns; T_{amb} = 25 °C.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
THD	total harmonic distortion	f_i = 20 Hz to 20 kHz; R_L = 32 Ω; see Figure 18	[1]				
		V_{CC} = 1.4 V; V_I = 1 V (p-p)		-	0.15	-	%
		V_{CC} = 1.65 V; V_I = 1.2 V (p-p)		-	0.10	-	%
		V_{CC} = 2.3 V; V_I = 1.5 V (p-p)		-	0.02	-	%
		V_{CC} = 2.7 V; V_I = 2 V (p-p)		-	0.02	-	%
		V_{CC} = 4.3 V; V_I = 2 V (p-p)		-	0.02	-	%
$f_{(-3dB)}$	−3 dB frequency response	R_L = 50 Ω; see Figure 19	[1]				
		V_{CC} = 1.4 V to 4.3 V		-	15	-	MHz
α_{iso}	isolation (OFF-state)	f_i = 100 kHz; R_L = 50 Ω; see Figure 20	[1]				
		V_{CC} = 1.4 V to 4.3 V		-	−90	-	dB
V_{ct}	crosstalk voltage	between digital inputs and switch; f_i = 1 MHz; C_L = 50 pF; R_L = 50 Ω; see Figure 21					
		V_{CC} = 1.4 V to 3.6 V		-	0.2	-	V
		V_{CC} = 3.6 V to 4.3 V		-	0.3	-	V
Xtalk	crosstalk	between switches; f_i = 100 kHz; R_L = 50 Ω; see Figure 22	[1]				
		V_{CC} = 1.4 V to 4.3 V		-	−90	-	dB
Q_{inj}	charge injection	f_i = 1 MHz; C_L = 0.1 nF; R_L = 1 MΩ; V_{gen} = 0 V; R_{gen} = 0 Ω; see Figure 23					
		V_{CC} = 1.5 V		-	3	-	pC
		V_{CC} = 1.8 V		-	4	-	pC
		V_{CC} = 2.5 V		-	6	-	pC
		V_{CC} = 3.3 V		-	9	-	pC
		V_{CC} = 4.3 V		-	15	-	pC

[1] f_i is biased at $0.5V_{CC}$.

12.3 Test circuits

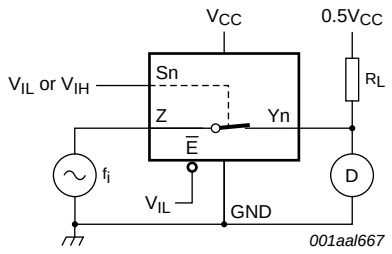
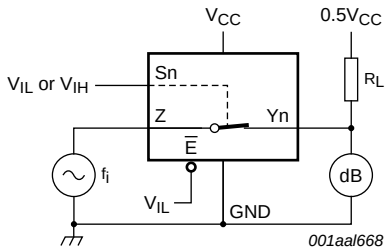
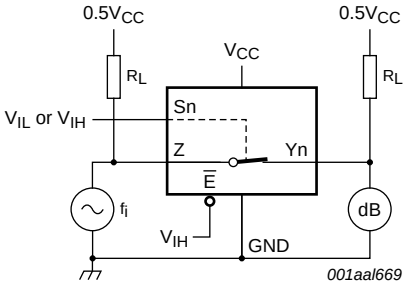


Fig 18. Test circuit for measuring total harmonic distortion



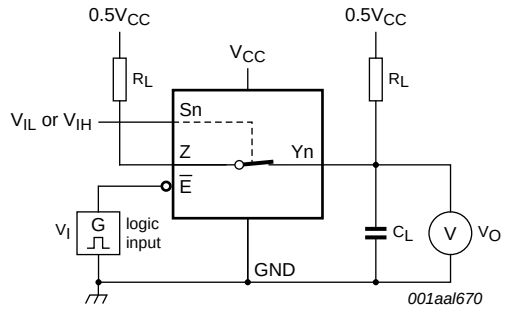
Adjust f_i voltage to obtain 0 dBm level at output. Increase f_i frequency until dB meter reads −3 dB.

Fig 19. Test circuit for measuring the frequency response when channel is in ON-state

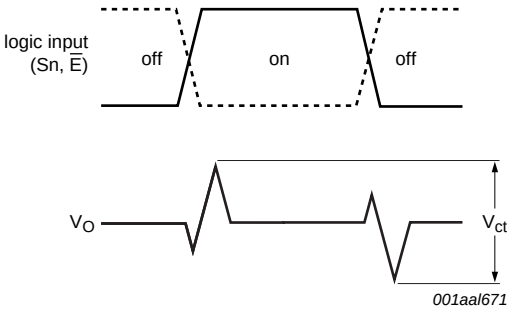


Adjust f_i voltage to obtain 0 dBm level at input.

Fig 20. Test circuit for measuring isolation (OFF-state)



a. Test circuit



b. Input and output pulse definitions

Fig 21. Test circuit for measuring crosstalk voltage between digital inputs and switch

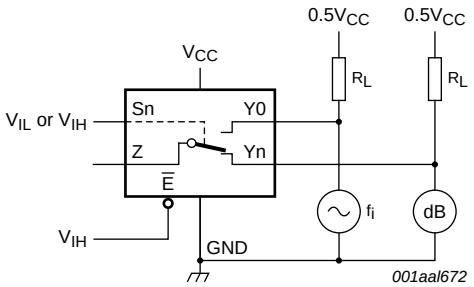
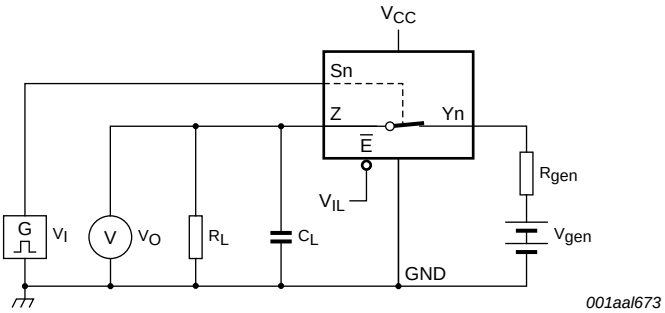
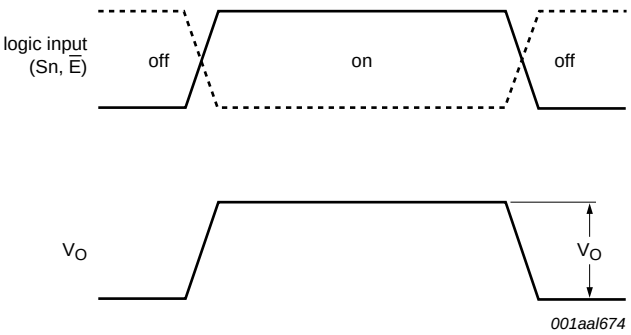


Fig 22. Test circuit for measuring crosstalk between switches



a. Test circuit



b. Input and output pulse definitions

Definition: $Q_{inj} = \Delta V_O \times C_L$.

ΔV_O = output voltage variation.

R_{gen} = generator resistance.

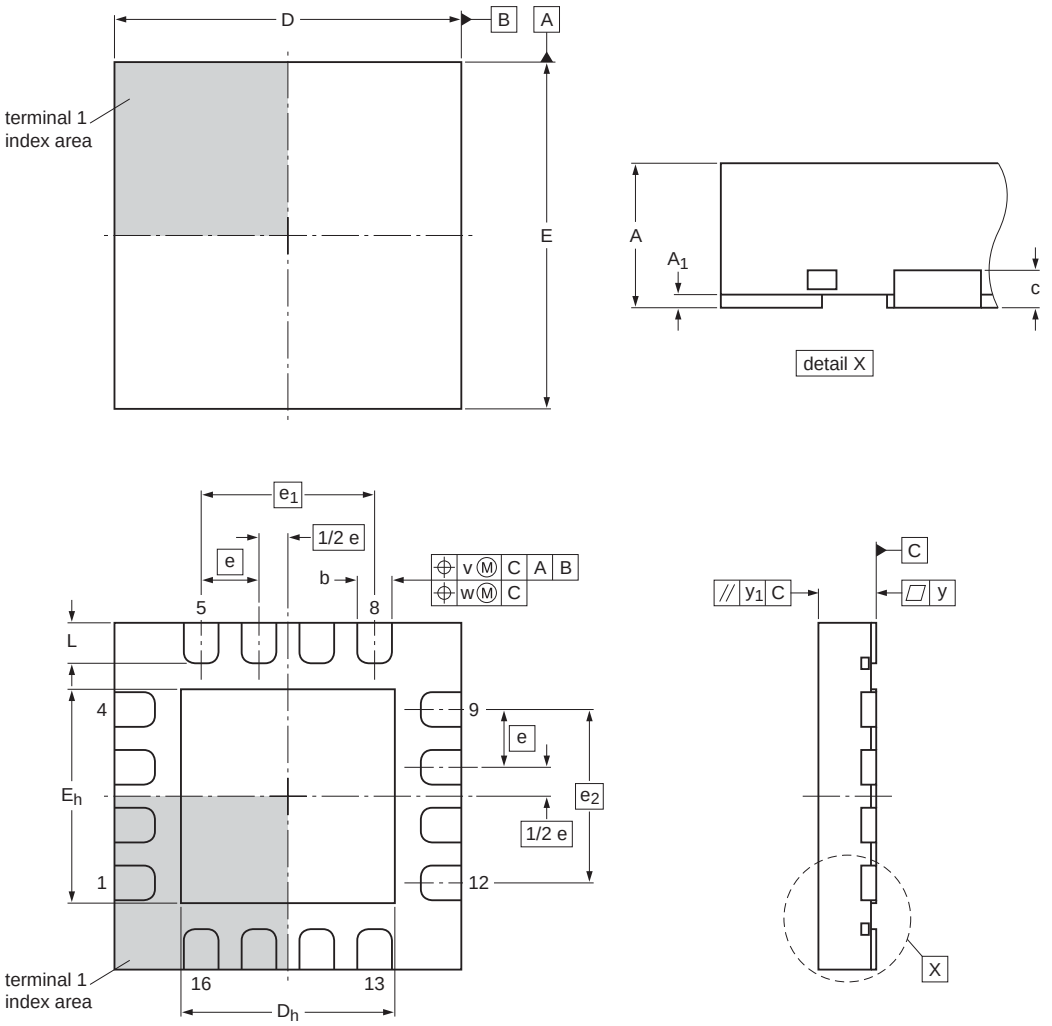
V_{gen} = generator voltage.

V_I may be connected to Sn or $\overline{E}$.

Fig 23. Test circuit for measuring charge injection

13. Package outline

HXQFN16: plastic thermal enhanced extremely thin quad flat package; no leads; 16 terminals; body 3 x 3 x 0.5 mm **SOT1039-2**



Dimensions

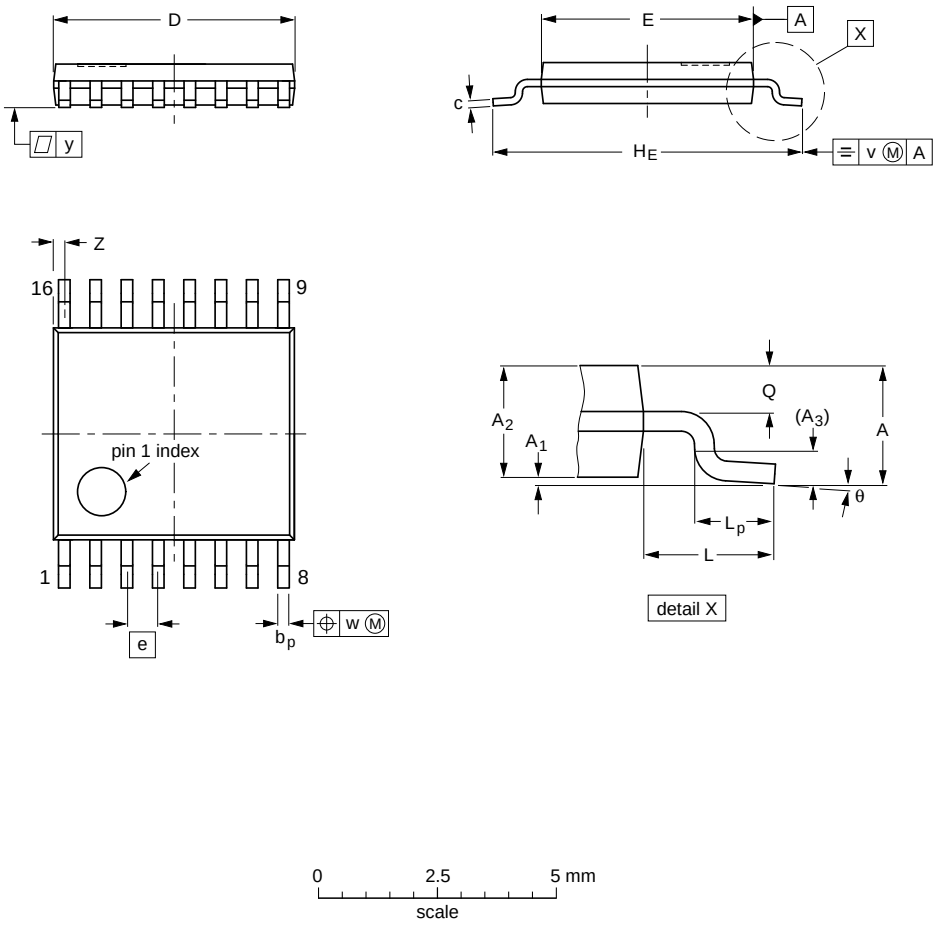
Unit		A	A_1	b	c	D	D_h	E	E_h	e	e_1	e_2	L	v	w	y	y_1
	max	0.5	0.05	0.35		3.1	1.95	3.1	1.95				0.40				
mm	nom			0.30	0.127	3.0	1.85	3.0	1.85	0.5	1.5	1.5	0.35	0.1	0.05	0.05	0.1
	min		0.00	0.25		2.9	1.75	2.9	1.75				0.30				

sot1039-2_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1039-2	- - -		- - -			~~10-07-29~~ 11-03-30

Fig 24. Package outline SOT1039-2 (HXQFN16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~99-12-27~~ 03-02-18

Fig 25. Package outline SOT403-1 (TSSOP16)

14. Abbreviations

Table 13. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
PDA	Personal Digital Assistant
MIL	Military

15. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NX3L4051_Q100 v.1	20120807	Product data sheet	-	-

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

16.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

16.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use in automotive applications — This NXP Semiconductors product has been qualified for use in automotive applications. Unless otherwise agreed in writing, the product is not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

16.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

17. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

18. Contents

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 7 August 2012
Document identifier: NX3L4051_Q100