PRODUCT DISCONTINUANCE NOTIFICATION

EOL-000172

Date: 22SEP2017

☒	Semtech Corporation, 200 Flynn Road, Camarillo CA 93012
☐	Semtech Canada Corporation, 4281 Harvester Road, Burlington, Ontario L7L 5M4 Canada
☐	Semtech Irvine, 5141 California Ave., Suite 100, Irvine CA 92617
☐	Semtech Neuchatel Sarl, Route des Gouttes d'Or 40, CH-2000 Neuchatel Switzerland
☐	Semtech Bristol, Nanotech Semiconductor, 2 West Point Court, Bristol, United Kingdom, BS32 4PY
☐	Semtech Corpus Christi SA de CV, Carretera Matamorros Edificio 7, Reynosa, Tamaulipas, Mexico 88780
☐	Semtech Plano, 1101 Resource Drive, Suite 121, Plano TX 75074
☐	

Product Discontinuance Details

Purpose, Description and Effect of Change:

This notification is to inform your company that Semtech is discontinuing the manufacture of the product listed below. In accordance with Semtech's product discontinuation policy, we are hereby giving notice of these product changes in order for your company to make any final lifetime purchases of the discontinued product that are still in supply.

Part Number(s) Affected:	**Customer Part Number(s) Affected:** ☒ N/A
RClamp1821Z RClamp0531Z RClamp0542Z uClamp0512Z	

Replacement or Alternate Part Number(s) ☐ N/A or Not Offered

RClamp1821Z ⇨RClamp1851ZA
RClamp0531Z ⇨RClamp5031ZA or RClamp5011ZA
RClamp0542Z ⇨RClamp0542ZA
μClamp0512Z ⇨μClamp0512ZA

Last Time Buy (LTB) Date	21MAR2018	**Must Accept Final Delivery by**	**22SEP2018**
Sample Availability of Alt. Part	22SEP2017 ☐ N/A	**Qualification Report Availability of Alt. Part**	22SEP2017 ☐ N/A

Supporting Documents for Alternate or Replacement parts/Attachments:

- **Data Sheet**
- **Qualification Report**

Last Time Buy Conditions

We request you carefully review this information and notify your purchasing offices and buyers to place your company's final purchases for available discontinued products as soon as possible according to the following last time buy terms and conditions.

1. **Availability:** The ***Last Time Buy Date*** and ***Date to Accept Final Delivery*** are noted above. All orders must have a ***requested ship date before the Date to Accept Final Delivery*** or the order will be rejected. ***The Last Time Buy Date automatically expires when the final available inventory quantity has been scheduled and sold.***

2. **Pricing:** The product unit price will be subject to Semtech's individual price quotation of your company's last time buy requirements.

3. **Order Acceptance/Change Conditions:**
   A. Semtech will accept last time orders from your company for the discontinued products as "Firm and Final". As such, these orders will not be subject to any reschedule, cancellation, or termination by your company without Semtech's prior written authorization and payment of full termination charges.
   B. Semtech reserves its right to make changes in the scheduled delivery dates, or to terminate remaining undelivered quantities of your company's last time buy order, due to changes in Semtech's last time manufacturing capabilities, or for commercially impracticable circumstances which makes delivery not feasible.

4. **Quantities:** The following applies to final buy quantities for the available discontinued product:
   A. **First:** The quantities in any existing unfilled orders and contracts acknowledged by Semtech will be honored, then
   B. **Next:** The unfilled quantities in any volume agreement(s) or quantities in unexpired standalone quote(s) will be accepted, and
   C. **Finally:** Any additional reasonable quantity of product that Semtech quotes based upon your company's identified requirements will be taken.

IN THE EVENT OF CONFLICT FOR THE LIMITED AVAILABILITY PRODUCT, QUANTITIES FOR CUSTOMER'S OR DISTRIBUTOR'S ORDERS WILL BE DETERMINED ON A FIRST-COME FIRST-SERVE BASIS; AND WILL BE SUBJECT TO SEMTECH'S AVAILABLE INVENTORY AND REMAINING MANUFACTURING CAPACITY FOR THE PRODUCT.

Limited Warranty

All discontinued product orders subject to this notice shall carry Semtech's standard limited warranty; or, if applicable, the warranty set forth in a duly executed formal contract between Semtech and your company will apply; except that:

1. Semtech will accept all valid warranty claims for credit only, unless a replacement order is otherwise agreed upon by Semtech and the replacement parts can be manufactured or delivered from remaining inventory.
2. The applicable warranty period for making any return claims for discontinued products will be no later than ninety (90) days following delivery of the discontinued products.
3. Any return claims must be made under Semtech's current Return Material Authorization "RMA" procedures.

Additional Provisions

SEMTECH ACCEPTS NO LIABILITY FOR EXCESS REPROCUREMENT COSTS OR FOR ANY SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES WHATSOEVER ASSOCIATED WITH THIS NOTICE, WITH ITS PRODUCTS, OR WITH THE FINAL MANUFACTURE AND PERFORMANCE AGAINST ANY LAST TIME BUY ORDERS RELATED TO THE DISCONTINUED PRODUCTS COVERED BY THIS NOTICE.

We regret the inconvenience and impact this notice may cause your company. Semtech's sales, marketing, and distribution personnel stand ready to assist you in placing your company's final orders, or in providing the product information you require.

For product inquiries or purchase order information, please contact your local Semtech sales representative.

PRODUCT DISCONTINUANCE NOTIFICATION

EOL-000172

Date: 22SEP2017

Issuing Authority		
Semtech Business Unit:		
Semtech Contact Info:	Les Fang Yuen Semtech Corporation Quality Assurance 200 Flynn Road Camarillo, CA 93012 lfangyuen@semtech.com Office: (949) 269-4443 Fax: (805) 498-3804	

FOR FURTHER INFORMATION & WORLDWIDE SALES COVERAGE: http://www.semtech.com/contact/index.html#support

RClamp1851ZA
Ultra Small RClamp®
1-Line, 18V ESD Protection

PROTECTION PRODUCTS - RailClamp®

Description

RClamp® TVS diodes are designed to protect sensitive electronics from damage or latch-up due to ESD. They are designed to replace multilayer varistors (MLVs) in portable applications such as cell phones, notebook computers, and other portable electronics. This device offers desirable characteristics for board level protection including fast response time, low operating and clamping voltage, and no device degradation.

RClamp®1851ZA is specifically designed for protection of Near Field Communications (NFC) interfaces. It features extremely good ESD protection characteristics including a low typical dynamic resistance of 0.16 Ohms, low peak ESD clamping voltage, and high ESD withstand voltage (+/-17kV contact per IEC 61000-4-2). Low typical capacitance (0.35pF at VR=0V) means that harmonic distortion the the RF signal is minimized. This device is bidirectional and has a working voltage of 18V for use on NFC resonator circuits without signal clipping.

RClamp1851ZA is in a 2-pin SLP0603P2X3F package measuring 0.6 x 0.3 mm with a nominal height of only 0.25mm. Leads are finished with NiAu. The small package gives the designer the flexibility to protect single lines in applications where arrays are not practical. The combination of small size and high ESD surge capability makes them ideal for use in portable applications such as cellular phones, digital cameras, and tablet PC's.

Features

- High ESD withstand Voltage: +/-17kV (Contact) and +/- 20kV (Air) per IEC 61000-4-2
- Ultra-small package
- Protects one high speed data line
- Low ESD clamping voltage
- Working voltage: 18V
- Low capacitance: 0.35pF typical
- Low leakage current
- Extremely low dynamic resistance: 0.16 Ohms (Typ)
- Solid-state silicon-avalanche technology

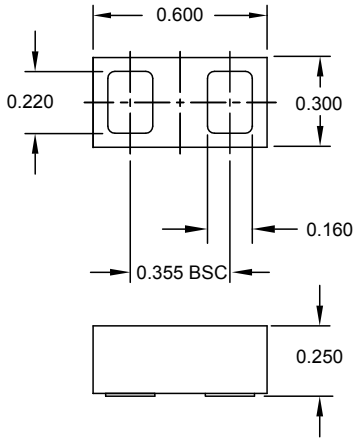
Mechanical Characteristics

- SLP0603P2X3F package
- Pb-Free, Halogen Free, RoHS/WEEE Compliant
- Nominal Dimensions: 0.6 x 0.3 x 0.25 mm
- Lead Finish: NiAu
- Marking: Marking code
- Packaging: Tape and Reel

Applications

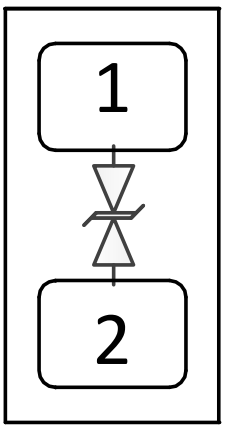
- Near Field Communication (NFC) lines
- RF signal lines
- Cellular Handsets
- Tablets
- FM Antenna

Package Dimensions



Nominal Dimensions in mm

Schematic & Pin Configuration



SLP0603P2X3F (Bottom View)

Absolute Maximum Ratings

Rating	Symbol	Value	Units
Peak Pulse Current (tp = 8/20μs)	I_{PP}	3	A
ESD per IEC 61000-4-2 (Air)(1) ESD per IEC 61000-4-2 (Contact)(1)	V_{ESD}	±20 ±17	kV
Operating Temperature	T_J	-40 to +85	°C
Storage Temperature	T_{STG}	-55 to +150	°C

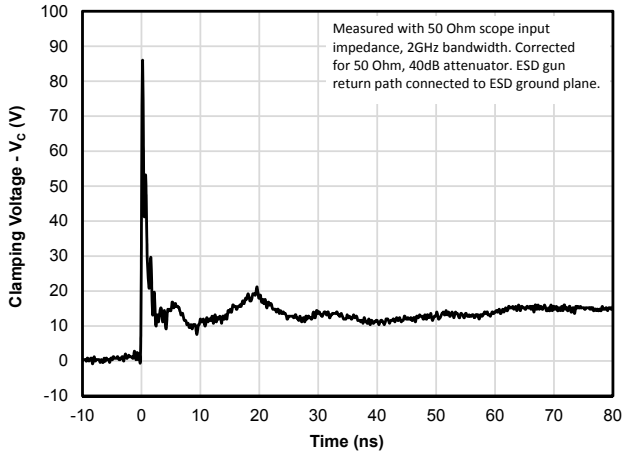
Electrical Characteristics (T=25°C unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Reverse Stand-Off Voltage	V_{RWM}	T = -40 to +85°C			18	V
Breakdown Voltage	V_{BR}	I_{BR} = 10μA	18.5	22.5	26.5	V
Reverse Leakage Current	I_R	V_{RWM} = 18V		<1	50	nA
ESD Clamping Voltage[2]	V_C	I_{PP} = 4A tp = 0.2/100ns		5.5		V
ESD Clamping Voltage[2]	V_C	I_{PP} = 16A tp = 0.2/100ns		7.5		V
Dynamic Resistance[2, 3]	R_{DYN}	tp = 0.2/100ns		0.16		Ohms
Junction Capacitance	C_J	VR = 0V; f = 1MHz		0.35	0.45	pF

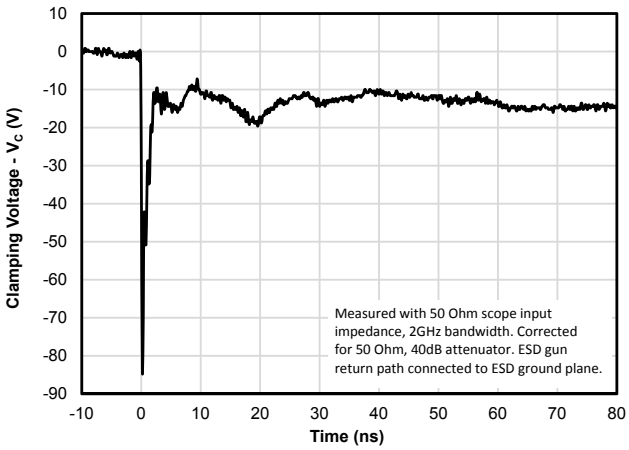
Notes
1)Measured with a 40dB attenuator, 50 Ohm scope input impedance, 2GHz bandwidth. ESD gun return path connected to ESD ground plane.
2)Transmission Line Pulse Test (TLP) Settings: tp = 100ns, tr = 0.2ns, I_{TLP} and V_{TLP} averaging window: t1 = 70ns to t2 = 90ns.
3)Dynamic resistance calculated from I_{TLP} = 4A to I_{TLP} = 16A
4)Device is electrically symmetrical

Typical Characteristics

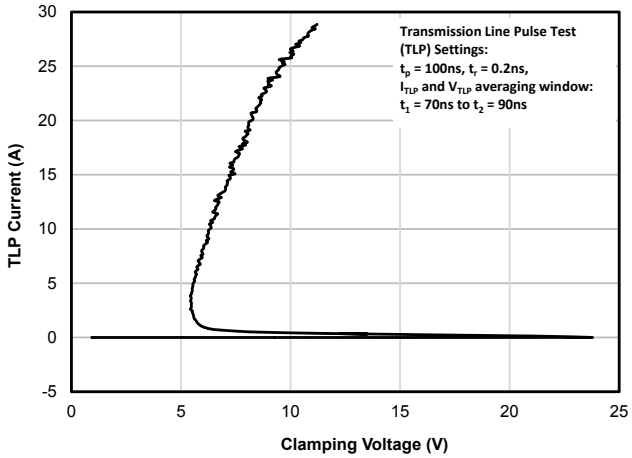
ESD Clamping (8kV Contact per IEC 61000-4-2)



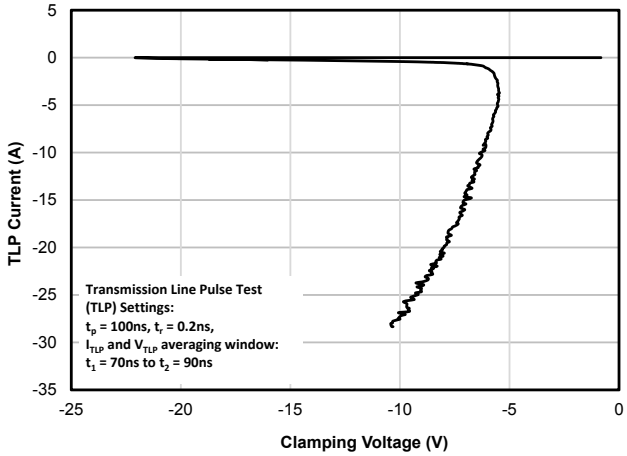
ESD Clamping (-8kV Contact per IEC 61000-4-2)



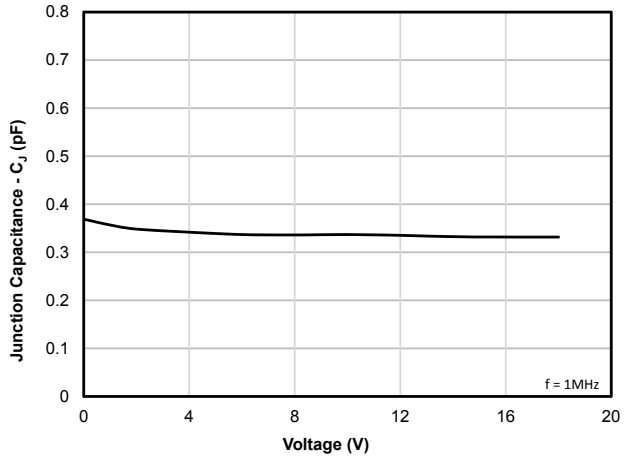
TLP Characteristic (Positive Pulse)



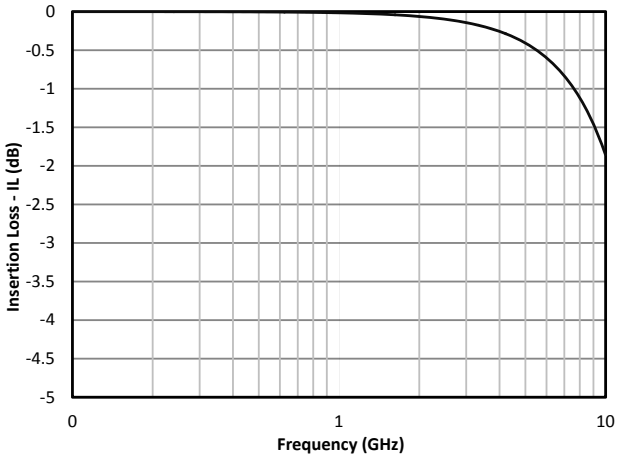
TLP Characteristic (Negative Pulse)



Capacitance vs. Reverse Voltage



Insertion Loss - S21 (dB)



Applications Information

ESD Protection of NFC Interfaces

The Near Field Communication (NFC) antenna is usually connected to the NFC controller IC via contact points on the phone. These contact points are user accessable and therefore may be subjected to ESD strikes. External protection (TVS) devices should be placed between the antenna and the NFC chip interface. The working voltage of the TVS should be high enough as not to clip the NFC signal. Additionaly, the capacitance of the device should be minimized in order to avoid harmonic disctortion of the RF signal. RClamp1851ZA meets these requirements and also features extremely low dynamic resistance resulting in low ESD clamping voltage. The low dynamic resistance also helps insure protection for Schottky diodes that may be used in the NFC circuit. RClamp1851ZA is designed to work on NFC circuits with AC signals as high as 18V. An example protection ciruit is shown below in Figure 1.

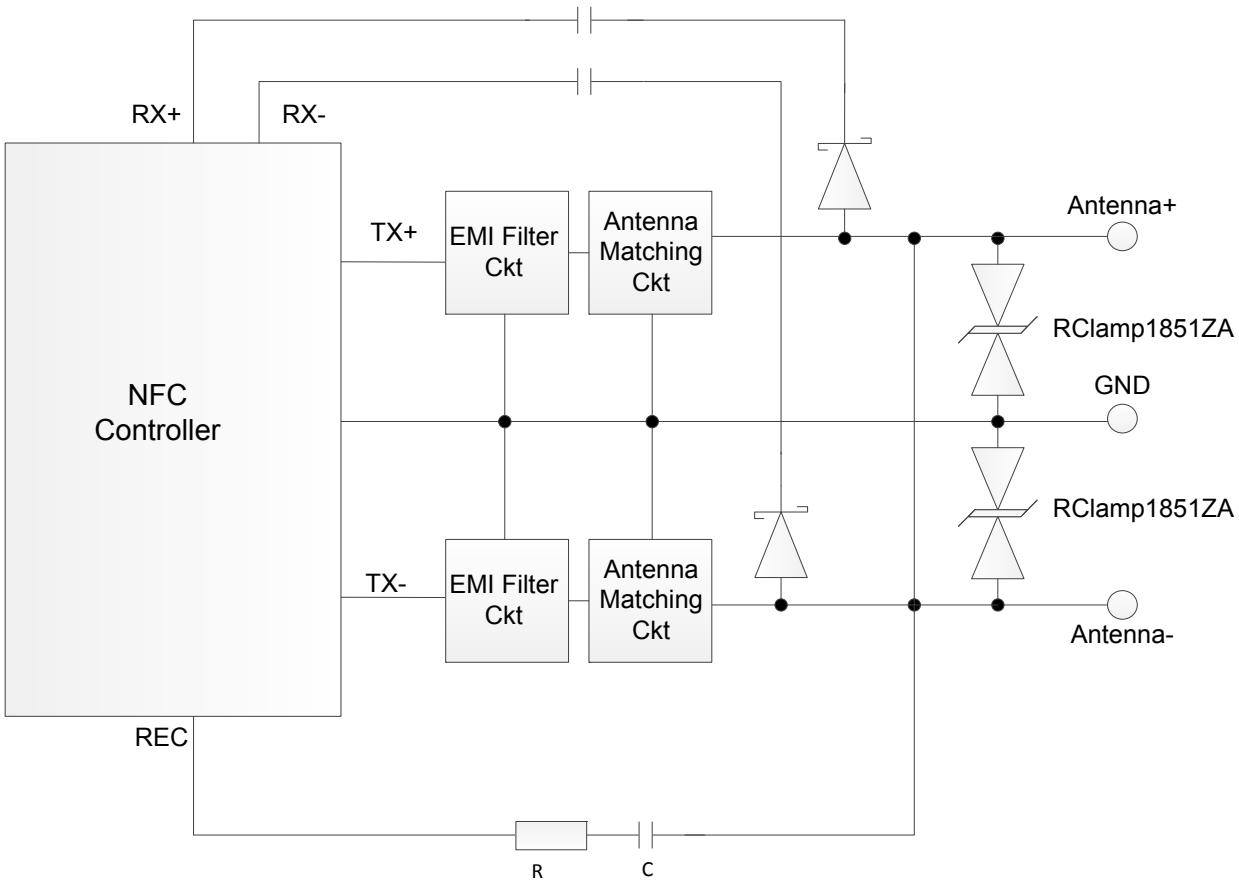


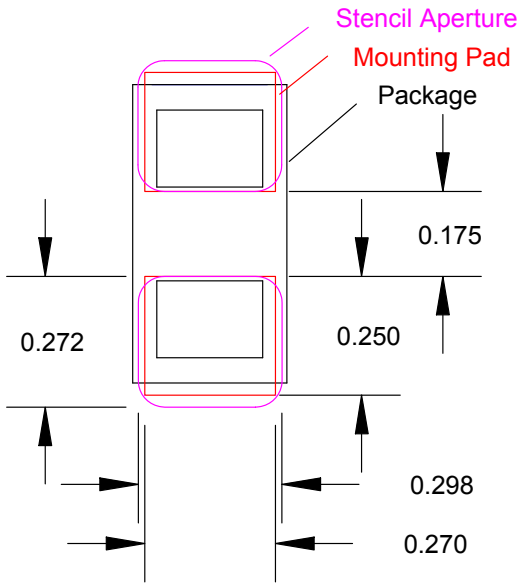
Figure 1 - NFC Protection Example

Applications Information

Assembly Guidelines

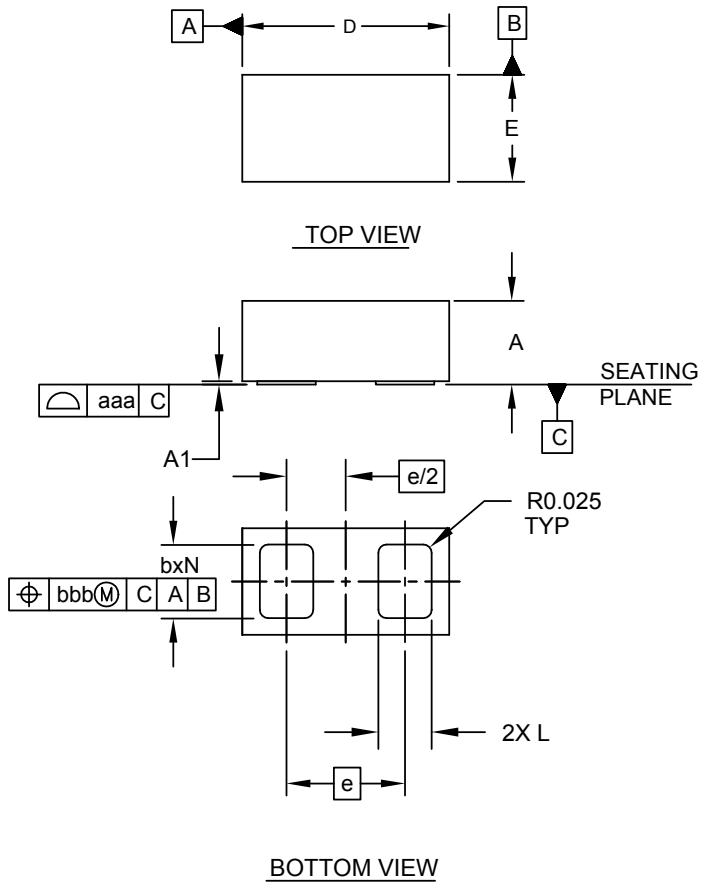
The small size of this device means that some care must be taken during the mounting process to insure reliable solder joint. The table below provides Semtech's recommended assembly guidelines for mounting this device. The figure at the right details Semtech's recommended aperture based on the below recommendations. Note that these are only recommendations and should serve only as a starting point for design since there are many factors that affect the assembly process. The exact manufacturing parameters will require some experimentation to get the desired solder application.

Assembly Parameter	Recommendation
Solder Stencil Design	Laser cut, Electro-polished
Aperture shape	Rectangular with rounded corners
Solder Stencil Thickness	0.100 mm (0.004")
Solder Paste Type	Type 4 size sphere or smaller
Solder Reflow Profile	Per JEDEC J-STD-020
PCB Solder Pad Design	Non-Solder mask defined
PCB Pad Finish	OSP OR NiAu



Recommended Mounting Pattern

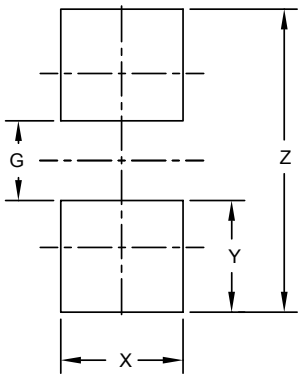
Outline Drawing - SLP0603P2X3F



DIMENSIONS			
DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.235	0.250	0.265
A1	0.000	0.010	0.050
b	0.200	0.220	0.240
D	0.580	0.600	0.620
E	0.280	0.300	0.320
e	0.355 BSC		
L	0.140	0.160	0.180
N	2		
aaa	0.08		
bbb	0.10		

NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).

Land Pattern - SLP0603P2X3F



DIMENSIONS	
DIM	MILLIMETERS
G	0.177
X	0.272
Y	0.247
Z	0.671

NOTES:
CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY.
CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR
COMPANY'S MANUFACTURING GUIDELINES ARE MET.

Marking

t

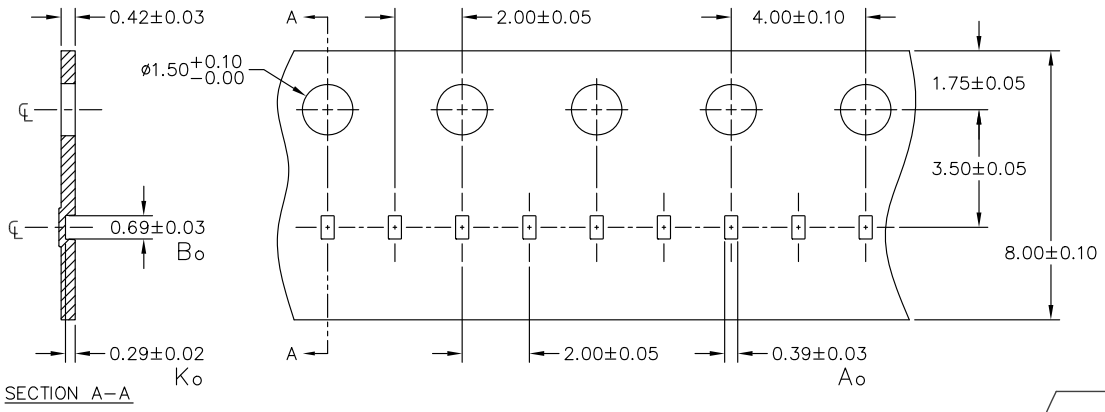
Notes: Device is Electrically Symmetrical

Ordering Information

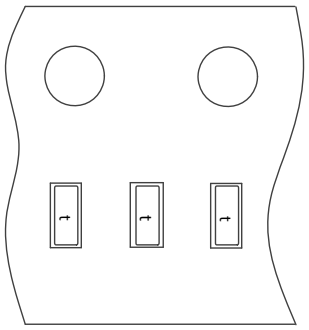
Part Number	Qty per Reel	Reel Size
RClamp1851ZATFT	15000	7”

Notes:
1) RailClamp and RClamp are trademarks of Semtech Corporation.

Tape and Reel Specification



NOTES: ALL DIMENSIONS IN MILLIMETERS UNLESS OTHERWISE SPECIFIED.



Contact Information

Semtech Corporation
Protection Products Division
200 Flynn Rd., Camarillo, CA 93012
Phone: (805)498-2111 FAX (805)498-3804

RClamp5031ZA
Ultra Small RClamp®
1 Line, 5V ESD Protection

PROTECTION PRODUCTS

Description

RClamp® TVS diodes are designed to protect sensitive electronics from damage or latch-up due to ESD. They are designed to replace 0201 size multilayer varistors (MLVs) in portable applications such as cell phones, notebook computers, and other portable electronics. This device offers desirable characteristics for board level protection including fast response time, low operating and clamping voltage, and no device degradation.

RClamp®5031ZA features extremely good ESD protection characteristics highlighted by low typical dynamic resistance of 0.17 Ohms, low peak ESD clamping voltage, and high ESD withstand voltage (+/-17kV contact per IEC 61000-4-2). Low maximum capacitance (0.45pF at VR=0V) minimizes loading on sensitive cirucuits. Each device will protect one high-speed data line operating at 5 Volts.

RClamp5031ZA is in a 2-pin SLP0603P2X3F package measuring 0.6 x 0.3 mm with a nominal height of only 0.25mm. Leads are finished with NiAu. The small package gives the designer the flexibility to protect single lines in applications where arrays are not practical. The combination of small size and high ESD surge capability makes them ideal for use in portable applications.

Features

- High ESD withstand Voltage: +/-17kV (Contact) per IEC 61000-4-2 and +/- 24kV (air) per IEC 61000-4-2
- Ultra-small package
- Protects one data line
- Low ESD clamping voltage
- Working voltage: 5V
- Low capacitance: 0.45pF maximum
- Low leakage current
- Low dynamic resistance: 0.17 Ω (typ)
- Solid-state silicon-avalanche technology

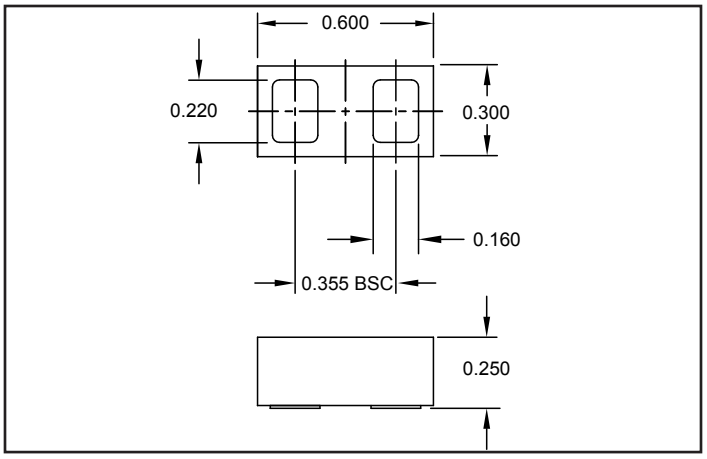
Mechanical Characteristics

- SLP0603P2X3F package
- Pb-Free, Halogen Free, RoHS/WEEE compliant
- Nominal Dimensions: 0.6 x 0.3 x 0.25 mm
- Lead Finish: NiAu
- Marking: Marking code
- Packaging: Tape and Reel

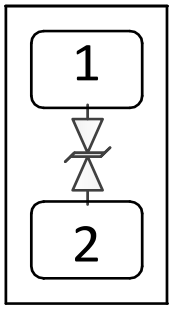
Applications

- USB3.0
- USB Type-C
- MiPi/MDDI
- MHL
- FM antenna
- Wearables

Package Dimension



Schematic & Pin Configuration



SLP0603P2X3F (Bottom View)

Absolute Maximum Rating

Rating	Symbol	Value	Units
Peak Pulse Current (tp = 1.2/50µs)	I_{PP}	4	A
ESD per IEC 61000-4-2 (Air)(2) ESD per IEC 61000-4-2 (Contact)(2)	V_{ESD}	±24 ±17	kV
Operating Temperature	T_J	-40 to +85	°C
Storage Temperature	T_{STG}	-55 to +150	°C

Electrical Characteristics (T=25°C unless otherwise specified)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Units
Reverse Stand-Off Voltage	V_{RWM}					5	V
Reverse Breakdown Voltage	V_{BR}	I_t = 10mA		6.5	8.5	10.5	V
Holding Current	I_H	$V=V_H$			100		mA
Reverse Leakage Current	I_R	V_{RWM} = 5V			<5	50	nA
Clamping Voltage	V_C	tp = 8/20µs	I_{PP} = 4A			13	V
ESD Clamping Voltage[2]	V_C	tp = 0.2/100ns	I_{PP} = 4A		5		V
			I_{PP} = 16A		7		
Dynamic Resistance[2,3]	R_{DYN}	tp = 0.2/100ns			0.17		Ω
Junction Capacitance	C_J	V_R = 0V, f = 1MHz	T = 25°C		0.35	0.45	pF

Notes

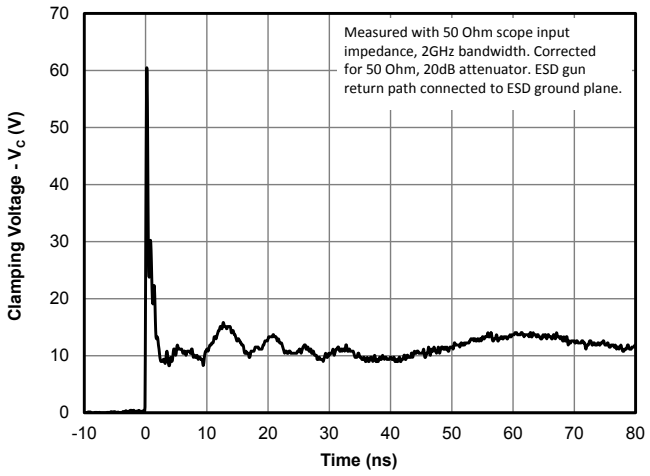
1) Measured with a 20dB attenuator, 50 Ohm scope input impedance, 2GHz bandwidth. ESD gun return path connected to ESD ground plane.

2) Transmission Line Pulse Test (TLP) Settings: tp = 100ns, tr = 0.2ns, I_{TLP} and V_{TLP} averaging window: t1 = 70ns to t2 = 90ns.

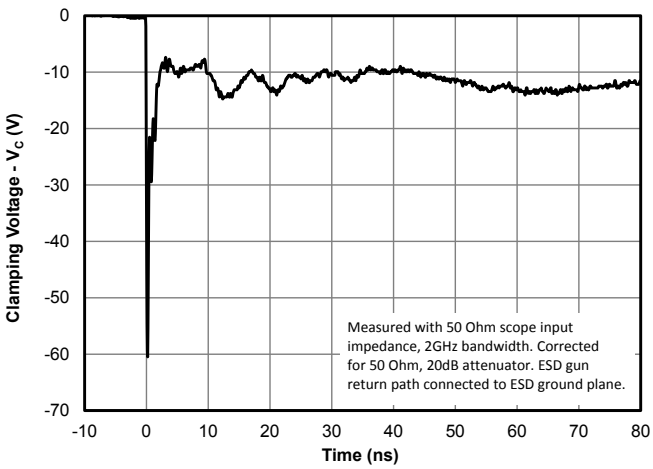
3) Dynamic resistance calculated from I_{TLP} = 4A to I_{TLP} = 16A

Typical Characteristics

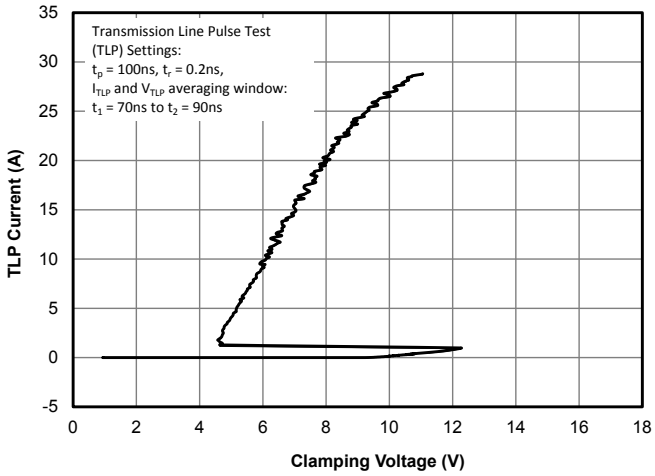
ESD Clamping (8kV Contact per IEC 61000-4-2)



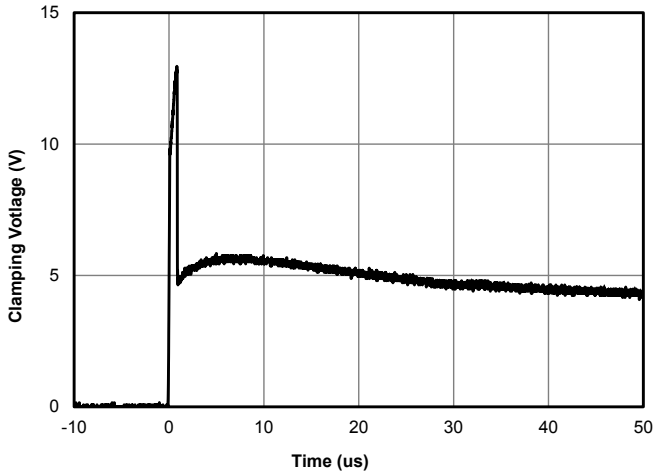
ESD Clamping (-8kV Contact per IEC 61000-4-2)



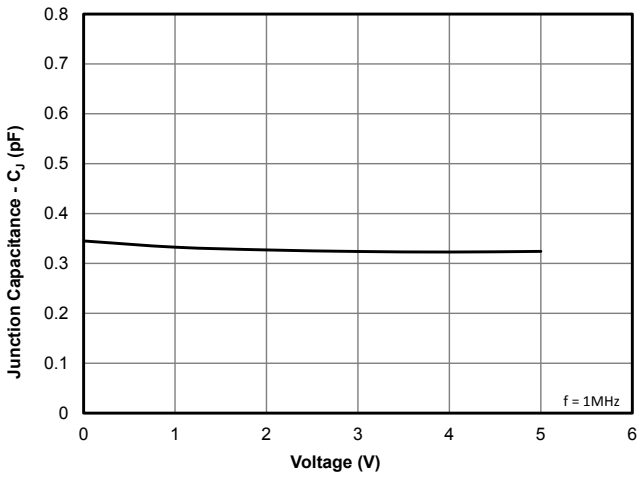
TLP Characteristic (Positive Pulse)



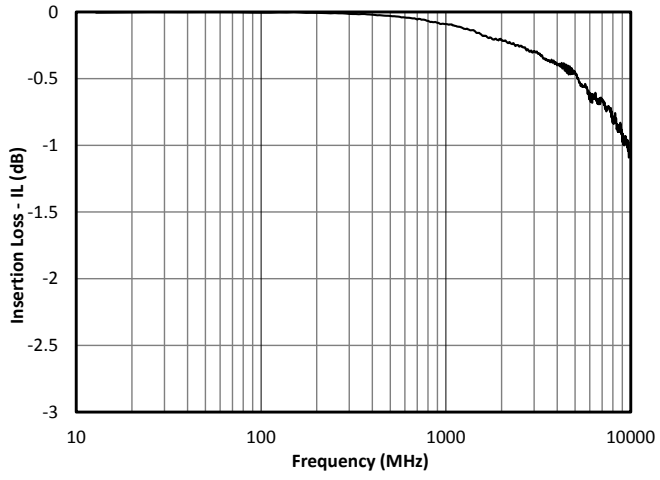
Clamping Voltage Waveform (tp=1.2/50µs)



Capacitance vs. Reverse Voltage

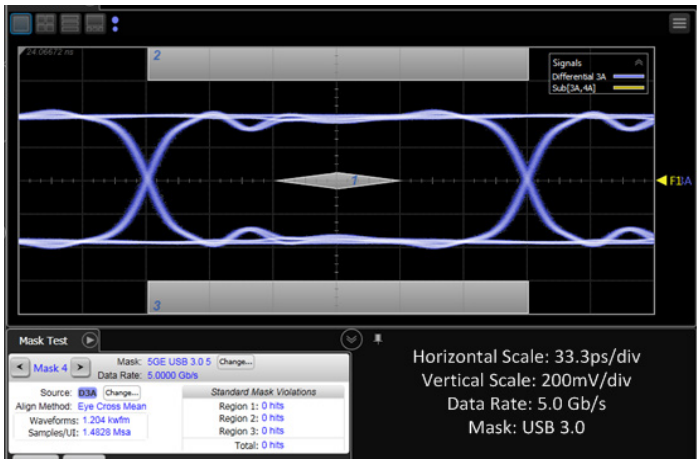


Insertion Loss - S21

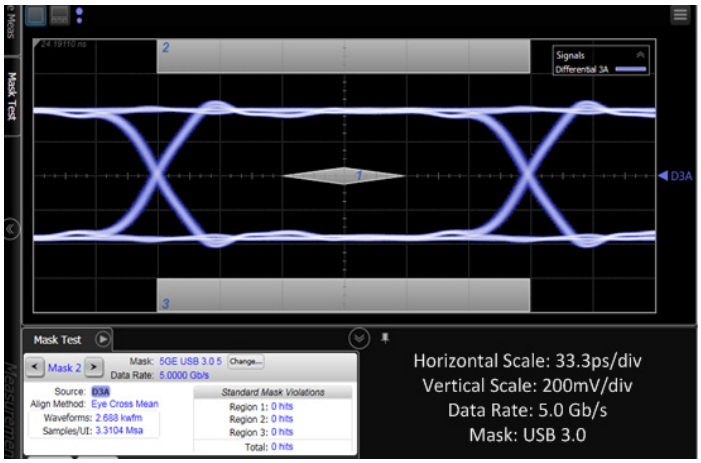


Typical Characteristics (Continued)

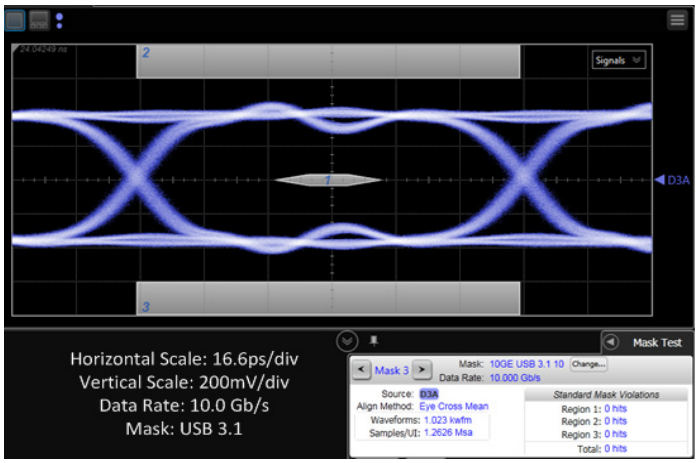
5Gb/s (USB 3.0) Eye Diagram with RClamp5031ZA



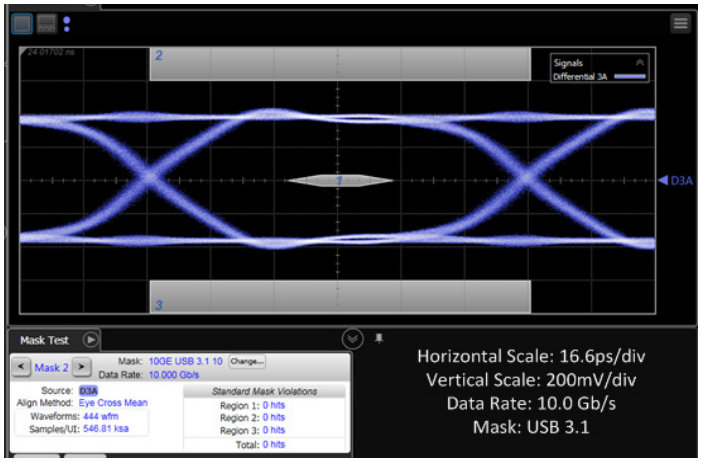
5Gb/s (USB 3.0) Eye Diagram without RClamp5031ZA



10Gb/s (USB 3.1) Eye Diagram with RClamp5031ZA



10Gb/s (USB 3.1) Eye Diagram without RClamp5031ZA



Application Information

Assembly Guidelines

The small size of this device means that some care must be taken during the mounting process to insure reliable-solder joints. The figure at the right details Semtech's recommended mounting pattern. Recommended assembly guidelines are shown in Table 1. Note that these are only recommendations and should serve only as a starting point for design since there are many factors that affect the assembly process. Exact manufacturing-parameters will require some experimentation to get the desired solder application. Semtech's recommend-edmounting pattern is based on the following design guidelines:

Land Pattern

The recommended land pattern follows IPC standards and is designed for maximum solder coverage. Detailed dimensions are shown elsewhere in this document.

Solder Stencil

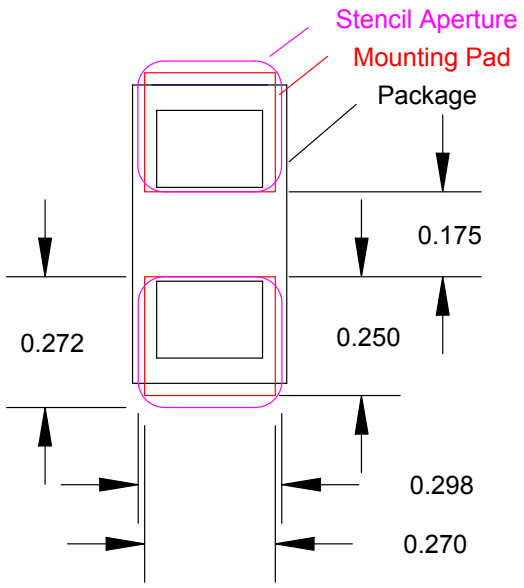
Stencil design is one of the key factors which will determine the volume of solder paste which is deposited onto the land pad. The area ratio of the stencil aperture will determine how well the stencil will print. The area ratio takes into account the aperture shape, aperture size, and stencil thickness. An area
ratio of 0.70 – 0.75 is preferred for the subject package. The area ratio of a rectangular aperture is given as:

Area Ratio = (L * W)/ (2 * (L + W) * T)

Where:
L = Aperture Length
W = Aperture Width
T = Stencil Thickness

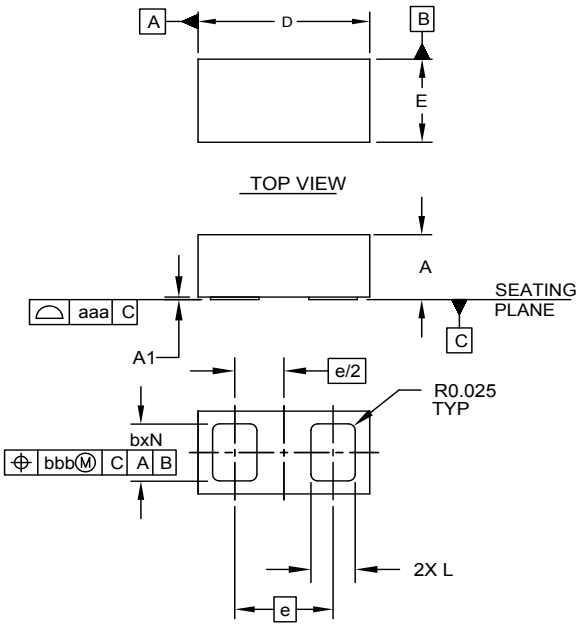
Semtech recommends a stencil thickness of 0.100mm for this device. The stencil should be laser cut with electrop-olishedfinish. The stencil should have a positive taper of approximately 5 degrees. Electro polishing and tapering the walls results in reduced surface friction and better paste release. For small pitch components, Semtech recommends a square aperture with rounded corners for consistent solder release. Due to the small aperture size, a solder paste withType 4 or smaller particles are recom-mended.

Recommended Mounting Pattern



Assembly Parameter	Recommendation
Solder Stencil Design	Laser cut, Electro-polished
Aperture shape	Rectangular with rounded corners
Solder Stencil Thickness	0.100 mm (0.004")
Solder Paste Type	Type 4 size sphere or smaller
Solder Reflow Profile	Per JEDEC J-STD-020
PCB Solder Pad Design	Non-Solder mask defined
PCB Pad Finish	OSP OR NiAu

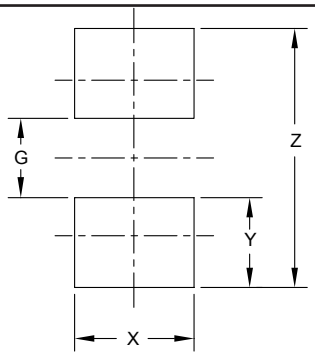
Outline Drawing - SLP0603P2X3F



DIMENSIONS			
DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.235	0.250	0.265
A1	0.000	0.010	0.050
b	0.200	0.220	0.240
D	0.580	0.600	0.620
E	0.280	0.300	0.320
e	0.355 BSC		
L	0.140	0.160	0.180
N	2		
aaa	0.08		
bbb	0.10		

NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).

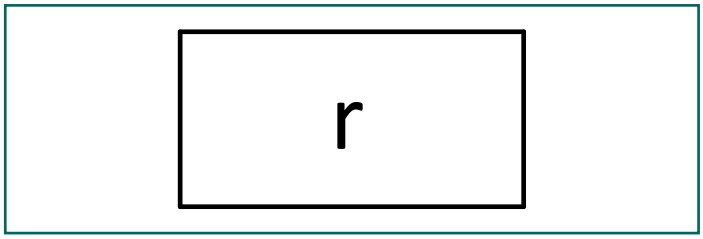
Land Pattern - SLP0603P2X3F



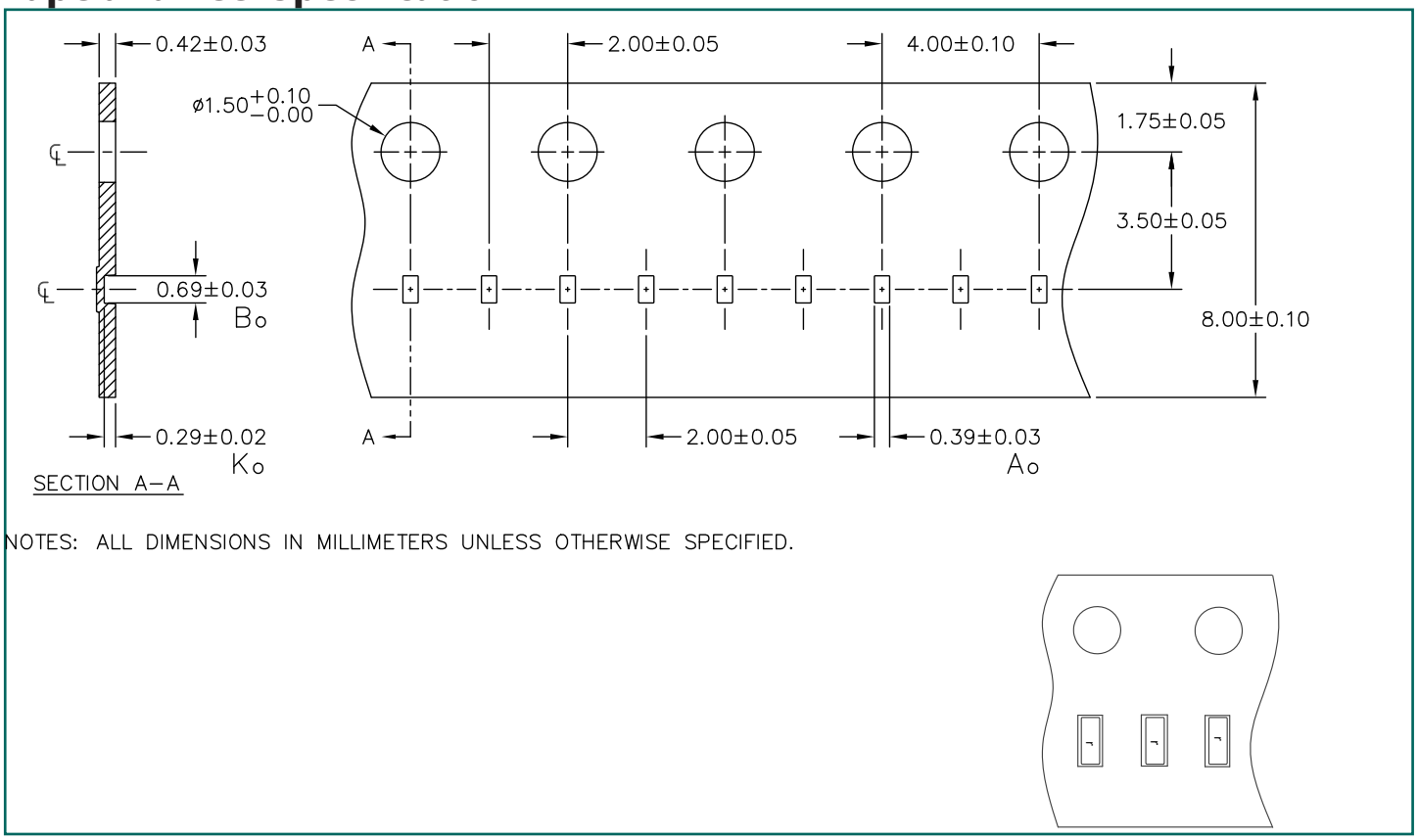
DIMENSIONS	
DIM	MILLIMETERS
G	0.181
X	0.273
Y	0.205
Z	0.591

NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY.
   CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR
   COMPANY'S MANUFACTURING GUIDELINES ARE MET.

Marking Code



Tape and Reel Specification



NOTES: ALL DIMENSIONS IN MILLIMETERS UNLESS OTHERWISE SPECIFIED.

Ordering Information

Part Number	Qty per Reel	Reel Size
RClamp5031ZATFT	15,000	7”

Contact Information

Semtech Corporation
200 Flynn Road, Camarillo, CA 93012
Phone: (805) 498-2111, Fax: (805) 498-3804
www.semtech.com

RClamp5011ZA
Ultra Small RailClamp®
1-Line, 5V ESD Protection

PROTECTION PRODUCTS

Description

RailClamp® TVS diodes are designed to protect sensitive electronics from damage or latch-up due to ESD. They are designed to replace 0201 size multilayer varistors (MLVs) in portable applications such as cell phones, notebook computers, and other portable electronics. This device offers desirable characteristics for board level protection including fast response time, low operating and clamping voltage, and no device degradation.

RClamp®5011ZA features extremely good ESD protection characteristics highlighted by low typical dynamic resistance of 0.25 Ohms, low peak ESD clamping voltage, and high ESD withstand voltage (+/-15kV contact per IEC 61000-4-2). Low maximum capacitance (0.45pF at VR=0V) minimizes loading on sensitive cirucuits. Each device will protect one high-speed data line operating at 5 Volts.

RClamp5011ZA is in a 2-pin SLP0603P2X3F package measuring 0.6 x 0.3 mm with a nominal height of only 0.25mm. Leads are finished with NiAu. The small package gives the designer the flexibility to protect single lines in applications where arrays are not practical. The combination of small size and high ESD surge capability makes them ideal for use in applications such as cellular phones, displays, and tablet PC's.

Features

- High ESD withstand Voltage: +/-15kV (Contact) and +/- 18kV (Air) per IEC 61000-4-2
- Ultra-small package
- Protects one data line
- Low ESD clamping voltage
- Working voltage: 5V
- Low capacitance: 0.45pF maximum
- Low leakage current
- Extremely low dynamic resistance: 0.25 Ohms (Typ)
- Solid-state silicon-avalanche technology

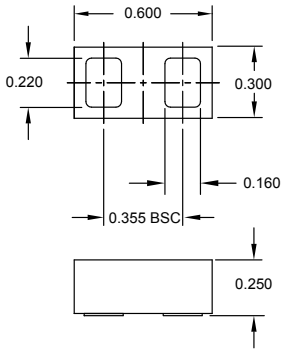
Mechanical Characteristics

- SLP0603P2X3F package
- Pb-Free, Halogen Free, RoHS/WEEE Compliant
- Nominal Dimensions: 0.6 x 0.3 x 0.25 mm
- Lead Finish: NiAu
- Marking: Marking code
- Packaging: Tape and Reel

Applications

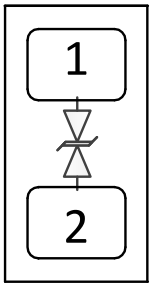
- HDMI
- USB 3.0
- MiPi / MDDI
- MHL
- FM Antenna

Package Dimension



Nominal Dimensions in mm

Schematic & Pin Configuration



SLP0603P2X3F (Bottom View)

Absolute Maximum Rating

Rating	Symbol	Value	Units
Peak Pulse Power (t_p = 8/20µs)	P_{PK}	50	W
Peak Pulse Current (t_p = 8/20µs)	I_{PP}	4	A
ESD per IEC 61000-4-2 (Air)(1) ESD per IEC 61000-4-2 (Contact)(1)	V_{ESD}	±18 ±15	kV
Operating Temperature	T_J	-40 to +85	°C
Storage Temperature	T_{STG}	-55 to +150	°C

Electrical Characteristics (T=25°C unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Reverse Stand-Off Voltage	V_{RWM}	T=-40 to +85°C			5	V
Reverse Breakdown Voltage	V_{BR}	I_{PT} = 1mA	6.5	7.5	10	V
Reverse Leakage Current	I_R	V_{RWM} = 5V		<5	50	nA
Clamping Voltage	V_C	I_{PP} = 2A, t_p = 8/20µs			11.5	V
		I_{PP} = 4A, t_p = 8/20µs			12.5	V
ESD Clamping Voltage(2)	V_C	I_{PP} = 4A, t_p = 0.2/100ns		8.5		V
		I_{PP} = 16A, t_p = 0.2/100ns		11.5		V
Dynamic Resistance(2), (3)	R_{DYN}	t_p = 0.2/100ns		0.25		Ω
Junction Capacitance	C_J	V_R = 0V, f = 1MHz		0.40	0.45	pF

Notes

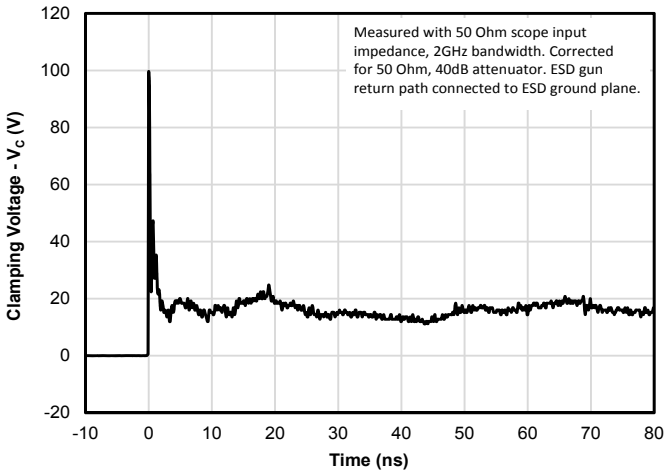
1) Measured with a 40dB attenuator, 50 Ohm scope input impedance, 2GHz bandwidth. ESD gun return path connected to ESD ground plane.

2) Transmission Line Pulse Test (TLP) Settings: tp = 100ns, tr = 0.2ns, I_{TLP} and V_{TLP} averaging window: t1 = 70ns to t2 = 90ns.

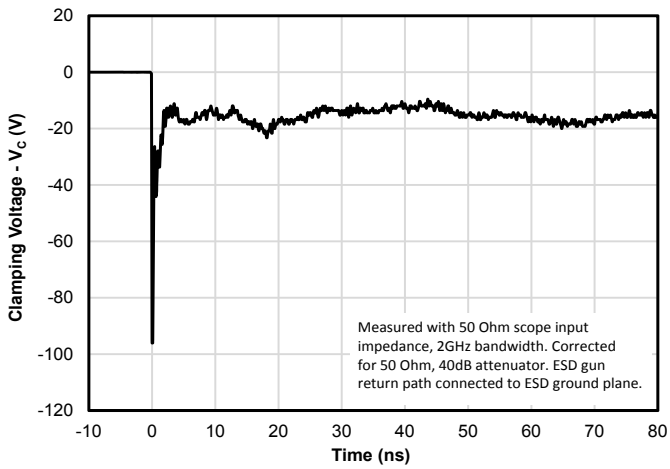
3) Dynamic resistance calculated from I_{TLP} = 4A to I_{TLP} = 16A

Typical Characteristics

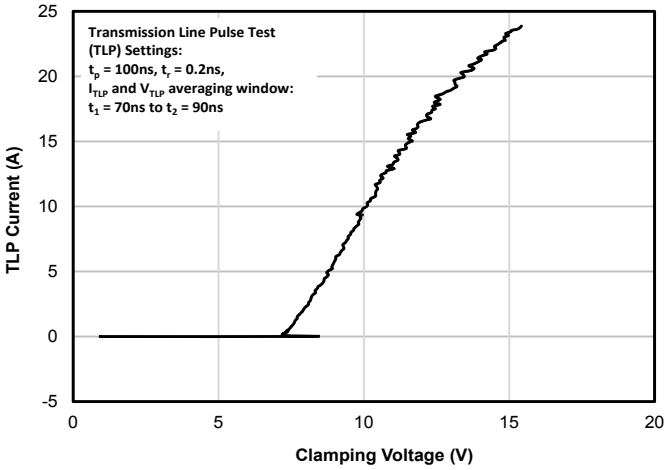
ESD Clamping (8kV Contact per IEC 61000-4-2)



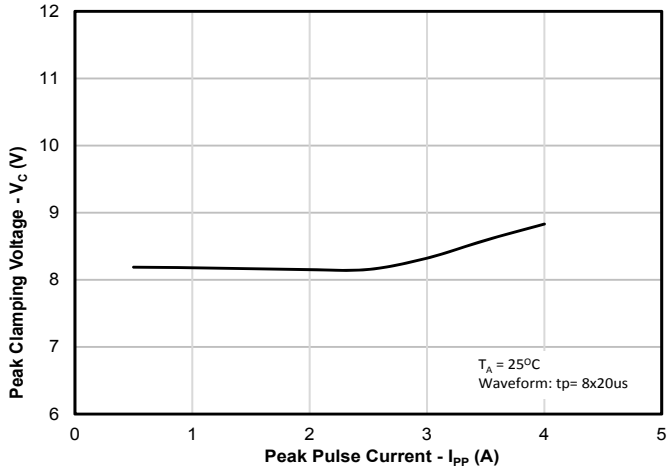
ESD Clamping (-8kV Contact per IEC 61000-4-2)



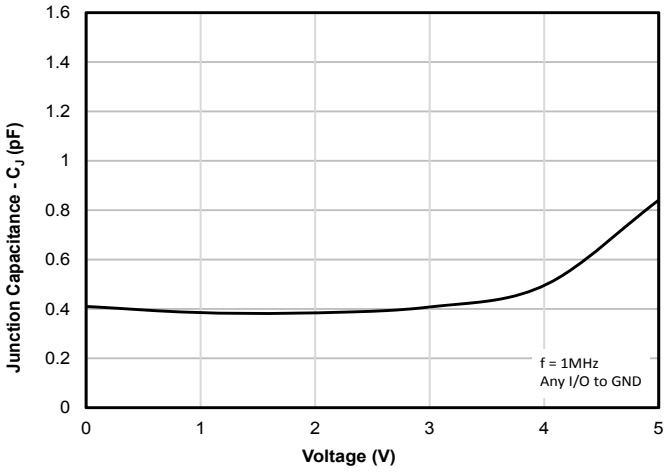
TLP Characteristic



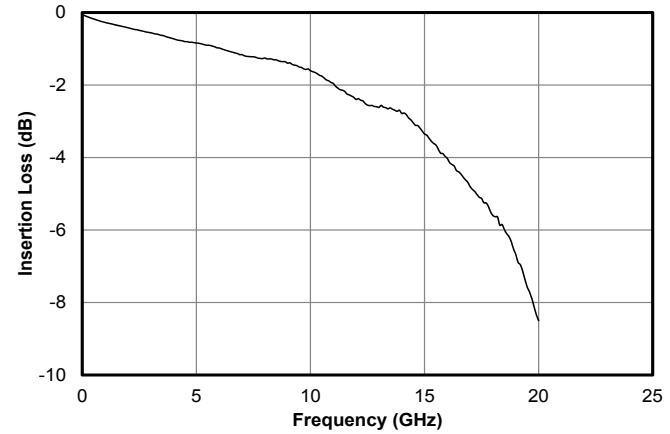
Clamping Voltage vs. Peak Pulse Current (t_p=8/20µs)



Capacitance vs. Reverse Voltage

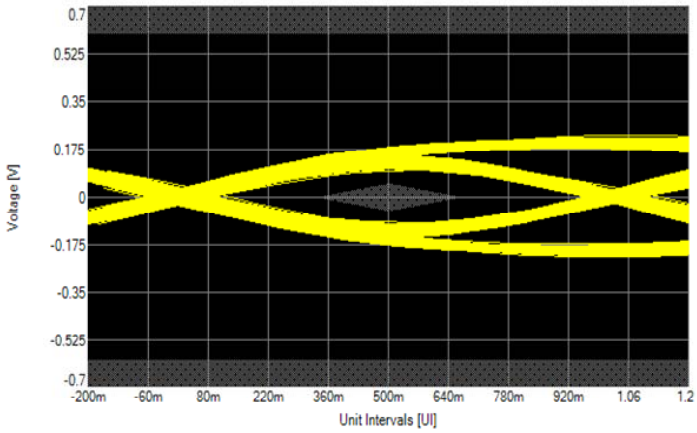


Insertion Loss-S21(dB)

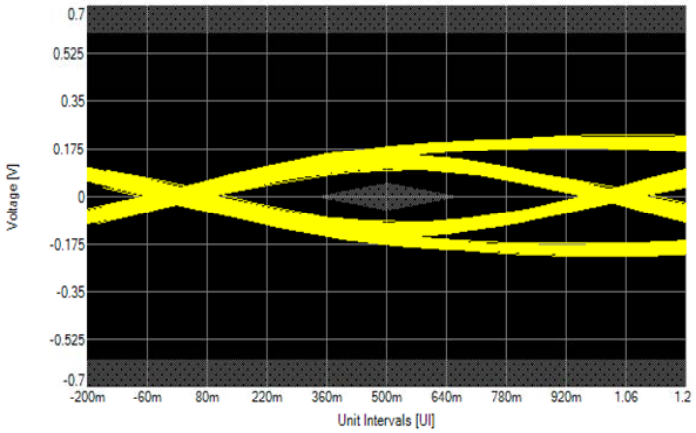


Typical Characteristics (Continued)

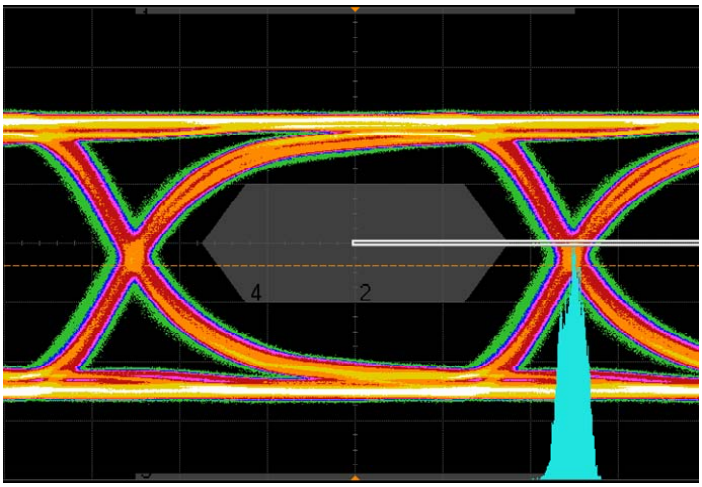
USB3.0 Eye Pattern without RClamp5011ZA



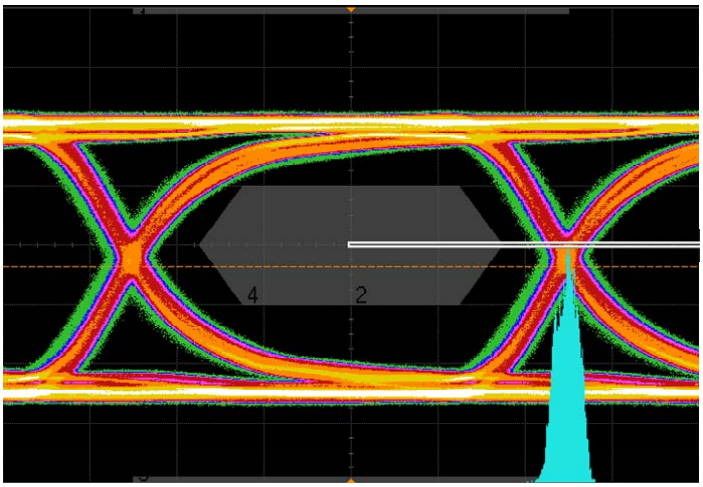
USB3.0 Eye Pattern with RClamp5011ZA



HDMI 1.4 Eye Pattern without RClamp5011ZA



HDMI 1.4 Eye Pattern with RClamp5011ZA



Application Information

Assembly Guidelines

The small size of this device means that some care must be taken during the mounting process to insure reliable-solder joints. The figure at the right details Semtech's recommended mounting pattern. Recommended assembly guidelines are shown in Table 1. Note that these are only recommendations and should serve only as a starting point for design since there are many factors that affect the assembly process. Exact manufacturing-parameters will require some experimentation to get the desired solder application. Semtech's recommend-edmounting pattern is based on the following design guidelines:

Land Pattern

The recommended land pattern follows IPC standards and is designed for maximum solder coverage. Detailed dimensions are shown elsewhere in this document.

Solder Stencil

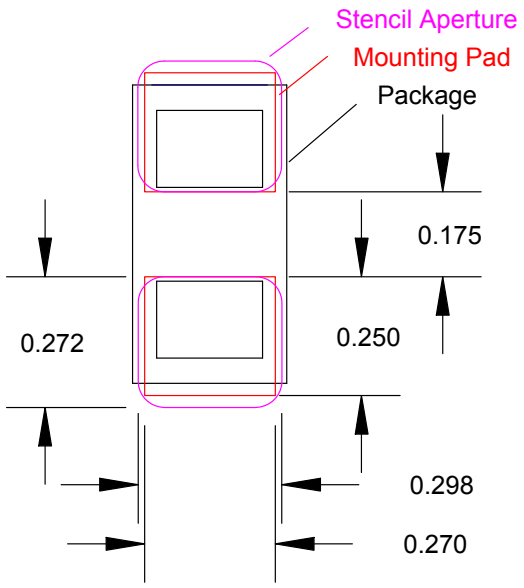
Stencil design is one of the key factors which will determine the volume of solder paste which is deposited onto the land pad. The area ratio of the stencil aperture will determine how well the stencil will print. The area ratio takes into account the aperture shape, aperture size, and stencil thickness. An area
ratio of 0.70 – 0.75 is preferred for the subject package. The area ratio of a rectangular aperture is given as:

Area Ratio = (L * W)/ (2 * (L + W) * T)

Where:
L = Aperture Length
W = Aperture Width
T = Stencil Thickness

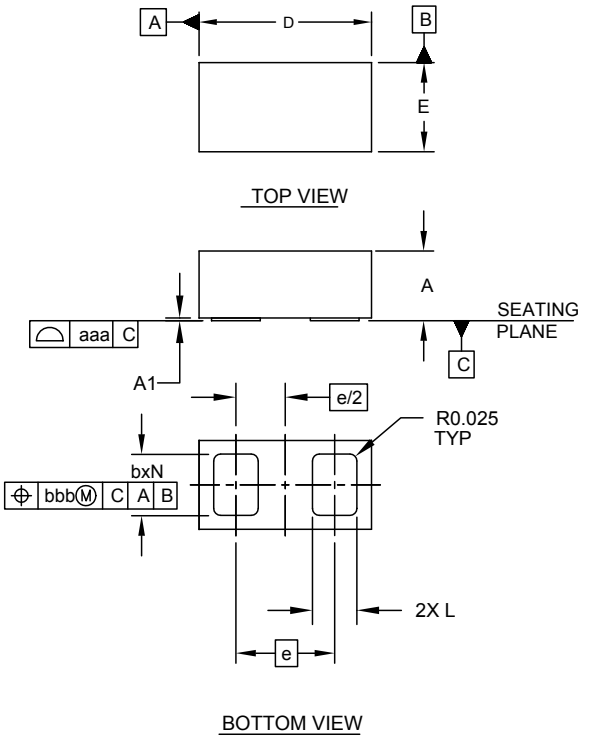
Semtech recommends a stencil thickness of 0.100mm for this device. The stencil should be laser cut with electrop-olishedfinish. The stencil should have a positive taper of approximately 5 degrees. Electro polishing and tapering the walls results in reduced surface friction and better paste release. For small pitch components, Semtech recommends a square aperture with rounded corners for consistent solder release. Due to the small aperture size, a solder paste with Type 4 or smaller particles are recom-mended.

Recommended Mounting Pattern



Assembly Parameter	Recommendation
Solder Stencil Design	Laser cut, Electro-polished
Aperture shape	Rectangular with rounded corners
Solder Stencil Thickness	0.100 mm (0.004")
Solder Paste Type	Type 4 size sphere or smaller
Solder Reflow Profile	Per JEDEC J-STD-020
PCB Solder Pad Design	Non-Solder mask defined
PCB Pad Finish	OSP OR NiAu

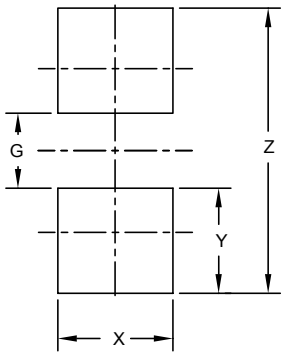
Outline Drawing - SLP0603P2X3F



DIMENSIONS			
DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.235	0.250	0.265
A1	0.000	0.010	0.050
b	0.200	0.220	0.240
D	0.580	0.600	0.620
E	0.280	0.300	0.320
e	0.355 BSC		
L	0.140	0.160	0.180
N	2		
aaa	0.08		
bbb	0.10		

NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).

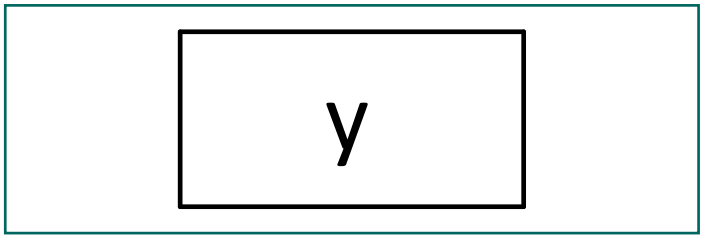
Land Pattern - SLP0603P2X3F



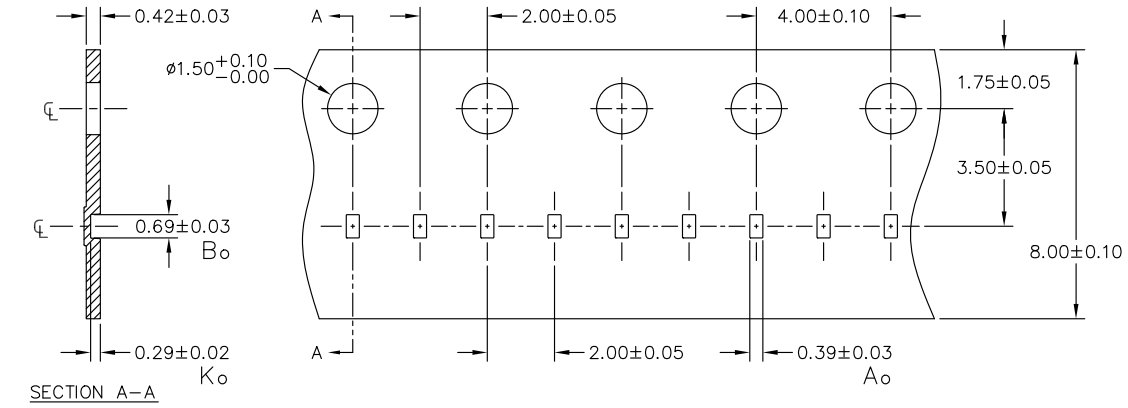
DIMENSIONS	
DIM	MILLIMETERS
G	0.177
X	0.272
Y	0.247
Z	0.671

NOTES:
CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY.
CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

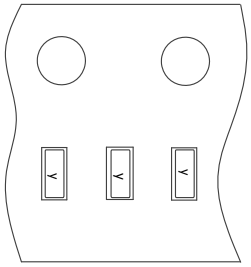
Marking Code



Tape and Reel Specification



NOTES: ALL DIMENSIONS IN MILLIMETERS UNLESS OTHERWISE SPECIFIED.



Ordering Information

Part Number	Qty per Reel	Reel Size
RClamp5011ZATFT	15,000	7”

RailClamp and RClamp are registered trademarks of Semtech Corporation.

Contact Information

Semtech Corporation
200 Flynn Road, Camarillo, CA 93012
Phone: (805) 498-2111, Fax: (805) 498-3804
www.semtech.com

RClamp0542ZA

Femto Farad RailClamp®
2-Line, 300fF ESD Protection

PROTECTION PRODUCTS

Description

RClamp®0542ZA is an ultra low capacitance ESD protection device designed to protect two high-speed lines in an 0201 footprint. This revolutionary package design reduces board space requirements by more than 50% over existing single line solutions. RClamp0542ZA is a three pin device with identical low capacitance TVS diodes connected to each pin. Any two pins may be connected to high-speed lines, while the third pin is connected to ground. This gives the designer maximum flexibility in pcb routing. Each line has a maximum capacitance of only 0.30pF resulting in a typical corner frequency of 12GHz.

RClamp0542ZA is in a 3-pin SLP0603P3X3F package. It measures 0.62 x 0.32 mm with a nominal height of only 0.25mm. Leads are finished with lead-free NiAu. The combination of small size and high ESD surge capability makes them ideal for use in portable applications such as cellular phones, digital cameras, and tablets.

Features

- High ESD withstand voltage
  - IEC 61000-4-2 (ESD) 17kV (air), 12kV (contact)
- Very small PCB area
- Protects two high-speed data lines
- Working voltage: 5V
- Low reverse leakage current: <1nA typ at VR=5V
- Low capacitance: 0.30pF maximum
- Dynamic resistance: 1.17 Ohms (Typ)
- Solid-state silicon-avalanche technology

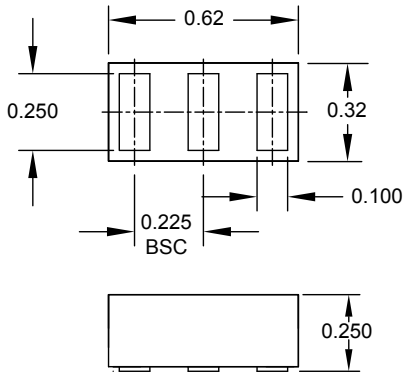
Mechanical Characteristics

- SLP0603P3X3F package
- Pb-Free, Halogen Free, RoHS/WEEE Compliant
- Nominal Dimensions: 0.62 x 0.32 x 0.25 mm
- Lead Finish: NiAu
- Marking : Marking code
- Packaging : Tape and Reel

Applications

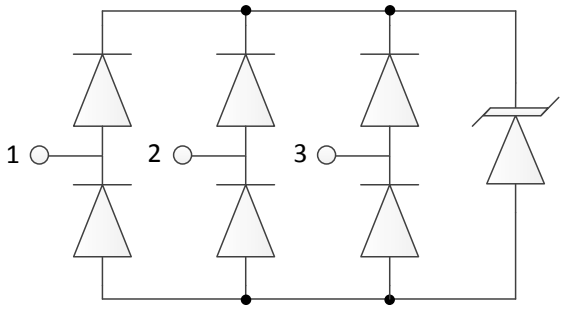
- High-Speed Lines
- MIPI / MDDI
- USB 3.0
- HDMI
- MHL
- eDP

Nominal Dimensions



Nominal Dimensions in mm

Functional Schematic



Device Schematic

Absolute Maximum Ratings

Rating	Symbol	Value	Units
Peak Pulse Power (tp = 8/20µs)	P_{PK}	40	W
Peak Pulse Current (tp = 8/20µs)	I_{PP}	2	A
ESD per IEC 61000-4-2 (Air)(1) ESD per IEC 61000-4-2 (Contact)(1)	V_{ESD}	±17 ±12	kV
Operating Temperature	T_J	-40 to +85	°C
Storage Temperature	T_{STG}	-55 to +150	°C

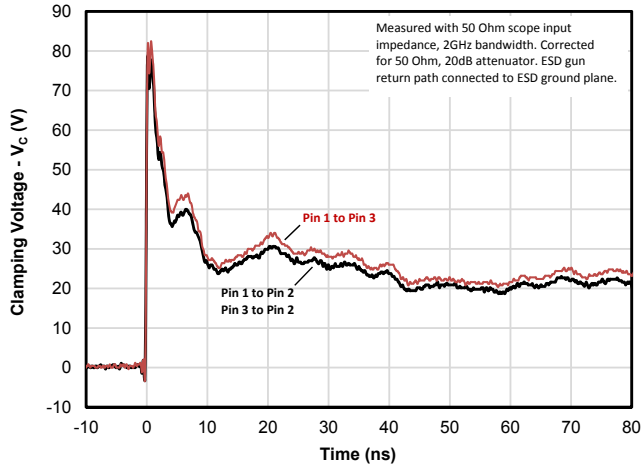
Electrical Characteristics (T=25°C unless otherwise specified)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Units
Reverse Stand-Off Voltage	V_{RWM}	-40°C to 85°C Between any two pins				5	V
Reverse Breakdown Voltage	V_{BR}	I_t = 10mA, Between any two pins	-40°C to 85°C	6.5	9.5	11.5	V
Reverse Leakage Current	I_R	V_{RWM} = 5V	T = 25°C		0.01	0.050	µA
			T = 85°C		0.05	0.250	µA
Clamping Voltage	V_C	I_{PP} = 2A, tp = 8/20µs, Between any two pins			12	20	V
ESD Clamping Voltage[2]	V_C	I_{PP} = 4A, tp = 0.2/100ns (TLP) Pin 1 to 2, Pin 3 to 2			16		V
ESD Clamping Voltage[2]	V_C	I_{PP} = 16A, tp = 0.2/100ns (TLP) Pin 1 to 2, Pin 3 to 2			30		V
Dynamic Resistance[2, 3]	R_{DYN}	tp = 0.2/100ns (TLP) Pin 1 to 2, Pin 3 to 2			1.17		Ohms
Cut-Off Frequency	f_C	Insertion Loss (S21) = -3dB			12		GHz
Junction Capacitance	C_J	V_R = 0V, f = 1MHz Between any two pins	T = 25°C		0.27	0.30	pF
Change in Capacitance over VR	ΔC_{jVR}	VR = 0 - 5V, f = 1MHz				0.030	pF

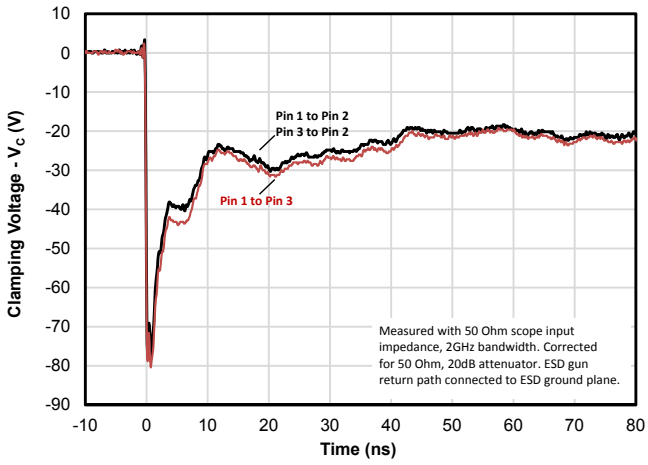
Notes:
(1): ESD Gun return path to Ground Reference Plane (GRP)
(2): Transmission Line Pulse Test (TLP) Settings: tp = 100ns, tr = 0.2ns, I_{TLP} and V_{TLP} averaging window: t_1 = 70ns to t_2 = 90ns.
(3): Dynamic resistance calculated from I_{TLP} = 4A to I_{TLP} = 16A

Typical Characteristics

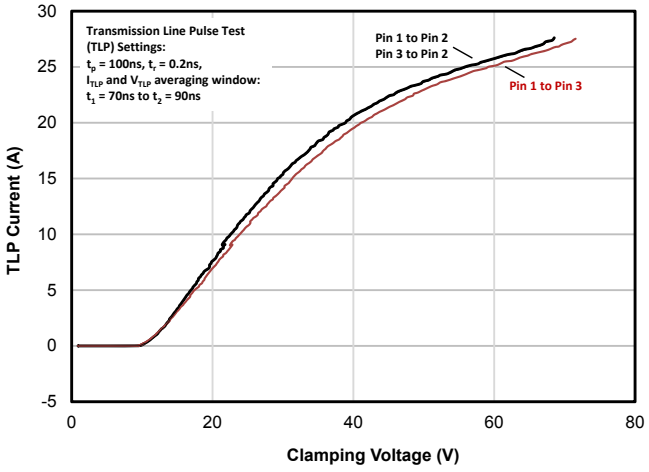
ESD Clamping (+8kV Contact per IEC 61000-4-2)



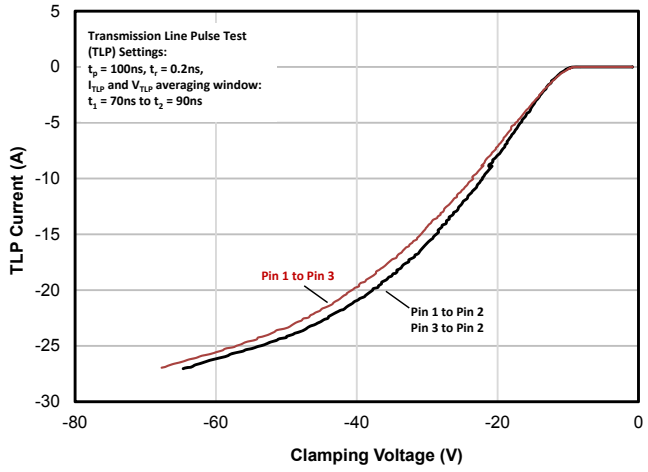
ESD Clamping (-8kV Contact per IEC 61000-4-2)



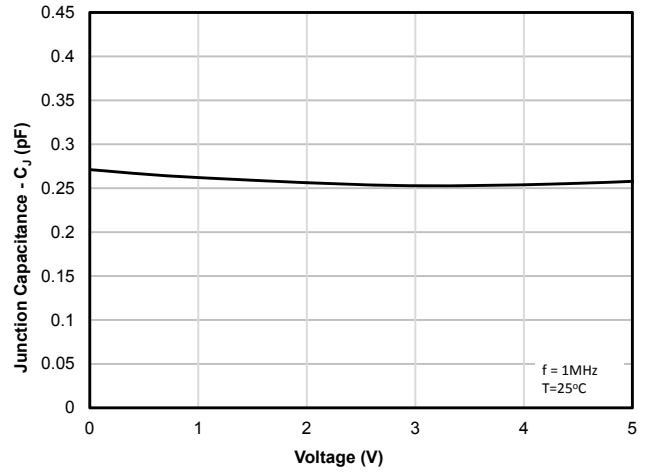
TLP IV Curve (Positive Pulse)



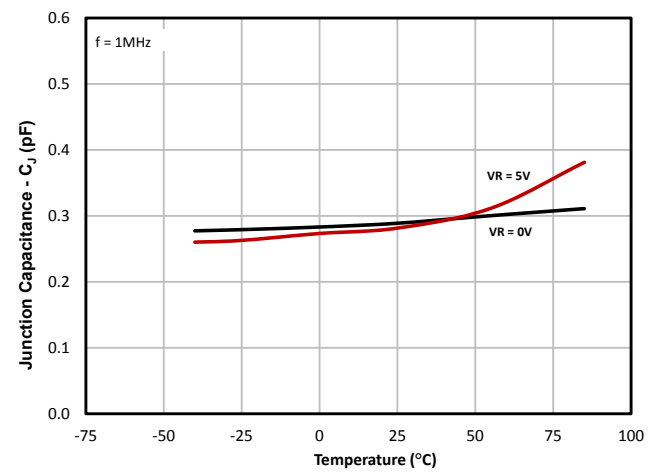
TLP IV Curve (Negative Pulse)



Capacitance vs. Reverse Voltage

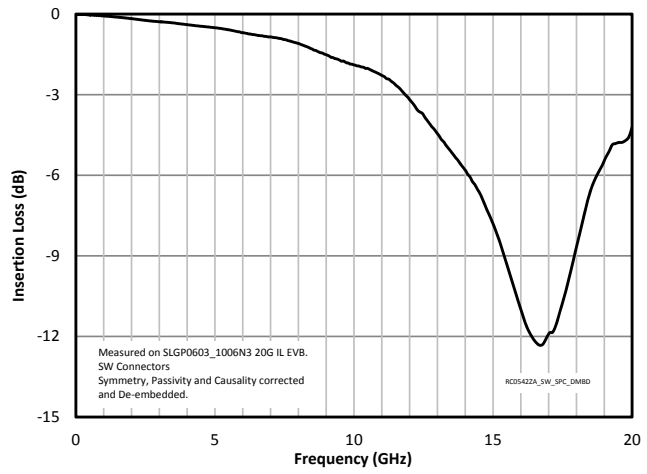


Capacitance vs. Temperature

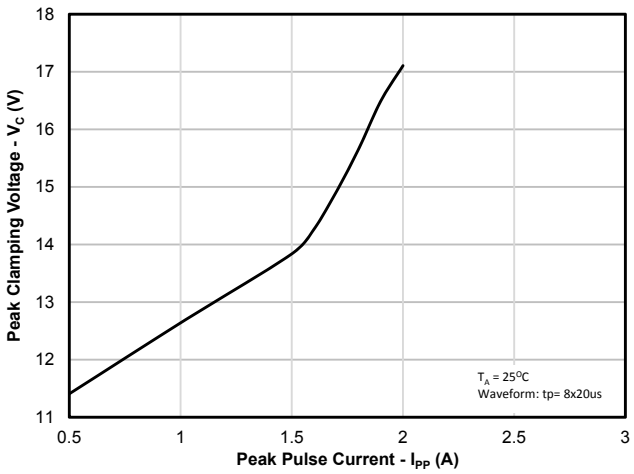


Typical Characteristics (Continued)

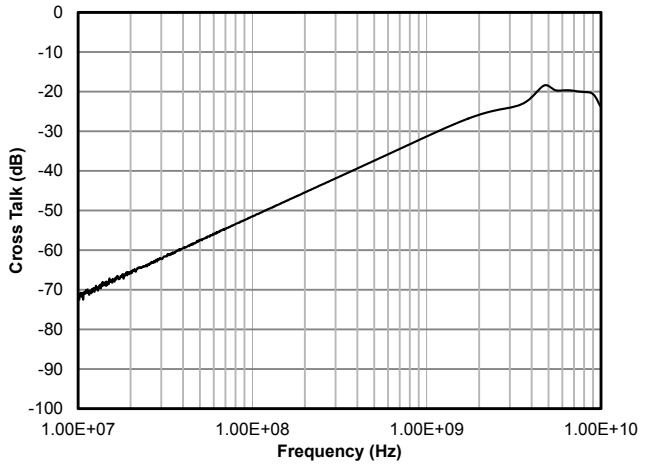
Insertion Loss - S21



Clamping Voltage vs. Peak Pulse Current (tp=8/20us)



Analog Crosstalk



Applications Information

Assembly Guidelines

The small size of this device means that some care must be taken during the mounting process to insure reliable solder joint. The figure at the right details Semtech's recommended mounting pattern. Recommended assembly guidelines are shown in Table 1. Note that these are only recommendations and should serve only as a starting point for design since there are many factors that affect the assembly process. Exact manufacturing parameters will require some experimentation to get the desired solder application. Semtech's recommended mounting pattern is based on the following design guidelines:

Land Pattern

The recommended land pattern follows IPC standards and is designed for maximum solder coverage. Detailed dimensions are shown elsewhere in this document.

Solder Stencil

Stencil design is one of the key factors which will determine the volume of solder paste which is deposited onto the land pad. The area ratio of the stencil aperture will determine how well the stencil will print. The area ratio takes into account the aperture shape, aperture size, and stencil thickness. An area ratio of 0.70 – 0.75 is preferred for the subject package. The area ratio of a rectangular aperture is given as:

Area Ratio = (L * W)/ (2 * (L + W) * T)

Where:
L = Aperture Length
W = Aperture Width
T = Stencil Thickness

Semtech recommends a stencil thickness of 0.100mm for this device. The stencil should be laser cut with electro-polished finish. The stencil should have a positive taper of approximately 5 degrees. Electro polishing and tapering the walls results in reduced surface friction and better paste release. For small pitch components, Semtech recommends a square aperture with rounded corners for consistent solder release. Due to the small aperture size, a solder paste with Type 4 or smaller particles are recommended.

Recommended Mounting Pattern

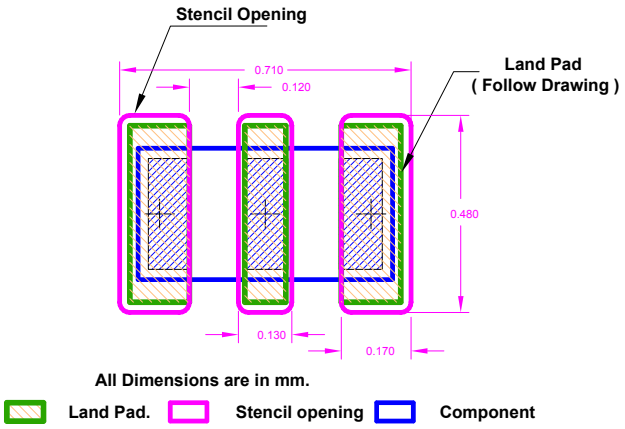
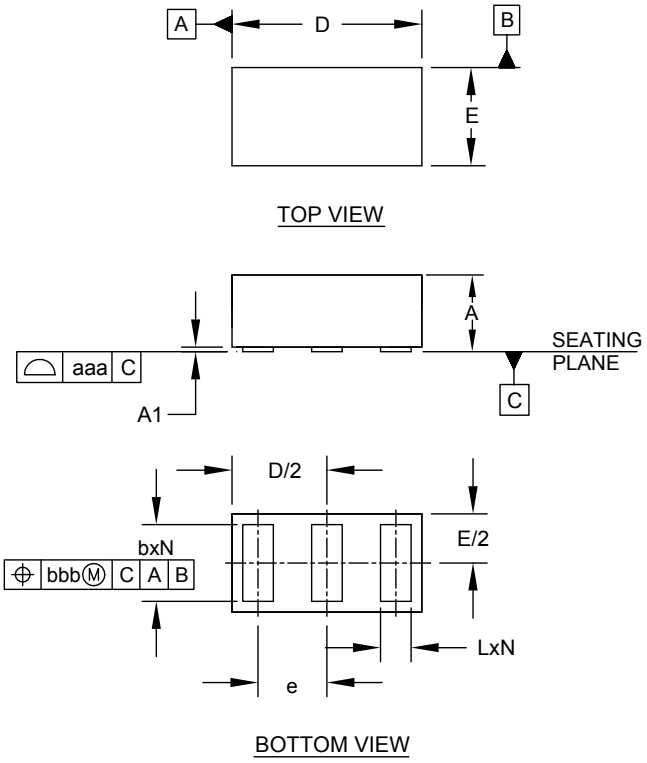


Table 1 - Recommended Assembly Guidelines

Assembly Parameter	Recommendation
Solder Stencil Design	Laser Cut, Electro-Polished
Aperture Shape	Rectangular with rounded corners
Solder Stencil Thickness	0.100mm (0.004")
Solder Paste Type	Type 4 size sphere or smaller
Solder Reflow Profile	Per JEDEC J-STD-020
PCB Solder pad Design	Non-Solder Mask Defined
PCB Pad Finish	OSP or NiAu

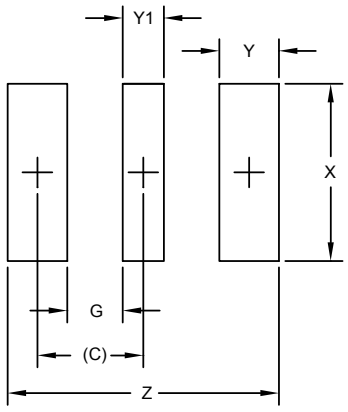
Outline Drawing - SLP0603P3X3F



DIMENSIONS			
DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.225	0.250	0.275
A1	0.005	0.015	0.050
b	0.230	0.250	0.270
D	0.580	0.62	0.650
E	0.280	0.32	0.350
e	0.225 BSC		
L	0.080	0.100	0.120
N	3		
aaa	0.08		
bbb	0.10		

NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).

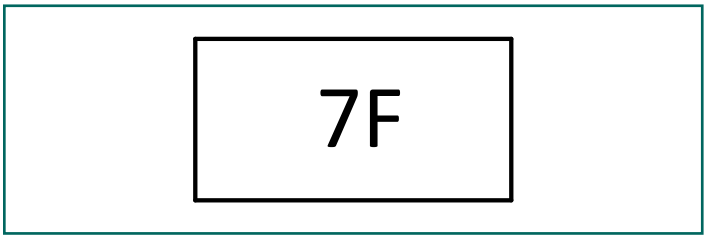
Land Pattern - SLP0603P3X3F



DIMENSIONS	
DIM	MILLIMETERS
C	(0.258)
G	0.135
X	0.430
Y	0.145
Y1	0.100
Z	0.660

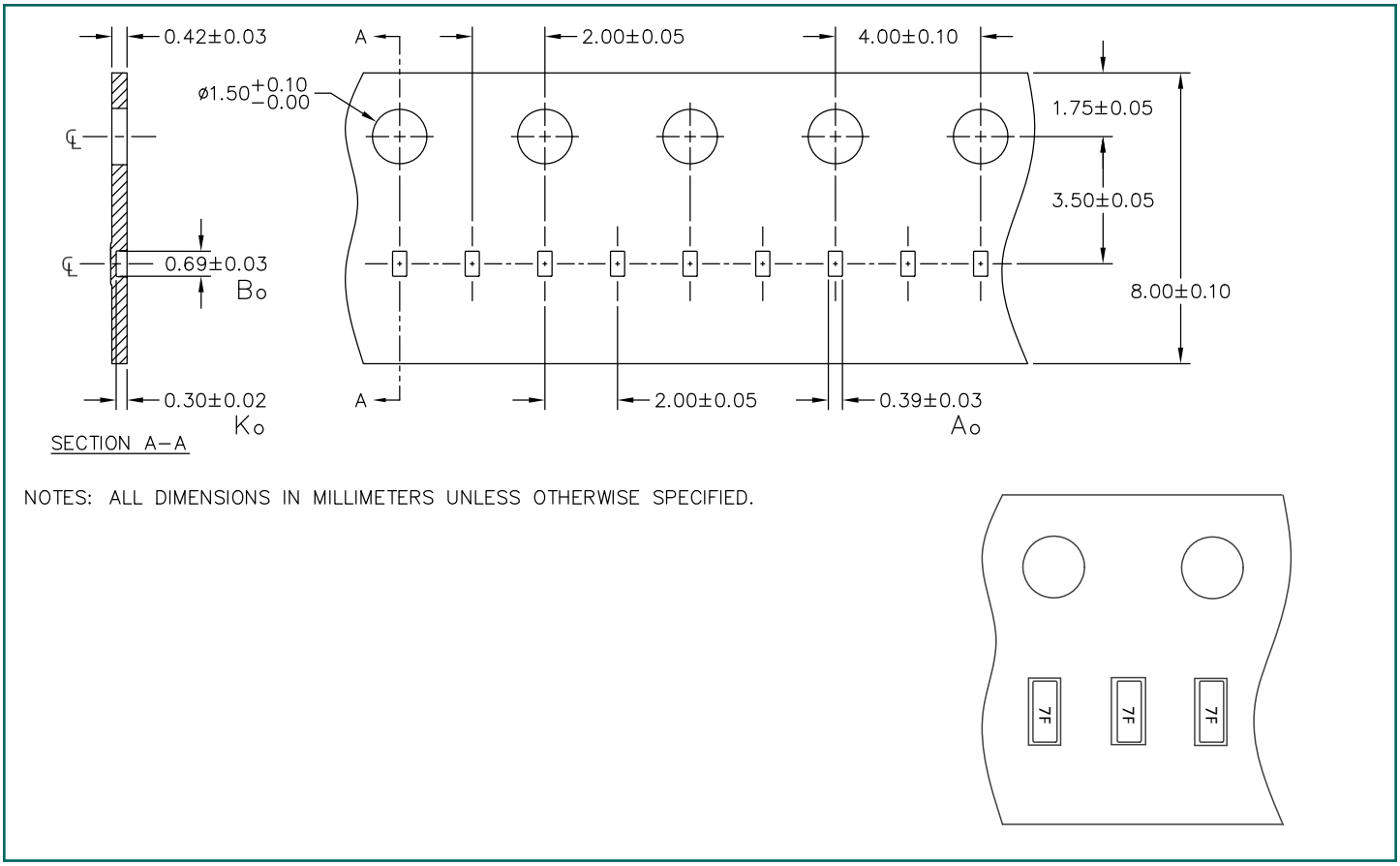
NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY.
   CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR
   COMPANY'S MANUFACTURING GUIDELINES ARE MET.

Marking Code



Notes: Device is electrically symmetrical

Tape and Reel Specification



Ordering Information

Part Number	Qty per Reel	Reel Size
RClamp0542ZATFT	15000	7 Inch
RailClamp and RClamp are registered trademarks of Semtech Corporation.		

Contact Information

Semtech Corporation
200 Flynn Road, Camarillo, CA 93012
Phone: (805) 498-2111, Fax: (805) 498-3804
www.semtech.com

µClamp0512ZA

Ultra Small µClamp®
2-Line ESD Protection

PROTECTION PRODUCTS

Description

uClamp®0512ZA is an ultra small ESD protection device designed to protect two high-speed lines in an 0201 footprint. This revolutionary package design reduces board space requirements by more than 50% over existing single line solutions. uClamp0512ZA is a three pin device with identical TVS diodes connected to each pin. Any two pins may be connected to vulnerable lines, while the third pin is connected to ground. This gives the designer maximum flexibility in pcb routing. These devices feature extremely good ESD protection characteristics highlighted by low dynamic resistance, low peak ESD clamping voltage, and high ESD withstand voltage (+/-12kV contact per IEC 61000-4-2).

uClamp0512ZA is in a 3-pin SLP0603P3X3F package. It measures 0.62 x 0.32 mm with a nominal height of only 0.25mm. Leads are finished with lead-free NiAu. The combination of small size and high ESD surge capability makes them ideal for use in portable applications such as cellular phones, digital cameras, and tablets.

Features

- High ESD withstand voltage
  - IEC 61000-4-2 (ESD) 15kV (air), 12kV (contact)
- Very small PCB area
- Protects two data lines
- Working Voltage: 5V
- Low reverse leakage current
- Low ESD peak clamping voltage
- Low dynamic resistance
- Solid-State silicon-avalanche technology

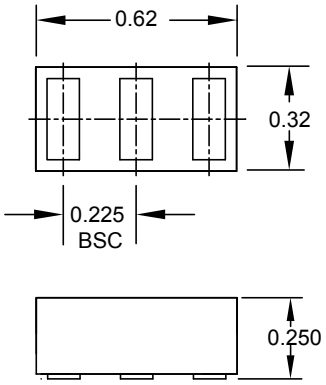
Mechanical Characteristics

- SLP0603P3X3F Package
- Pb-Free, Halogen Free, RoHS/WEEE compliant
- Nominal dimensions: 0.62 x 0.32 x 0.25 mm
- Lead finish: NiAu
- Marking : Marking code + date code
- Packaging : Tape and Reel

Applications

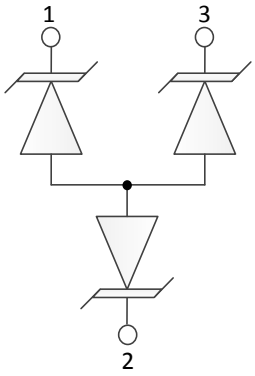
- Cellular Handsets & Accessories
- Keypads, Side Keys, Audio Ports
- Portable Instrumentation
- Notebook Computers
- Tablet PC

Nominal Dimensions



Nominal Dimensions in mm

Functional Schematic



Device Schematic

Absolute Maximum Ratings

Rating	Symbol	Value	Units
Peak Pulse Power (tp = 1.2/50µs)	P_{PK}	30	W
Peak Pulse Current (tp = 1.2/50µs)	I_{PP}	2	A
ESD per IEC 61000-4-2 (Air)(1) ESD per IEC 61000-4-2 (Contact)(1)	V_{ESD}	±15 ±12	kV
Operating Temperature	T_J	-40 to +125	°C
Storage Temperature	T_{STG}	-55 to +150	°C

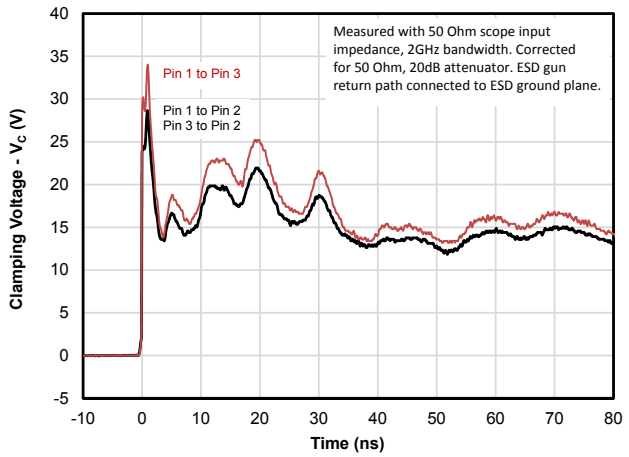
Electrical Characteristics (T=25°C unless otherwise specified)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Units
Reverse Stand-Off Voltage	V_{RWM}	-40°C to 125°C Between any two pins				5	V
Reverse Breakdown Voltage	V_{BR}	I_t = 1mA, Between any two pins	-40°C to 125°C	6.5	8	9.5	V
Reverse Leakage Current	I_R	V_{RWM} = 5V Between any two pins	T = 25°C		0.03	0.050	µA
			T = 125°C		0.05	0.250	µA
Clamping Voltage	V_C	I_{PP} = 2A, tp = 8/20µs, Between any two pins			10.5	15	V
ESD Clamping Voltage[2]	V_C	I_{PP} = 4A, tp = 0.2/100ns (TLP)	Pin 1 to 2, Pin 3 to 2		10.5		V
			Pin 1 to 3		11		V
ESD Clamping Voltage[2]	V_C	I_{PP} = 16A, tp = 0.2/100ns (TLP)	Pin 1 to 2, Pin 3 to 2		17.5		V
			Pin 1 to 3		20		V
Dynamic Resistance[2, 3]	R_{DYN}	tp = 0.2/100ns (TLP)	Pin 1 to 2, Pin 3 to 2		0.58		Ohms
			Pin 1 to 3		0.75		Ohms
Junction Capacitance	C_J	V_R = 0V, f = 1MHz Between any two pins	T = 25°C		5	7	pF

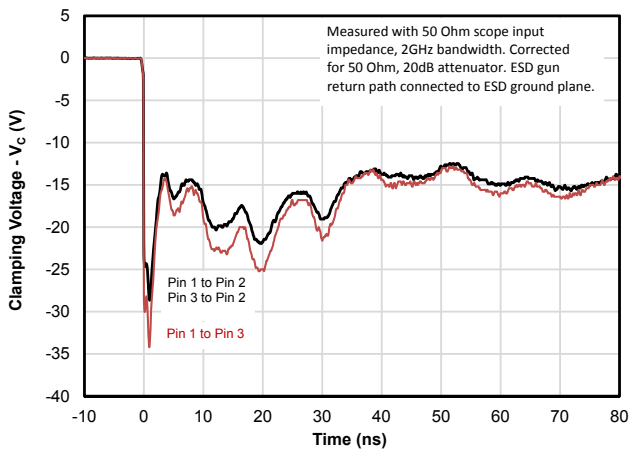
Notes:
(1): ESD Gun return path to Ground Reference Plane (GRP)
(2): Transmission Line Pulse Test (TLP) Settings: tp = 100ns, tr = 0.2ns, I_{TLP} and V_{TLP} averaging window: t_1 = 70ns to t_2 = 90ns.
(3): Dynamic resistance calculated from I_{TLP} = 4A to I_{TLP} = 16A

Typical Characteristics

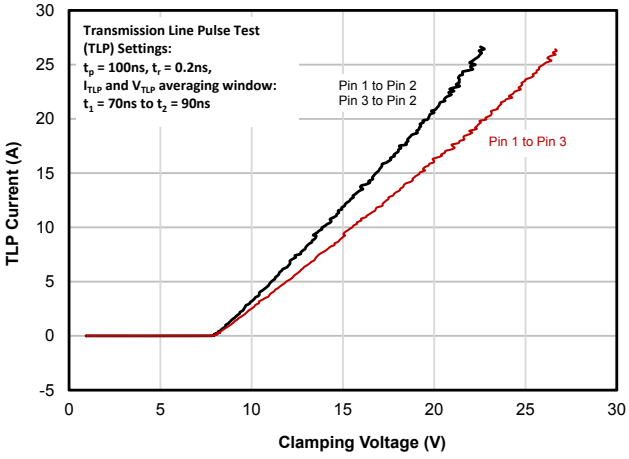
ESD Clamping (+8kV Contact per IEC 61000-4-2)



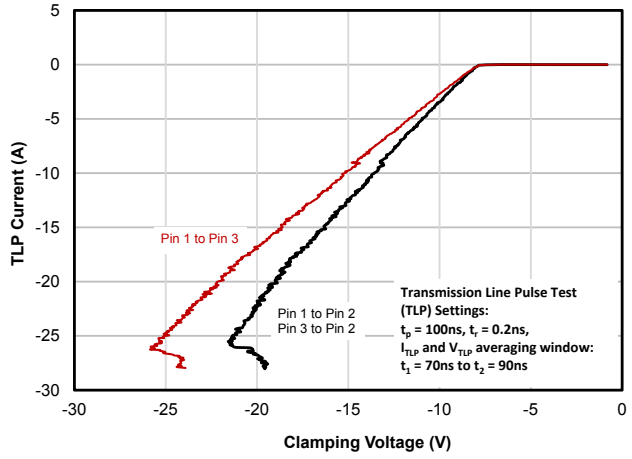
ESD Clamping (-8kV Contact per IEC 61000-4-2)



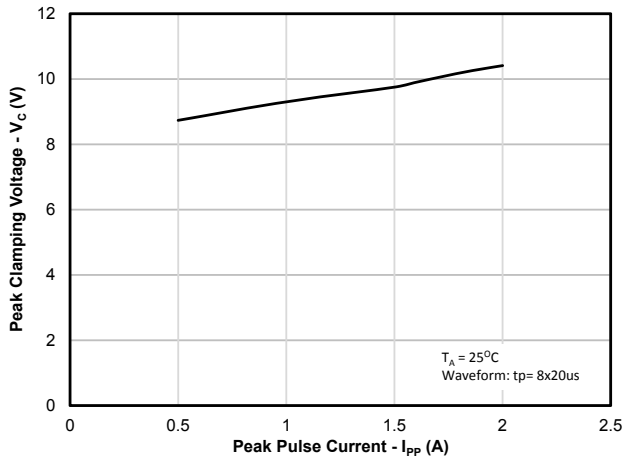
TLP IV Curve (Positive Pulse)



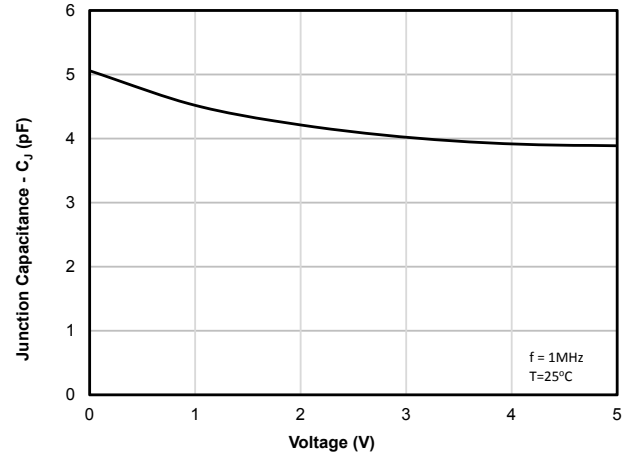
TLP IV Curve (Negative Pulse)



Clamping Voltage vs. Peak Pulse Current (tp=8/20us)

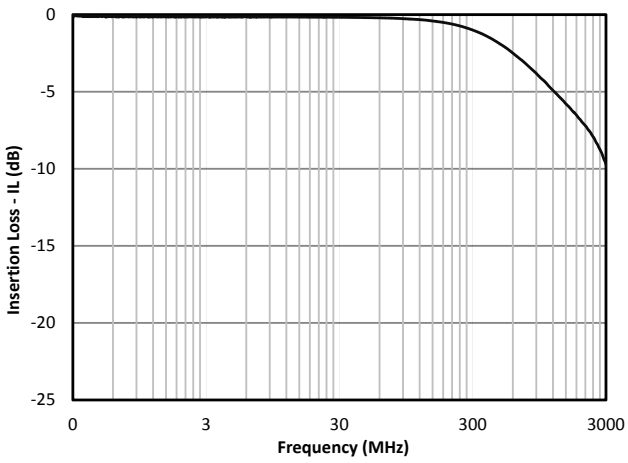


Capacitance vs. Reverse Voltage

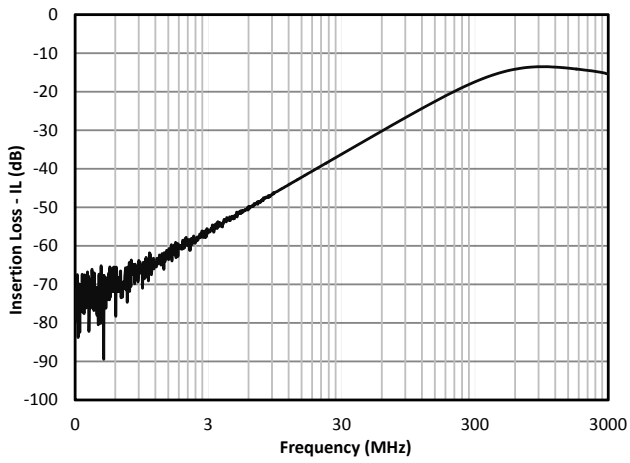


Typical Characteristics (Continued)

Insertion Loss - S21



Analog Crosstalk



Applications Information

Assembly Guidelines

The small size of this device means that some care must be taken during the mounting process to insure reliable solder joint. The figure at the right details Semtech's recommended mounting pattern. Recommended assembly guidelines are shown in Table 1. Note that these are only recommendations and should serve only as a starting point for design since there are many factors that affect the assembly process. Exact manufacturing parameters will require some experimentation to get the desired solder application. Semtech's recommended mounting pattern is based on the following design guidelines:

Land Pattern

The recommended land pattern follows IPC standards and is designed for maximum solder coverage. Detailed dimensions are shown elsewhere in this document.

Solder Stencil

Stencil design is one of the key factors which will determine the volume of solder paste which is deposited onto the land pad. The area ratio of the stencil aperture will determine how well the stencil will print. The area ratio takes into account the aperture shape, aperture size, and stencil thickness. An area ratio of 0.70 – 0.75 is preferred for the subject package. The area ratio of a rectangular aperture is given as:

Area Ratio = (L * W)/ (2 * (L + W) * T)

Where:
L = Aperture Length
W = Aperture Width
T = Stencil Thickness

Semtech recommends a stencil thickness of 0.100mm for this device. The stencil should be laser cut with electro-polished finish. The stencil should have a positive taper of approximately 5 degrees. Electro polishing and tapering the walls results in reduced surface friction and better paste release. For small pitch components, Semtech recommends a square aperture with rounded corners for consistent solder release. Due to the small aperture size, a solder paste with Type 4 or smaller particles are recommended.

Recommended Mounting Pattern

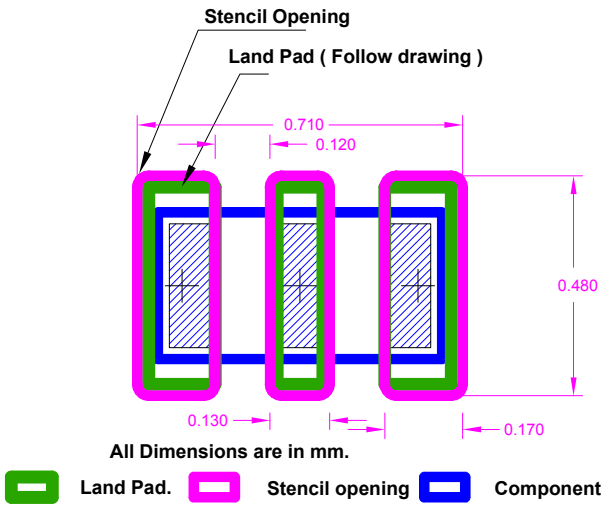
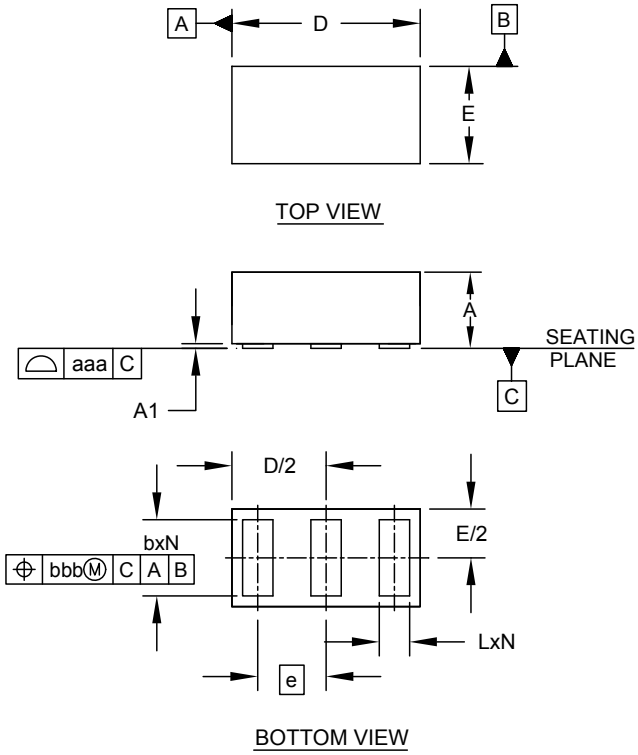


Table 1 - Recommended Assembly Guidelines	
Assembly Parameter	**Recommendation**
Solder Stencil Design	Laser Cut, Electro-Polished
Aperture Shape	Rectangular with rounded corners
Solder Stencil Thickness	0.100mm (0.004")
Solder Paste Type	Type 4 size sphere or smaller
Solder Reflow Profile	Per JEDEC J-STD-020
PCB Solder pad Design	Non-Solder Mask Defined
PCB Pad Finish	OSP or NiAu

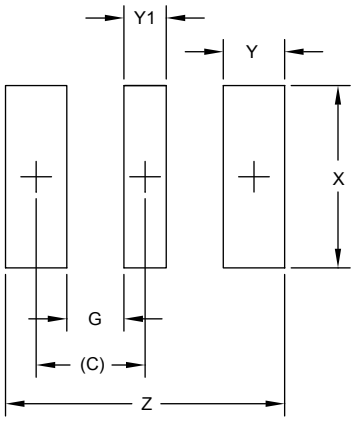
Outline Drawing - SLP0603P3X3F



DIMENSIONS			
DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.235	0.250	0.275
A1	0.005	0.015	0.050
b	0.230	0.250	0.270
D	0.580	0.62	0.650
E	0.280	0.32	0.350
e	0.225 BSC		
L	0.080	0.100	0.120
N	3		
aaa	0.08		
bbb	0.10		

NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).

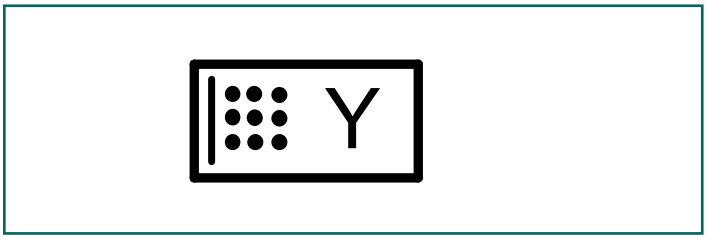
Land Pattern - SLP0603P3X3F



DIMENSIONS	
DIM	MILLIMETERS
C	(0.258)
G	0.135
X	0.430
Y	0.145
Y1	0.100
Z	0.660

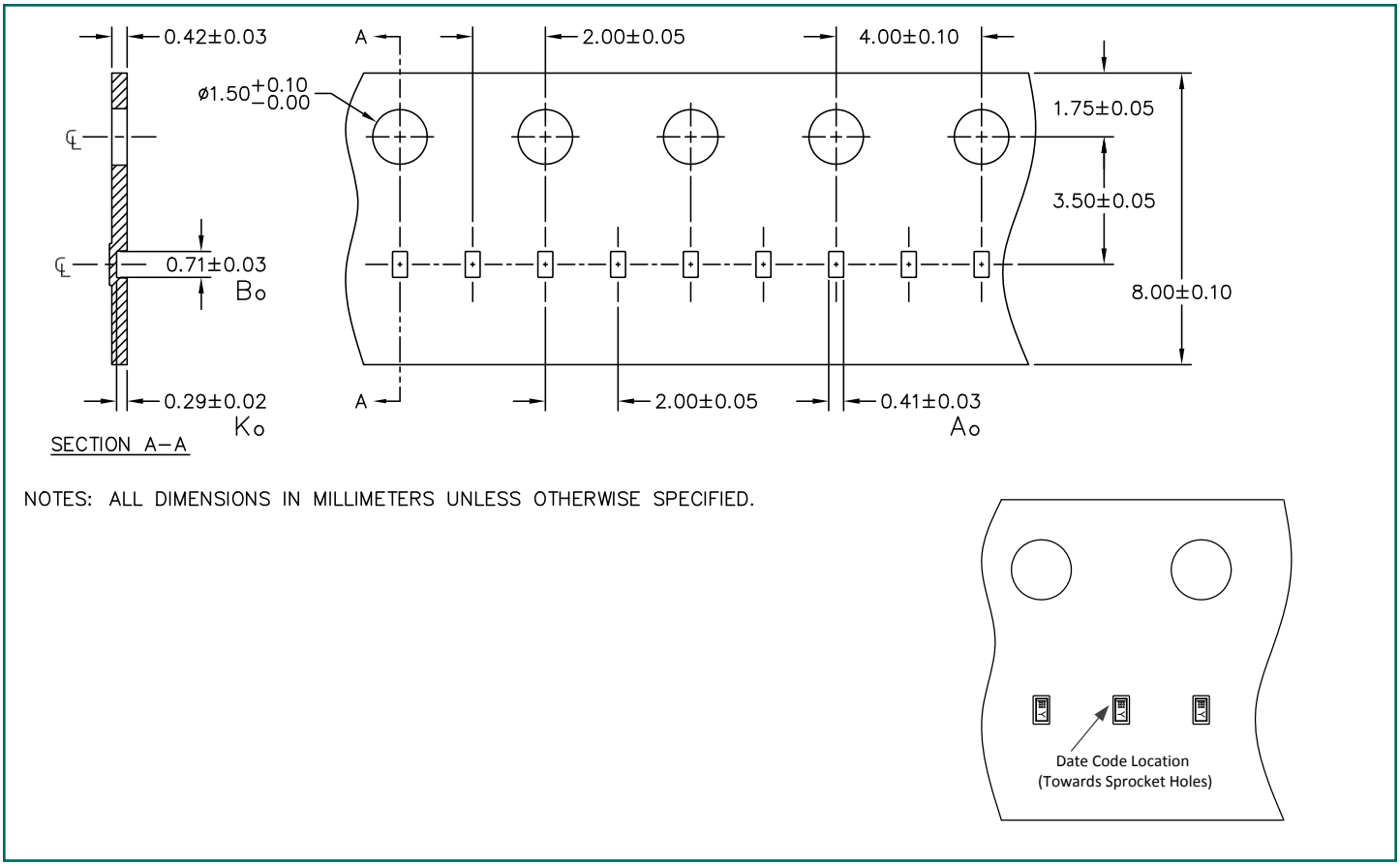
NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY.
   CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR
   COMPANY'S MANUFACTURING GUIDELINES ARE MET.

Marking Code



Notes: Device is electrically symmetrical

Tape and Reel Specification



Ordering Information

Part Number	Qty per Reel	Reel Size
uClamp0512ZATFT	15000	7 Inch

MicroClamp, uClamp and µClamp are registered trademarks of Semtech Corporation.

Contact Information

Semtech Corporation
200 Flynn Road, Camarillo, CA 93012
Phone: (805) 498-2111, Fax: (805) 498-3804
www.semtech.com

Rel Job Detail Report

by Sublot, by Sequence
Contact: Gurmail Sajjan
(805) 480 2142
gsajjan@semtech.com

Businessunit	Protection			
Reljob#	**Part_Number, Job Name/Type**	**Fab, Package**	**Rel Job Status**	**Key Dates:**
5929	RClamp1851ZA New Device Qual New Product on qualified process and qualified package	Tower SLP0603P2X3F	Rel Testing Complete Passes All Requirements	**Job Accepted:** 21-Jan-2015 **Requested CD:** **Actual Start Date:** 17-Dec-2014 **ECD for Conditional:** **Job ECD:** 19-Mar-2015

Completed Tasks

1.0 **Lot** AER2241 **AssemblyLot** AER2241 **DateCode** 1504

Seq	TaskCode	SampleSize	Criteria	Complete	Failures	DataSource	Results/Comments
1	Data-Prep	None	None	19-Feb-2015		Camarillo	
2	HTRB_Pre_Elect_150°C_RT24	210	Pass on Zero Fails	20-Feb-2015	0	Camarillo	
3	HTRB_150°C_Real Time_0024	210	Pass on Zero Fails	06-Mar-2015	0	Camarillo	
4	HTRB_Pre_Elect	105	Pass on Zero Fails	19-Feb-2015	0	Camarillo	
5	HTRB_150°C_0072	105	Pass on Zero Fails	23-Feb-2015	0	Camarillo	
6	HTRB_150°C _0408	105	Pass on Zero Fails	06-Mar-2015	0	Camarillo	
7	85/85_Pre Elec	20	Pass on Zero Fails	19-Feb-2015	0	Camarillo	
8	85/85_120hr_On/Off	20	Pass on Zero Fails	24-Feb-2015	0	Camarillo	
9	Pack_Clos	0	0	07-Mar-2015		Camarillo	

Rel Job Detail Report

by Sublot, by Sequence
Contact: Gurmail Sajjan
(805) 480 2142
gsajjan@semtech.com

Businessunit	Protection			
Reljob#	**Part_Number, Job Name/Type**	**Fab, Package**	**Rel Job Status**	**Key Dates:**
5940	RClamp5031ZA New Device Qual New Product on qualified process and qualified package	Tower SLP0603P2X3F	Rel Testing Complete Passes All Requirements	**Job Accepted:** 21-May-2015 **Requested CD:** **Actual Start Date:** 23-Jan-2015 **ECD for Conditional:** **Job ECD:** 29-May-2015

Completed Tasks

1.0 Lot AER2297 **AssemblyLot** AER2297 **DateCode** 1515

Seq	TaskCode	SampleSize	Criteria	Complete	Failures	DataSource	Results/Comments
1	Data-Prep	None	None	24-Apr-2015		Camarillo	
2	HTRB_Pre_Elect_150°C_RT24	210	Pass on Zero Fails	01-May-2015	0	Camarillo	
3	HTRB_150°C_Real Time_0024	210	Pass on Zero Fails	21-May-2015	0	Camarillo	
4	HTRB_Pre_Elect	105	Pass on Zero Fails	29-Apr-2015	0	Camarillo	
5	BI_BD_Valid	NA	Meet HTOL Schematics	29-Apr-2015	0	Camarillo	
6	HTRB_150°C_0072	105	Pass on Zero Fails	04-May-2015	0	Camarillo	
7	HTRB_150°C _0408	105	Pass on Zero Fails	18-May-2015	0	Camarillo	
8	85/85_Pre Elec	20	Pass on Zero Fails	29-Apr-2015	0	Camarillo	
9	85/85_120hr_On/Off	20	Pass on Zero Fails	05-May-2015	0	Camarillo	
10	Pack_Clos	0	0	22-May-2015		Camarillo	

Rel Job Detail Report

by Sublot, by Sequence
Contact: Gurmail Sajjan
(805) 480 2142
gsajjan@semtech.com

Businessunit	Protection			
Reljob#	**Part_Number, Job Name/Type**	**Fab, Package**	**Rel Job Status**	**Key Dates:**
6276.2	RCLAMP3331ZA/RCLAMP5011ZA Process Qual (TJT) New Product on un-qualified process with qualified package	TJT/PALM-D SLP0603P2X3F	Rel Testing Complete Passes All Requirem.ents	**Job Accepted:** 06-Dec-2016 **Requested CD:** **Actual Start Date:** 06-Dec-2016 **ECD for Conditional:** **Job ECD:** 02-Mar-2017

Completed Tasks

1.0 **Lot** AER3682 **AssemblyLot** AER3682 **DateCode** 1647

Seq	TaskCode	SampleSize	Criteria	Complete	Failures	DataSource	Results/Comments
1	Data-Prep	None	None	09-Dec-2016		Camarillo	
2	HTRB_Pre_Elect_150°C_RT24	210	Pass on Zero Fails	13-Dec-2016	0	Camarillo	
3	HTRB_150°C_Real Time_0024	210	Pass on Zero Fails	15-Dec-2016	0	Camarillo	
4	HTRB_Pre_Elect	105	Pass on Zero Fails	09-Dec-2016	0	Camarillo	
5	BI_BD_Valid	NA	Meet HTOL Schematics	09-Dec-2016		Camarillo	
6	HTRB_150°C_0072	105	Pass on Zero Fails	12-Dec-2016	0	Camarillo	
7	HTRB_150°C _0408	105	Pass on Zero Fails	04-Jan-2017	0	Camarillo	
8	HTS_Pre_Elect	77	Pass on Zero Fails	09-Dec-2016	0	Camarillo	
10	HTS_0500	77	Pass on Zero Fails	04-Jan-2017	0	Camarillo	
11	HTS_1000	77	Pass on Zero Fails	23-Jan-2017	0	Camarillo	
12	85/85_W/Pre_Pre Elec	20		13-Dec-2016	0	Camarillo	
13	85°C/85%RH_BD_Valid	20	Pass on Zero Fails	06-Jan-2017		Camarillo	
14	85/85_120hr_On/Off	20	Pass on Zero Fails	11-Jan-2017	0	Camarillo	
15	Pre_Elect_Precond	154	Pass on Zero Fails	13-Dec-2016	0	Camarillo	
16	Precond_Temp_Cyc_5cyc	154	Pass on Zero Fails	04-Jan-2017	0	Camarillo	

Contact: Gurmail Sajjan
(805) 480 2142
gsajjan@semtech.com

17	Precond_HTS_24hr	154	Pass on Zero Fails	05-Jan-2017	0	Camarillo
18	Precond_85/85_NoElec168hr	154	Pass on Zero Fails	12-Jan-2017	0	Camarillo
19	Precond_IR_Refl_Char	154	Pass on Zero Fails	12-Jan-2017	0	Camarillo
20	T/C_Pre_Elect	77	Pass on Zero Fails	12-Jan-2017	0	Camarillo
21	T/C_wPre_0250	77	Pass on Zero Fails	18-Jan-2017	0	Camarillo
22	T/C_wPre_0500	77	Pass on Zero Fails	23-Jan-2017	0	Camarillo
23	T/C_wPre_1000	77	Pass on Zero Fails	02-Feb-2017	0	Camarillo
23	X_Sect	15	Pass on Zero Fails	24-Feb-2017	0	Camarillo
24	85°C/85%RH_W/Pre_Pre Elec	77	Pass on Zero Fails	12-Jan-2017	0	Camarillo
25	85°C/85%RH_BD_Valid	77	Pass on Zero Fails	13-Jan-2017	0	Camarillo
26	85°C/85%RH_Biased_168hrs	77	Pass on Zero Fails	20-Jan-2017	0	Camarillo
27	85°C/85%RH_Biased_500hrs	77	Pass on Zero Fails	03-Feb-2017	0	Camarillo
28	85°C/85%RH_Biased_1000hrs	77	Pass on Zero Fails	24-Feb-2017	0	Camarillo
28	X_Sect	15	Pass on Zero Fails	24-Feb-2017	0	Camarillo
29	Rider_Card_Wash/Bake	154	Pass on Zero Fails	12-Dec-2017	0	Camarillo
30	Pack_Clos	0	0	27-Feb-2017		Camarillo

2.0 ***Lot*** AER3318 ***AssemblyLot*** AER3318 ***DateCode*** 1648

Seq	TaskCode	SampleSize	Criteria	Complete	Failures	DataSource	Results/Comments
1	Data-Prep	None	None	09-Dec-2016		Camarillo	
2	HTRB_Pre_Elect_150°C_RT24	210	Pass on Zero Fails	13-Dec-2016	0	Camarillo	
3	HTRB_150°C_Real Time_0024	210	Pass on Zero Fails	14-Dec-2016	0	Camarillo	
4	HTRB_Pre_Elect	105	Pass on Zero Fails	09-Dec-2016	0	Camarillo	
5	BI_BD_Valid	NA	Meet HTOL Schematics	09-Dec-2016		Camarillo	
6	HTRB_150°C_0072	105	Pass on Zero Fails	12-Dec-2016	0	Camarillo	
7	HTRB_150°C _0408	105	Pass on Zero Fails	04-Jan-2017	0	Camarillo	
8	HTS_Pre_Elect	77	Pass on Zero Fails	12-Dec-2016	0	Camarillo	
10	HTS_0500	77	Pass on Zero Fails	04-Jan-2017	0	Camarillo	

Contact: Gurmail Sajjan
(805) 480 2142
gsajjan@semtech.com

11	HTS_1000	77	Pass on Zero Fails	23-Jan-2017	0	Camarillo	
12	85/85_W/Pre_Pre Elec	20	Pass on Zero Fails	13-Dec-2016	0		Camarillo
13	85°C/85%RH_BD_Valid	20	Pass on Zero Fails	06-Jan-2017	0	Camarillo	
14	85/85_120hr_On/Off	20	Pass on Zero Fails	11-Jan-2017	0	Camarillo	
15	Pre_Elect_Precond	154	Pass on Zero Fails	13-Dec-2016	0	Camarillo	
16	Precond_Temp_Cyc_5cyc	154	Pass on Zero Fails	04-Jan-2017	0	Camarillo	
17	Precond_HTS_24hr	154	Pass on Zero Fails	05-Jan-2017	0	Camarillo	
18	Precond_85/85_NoElec168hr	154	Pass on Zero Fails	12-Jan-2017	0	Camarillo	
19	Precond_IR_Refl_Char	154	Pass on Zero Fails	12-Jan-2017	0	Camarillo	
20	T/C_Pre_Elect	77	Pass on Zero Fails	12-Jan-2017	0	Camarillo	
21	T/C_wPre_0250	77	Pass on Zero Fails	18-Jan-2017	0	Camarillo	
22	T/C_wPre_0500	77	Pass on Zero Fails	23-Jan-2017	0	Camarillo	
23	T/C_wPre_1000	77	Pass on Zero Fails	02-Feb-2017	0	Camarillo	
23	X_Sect	15	Pass on Zero Fails	24-Feb-2017	0	Camarillo	
24	85°C/85%RH_W/Pre_Pre Elec	77	Pass on Zero Fails	12-Jan-2017	0	Camarillo	
25	85°C/85%RH_BD_Valid	77	Pass on Zero Fail	13-Jan-2017	0	Camarillo	
26	85°C/85%RH_Biased_168hrs	77	Pass on Zero Fails	20-Jan-2017	0	Camarillo	
27	85°C/85%RH_Biased_500hrs	77	Pass on Zero Fails	03-Feb-2017	0	Camarillo	
28	85°C/85%RH_Biased_1000hrs	77	Pass on Zero Fails	24-Feb-2017	0	Camarillo	
28	X_Sect	15	Pass on Zero Fails	24-Feb-2017	0	Camarillo	
29	Rider_Card_Wash/Bake	154	Pass on Zero Fails	24-Dec-2017	0	Camarillo	
30	Pack_Clos	0	0	27-Feb-2017		Camarillo	

3.0 ***Lot*** AER3808 ***AssemblyLot*** AER3808 ***DateCode*** 1648

Seq	TaskCode	SampleSize	Criteria	Complete	Failures	DataSource	Results/Comments
1	Data-Prep	None	None	04-Jan-2017	0	Camarillo	
2	HTRB_Pre_Elect_150°C_RT24	100	Pass on Zero Fails	10-Jan-2017	0	Camarillo	
3	HTRB_150°C_Real Time_0024	105	Pass on Zero Fails	16-Jan-2017	0	Camarillo	

Contact: Gurmail Sajjan
(805) 480 2142
gsajjan@semtech.com

4	HTRB_Pre_Elect	105	Pass on Zero Fails	10-Jan-2017	0	Camarillo
5	BI_BD_Valid	NA	Meet HTOL Schematics	10-Jan-2017	0	Camarillo
6	HTRB_150°C_0072	105	Pass on Zero Fails	13-Jan-2017	0	Camarillo
7	HTRB_150°C _0408	105	Pass on Zero Fails	27-Jan-2017	0	Camarillo
8	HTS_Pre_Elect	77	Pass on Zero Fails	09-Jan-2017	0	Camarillo
9	HTS_0168	77	Pass on Zero Fails	16-Jan-2017	0	Camarillo
10	HTS_0500	77	Pass on Zero Fails	30-Jan-2017	0	Camarillo
11	HTS_1000	77	Pass on Zero Fails	22-Feb-2017	0	Camarillo
12	85/85_W/Pre_Pre Elec	20	Pass on Zero Fails	10-Jan-2017	0	Camarillo
13	85°C/85%RH_BD_Valid	20	Pass on Zero Fails	11-Jan-2017	0	Camarillo
14	85/85_120hr_On/Off	20	Pass on Zero Fails	16-Jan-2017	0	Camarillo
15	Pre_Elect_Precond	154	Pass on Zero Fails	09-Jan-2017	0	Camarillo
16	Precond_Temp_Cyc_5cyc	154	Pass on Zero Fails	09-Jan-2017	0	Camarillo
17	Precond_HTS_24hr	154	Pass on Zero Fails	10-Jan-2017	0	Camarillo
18	Precond_85/85_NoElec168hr	154	Pass on Zero Fails	17-Jan-2017	0	Camarillo
19	Precond_IR_Refl_Char	154	Pass on Zero Fails	17-Jan-2017	0	Camarillo
20	T/C_Pre_Elect	77	Pass on Zero Fails	17-Jan-2017	0	Camarillo
21	T/C_wPre_0250	77	Pass on Zero Fails	23-Jan-2017	0	Camarillo
22	T/C_wPre_0500	77	Pass on Zero Fails	30-Jan-2017	0	Camarillo
23	T/C_wPre_1000	77	Pass on Zero Fails	07-Feb-2017	0	Camarillo
23	X_Sect	15	Pass on Zero Fails	11-Mar-2017	0	Camarillo
24	85°C/85%RH_W/Pre_Pre Elec	77	Pass on Zero Fails	17-Jan-2017	0	Camarillo
25	85°C/85%RH_BD_Valid	77	Pass on Zero Fails	18-Jan-2017	0	Camarillo
26	85°C/85%RH_Biased_168hrs	77	Pass on Zero Fails	16-Jan-2017	0	Camarillo
27	85°C/85%RH_Biased_500hrs	77	Pass on Zero Fails	18-Feb-2017	0	Camarillo
28	85°C/85%RH_Biased_1000hrs	77	Pass on Zero Fails	11-Mar-2017	0	Camarilloo
28	X_Sect	15		01-Mar-2017		Camarillo

Contact: Gurmail Sajjan
(805) 480 2142
gsajjan@semtech.com

29	Rider_Card_Wash/Bake	154		05-Jan-2017	0	Camarillo
30	Pack_Clos	0	0	02-Mar-2017		Camarillo

Rel Job Detail Report

by Sublot, by Sequence
Contact: Gurmail Sajjan
(805) 480 2142
gsajjan@semtech.com

Businessunit *Protection*

Reljob#	*Part_Number, Job Name/Type*	*Fab, Package*	*Rel Job Status*	*Key Dates:*
6074	RClamp0542ZA New Device Qual New Product on qualified process and qualified package	ASMC21 TVS SLP0603P3X3F	Rel Testing Complete Passes All Requirements	***Job Accepted:*** 09-Oct-2015 ***Requested CD:*** ***Actual Start Date:*** 30-Sep-2015 ***ECD for Conditional:*** ***Job ECD:*** 10-Nov-2015

Completed Tasks

1.0 ***Lot*** AER2729 ***AssemblyLot*** AER2729 ***DateCode*** 1538

Seq	*TaskCode*	*SampleSize*	*Criteria*	*Complete*	*Failures*	*DataSource*	*Results/Comments*
1	Data-Prep	None	None	13-Oct-2015		Camarillo	
2	HTRB_Pre_Elect_150°C_RT24	105	Pass on Zero Fails	13-Oct-2015	0	Camarillo	
3	HTRB_150°C_Real Time_0024	105	Pass on Zero Fails	16-Oct-2015	0	Camarillo	
4	HTRB_Pre_Elect	105	Pass on Zero Fails	13-Oct-2015	0	Camarillo	
5	HTRB_150°C_0072	105	Pass on Zero Fails	16-Oct-2015	0	Camarillo	
6	HTRB_150°C _0408	105	Pass on Zero Fails	30-Oct-2015	0	Camarillo	
7	85/85_Pre Elec	20	Pass on Zero Fails	13-Oct-2015	0	Camarillo	
8	85/85_120hr_On/Off	20	Pass on Zero Fails	20-Oct-2015	0	Camarillo	
12	Pack_Clos	0	0	10-Nov-2015		Camarillo	

Rel Job Detail Report

by Sublot, by Sequence
Contact: Gurmail Sajjan
(805) 480 2142
gsajjan@semtech.com

Businessunit	Protection			
Reljob#	**Part_Number, Job Name/Type**	**Fab, Package**	**Rel Job Status**	**Key Dates:**
6045	uClamp0512ZA	ASMC12TVS	Rel Testing Complete Passes All Requirements	**Job Accepted:** 06-Aug-2015
	uClamp0512ZA New Device / Package Qualif	SLP0603P3X3F		**Requested CD:**
	New Product on qualified process with un-qualified package		.	**Actual Start Date:** 06-Aug-2015
				ECD for Conditional:
.				**Job ECD:** 04-Dec-2015

Completed Tasks

1.0 **Lot** GDA416600 **AssemblyLot** AER-002558 **DateCode** 1531

Seq	TaskCode	SampleSize	Criteria	Complete	Failures	DataSource	Results/Comments
1	Data-Prep	None	None	14-Aug-2015		Camarillo	
2	HTRB Pre Ele 150°C RT24 B	210	Pass on Zero Fails	18-Aug-2015	0	Camarillo	
3	HTRB_150°C_Real Time_0024	210	Pass on Zero Fails	20-Aug-2015	0	Camarillo	
4	HTRB_Pre_Elect	105	Pass on Zero Fails	17-Aug-2015	0	Camarillo	
5	BI_BD_Valid	NA	Meet HTOL Schematics	18-Aug-2015	0	Camarillo	
6	HTRB_150°C_0072	105	Pass on Zero Fails	21-Aug-2015	0	Camarillo	
7	HTRB_150°C _0408	105	Pass on Zero Fails	04-Sep-2015	0	Camarillo	
8	HTS_Pre_Elect	77	Pass on Zero Fails	17-Aug-2015	0	Camarillo	
9	HTS_0168	77	Pass on Zero Fails	24-Aug-2015	0	Camarillo	
10	HTS_0500	77	Pass on Zero Fails	08-Sep-2015	0	Camarillo	
11	HTS_1000	77	Pass on Zero Fails	28-Sep-2015	0	Camarillo	
12	Pre_Conditioning_Level_1	NA	MSL 1	17-Aug-2015	0	Camarillo	
13	Rider_Card_Wash/Bake	NA		17-Aug-2015	0	Camarillo	
14	Pre_Elect_Precond	154	Pass on Zero Fails	18-Aug-2015	0	Camarillo	
15	Precond_Temp_Cyc_5cyc	154	Pass on Zero Fails	18-Aug-2015	0	Camarillo	

Contact: Gurmail Sajjan
(805) 480 2142
gsajjan@semtech.com

16	Precond_HTS_24hr	154	Pass on Zero Fails	19-Aug-2015	0	Camarillo	
17	Precond_85/85_NoElec168hr	154	Pass on Zero Fails	26-Aug-2015	0	Camarillo	
18	Precond_260°C_IR_Ref_Char	154	Pass on Zero Fails	26-Aug-2015	0	Camarillo	
19	T/C_Pre_Elect	77	Pass on Zero Fails	26-Aug-2015	0	Camarillo	
20	T/C_wPre_0250	77	Pass on Zero Fails	01-Sep-2015	0	Camarillo	
21	T/C_wPre_0500	77	Pass on Zero Fails	08-Sep-2015	0	Camarillo	
22	T/C_wPre_1000	77	Pass on Zero Fails	16-Sep-2015	0	Camarillo	
23	Pre_Elect_Precond	77	Pass on Zero Fails	25-Sep-2015	0	Camarillo	
24	Precond_Temp_Cyc_5cyc	77	Pass on Zero Fails	28-Sep-2015	0	Camarillo	
25	Precond_HTS_24hr	77	Pass on Zero Fails	29-Sep-2015	0	Camarillo	
26	Precond_85/85_NoElec168hr	77	Pass on Zero Fails	06-Oct-2015	0	Camarillo	
27	Precond_260°C_IR_Ref_Char	77	Pass on Zero Fails	06-Oct-2015	0	Camarillo	
28	85/85_W/Pre_Pre Elec	77	Pass on Zero Fails	06-Oct-2015	0	Camarillo	
29	85°C/85%RH_BD_Valid	77	Pass on Zero Fails	05-Oct-2015	0	Camarillo	
30	85°C/85%RH_Biased_168hrs	77	Pass on Zero Fails	03-Nov-2015	2	Camarillo	Rel. Eng.: Submitted to FA (FA-004024)
31	85°C/85%RH_Biased_500hrs	75	Pass on Zero Fails	17-Nov-2015	0	Camarillo	Rel. Eng.: Submitted to FA (FA-004024)
32	85°C/85%RH_Biased_1000hrs	43	Pass on Zero Fails	18-Nov-2015	0	Camarillo	
33	Construct_Package	5 unique packaged devices minimum.	No Major Findings, Q&R to review construction analysis report.	21-Sep-2015		Camarillo	
34	FA_85/85_0168hr	3	FAs must be resolved, resulting in discounting the failure or corrective action taken.	03-Nov-2015	2	Camarillo	Rel. Eng.:FA indicated that A board issue was identified as well as a chemical reaction was responsible for the corrosion. Group agreed to rerun and follow up with ORT and CAR (CAR-001285). Release this qual on condition of the new material qual pass.
35	FA_85/85_0500hr	12	FAs must be resolved, resulting in discounting the failure or corrective action taken.	17-Nov-2015	12	Camarillo	Rel. Eng.:FA indicated that A board issue was identified as well as a chemical reaction was responsible for the corrosion. Group agreed to rerun and follow up with ORT and CAR (CAR-001285). Release this qual on condition of the new material qual pass.
36	Pack_Clos	0	0	19-Nov-2015		Camarillo	

Contact: Gurmail Sajjan
(805) 480 2142
gsajjan@semtech.com

2.0 **Lot** GDA416600 **AssemblyLot** AER-002559 **DateCode** 1531

Seq	TaskCode	SampleSize	Criteria	Complete	Failures	DataSource	Results/Comments
1	Data-Prep	None	None	14-Aug-2015		Camarillo	
2	HTRB Pre Ele 150°C RT24 B	210	Pass on Zero Fails	20-Aug-2015	0	Camarillo	
3	HTRB_150°C_Real Time_0024	210	Pass on Zero Fails	25-Aug-2015	0	Camarillo	
4	HTRB_Pre_Elect	105	Pass on Zero Fails	17-Aug-2015	0	Camarillo	
5	BI_BD_Valid	NA	Meet HTOL Schematics	18-Aug-2015	0	Camarillo	
6	HTRB_150°C_0072	105	Pass on Zero Fails	21-Aug-2015	0	Camarillo	
7	HTRB_150°C _0408	105	Pass on Zero Fails	04-Sep-2015	0	Camarillo	
8	HTS_Pre_Elect	77	Pass on Zero Fails	17-Aug-2015	0	Camarillo	
9	HTS_0168	77	Pass on Zero Fails	24-Aug-2015	0	Camarillo	
10	HTS_0500	77	Pass on Zero Fails	08-Sep-2015	0	Camarillo	
11	HTS_1000	77	Pass on Zero Fails	28-Sep-2015	0	Camarillo	
12	Pre_Conditioning_Level_1	NA	MSL 1	17-Aug-2015	0	Camarillo	
13	Rider_Card_Wash/Bake	NA		17-Aug-2015	0	Camarillo	
14	Pre_Elect_Precond	154	Pass on Zero Fails	18-Aug-2015	0	Camarillo	
15	Precond_Temp_Cyc_5cyc	154	Pass on Zero Fails	18-Aug-2015	0	Camarillo	
16	Precond_HTS_24hr	154	Pass on Zero Fails	19-Aug-2015	0	Camarillo	
17	Precond_85/85_NoElec168hr	154	Pass on Zero Fails	26-Aug-2015	0	Camarillo	
18	Precond_260°C_IR_Ref_Char	154	Pass on Zero Fails	26-Aug-2015	0	Camarillo	
19	T/C_Pre_Elect	77	Pass on Zero Fails	26-Aug-2015	0	Camarillo	
20	T/C_wPre_0250	77	Pass on Zero Fails	01-Sep-2015	0	Camarillo	
21	T/C_wPre_0500	77	Pass on Zero Fails	08-Sep-2015	0	Camarillo	
22	T/C_wPre_1000	77	Pass on Zero Fails	16-Sep-2015	0	Camarillo	
23	Pre_Elect_Precond	77	Pass on Zero Fails	25-Sep-2015	0	Camarillo	
24	Precond_Temp_Cyc_5cyc	77	Pass on Zero Fails	28-Sep-2015	0	Camarillo	
25	Precond_HTS_24hr	77	Pass on Zero Fails	29-Sep-2015	0	Camarillo	

Contact: Gurmail Sajjan
(805) 480 2142
gsajjan@semtech.com

26	Precond_85/85_NoElec168hr	77	Pass on Zero Fails	06-Oct-2015	0	Camarillo	
27	Precond_260°C_IR_Ref_Char	77	Pass on Zero Fails	06-Oct-2015	0	Camarillo	
28	85/85_W/Pre_Pre Elec	77	Pass on Zero Fails	06-Oct-2015	0	Camarillo	
29	85°C/85%RH_BD_Valid	77	Pass on Zero Fails	05-Oct-2015	0	Camarillo	
30	85°C/85%RH_Biased_168hrs	77	Pass on Zero Fails	03-Nov-2015	3	Camarillo	Rel. Eng.: Submitted to FA (FA-004024)
31	85°C/85%RH_Biased_500hrs	74	Pass on Zero Fails	17-Nov-2015	16	Camarillo	Rel. Eng.: Submitted to FA (FA-004024)
32	85°C/85%RH_Biased_1000hrs	32	Pass on Zero Fails	18-Nov-2015	0		Camarillo
33	FA_85/85_0168hr	3	FAs must be resolved, resulting in discounting the failure or corrective action taken.	03-Nov-2015	3	Camarillo	Rel. Eng.:FA indicated that A board issue was identified as well as a chemical reaction was responsible for the corrosion. Group agreed to rerun and follow up with ORT and CAR (CAR-001285). Release this qual on condition of the new material qual pass.
34	FA_85/85_0500hr	16	FAs must be resolved, resulting in discounting the failure or corrective action taken.	17-Nov-2015	16	Camarillo	Rel. Eng.:FA indicated that A board issue was identified as well as a chemical reaction was responsible for the corrosion. Group agreed to rerun and follow up with ORT and CAR (CAR-001285). Release this qual on condition of the new material qual pass.
35	Pack_Clos	0	0	19-Nov-2015		Camarillo	

3.0 Lot GDA416600 AssemblyLot AER-002560 DateCode 1531

Seq	TaskCode	SampleSize	Criteria	Complete	Failures	DataSource	Results/Comments
1	Data-Prep	None	None	14-Aug-2015		Camarillo	
2	HTRB Pre Ele 150°C RT24 B	210	Pass on Zero Fails	20-Aug-2015	0	Camarillo	
3	HTRB_150°C_Real Time_0024	210	Pass on Zero Fails	26-Aug-2015	0	Camarillo	
4	HTRB_Pre_Elect	105	Pass on Zero Fails	17-Aug-2015	0	Camarillo	
5	BI_BD_Valid	NA	Meet HTOL Schematics	18-Aug-2015	0	Camarillo	
6	HTRB_150°C_0072	105	Pass on Zero Fails	21-Aug-2015	0	Camarillo	
7	HTRB_150°C _0408	105	Pass on Zero Fails	04-Sep-2015	0	Camarillo	
8	HTS_Pre_Elect	77	Pass on Zero Fails	17-Aug-2015	0	Camarillo	
9	HTS_0168	77	Pass on Zero Fails	24-Aug-2015	0	Camarillo	
10	HTS_0500	77	Pass on Zero Fails	08-Sep-2015	0	Camarillo	

Contact: Gurmail Sajjan
(805) 480 2142
gsajjan@semtech.com

11	HTS_1000	77	Pass on Zero Fails	28-Sep-2015	0	Camarillo	
12	Pre_Conditioning_Level_1	NA	MSL 1	17-Aug-2015	0	Camarillo	
13	Rider_Card_Wash/Bake	NA		17-Aug-2015	0	Camarillo	
14	Pre_Elect_Precond	154	Pass on Zero Fails	18-Aug-2015	0	Camarillo	
15	Precond_Temp_Cyc_5cyc	154	Pass on Zero Fails	18-Aug-2015	0	Camarillo	
16	Precond_HTS_24hr	154	Pass on Zero Fails	19-Aug-2015	0	Camarillo	
17	Precond_85/85_NoElec168hr	154	Pass on Zero Fails	26-Aug-2015	0	Camarillo	
18	Precond_260°C_IR_Ref_Char	154	Pass on Zero Fails	26-Aug-2015	0	Camarillo	
19	T/C_Pre_Elect	77	Pass on Zero Fails	26-Aug-2015	0	Camarillo	
20	T/C_wPre_0250	77	Pass on Zero Fails	01-Sep-2015	0	Camarillo	
21	T/C_wPre_0500	77	Pass on Zero Fails	08-Sep-2015	0	Camarillo	
22	T/C_wPre_1000	77	Pass on Zero Fails	16-Sep-2015	0	Camarillo	
23	Pre_Elect_Precond	77	Pass on Zero Fails	25-Sep-2015	0	Camarillo	
24	Precond_Temp_Cyc_5cyc	77	Pass on Zero Fails	28-Sep-2015	0	Camarillo	
25	Precond_HTS_24hr	77	Pass on Zero Fails	29-Sep-2015	0	Camarillo	
26	Precond_85/85_NoElec168hr	77	Pass on Zero Fails	06-Oct-2015	0	Camarillo	
27	Precond_260°C_IR_Ref_Char	77	Pass on Zero Fails	06-Oct-2015	0	Camarillo	
28	85/85_W/Pre_Pre Elec	77	Pass on Zero Fails	06-Oct-2015	0	Camarillo	
29	85°C/85%RH_BD_Valid	77	Pass on Zero Fails	05-Oct-2015	0	Camarillo	
30	85°C/85%RH_Biased_168hrs	77	Pass on Zero Fails	03-Nov-2015	1	Camarillo	Rel. Eng.: Submitted to FA (FA-004024)
31	85°C/85%RH_Biased_500hrs	76	Pass on Zero Fails	17-Nov-2015	0	Camarillo	Rel. Eng.: No new failure.
32	85°C/85%RH_Biased_1000hrs	40	Pass on Zero Fails	03-Dec-2015	2	Camarillo	Rel. Eng.: Submitted to FA (FA-004024)
33	FA_85/85_0168hr	1	FAs must be resolved, resulting in discounting the failure or corrective action taken.	03-Nov-2015	1	Camarillo	Rel. Eng.:FA indicated that A board issue was identified as well as a chemical reaction was responsible for the corrosion. Group agreed to rerun and follow up with ORT and CAR (CAR-001285). Release this qual on condition of the new material qual pass.

Contact: Gurmail Sajjan
(805) 480 2142
gsajjan@semtech.com

34	FA_85/85_1000hr	2	FAs must be resolved, resulting in discounting the failure or corrective action taken.	03-Dec-2015	2	Camarillo	Rel. Eng.:FA indicated that A board issue was identified as well as a chemical reaction was responsible for the corrosion. Group agreed to rerun and follow up with ORT and CAR (CAR-001285). Release this qual on condition of the new material qual pass.
35	Pack_Clos	0	0	04-Dec-2015		Camarillo	