TPS6226x 2.25-MHz 600-mA Step Down Converter in 2 x 2 WSON and SOT Package

1 Features

- High Efficiency Step-Down Converter
- Output Current up to 600 mA
- V_{IN} Range from 2 V to 6 V for Li-ion Batteries with Extended Voltage Range
- 2.25-MHz Fixed Frequency Operation
- Power Save Mode at Light Load Currents
- Output Voltage Accuracy in PWM Mode ±1.5%
- Typical 15-μA Quiescent Current
- 100% Duty Cycle for Lowest Dropout
- Voltage Positioning at Light Loads
- Available in a SOT (5) and 2-mm × 2-mm × 0.8-mm WSON (6) Package
- Allows <1-mm Solution Height

2 Applications

- Mobile Phones, Smart Phones
- Low Power DSP Supply
- Portable Media Players
- Point-of-Load (POL) Applications

3 Description

The TPS6226x device is a highly efficient synchronous step-down DC/DC converter. The TPS6226x provides up to 600-mA output current from a single Li-Ion cell, and is ideal for battery-powered applications such as mobile phones and other portable equipment.

With an wide input voltage range of 2 V to 6 V, the device also supports two- and three-cell alkaline batteries, 3.3-V and 5-V input voltage rails.

The TPS6226x operates at 2.25-MHz fixed-switching frequency, and enters power save mode operation at light load currents to maintain high efficiency over the entire load current range.

The power save mode is optimized for low-output voltage ripple. For low noise applications, the device can be forced into fixed frequency pulse-width modulation (PWM) mode by pulling the MODE pin high. In the shutdown mode, the current consumption is reduced to less than 1 μA. The TPS6226x allows the use of small inductors and capacitors to achieve a small solution size.

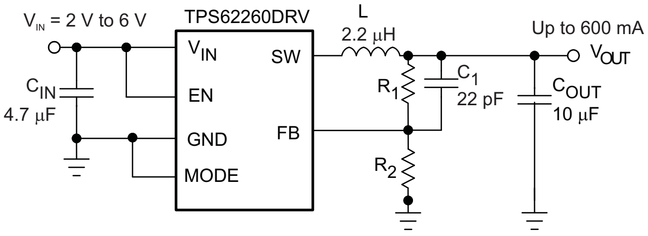
The TPS6226x operates over a free air temperature range of –40°C to 85°C. It is available in a 5-pin SOT and a 6-pin 2-mm × 2-mm WSON package.

Device Information[1]

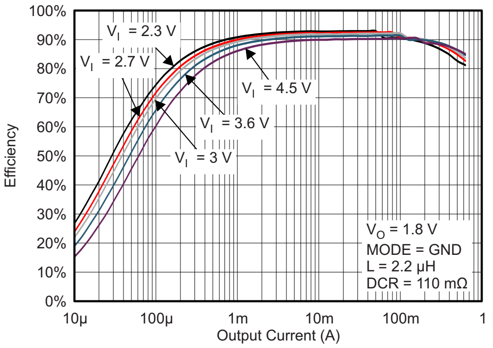
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS62260	WSON (6)	2.00 mm × 2.00 mm
	SOT (5)	2.90 mm × 1.60 mm
TPS62261	WSON (6)	2.00 mm × 2.00 mm
TPS62262	WSON (6)	2.00 mm × 2.00 mm
	SOT (5)	2.90 mm × 1.60 mm
TPS62263	WSON (6)	2.00 mm × 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Schematic



Efficiency vs Output Current



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (February 2011) to Revision E	**Page**
• Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

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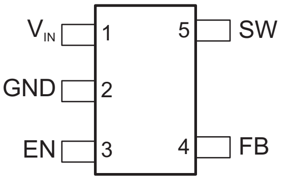
5 Device Comparison Table

PART NUMBER	OUTPUT VOLTAGE[1]	PACKAGE[2]	PACKAGE DESIGNATOR	MODE PIN	PACKAGE MARKING
TPS62260	Adjustable	WSON (6)	DRV	Yes	BYK
		SOT (5)	DDC	No, PFM/PWM auto transition	BYP
TPS62261	1.8 V fixed	WSON (6)	DRV	Yes	BYL
TPS62262	1.2 V fixed	WSON (6)	DRV	Yes	BYM
		SOT (5)	DDC	No, PFM/PWM auto transition	QXS
TPS62263	2.5 V fixed	WSON (6)	DRV	Yes	CFX

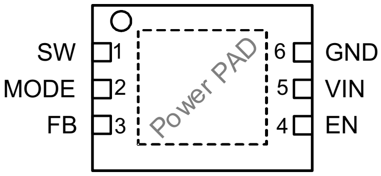
(1) Contact TI for other fixed output voltage options
(2) For the most current package and ordering information, see *Mechanical, Packaging, and Orderable Information*, or see the TI website at www.ti.com.

6 Pin Configuration and Functions

DDC Package
5-Pin SOT
Top View



DRV Package
6-Pin WSON
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	WSON	SOT		
EN	4	3	IN	This is the enable pin of the device. Pulling this pin to low forces the device into shutdown mode. Pulling this pin to high enables the device. This pin must be terminated.
FB	3	4	IN	Feedback pin for the internal regulation loop. Connect the external resistor divider to this pin. In case of fixed output voltage option, connect this pin directly to the output capacitor
GND	6	2	PWR	GND supply pin.
MODE	2	—	IN	This pin is only available at WSON package option. MODE pin = High forces the device to operate in fixed frequency PWM mode. MODE pin = Low enables the power save mode with automatic transition from PFM mode to fixed frequency PWM mode.
SW	1	5	OUT	This is the switch pin and is connected to the internal MOSFET switches. Connect the external inductor between this terminal and the output capacitor.
VIN	5	1	PWR	V_{IN} power supply pin.

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7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

		MAX	MIN	UNIT
V_{IN}	Input voltage (2)	–0.3	7	V
	Voltage at EN, MODE	–0.3	V_{IN} +0.3 ≤ 7	
	Voltage on SW	–0.3	7	
	Peak output current	Internally limited		A
T_J	Maximum operating junction temperature	–40	125	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{IN}	Supply voltage	2		6	V
	Output voltage range for adjustable voltage	0.6		V_{IN}	V
T_A	Operating ambient temperature	–40		85	°C
T_J	Operating junction temperature	–40		125	°C

7.4 Thermal Information

THERMAL METRIC(1)		TPS62260, TPS62261, TPS62262, TPS62263	TPS62260, TPS62262	UNIT
		DRV [WSON]	DDC [SOT]	
		6 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	67.8	226.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	88.5	40.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	37.2	48.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.0	0.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	37.6	48.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	7.9	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

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7.5 Electrical Characteristics

Over full operating ambient temperature range, typical values are at T_A = 25°C. Unless otherwise noted, specifications apply for condition V_{IN} = EN = 3.6 V. External components C_{IN} = 4.7 µF 0603, C_{OUT} = 10 µF 0603, L = 2.2 µH, see the parameter measurement information.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
V_{IN}	Input voltage range		2.3		6	V
I_{OUT}	Output current	V_{IN} 2.5 V to 6 V			600	mA
		V_{IN} 2.3 V to 2.5 V			300	
		V_{IN} 2 V to 2.3 V			150	
I_Q	Operating quiescent current	I_{OUT} = 0 mA, PFM mode enabled (MODE = GND) device not switching		15		µA
		I_{OUT} = 0 mA, PFM mode enabled (MODE = GND) device switching, V_{OUT} = 1.8 V, see [1]		18.5		
		I_{OUT} = 0 mA, switching with no load (MODE = V_{IN}), PWM operation, V_{OUT} = 1.8 V, V_{IN} = 3 V		3.8		mA
I_{SD}	Shutdown current	EN = GND		0.1	1	µA
UVLO	Undervoltage lockout threshold	Falling		1.85		V
		Rising		1.95		
ENABLE, MODE						
V_{IH}	High level input voltage, EN, MODE	2 V ≤ V_{IN} ≤ 6 V	1		VIN	V
V_{IL}	Low level input voltage, EN, MODE	2 V ≤ V_{IN} ≤ 6 V	0		0.4	V
I_{IN}	Input bias current, EN, MODE	EN, MODE = GND or VIN		0.01	1	µA
POWER SWITCH						
$R_{DS(on)}$	High side MOSFET on-resistance	V_{IN} = V_{GS} = 3.6 V, T_A = 25°C		240	480	mΩ
	Low side MOSFET on-resistance			185	380	
I_{LIMF}	Forward current limit MOSFET high side and low side	V_{IN} = V_{GS} = 3.6 V	0.8	1	1.2	A
T_{SD}	Thermal shutdown	Increasing junction temperature		140		°C
	Thermal shutdown hysteresis	Decreasing junction temperature		20		
OSCILLATOR						
f_{SW}	Oscillator frequency	2 V ≤ V_{IN} ≤ 6 V	2	2.25	2.5	MHz
OUTPUT						
V_{OUT}	Adjustable output voltage range		0.6		V_{IN}	V
V_{REF}	Reference voltage			600		mV
V_{FB}	Feedback voltage PWM mode	MODE = V_{IN}, PWM operation, for fixed output voltage versions V_{FB} = V_{OUT}, 2.5 V ≤ V_{IN} ≤ 6 V, 0 mA ≤ I_{OUT} ≤ 600 mA [2]	–1.5%	0%	1.5%	
	Feedback voltage PFM mode	MODE = GND, device in PFM mode, voltage positioning active[1]		1%		
	Load regulation	PWM mode		–0.5		%/A
$t_{Start\ Up}$	Start-up time	Time from active EN to reach 95% of V_{OUT} nominal		500		µs
t_{Ramp}	V_{OUT} ramp-up time	Time to ramp from 5% to 95% of V_{OUT}		250		µs
I_{lkg}	Leakage current into SW pin	V_{IN} = 3.6 V, V_{IN} = V_{OUT} = V_{SW}, EN = GND [3]		0.1	1	µA

(1) In PFM mode, the internal reference voltage is set to typ. 1.01 × V_{REF}. See the parameter measurement information.
(2) For V_{IN} = V_{OUT}+ 0.6 V.
(3) In fixed output voltage versions, the internal resistor divider network is disconnected from FB pin.

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7.6 Typical Characteristics

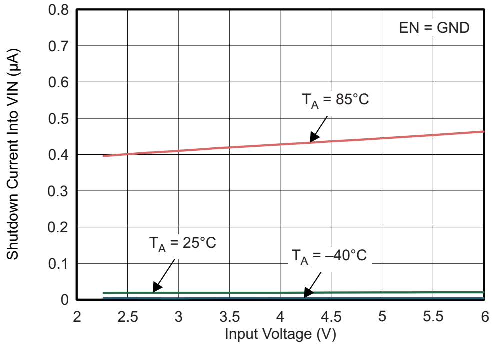

Figure 1. Shutdown Current Into VIN vs Input Voltage

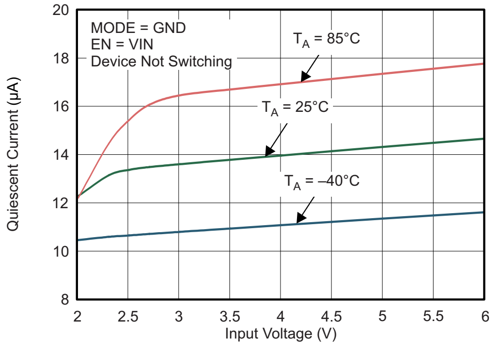

Figure 2. Quiescent Current vs Input Voltage

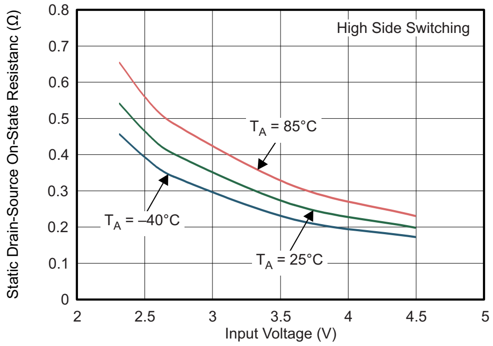

Figure 3. Static Drain-Source On-State Resistance vs Input Voltage

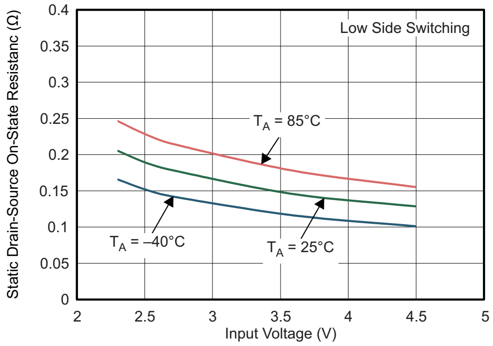

Figure 4. Static Drain-Source On-State Resistance vs Input Voltage

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8 Detailed Description

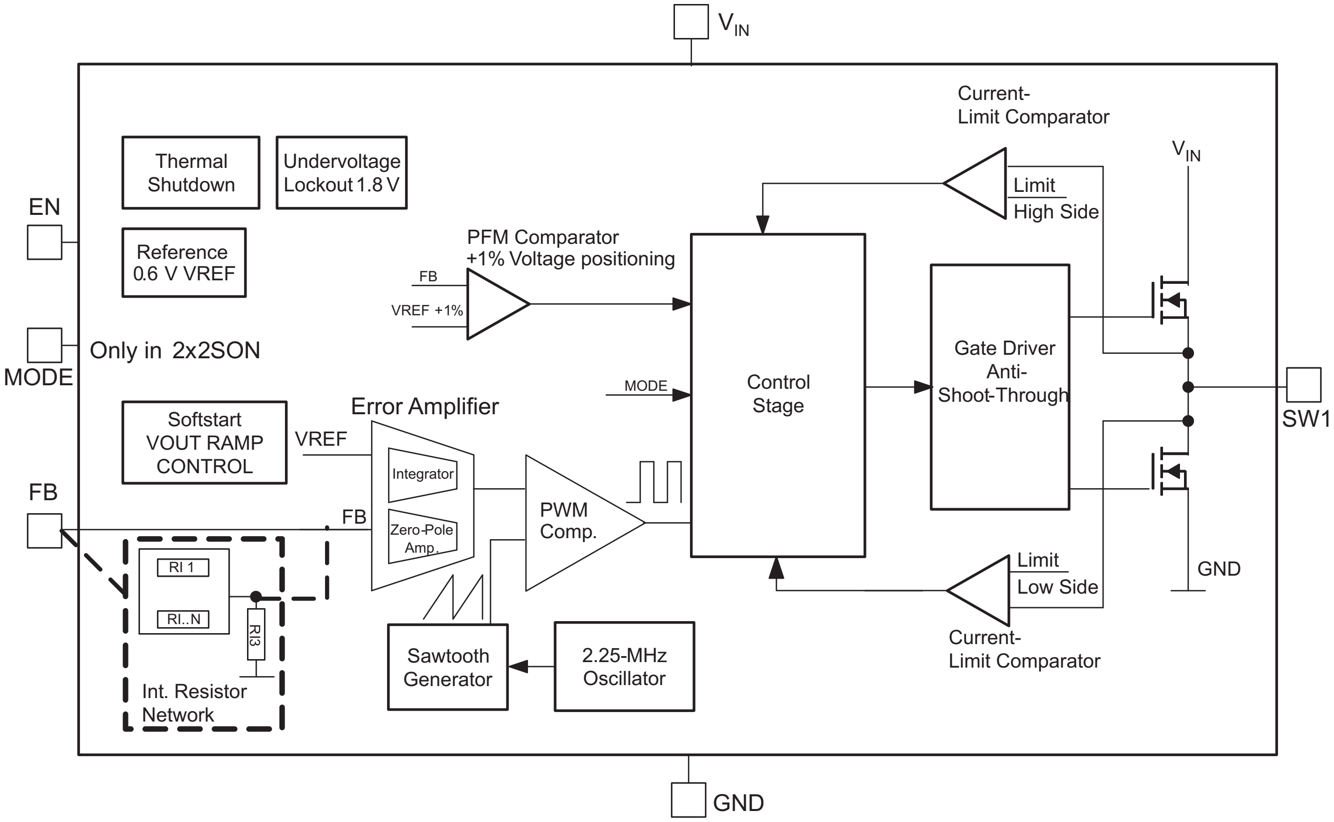
8.1 Overview

The TPS6226x step-down converter operates with typically 2.25-MHz fixed frequency pulse-width modulation (PWM) at moderate to heavy load currents. At light load currents, the converter can automatically enter power save mode and operate in pulse-frequency modulation (PFM) mode.

During PWM operation, the converter uses a unique fast-response voltage mode control scheme with input voltage feed-forward to achieve good line and load regulation, allowing the use of small ceramic input and output capacitors. At the beginning of each clock cycle initiated by the clock signal, the high-side MOSFET switch is turned on. The current then flows from the input capacitor, through the high-side MOSFET switch, through the inductor, and to the output capacitor and load. During this phase, the current ramps up until the PWM comparator trips and the control logic turns off the switch. The current limit comparator also turns off the switch if the current limit of the high-side MOSFET switch is exceeded. After a dead time preventing shoot-through current, the low-side MOSFET rectifier is turned on and the inductor current ramps down. The current then flows from the inductor to the output capacitor and to the load. It returns back to the inductor through the low-side MOSFET rectifier.

The next cycle is initiated by the clock signal, turning off the low-side MOSFET rectifier and turning on the high-side MOSFET switch.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Dynamic Voltage Positioning

This feature reduces the voltage undershoots/overshoots at load steps from light to heavy load and vice versa. It is active in power save mode and regulates the output voltage 1% higher than the nominal value. This provides more headroom for both the voltage drop at a load step, and the voltage increase at a load throw-off.

Feature Description (continued)

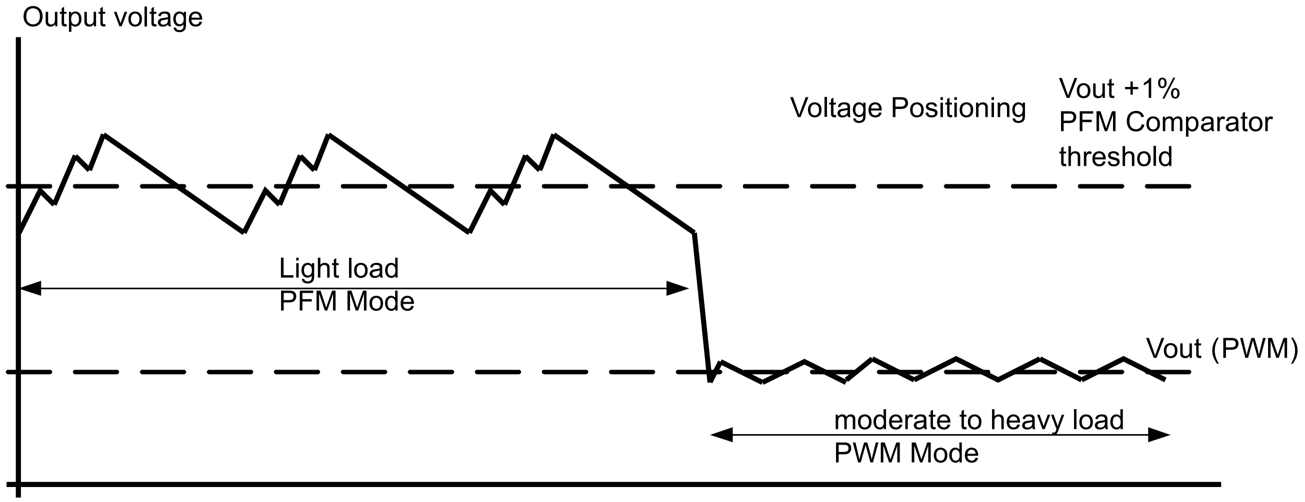


Figure 5. Power Save Mode Operation With Automatic Mode Transition

8.3.2 Undervoltage Lockout

The undervoltage lockout circuit prevents the device from malfunctioning at low input voltages and from excessive discharge of the battery and disables the output stage of the converter. The undervoltage lockout threshold is typically 1.85 V with falling V_{IN}.

8.3.3 Mode Selection

The MODE pin allows mode selection between forced PWM mode and power save mode.

Connecting this pin to GND enables the power save mode with automatic transition between PWM and PFM mode. Pulling the MODE pin high forces the converter to operate in fixed frequency PWM mode even at light load currents. This allows simple filtering of the switching frequency for noise sensitive applications. In this mode, the efficiency is lower compared to the power save mode during light loads.

The condition of the MODE pin can be changed during operation and allows efficient power management by adjusting the operation mode of the converter to the specific system requirements.

8.3.4 Enable

The device is enabled by setting the EN pin to high. During the start up time $t_{Start\ Up}$ the internal circuits are settled and the soft start circuit is activated. The EN input can be used to control power sequencing in a system with various DC/DC converters. The EN pin can be connected to the output of another converter, to drive the EN pin high and getting a sequencing of supply rails. With EN = GND, the device enters shutdown mode in which all internal circuits are disabled. In fixed output voltage versions, the internal resistor divider network is then disconnected from FB pin.

8.3.5 Thermal Shutdown

As soon as the junction temperature, T_J, exceeds 140°C (typical) the device goes into thermal shutdown. In this mode, the high side and low side MOSFETs are turned off. The device continues its operation when the junction temperature falls below the thermal shutdown hysteresis.

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8.4 Device Functional Modes

8.4.1 Soft-Start

The TPS6226x has an internal soft start circuit that controls the ramp up of the output voltage. The output voltage ramps up from 5% to 95% of its nominal value within typical 250 µs. This limits the inrush current in the converter during ramp up and prevents possible input voltage drops when a battery or high impedance power source is used. The soft start circuit is enabled within the start up time $t_{Start\ Up}$.

8.4.2 Power Save Mode

The power save mode is enabled with MODE pin set to low level. If the load current decreases, the converter will enter power save mode operation automatically. During power save mode the converter skips switching and operates with reduced frequency in PFM mode with a minimum quiescent current to maintain high efficiency. The converter will position the output voltage typically +1% above the nominal output voltage. This voltage positioning feature minimizes voltage drops caused by a sudden load step.

The transition from PWM mode to PFM mode occurs once the inductor current in the low side MOSFET switch becomes zero, which indicates discontinuous conduction mode.

During the power save mode the output voltage is monitored with a PFM comparator. As the output voltage falls below the PFM comparator threshold of V_{OUT} nominal +1%, the device starts a PFM current pulse. The high side MOSFET switch will turn on, and the inductor current ramps up. After the on-time expires, the switch is turned off and the low side MOSFET switch is turned on until the inductor current becomes zero.

The converter effectively delivers a current to the output capacitor and the load. If the load is below the delivered current, the output voltage will rise. If the output voltage is equal to or higher than the PFM comparator threshold, the device stops switching and enters a sleep mode with typical 15-µA current consumption.

If the output voltage is still below the PFM comparator threshold, a sequence of further PFM current pulses are generated until the PFM comparator threshold is reached. The converter starts switching again once the output voltage drops below the PFM comparator threshold.

With a fast single threshold comparator, the output voltage ripple during PFM mode operation can be kept small. The PFM pulse is time controlled, which allows to modify the charge transferred to the output capacitor by the value of the inductor. The resulting PFM output voltage ripple and PFM frequency depend in first order on the size of the output capacitor and the inductor value. Increasing output capacitor values and inductor values will minimize the output ripple. The PFM frequency decreases with smaller inductor values and increases with larger values.

The PFM mode is left and PWM mode entered in case the output current can not longer be supported in PFM mode. The power save mode can be disabled through the MODE pin set to high. The converter will then operate in fixed frequency PWM mode.

8.4.3 100% Duty Cycle Low Dropout Operation

The device starts to enter 100% duty cycle mode once the input voltage comes close to the nominal output voltage. In order to maintain the output voltage, the high side MOSFET switch is turned on 100% for one or more cycles.

With further decreasing V_{IN} the high side MOSFET switch is turned on completely. In this case the converter offers a low input-to-output voltage difference. This is particularly useful in battery-powered applications to achieve longest operation time by taking full advantage of the whole battery voltage range.

The minimum input voltage to maintain regulation depends on the load current and output voltage, and can be calculated as:

$$V_{IN}min = V_{OUT}max + I_{OUT}max \times (R_{DS(on)}max + R_L)$$

where

- I_{OUT}max = Maximum output current plus inductor ripple current
- $R_{DS(on)}$max = Maximum P-channel switch $R_{DS(on)}$
- R_L = DC resistance of the inductor
- V_{OUT}max = Nominal output voltage plus maximum output voltage tolerance (1)

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Device Functional Modes (continued)

8.4.4 Short-Circuit Protection

The high side and low side MOSFET switches are short-circuit protected with maximum switch current equal to I_{LIMF}. The current in the switches is monitored by current limit comparators. Once the current in the high side MOSFET switch exceeds the threshold of its current limit comparator, it turns off and the low side MOSFET switch is activated to ramp down the current in the inductor and high side MOSFET switch. The high side MOSFET switch can only turn on again, once the current in the low side MOSFET switch has decreased below the threshold of its current limit comparator.

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS6226x device is a high-efficiency synchronous step-down DC/DC converter featuring power save mode or 2.25 MHz fixed frequency operation.

9.2 Typical Application

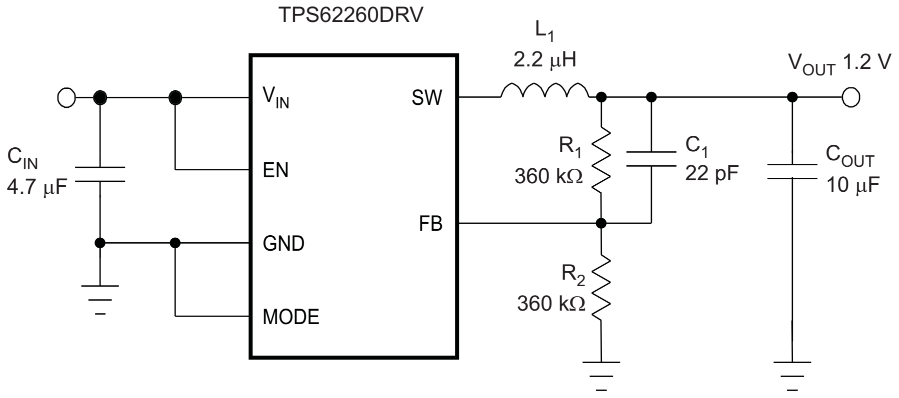

Figure 6. TPS62260DRV Adjustable 1.2-V Output

9.2.1 Design Requirements

The device operates over an input voltage range from 2 V to 6 V. The output voltage is adjustable using an external feedback divider.

9.2.2 Detailed Design Procedure

Table 1. List of Components

COMPONENT REFERENCE	PART NUMBER	MANUFACTURER	VALUE
C_{IN}	GRM188R60J475K	Murata	4.7 µF, 6.3 V. X5R Ceramic
C_{OUT}	GRM188R60J106M	Murata	10 µF, 6.3 V. X5R Ceramic
C_1		Murata	22 pF, COG Ceramic
L_1	LPS3015	Coilcraft	2.2 µH, 110 mΩ
R_1, R_2	Values depending on the programmed output voltage		

9.2.2.1 Output Voltage Setting

The output voltage can be calculated to:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_1}{R_2}\right)$$ with an internal reference voltage V_{REF} typical 0.6 V.

To minimize the current through the feedback divider network, R_2 should be 180 kΩ or 360 kΩ. The sum of R_1 and R_2 should not exceed ~1 MΩ, to keep the network robust against noise.

An external feed forward capacitor C_1 is required for optimum load transient response. The value of C_1 should be in the range between 22 pF and 33 pF.

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Route the FB line away from noise sources, such as the inductor or the SW line.

9.2.2.2 Output Filter Design (Inductor and Output Capacitor)

The TPS6226x is designed to operate with inductors in the range of 1.5 µH to 4.7 µH and with output capacitors in the range of 4.7 µF to 22 µF. The part is optimized for operation with a 2.2-µH inductor and 10-µF output capacitor.

Larger or smaller inductor values can be used to optimize the performance of the device for specific operation conditions. For stable operation, the L and C values of the output filter may not fall below 1-µH effective inductance and 3.5-µF effective capacitance.

Selecting larger capacitors is less critical because the corner frequency of the L-C filter moves to lower frequencies with fewer stability problems.

9.2.2.2.1 Inductor Selection

The inductor value has a direct effect on the ripple current. The selected inductor has to be rated for its DC resistance and saturation current. The inductor ripple current (ΔI_L) decreases with higher inductance and increases with higher V_{IN} or V_{OUT}.

The inductor selection also has an impact on the output voltage ripple in the PFM mode. Higher inductor values will lead to lower output voltage ripple and higher PFM frequency, lower inductor values will lead to a higher output voltage ripple but lower PFM frequency.

Equation 2 calculates the maximum inductor current in PWM mode under static load conditions. The saturation current of the inductor should be rated higher than the maximum inductor current as calculated with Equation 3. This is recommended because during heavy load transient the inductor current will rise above the calculated value.

$$\Delta I_L = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f}$$

where

- f = Switching frequency (2.25-MHz typical)
- L = Inductor value
- ΔI_L = Peak-to-peak inductor ripple current (2)

$$I_L \max = I_{OUT} \max + \frac{\Delta I_L}{2}$$

where

- ΔI_L = Peak-to-peak inductor ripple current
- I_{Lmax} = Maximum inductor current (3)

A more conservative approach is to select the inductor current rating just for the maximum switch current limit I_{LIMF} of the converter.

Accepting larger values of ripple current allows the use of lower inductance values, but results in higher output voltage ripple, greater core losses, and lower output current capability.

The total losses of the coil have a strong impact on the efficiency of the DC/DC conversion and consist of both the losses in the dc resistance ($R_{(DC)}$) and the following frequency-dependent components:

- The losses in the core material (magnetic hysteresis loss, especially at high switching frequencies)
- Additional losses in the conductor from the skin effect (current displacement at high frequencies)
- Magnetic field losses of the neighboring windings (proximity effect)
- Radiation losses

Table 2. List of Inductors

DIMENSIONS [mm^3]	Inductance µH	INDUCTOR TYPE	SUPPLIER
2.5 × 2.0 × 1.0 max	2.0	MIPS2520D2R2	FDK
2.5 × 2.0 ×1.2 max	2.0	MIPSA2520D2R2	FDK
2.5 × 2.0 × 1.0 max	2.2	KSLI-252010AG2R2	Htachi Metals
2.5 ×2.0 × 1.2 max	2.2	LQM2HPN2R2MJ0L	Murata
3 × 3 × 1.5 max	2.2	LPS3015 2R2	Coilcraft

9.2.2.2.2 Output Capacitor Selection

The advanced fast-response voltage mode control scheme of the TPS6226x allows the use of tiny ceramic capacitors. Ceramic capacitors with low ESR values have the lowest output voltage ripple and are recommended. The output capacitor requires either an X7R or X5R dielectric. Y5V and Z5U dielectric capacitors, aside from their wide variation in capacitance over temperature, become resistive at high frequencies.

At nominal load current, the device operates in PWM mode and the RMS ripple current is calculated as:

$$I_{RMSC_{OUT}} = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f} \times \frac{1}{2 \times \sqrt{3}} \tag{4}$$

At nominal load current, the device operates in PWM mode and the overall output voltage ripple is the sum of the voltage spike caused by the output capacitor ESR plus the voltage ripple caused by charging and discharging the output capacitor:

$$\Delta V_{OUT} = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f} \times \left(\frac{1}{8 \times C_{OUT} \times f} + ESR \right) \tag{5}$$

At light load currents, the converter operates in power save mode and the output voltage ripple is dependent on the output capacitor and inductor value. Larger output capacitor and inductor values minimize the voltage ripple in PFM mode and tighten DC output accuracy in PFM mode.

9.2.2.2.3 Input Capacitor Selection

An input capacitor is required for best input voltage filtering, and minimizing the interference with other circuits caused by high input voltage spikes. For most applications, a 4.7-µF to 10-µF ceramic capacitor is recommended. Because ceramic capacitor loses up to 80% of its initial capacitance at 5 V, it is recommended that 10-µF input capacitors be used for input voltages >4.5 V. The input capacitor can be increased without any limit for better input voltage filtering. Take care when using only small ceramic input capacitors. When a ceramic capacitor is used at the input and the power is being supplied through long wires, such as from a wall adapter, a load step at the output or V_{IN} step on the input can induce ringing at the VIN pin. This ringing can couple to the output and be mistaken as loop instability or could even damage the part by exceeding the maximum ratings.

Table 3. List of Capacitors

CAPACITANCE	TYPE	SIZE	SUPPLIER
4.7 µF	GRM188R60J475K	0603 1.6 × 0.8 × 0.8 mm^3	Murata
10 µF	GRM188R60J106M69D	0603 1.6 × 0.8 × 0.8 mm^3	Murata

Table 1 shows the list of components for the *Application Curves*.

9.2.3 Application Curves

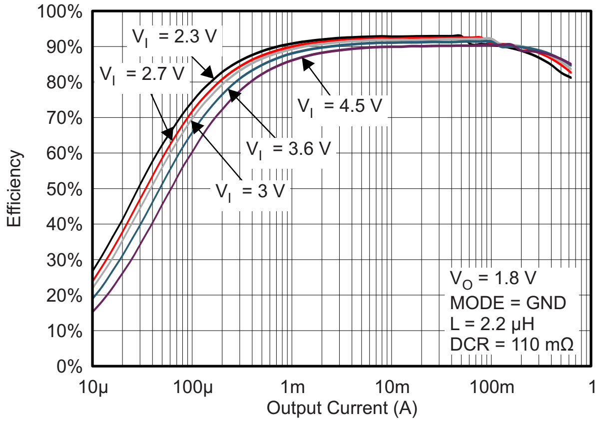

Figure 7. Efficiency (Power Save Mode) vs Output Current

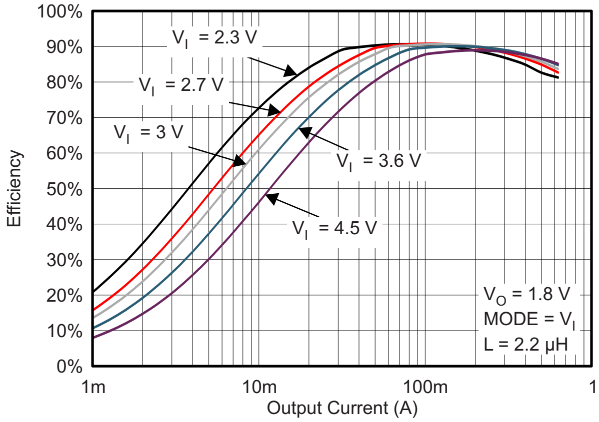

Figure 8. Efficiency (PWM Mode) vs Output Current

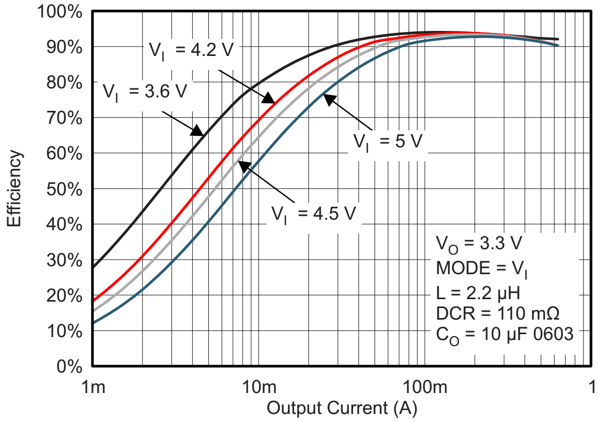

Figure 9. Efficiency (PWM Mode) vs Output Current

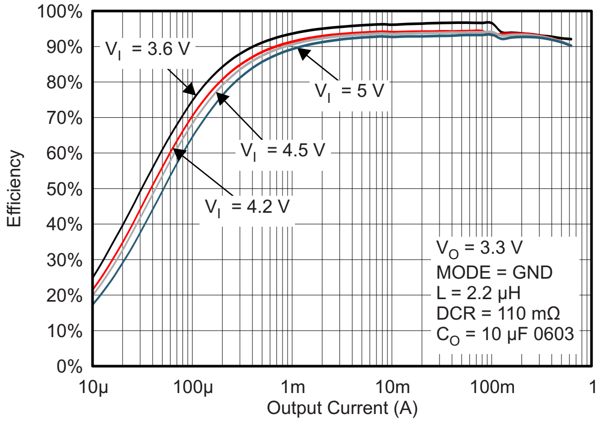

Figure 10. Efficiency (Power Save Mode) vs Output Current

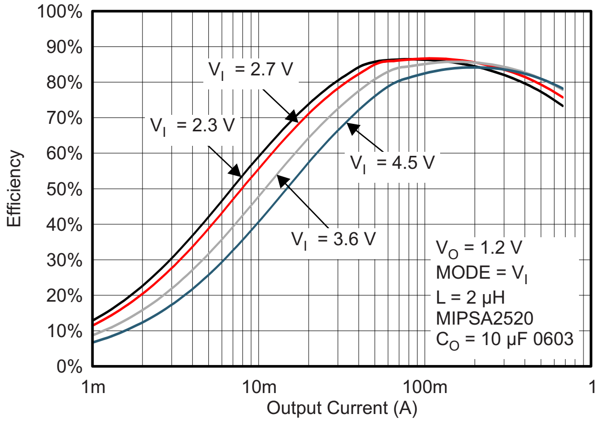

Figure 11. Efficiency vs Output Current

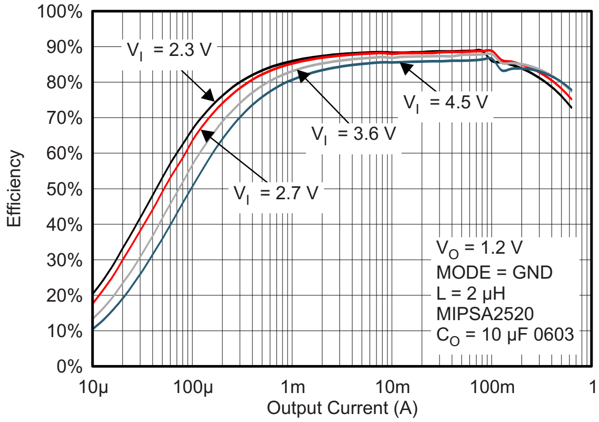

Figure 12. Efficiency vs Output Current

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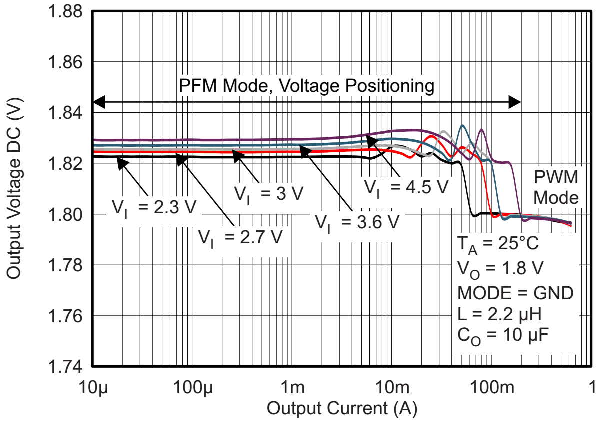

Figure 13. Output Voltage Accuracy vs Output Current

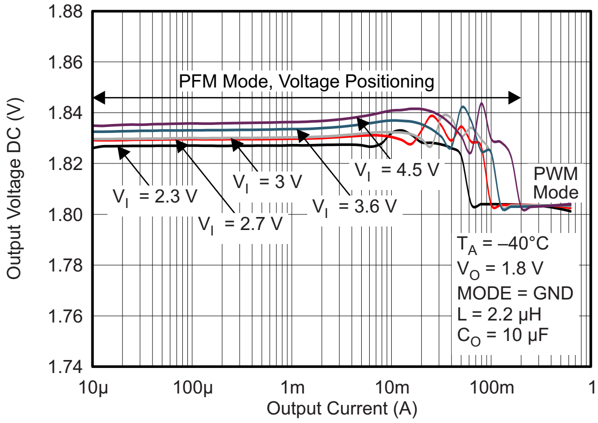

Figure 14. Output Voltage Accuracy (Power Save Mode) vs Output Current

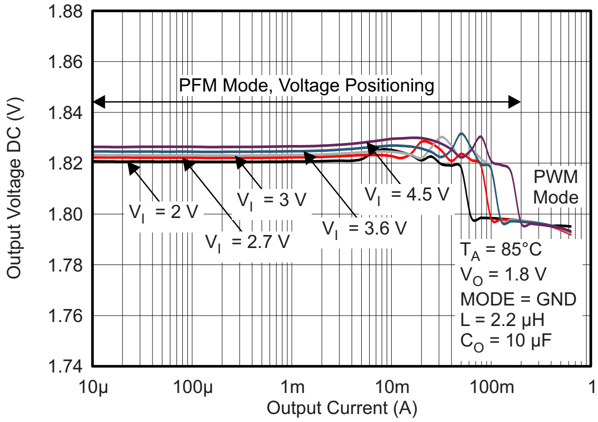

Figure 15. Output Voltage Accuracy (Power Save Mode) vs Output Current

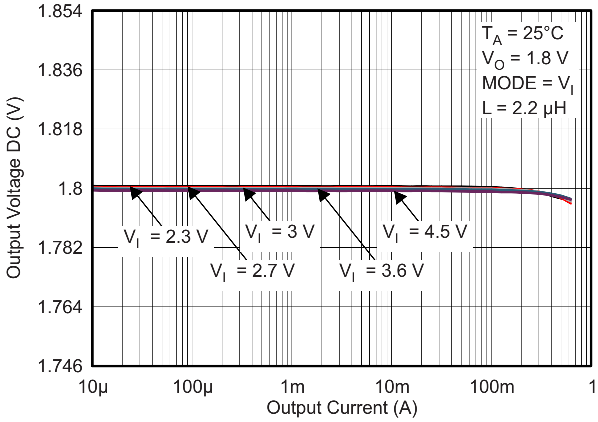

Figure 16. Output Voltage Accuracy (PWM Mode) vs Output Current

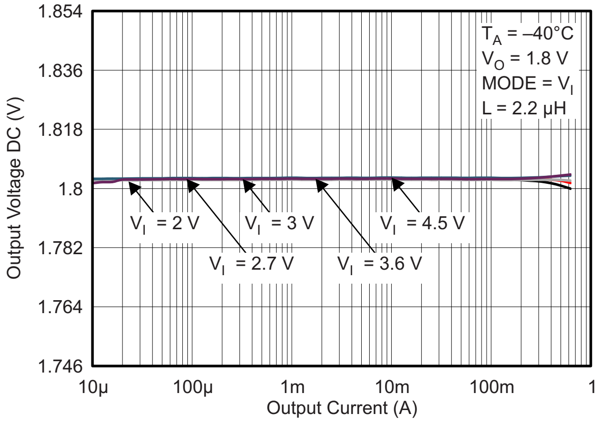

Figure 17. Output Voltage Accuracy (PWM Mode) vs Output Current

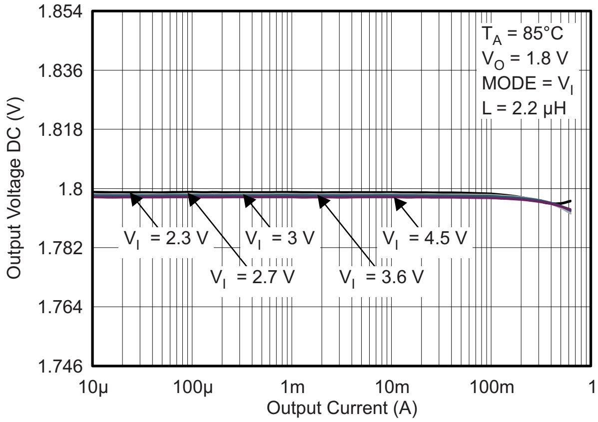

Figure 18. Output Voltage Accuracy (PWM Mode) vs Output Current

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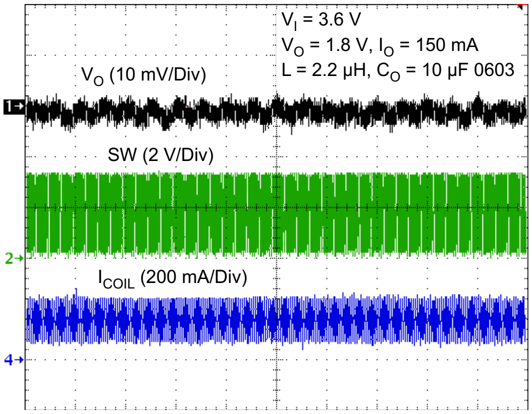

Figure 19. Typical Operation (PWM Mode)

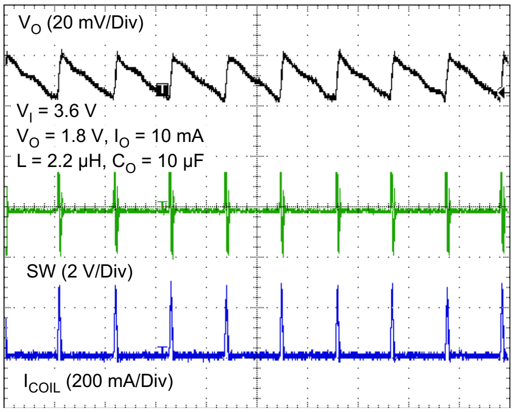

Figure 20. Typical Operation (PFM Mode)

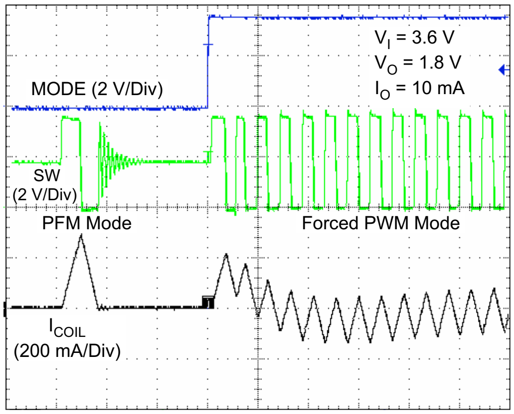

Figure 21. Mode Pin Transition from PFM to Forced PWM Mode at Light Load

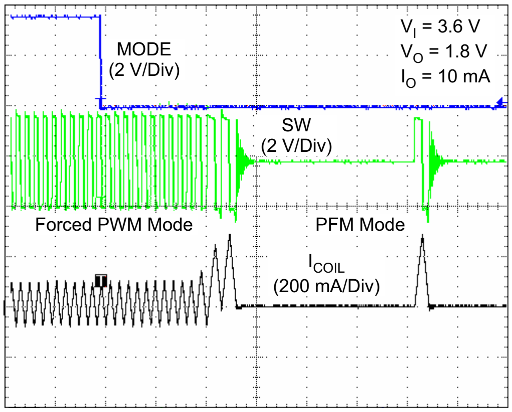

Figure 22. Mode Pin Transition from PWM to PFM Mode at Light Load

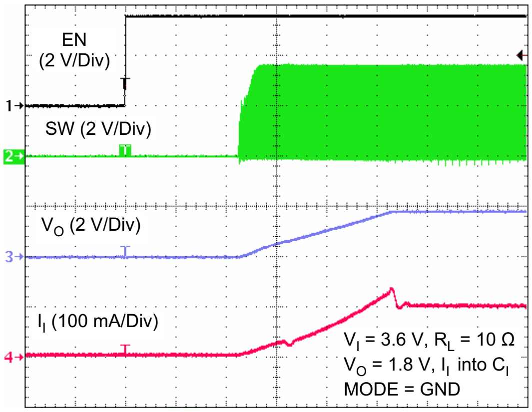

Figure 23. Start-Up Timing

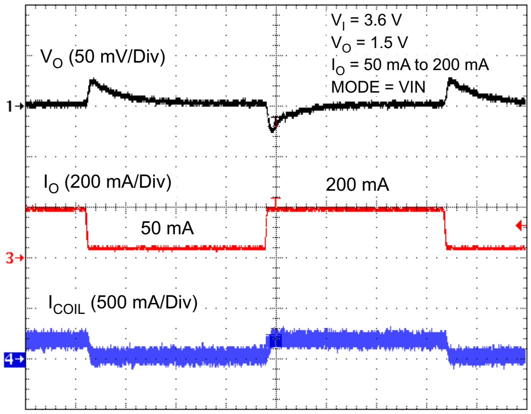

Figure 24. Load Transient (Forced PWM Mode)

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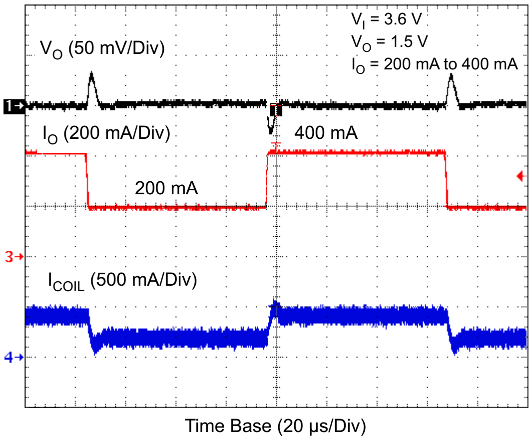

Figure 25. Load Transient (Forced PWM Mode)

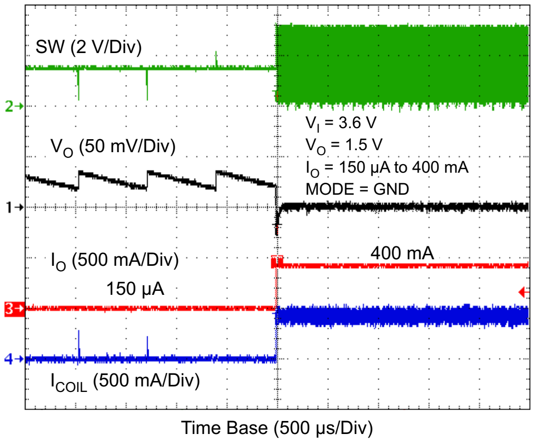

Figure 26. Load Transient (PFM Mode to PWM Mode)

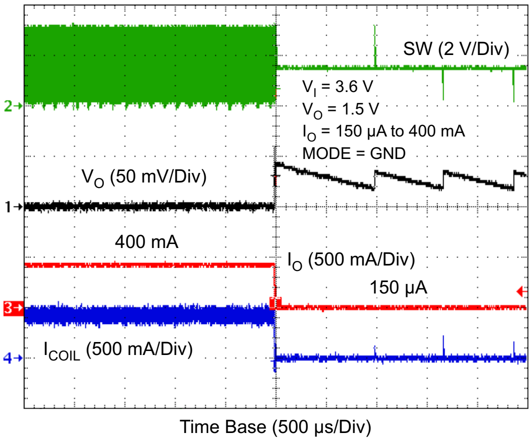

Figure 27. Load Transient (PWM Mode to PFM Mode)

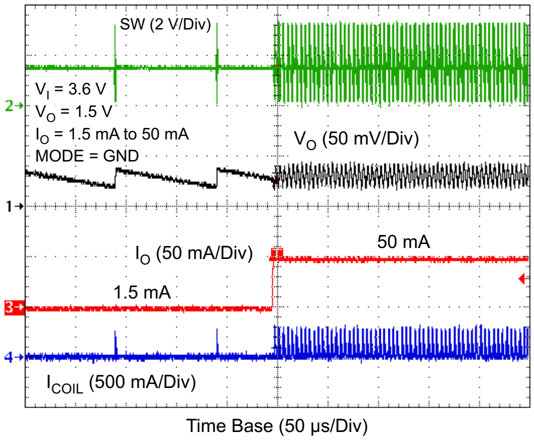

Figure 28. Load Transient (PFM Mode)

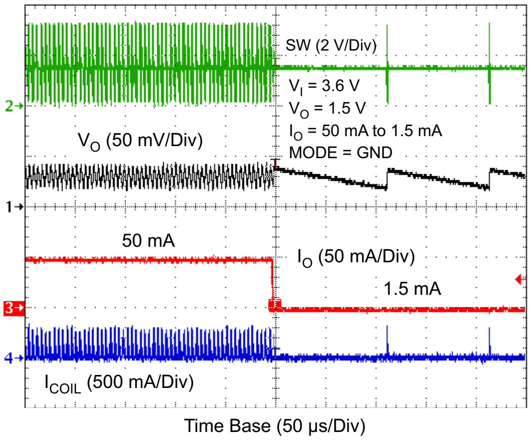

Figure 29. Load Transient (PFM Mode)

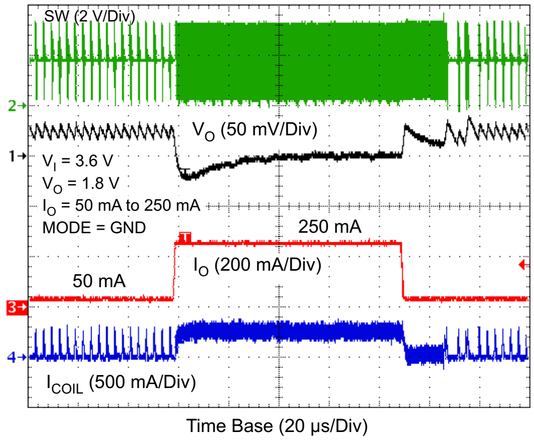

Figure 30. Load Transient (PFM Mode to PWM Mode)

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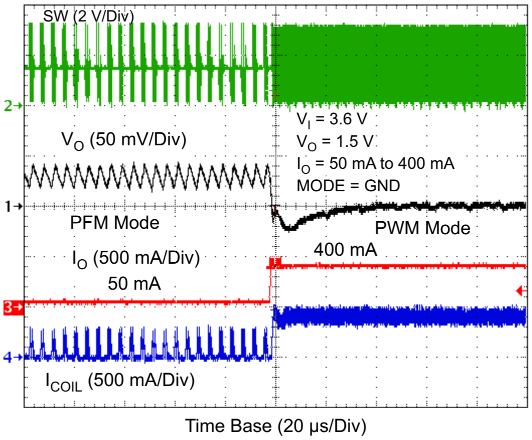

Figure 31. Load Transient (PFM Mode to PWM Mode)

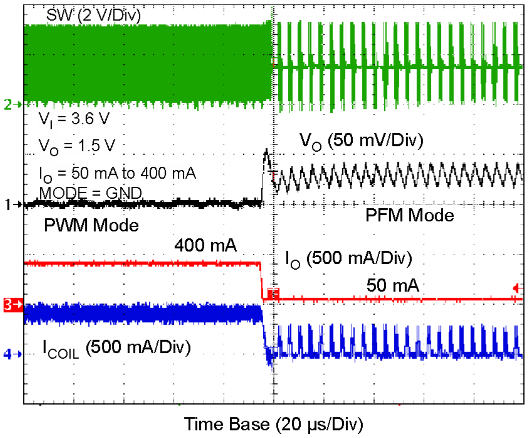

Figure 32. Load Transient (PWM Mode to PFM Mode)

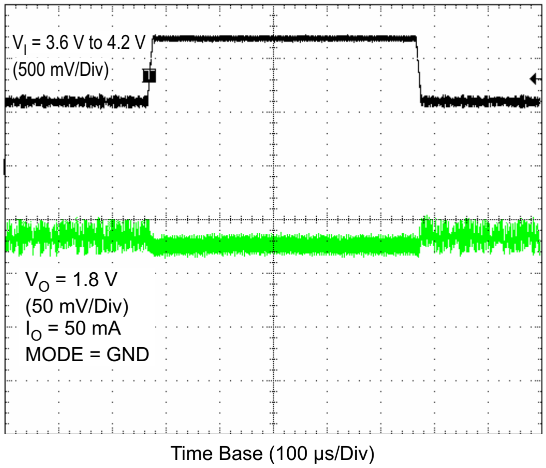

Figure 33. Line Transient (PFM Mode)

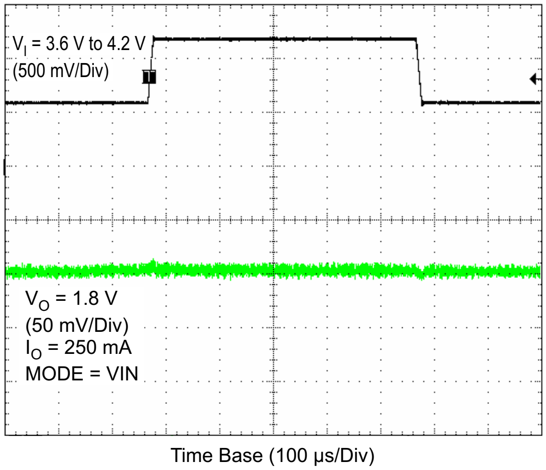

Figure 34. Line Transient (Forced PWM Mode)

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9.3 System Examples

9.3.1 TPS62260, Adjustable 1.5-V Output

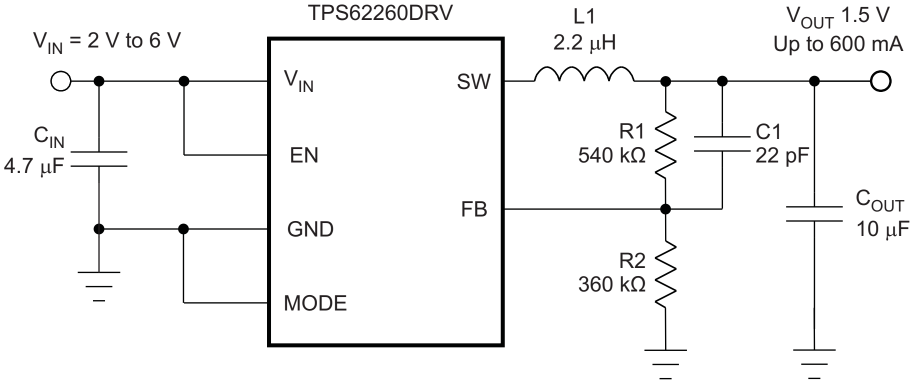

Figure 35. TPS62260 Adjustable 1.5-V Output

9.3.2 TPS62262, Fixed 1.2-V Output

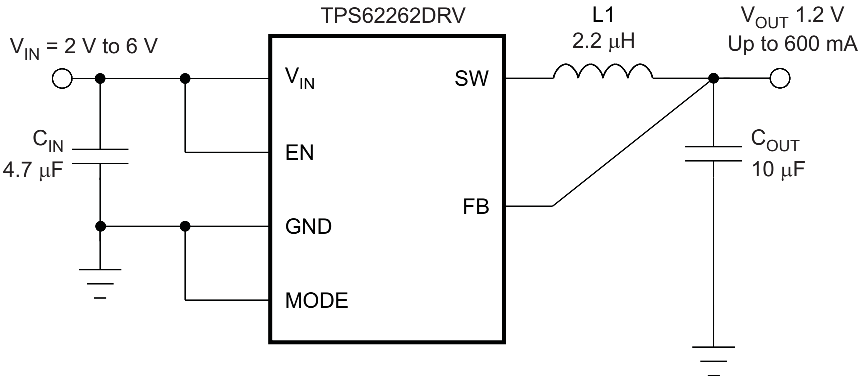

Figure 36. TPS62262 Fixed 1.2-V Output

9.3.3 TPS62261, Fixed 1.8-V Output

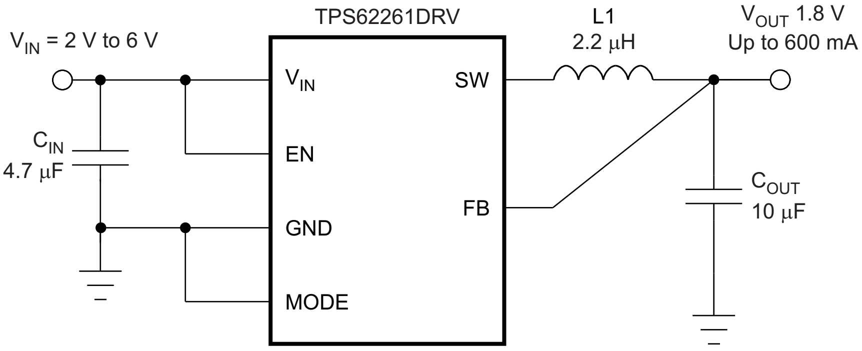

Figure 37. TPS62261 Fixed 1.8-V Output

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10 Power Supply Recommendations

The TPS6226x device has no special requirements for its input power supply. The input power supply output current must be rated according to the supply voltage, output voltage, and output current of the TPS6226x.

11 Layout

11.1 Layout Guidelines

As for all switching power supplies, the layout is an important step in the design. Proper function of the device demands careful attention to PCB layout. Care must be taken in board layout to get the specified performance. If the layout is not carefully done, the regulator could show poor line and/or load regulation, and additional stability issues as well as EMI problems. It is critical to provide a low inductance, impedance ground path. Therefore, use wide and short traces for the main current paths. The input capacitor should be placed as close as possible to the IC pins as well as the inductor and output capacitor.

Connect the GND pin of the device to the PowerPAD™ land of the PCB and use this pad as a star point. Use a common power GND node and a different node for the signal GND to minimize the effects of ground noise. Connect these ground nodes together to the PowerPAD land (star point) underneath the IC. Keep the common path to the GND pin, which returns the small signal components and the high current of the output capacitors as short as possible to avoid ground noise. The FB line should be connected right to the output capacitor and routed away from noisy components and traces (for example, the SW line).

11.2 Layout Examples

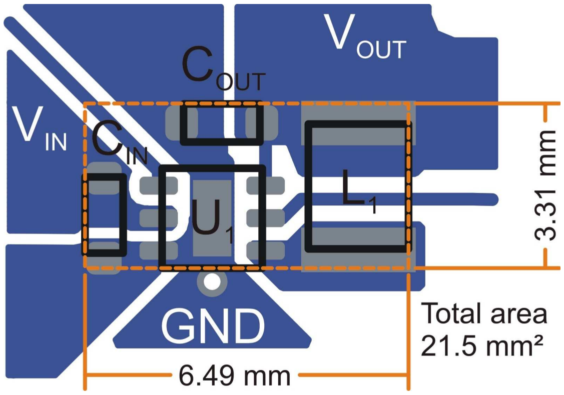

Figure 38. Suggested Layout for Fixed Output Voltage Options

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Layout Examples (continued)

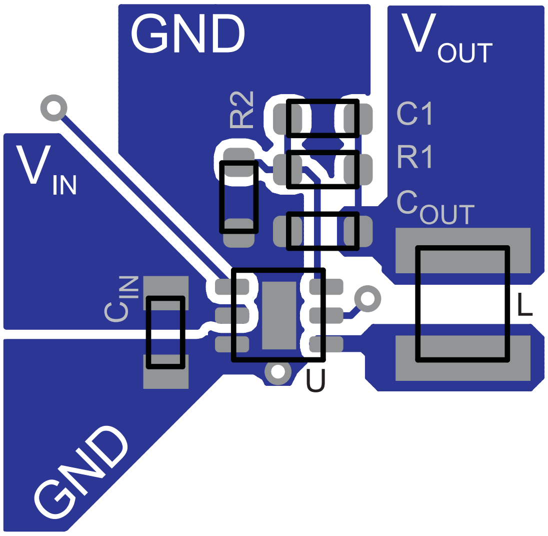

Figure 39. Suggested Layout for Adjustable Output Voltage Version

12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 4. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS62260	Click here	Click here	Click here	Click here	Click here
TPS62261	Click here	Click here	Click here	Click here	Click here
TPS62262	Click here	Click here	Click here	Click here	Click here
TPS62263	Click here	Click here	Click here	Click here	Click here

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS62260DDCR	ACTIVE	SOT-23-THIN	DDC	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BYP	Samples
TPS62260DDCRG4	ACTIVE	SOT-23-THIN	DDC	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BYP	Samples
TPS62260DDCT	ACTIVE	SOT-23-THIN	DDC	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BYP	Samples
TPS62260DDCTG4	ACTIVE	SOT-23-THIN	DDC	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BYP	Samples
TPS62260DRVR	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	BYK	Samples
TPS62260DRVT	ACTIVE	WSON	DRV	6	250	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	BYK	Samples
TPS62260DRVTG4	ACTIVE	WSON	DRV	6	250	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	BYK	Samples
TPS62261DRVR	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BYL	Samples
TPS62261DRVT	ACTIVE	WSON	DRV	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BYL	Samples
TPS62262DDCR	ACTIVE	SOT-23-THIN	DDC	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	QXS	Samples
TPS62262DDCT	ACTIVE	SOT-23-THIN	DDC	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	QXS	Samples
TPS62262DRVR	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	BYM	Samples
TPS62262DRVT	ACTIVE	WSON	DRV	6	250	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	BYM	Samples
TPS62263DRVR	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CFX	Samples
TPS62263DRVT	ACTIVE	WSON	DRV	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CFX	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS62260, TPS62261, TPS62262, TPS62263 :

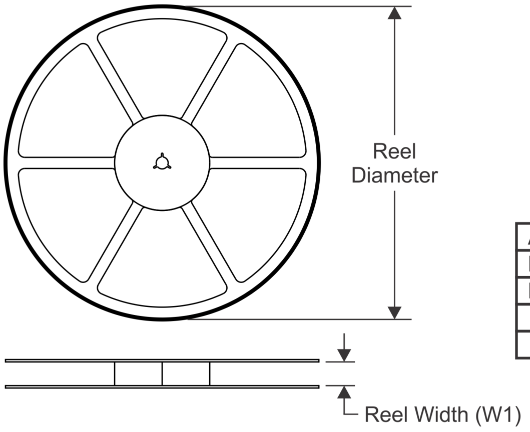
- Automotive: TPS62260-Q1, TPS62261-Q1, TPS62262-Q1, TPS62263-Q1

NOTE: Qualified Version Definitions:

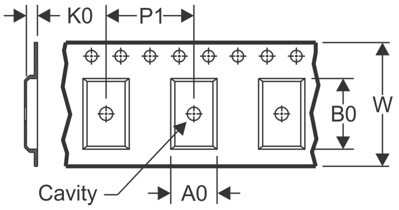
  - Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

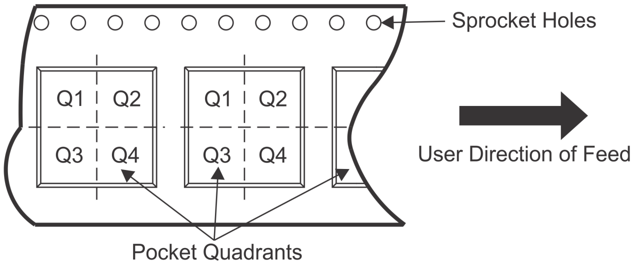


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

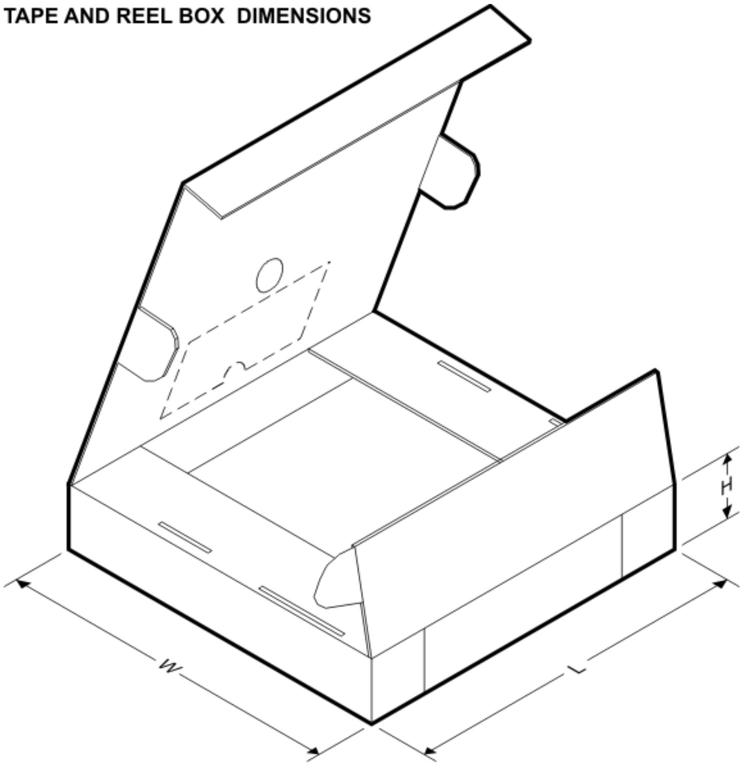
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS62260DDCR	SOT-23-THIN	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS62260DDCT	SOT-23-THIN	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS62261DRVR	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS62262DDCR	SOT-23-THIN	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS62262DDCT	SOT-23-THIN	DDC	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS62262DRVR	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS62262DRVT	WSON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS62263DRVR	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS62263DRVT	WSON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2

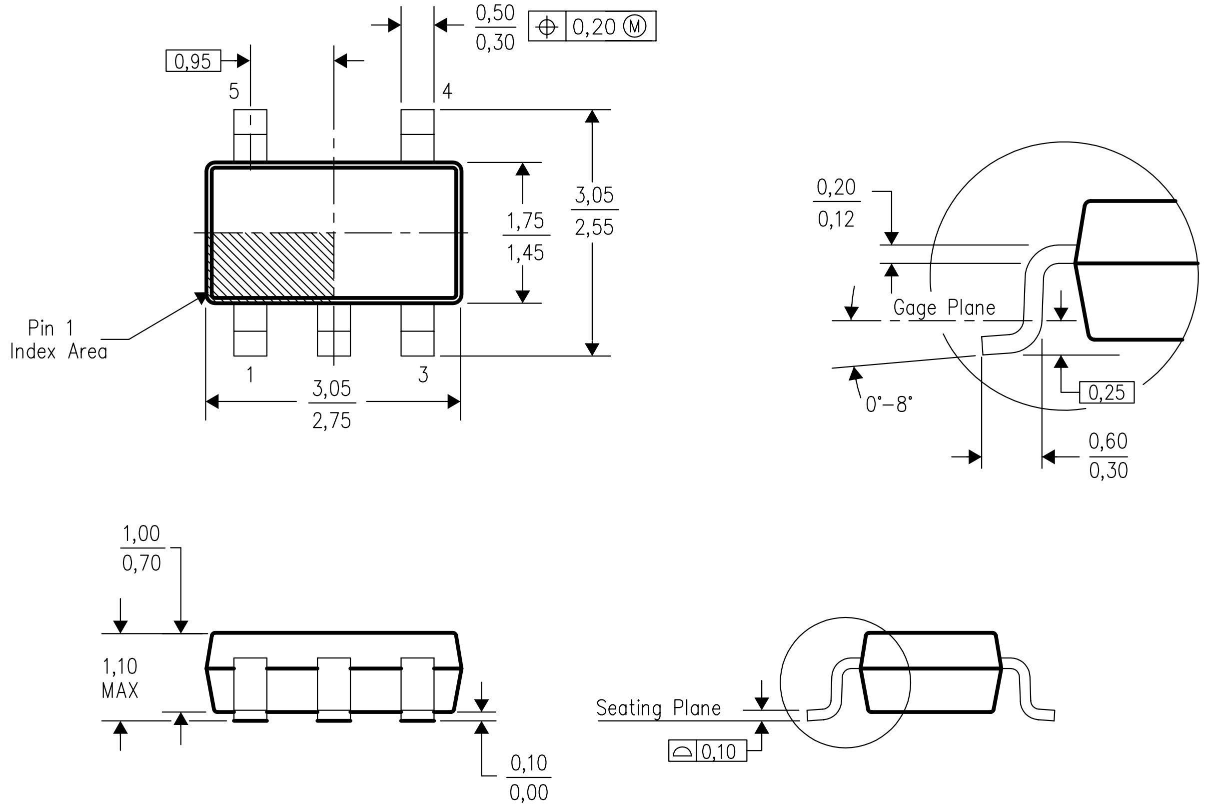
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS62260DDCR	SOT-23-THIN	DDC	5	3000	200.0	183.0	25.0
TPS62260DDCT	SOT-23-THIN	DDC	5	250	200.0	183.0	25.0
TPS62261DRVR	WSON	DRV	6	3000	200.0	183.0	25.0
TPS62262DDCR	SOT-23-THIN	DDC	5	3000	200.0	183.0	25.0
TPS62262DDCT	SOT-23-THIN	DDC	5	250	200.0	183.0	25.0
TPS62262DRVR	WSON	DRV	6	3000	200.0	183.0	25.0
TPS62262DRVT	WSON	DRV	6	250	200.0	183.0	25.0
TPS62263DRVR	WSON	DRV	6	3000	200.0	183.0	25.0
TPS62263DRVT	WSON	DRV	6	250	200.0	183.0	25.0

DDC (R–PDSO–G5) PLASTIC SMALL–OUTLINE



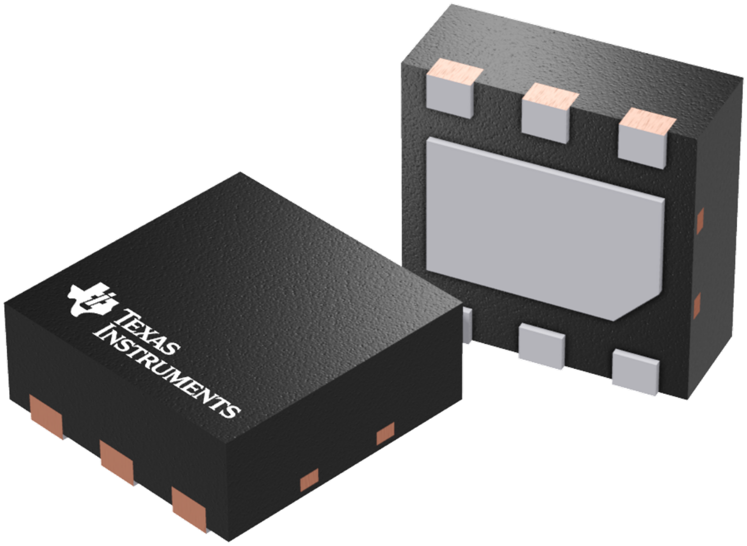
4204403–2/E 06/05

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion.
- D. Falls within JEDEC MO–193 variation AB (5 pin).

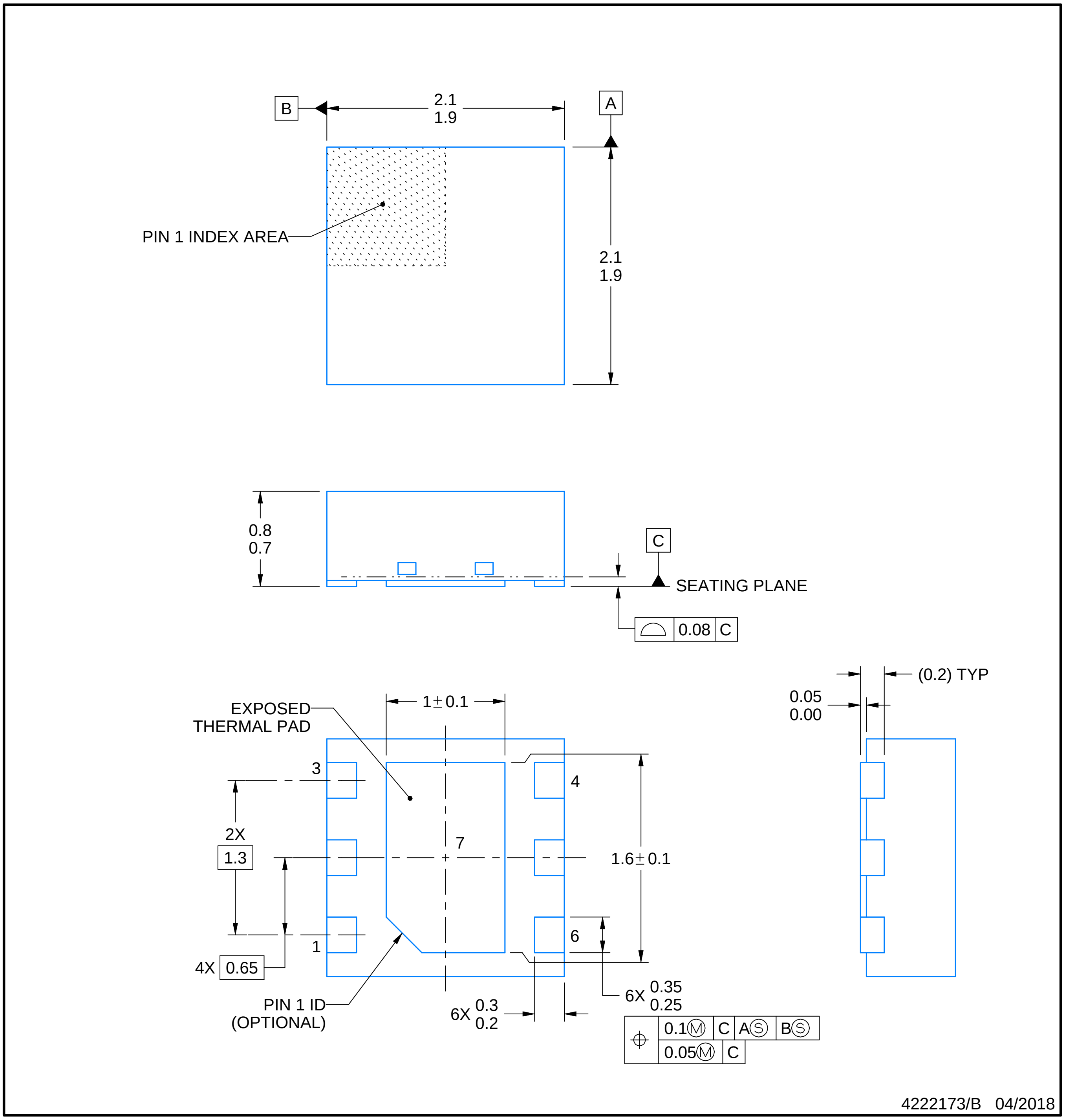
GENERIC PACKAGE VIEW

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

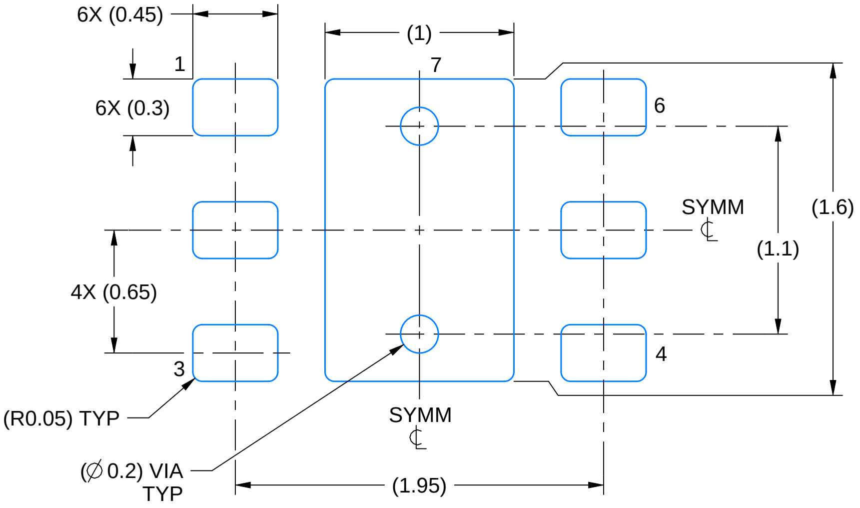


Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

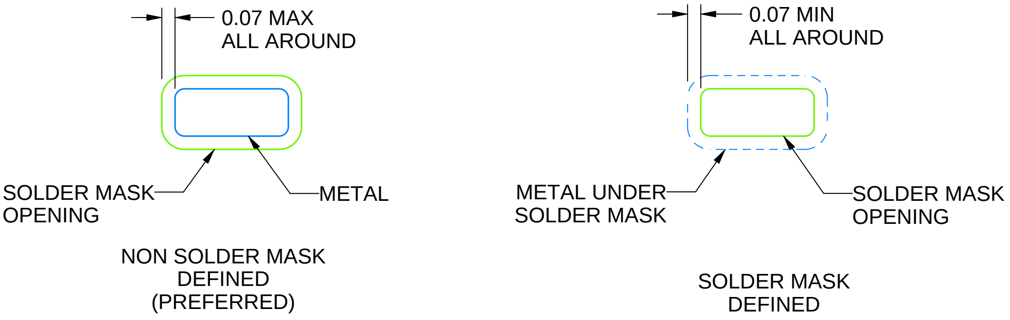


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:25X

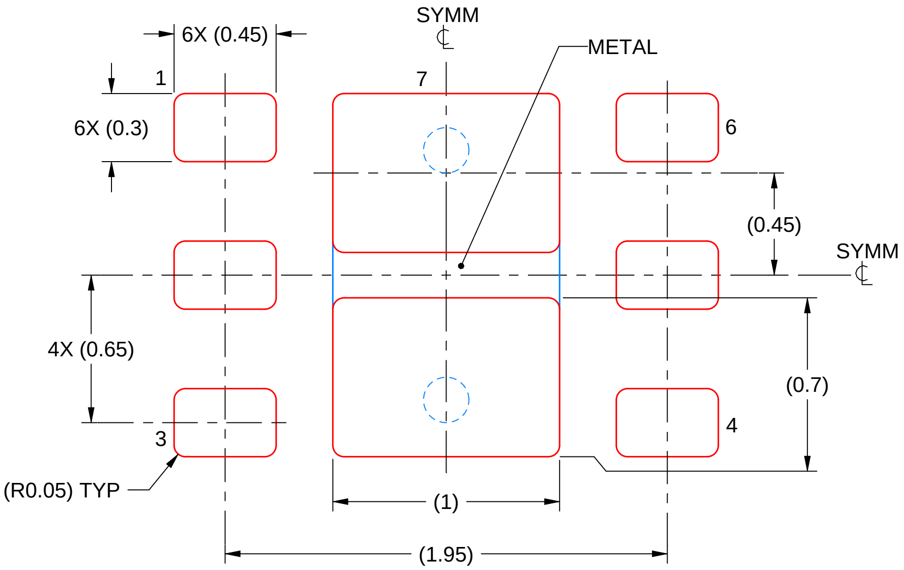


SOLDER MASK DETAILS

4222173/B 04/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



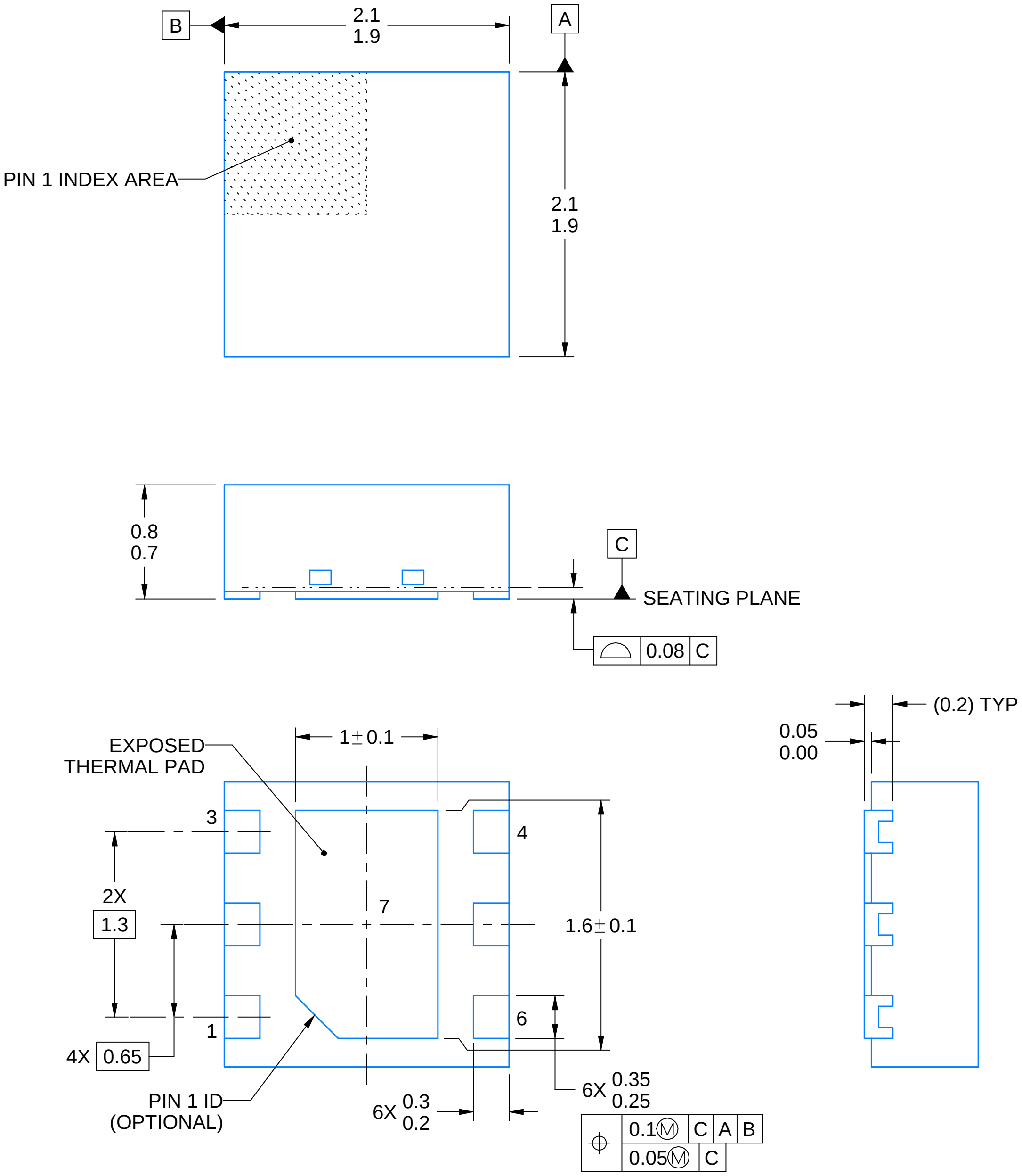
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

4222173/B 04/2018

NOTES: (continued)

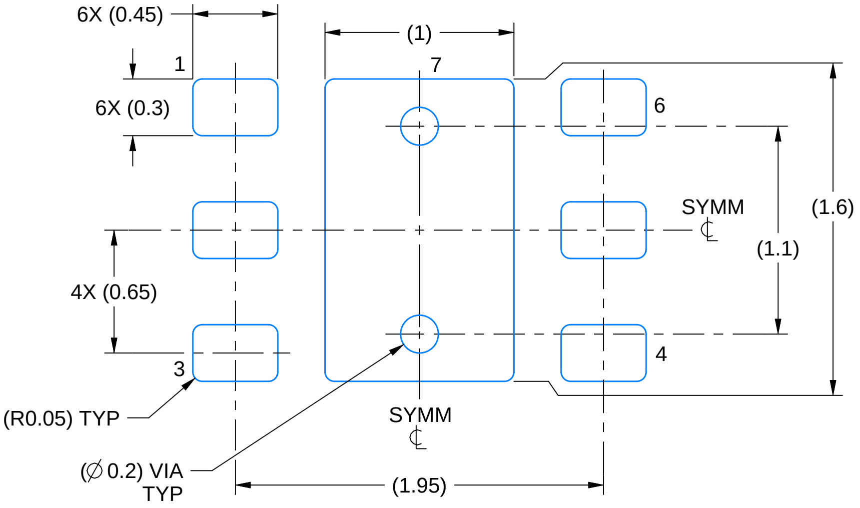
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



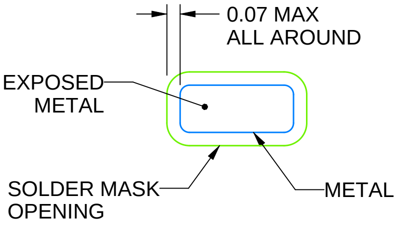
4225563/A 12/2019

NOTES:

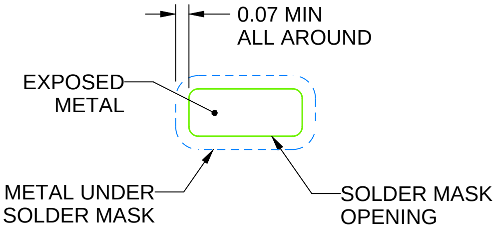
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:25X



NON SOLDER MASK
DEFINED
(PREFERRED)

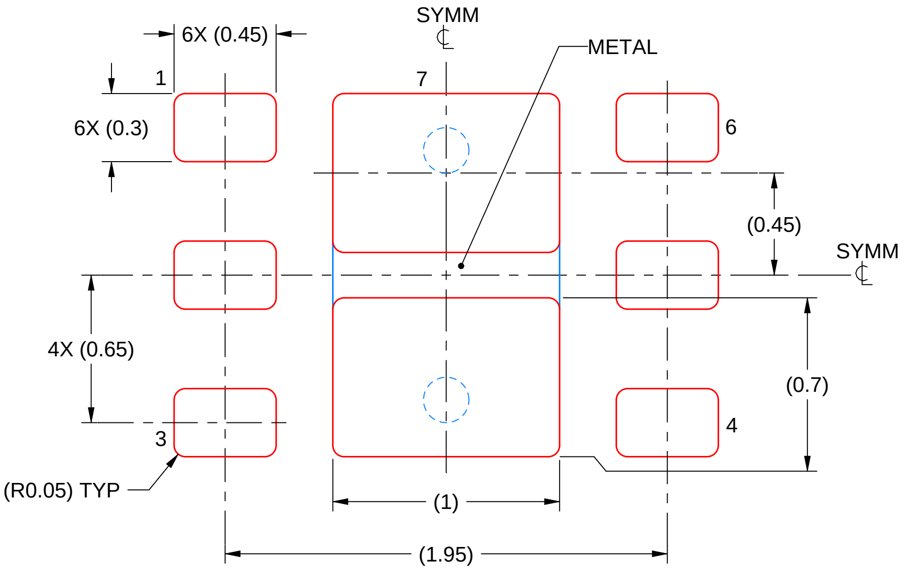


SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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