36 Channel Fuel Cell Monitor

FEATURES

- **36 Measurement Channels Monitor up to 144 Fuel Cells in Series**
- **Channel Measurement Range: ±5V**
- **Cell Stack Voltage Range: –80V to 150V**
- **Operates from a Single 5V Supply**
- **Stackable Architecture Supports Large Fuel Cell Stacks**
- Built-In isoSPI™ Interface
  - 1MB/s Isolated Serial Communications
  - Uses a Single Twisted Pair, Up to 100 Meters
  - Low EMI Susceptibility and Emissions
  - Bidirectional for Broken Wire Protection
- 15mV Total Measurement Error
- 6.75ms to Measure All Cells in a System
- Delta-Sigma Converter with Built-In Noise Filter
- Six General Purpose Digital I/O or Analog Inputs
  - Temperature or Other Sensor Inputs
- 12µA Sleep Mode Supply Current
- 64-Lead LQFP Package
- AEC-Q100 Qualified for Automotive Applications

APPLICATIONS

- Fuel Cell Electric and Hybrid Electric Vehicles
- Backup Power Systems
- High Power Portable Equipment

DESCRIPTION

The LTC®6806 is a fuel cell monitor that measures up to 144 Series Connected Fuel cells with a total measurement error of less than 15mV. The LTC6806 includes 36 input channels, each with a ±5V measurement range allowing each channel to measure from 1 to 4 series-connected fuel cells.

All 36 inputs can be measured within 6.75ms in fast ADC mode. Lower data acquisition rates can be selected for high noise reduction. In the normal ADC mode, all cells are measured within 10.3ms, with a total measurement error of less than 15mV.

Each LTC6806 has an isoSPI interface for high speed, RF-immune, long distance communications. Two communication modes are available by pin selection: in daisy-chain mode, multiple devices are connected in a daisy chain with one host processor connection for all devices; in parallel mode, multiple devices are connected in parallel to the host processor, with each device individually addressed.

Multiple LTC6806 devices can be connected in series, permitting simultaneous cell monitoring of very large fuel cell stacks. As shown in the typical application, twelve LTC6806s are connected in series to monitor 432 fuel cells. Alternatively, 432 cells can be monitored using six ICs by monitoring groups of two cells, or four ICs by monitoring groups of three cells.

TYPICAL APPLICATION

432 Fuel Cells Monitored by 4, 6 or 12 LTC6806 ICs

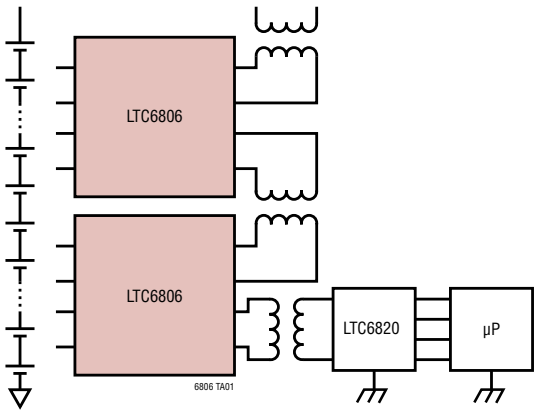


TABLE OF CONTENTS

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Voltage of C Pins Relative to V^- :
- for n = 0 to 12 ..... –60V < C[n] < 75V
- for n = 13 to 24 ..... –60V < C[n] < 105V
- for n = 25 to 36 ..... –80V < C[n] < 150V

Operating Temperature Range: ..... –40°C to 125°C

GPIO Pins 49 to 54 Relative to V^-: ..... –0.3V < Pin Voltage < V^+ + 0.3V

All Other Pins Relative to V^-: ..... –0.3V < Pin Voltage < 6.5V

Current in/out of Pins:
- All pins except for IPA, IMA, IPB, and IMB ..... <10mA
- IPA, IMA, IPB, and IMB ..... <30mA

Specified Junction Temperature Range
- LTC6806I ..... –40°C to 85°C
- LTC6806H ..... –40°C to 125°C

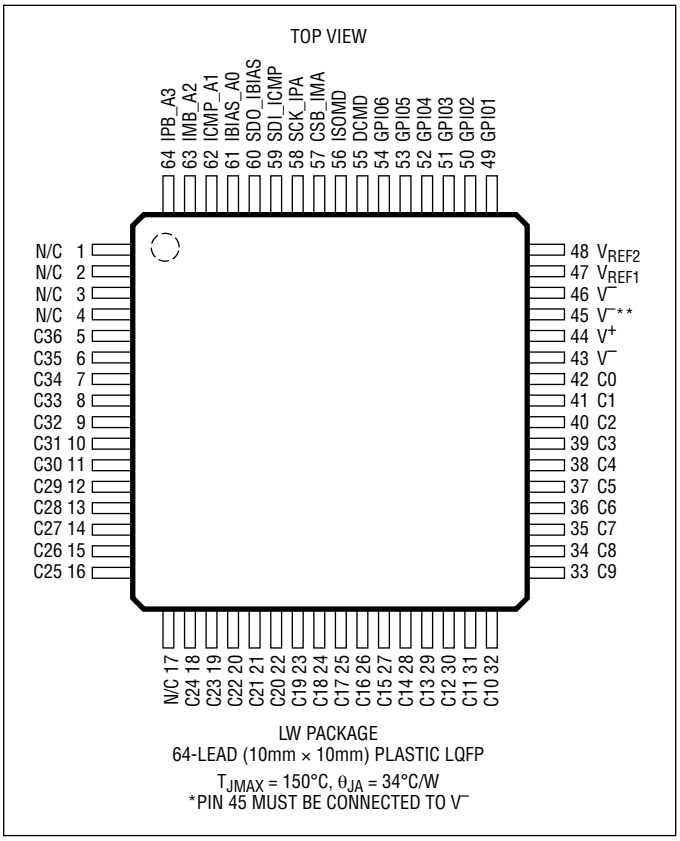
Maximum Junction Temperature ..... 150°C

Storage Temperature Range ..... –65°C to 150°C

Device HBM ESD Classification Level 3A

Device CDM ESD Classification Level C4A

PIN CONFIGURATION



LW PACKAGE
64-LEAD (10mm × 10mm) PLASTIC LQFP

T_{JMAX} = 150°C, θ_{JA} = 34°C/W

*PIN 45 MUST BE CONNECTED TO V^-

ORDER INFORMATION

AUTOMOTIVE PRODUCTS**

TRAY (160PC)	TAPE AND REEL (1500PC)	PART MARKING*	PACKAGE DESCRIPTION	MSL RATING	SPECIFIED JUNCTION TEMPERATURE RANGE
LTC6806ILW#3ZZPBF	LTC6806ILW#3ZZTRPBF	LTC6806LW	64-Lead Plastic LQFP	3	–40°C to 85°C
LTC6806HLW#3ZZPBF	LTC6806HLW#3ZZTRPBF	LTC6806LW	64-Lead Plastic LQFP	3	–40°C to 125°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

**Versions of this part are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. These models are designated with a #3ZZ suffix. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full specified temperature range, otherwise specifications are at T_A = 25°C. The test conditions are V^+ = +5.0V unless otherwise noted. The ISOMD pin is tied to the V^- pin, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
ADC DC Specifications							
	Cell Measurement Range, C(n) to C(n-1)	Cell Measurements with HIRNG = 0 Cell Measurements with HIRNG = 1	● ●	–2.5 –5.0		2.5 5.0	V V
	V^+ Measurement Range (Relative to V^-)		●	4.75		5.5	V
	Other Non-Cell Measurement Range (Relative to V^-)	V^+ = 4.75V V^+ = 5.5V	●	0 0		4.2 5.0	V V
	Cell Measurement Resolution, C(n) to C(n-1)	Cell Measurements with HIRNG = 0 Cell Measurements with HIRNG = 1			1.5 3.0		mV/bit mV/bit
	V^+ Measurement Resolution (Relative to V^-)				1.875		mV/bit
	Other Non-Cell Measurement Resolution (Relative to V^-)				1.5		mV/bit
	ADC Offset Voltage	(Note 2)			1		mV
	ADC Gain Error	(Note 2)			0.2		%
TME.1	Total Measurement Error (TME) of Cell Inputs in Alternate/Filtered Modes, with HIRNG = 0 (Notes 7, 8, and 9)	C(n) to C(n-1) = 0V, VCx > 0V, 72V Stack C(n) to C(n-1) = 0V, VCx > 0V, 72V Stack	 ●	–12 –20		12 20	mV mV
		C(n) to C(n-1) = ±1.25V, VCx > 0V, 72V Stack C(n) to C(n-1) = ±1.25V, VCx > 0V, 72V Stack	 ●	–15 –20		15 20	mV mV
		C(n) to C(n-1) = ±2.5V, VCx > 0V, 72V Stack C(n) to C(n-1) = ±2.5V, VCx > 0V, 72V Stack	 ●	–19 –24		19 24	mV mV
	Total Measurement Error (TME) of Cell Inputs in Normal Modes, with HIRNG = 0	C(n) to C(n-1) = 0V, VCx > –5V, 72V stack C(n) to C(n-1) = 0V, VCx > –5V, 72V stack	 ●	–18 25		18 25	mV mV
		C(n) to C(n-1) = 0V, VCx > 0V, 72V stack C(n) to C(n-1) = 0V, VCx > 0V, 72V stack	 ●	–15 –20		15 20	mV mV
		C(n) to C(n-1) = ±1.25 V, VCx > 0V, 72V stack C(n) to C(n-1) = ±1.25 V, VCx > 0V, 72V stack	 ●	–17 –20		17 20	mV mV
		C(n) to C(n-1) = ±1.25 V, n=2 to 14, VCx =60V C(n) to C(n-1) = ±1.25 V, n=15 to 25, VCx =95V C(n) to C(n-1) = ±1.25 V, n=26 to 36, VCx =140V	● ● ●	–27 –27 –27		27 27 27	mV mV mV
		C(n) to C(n-1) = ±2.5 V, VCx > –5V, 72V stack C(n) to C(n-1) = ±2.5 V, VCx > –5V, 72V stack	 ●	–28 –35		28 35	mV mV
		C(n) to C(n-1) = ±2.5 V, VCx > 0V, 72V stack C(n) to C(n-1) = ±2.5 V, VCx > 0V, 72V stack	 ●	–22 30		22 30	mV mV
TME.2	Total Measurement Error (TME) of Cell Inputs in Norma/Alternate/Filtered Modes, with HIRNG = 1	C(n) to C(n-1) = 0V, VCx > 0V, 72V stack C(n) to C(n-1) = 0V, VCx > 0V, 72V stack	 ●	–17 –24		17 24	mV mV
		C(n) to C(n-1) = ±5 V, VCx > 0V, 72V stack C(n) to C(n-1) = ±5 V, VCx > 0V, 72V stack	 ●	–34 –40		34 40	mV mV
		C(n) to C(n-1) = +5 V, VCx > –5V, 72V stack	●	–40		40	mV
TME.3	Total Measurement Error (TME) of V^+ (Relative to V^-) in Normal/Alternative/ Filtered Modes		 ●	–55 –65		55 65	mV mV

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full specified temperature range, otherwise specifications are at T_A = 25°C. The test conditions are V^+ = +5.0V unless otherwise noted. The ISOMD pin is tied to the V^- pin, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
TME.4	Total Measurement Error (TME) of GPIO in Normal/Alternative/Filtered Modes	GPIO(n) to V^- = +1.25V GPIO(n) to V^- = +1.25V	 ●	–15 –20		15 20	mV mV
		GPIO(n) to V^- = +2.5V GPIO(n) to V^- = +2.5V	 ●	–25 –32		25 32	mV mV
		GPIO(n) to V^- = +4.2V, V^+ = 4.75V GPIO(n) to V^- = +4.2V, V^+ = 4.75V	 ●	–42 –50		42 50	mV mV
		GPIO(n) to V^- = +5V, V^+ = 5.5V GPIO(n) to V^- = +5V, V^+ = 5.5V	 ●	–42 –50		42 50	mV mV
	Total Measurement Error (TME) of Sum of Cells Normal/Alternate/Filtered Modes	Sum of Cells, VC36 = 150V	●	–1.2		1.2	%
		Sum of Cells, VC36 = 25V	●	–2		2	%
	Total Measurement Error (TME) of Junction Temperature in Normal/Alternate/Filtered Modes				±14.5		°C
	Total Measurement Error (TME) of VREF2 in Normal/Alternative/Filtered Modes		●	–30		30	mV
TME.1F	Total Measurement Error (TME) of Cell Inputs in Fast Mode, with HIRNG = 0	C(n) to C(n-1) = ±1.25 V, VCx > 0V	●	–95		95	mV
		C(n) to C(n-1) = ±2.5 V, VCx > 0V	●	–225		225	mV
		C(n) to C(n-1) = ±2.5 V, VCx > -5V	●	–250		250	mV
TME.3F	Total Measurement Error (TME) of V^+ (Relative to V^-) in Fast Mode		●	–120		120	mV
TME.4F	Total Measurement Error (TME) of GPIO in Fast Mode	GPIO(n) to V^- = +1.25V	●	–55		55	mV
		GPIO(n) to V^- = +2.5V	●	–60		60	mV
		GPIO(n) to V^- = +4.2V, V^+ = 4.75V	●	–90		90	mV
	Total Measurement Error (TME) of Sum of Cells Fast Mode	Sum of Cells, VC36 = 150V	●	–2.5		2.5	%
	Total Measurement Error (TME) of Junction Temperature in Fast Mode				±20		°C
	Total Measurement Error (TME) of VREF2 in Fast Mode				±75		mV
	Input Voltage Range	C0 – C13 to V^-	●	-5		60	V
		C14 – C24 to V^-	●	-5		95	V
		C25 – C36 to V^-	●	-5		140	V
		GPIO(n) = 1 to 6, $V^+ \leq$ 5V	●	0		V^+	V
		GPIO(n) = 1 to 6, V^+ > 5V	●	0		5	V
I_{LM}	Input Leakage Current (I_L) when Inputs Are Being Measured	C(n) n = 0 to 36, $V_{C(n)} - V^-$ > 5V C(n) n = 1 to 36, $V_{C(n)} - V^-$ < 5V GPIO(n) n = 1 to 6		5 –550 5	30 10	60 60 30	µA µA µA
I_{LO}	Input Leakage Current (I_L) when Inputs Are Not Being Measured, in all modes	C(n) n = 0 to 36, $V_{C(n)} - V^-$ > 5V C(n) n = 1 to 36, $V_{C(n)} - V^-$ < 5V GPIO(n) n = 1 to 6	● ● ●	–1.6 –550	0	1.6 0 10	µA µA µA
I_{LS}	Input Leakage Current (I_L) in SLEEP/ STANDBY mode	C(n) n = 0 to 36, $V_{C(n)} - V^-$ > 0V	●	–1.6	0	1.6	µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full specified temperature range, otherwise specifications are at T_A = 25°C. The test conditions are V^+ = +5.0V unless otherwise noted. The ISOMD pin is tied to the V^- pin, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
I_{LOPW}	Additional Input Current During Open Wire Detection (n= 1 to 36)	C(n) to V^- = 0V, n ≠ 13 or 24, pull up current				– 20		µA
		C(n) to V^- = 0V, n = 13 and 24, pull up current				– 40		µA
		C(n) to V^- = 2V, n ≠ 13 or 24, pull up current				– 8		µA
		C(n) to V^- = 2V, n = 13 and 24, pull up current				– 16		µA
		C(n) to V^- = 2V, n ≠ 13 or 24, pull down current				8		µA
		C(n) to V^- = 2V, n = 13 and 24, pull down current				16		µA
		C(n) to V^- = 4V, n ≠ 13 or 24, pull down current				18		µA
		C(n) to V^- = 4V, n = 13 and 24, pull down current				36		µA
		C(n) to V^- ≥ 6V, n ≠ 13 or 24, pull down current		●	4	25	50	µA
		C(n) to V^- ≥ 6V, n = 13 and 24, pull down current		●	4	50	100	µA
Voltage Reference Specifications								
V_{REF1}	1st Reference Voltage	V_{REF1} Pin, No Load		●	2.700	3.060	3.300	V
	1st Reference Voltage TC	V_{REF1} Pin, No Load				10		ppm/°C
	1st Reference Voltage Hysteresis	V_{REF1} Pin, No Load				100		ppm
	1st Reference Voltage Long Term Drift	V_{REF1} Pin, No Load				60		ppm/√khr
V_{REF2}	2nd Reference Voltage	V_{REF2} Pin, No Load V_{REF2} Pin, 1mA Load to V^-		● ●	2.300 2.200	2.500 2.500	2.700 2.700	V V
	2nd Reference Voltage TC	V_{REF2} Pin, No Load				40		ppm/°C
	2nd Reference Voltage Hysteresis	V_{REF2} Pin, No Load				500		ppm
	2nd Reference Voltage Long Term Drift	V_{REF2} Pin, No Load				500		ppm/√khr
General DC Specifications								
I_{V+}	V^+ Supply Current (see Figure 1)	SLEEP Mode, Serial = OFF		●		12	25	µA
		STANDBY Mode, Serial = OFF		●		0.5	0.85	mA
		REFUP Mode, Serial = OFF		●		2.25	3.1	mA
		MEASURE/MONITOR Modes, Serial = OFF		●		4.25	5.75	mA
	Additional V^+ Supply Current if isoSPI in READY/ACTIVE States Note: Active State Current Assumes t_{CLK} = 1µs. (Note 3)	LTC6806, DCMD = 0, ISOMD = 1 $R_{B1} + R_{B2}$ = 2k	READY	●	3.6	4.5	5.4	mA
			ACTIVE	●	4.6	5.8	7.0	mA
		LTC6806, DCMD = 1, ISOMD = 0 $R_{B1} + R_{B2}$ = 2k	READY	●	3.6	4.5	5.2	mA
			ACTIVE	●	5.6	6.8	8.1	mA
		LTC6806, DCMD = 1, ISOMD = 1 $R_{B1} + R_{B2}$ = 2k	READY	●	4.0	5.2	6.5	mA
			ACTIVE	●	7.0	8.5	10.5	mA
		LTC6806, DCMD = 0, ISOMD = 1 $R_{B1} + R_{B2}$ = 20k	READY	●	1.0	1.8	2.6	mA
			ACTIVE	●	1.2	2.2	3.2	mA
		LTC6806, DCMD = 1, ISOMD = 0 $R_{B1} + R_{B2}$ = 20k	READY	●	1.0	1.8	2.4	mA
			ACTIVE	●	1.3	2.3	3.3	mA
		LTC6806, DCMD = 1, ISOMD = 1 $R_{B1} + R_{B2}$ = 20k	READY	●	1.6	2.5	3.5	mA
			ACTIVE	●	1.8	3.1	4.8	mA
V_{SUP}	V^+ Supply Voltage Where TME Specifications Are Met			●	4.75	5	5.5	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full specified temperature range, otherwise specifications are at T_A = 25°C. The test conditions are V^+ = +5.0V unless otherwise noted. The ISOMD pin is tied to the V^- pin, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
ADC Timing Specifications							
T_{CYCLE} (Figure 4)	Calibration Cycle + Measure Time when Starting from the REFUP State, MD = 00 (Note 6)	ADCV 1 Cell ADCV/CVST 36 Cells ADAX/ADSTAT 1 Channel ADAX/AXST 7 Channels ADSTAT/STATST/ADAXSC 3 Channels ADCVSC 37 Channels			0.38 6.75 0.25 0.95 0.48 7.16		ms ms ms ms ms ms
	Calibration Cycle + Measure Time when Starting from the REFUP State, MD = 01 (Note 6)	ADCV 1 Cell ADCV/CVST 36 Cells ADAX/ADSTAT 1 Channel ADAX/AXST 7 Channels ADSTAT/STATST/ADAXSC 3 Channels ADCVSC 37 Channels			0.57 10.30 0.44 1.72 0.87 11.00		ms ms ms ms ms ms
	Calibration Cycle + Measure Time when Starting from the REFUP State, MD = 10 (Note 6)	ADCV 1 Cell ADCV/CVST 36 Cells ADAX/ADSTAT 1 Channel ADAX/AXST 7 Channels ADSTAT/STATST/ADAXSC 3 Channels ADCVSC 37 Channels			0.83 15.03 0.70 2.75 1.38 16.12		ms ms ms ms ms ms
	Calibration Cycle + Measure Time when Starting from the REFUP State, MD = 11 (Note 6)	ADCV 1 Cell ADCV/CVST 36 Cells ADAX/ADSTAT 1 Channel ADAX/AXST 7 Channels ADSTAT/STATST/ADAXSC 3 Channels ADCVSC 37 Channels			2.36 43.45 2.23 8.89 4.46 46.84		ms ms ms ms ms ms
$T_{MONITOR}$	Monitor Cycle Time when Starting from the REFUP State (Note 6)	MM = 01 MM = 10 MM = 11			11.15 16.40 47.89		ms ms ms
$T_{DIAGNOSE}$	DIAGN Time when Starting from the REFUP State (Note 6)				0.60		ms
t_{WAKE}	Wake Up Time		●		100	300	µs
t_{SLEEP}	Sleep Timeout		●		1.5		s
t_{REFUP}	Reference Wake-Up Time	State: Core = STANDBY (Note 6) State: Core = REFUP	●	5.6	6.8	8 0	ms ms
f_S	Clock Frequency		●	1.7	2.0	2.5	MHz
Pin DC Specifications							
V_{IH}	Digital Input Voltage High	Pins CSB_IMA, SCK_IPA, SDI_ICMP, IBIAS_A0, ICMP_A1, IMB_A2, IPB_A3 when DCMD = 0 Pins ISOMD, DCMD, GPIO[1:6]	●	2.0			V
V_{IL}	Digital Input Voltage Low	Pins CSB_IMA, SCK_IPA, SDI_ICMP, IBIAS_A0, ICMP_A1, IMB_A2, IPB_A3 when DCMD = 0 Pins ISOMD, DCMD, GPIO[1:6]	●			0.8	V
$I_{LEAK(DIG)}$	Digital Input Current	Pins CSB_IMA, SCK_IPA, SDI_ICMP, IBIAS_A0, ICMP_A1, IMB_A2, IPB_A3 when DCMD = 0 Pins ISOMD, DCMD, GPIO[1:6]	●			±5	µA
V_{OL}	Digital Output Low	Pins SDO, GPIO[1:6] Sinking 1mA	●			0.1	V
isoSPI DC Specifications							
V_{BIAS}	Voltage on IBIAS Pin	READY/ACTIVE State IDLE State	●	1.9	2.0 0	2.1	V V
I_B	Isolated Interface Bias Current	R_B = 2kΩ to 20kΩ	●	0.1		1.0	mA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full specified temperature range, otherwise specifications are at T_A = 25°C. The test conditions are V^+ = +5.0V unless otherwise noted. The ISOMD pin is tied to the V^- pin, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
A_{IB}	Isolated Interface Current Gain	$V_{TCMP} \le 1.6V$ I_B = 1mA I_B = 0.1mA	●	18 18	20 20	23 26	mA/mA mA/mA
VA	Transmitter Pulse Amplitude	VA = $\lvert V_{IP}–V_{IM}\rvert$	●			1.6	V
V_{ICMP}	Threshold-Setting Voltage on ICMP Pin	$V_{TCMP} = A_{TCMP} \bullet V_{ICMP}$	●	0.2		1.5	V
$I_{LEAK(ICMP)}$	Input Leakage Current on ICMP Pin	V_{TCMP} = 0V to V^+	●			±1	µA
$I_{LEAK(IP/IM)}$	Leakage Current on IP and IM Pins	IDLE State, V_{IP} or V_{IM} = 0V to V^+	●			±1	µA
A_{TCMP}	Receiver Comparator Threshold Voltage Gain	$V_{CM} = V^+/2$ to $V^+ – 0.2V$, V_{ICMP} = 0.2V to 1.5V	●	0.4	0.5	0.6	V/V
V_{CM}	Receiver Common Mode Bias	IP/IM Not Driving		($V^+ – V_{ICMP}/3 – 167mV$)			V
R_{IN}	Receiver Input Resistance	Single-Ended to IPA, IMA, IPB, IMB	●	26	35	45	kΩ
isoSPI Idle/Wake up Specifications							
V_{WAKE}	Differential Wake-Up Voltage	t_{DWELL} = 240ns	●	250			mV
t_{DWELL}	Dwell Time at V_{WAKE} Before Wake Detection		●	240			ns
t_{READY}	Start-Up Time After Wake Detection		●			10	µs
t_{IDLE}	Idle Timeout Duration	(Note 6)	●		10		ms
isoSPI Pulse Timing Specifications							
$t_{½PW(CS)}$	Chip-Select Half-Pulse Width	Transmitter	●	120	150	180	ns
$t_{FILT(CS)}$	Chip-Select Signal Filter	Receiver	●	70	90	110	ns
$t_{INV(CS)}$	Chip-Select Pulse Inversion Delay	Transmitter	●	120	155	190	ns
$t_{WNDW(CS)}$	Chip-Select Valid Pulse Window	Receiver	●	220	270	330	ns
$t_{½PW(D)}$	Data Half-Pulse Width	Transmitter	●	40	50	60	ns
$t_{FILT(D)}$	Data Signal Filter	Receiver	●	10	25	35	ns
$t_{INV(D)}$	Data Pulse Inversion Delay	Transmitter	●	40	55	65	ns
$t_{WNDW(D)}$	Data Valid Pulse Window	Receiver	●	70	90	110	ns
SPI Timing Requirements (See Figure 18)							
t_{CLK}	SCK Period	(Note 4)	●	1			µs
t_1	SDI Setup Time Before SCK Rising Edge		●	25			ns
t_2	SDI Hold Time After SCK Rising Edge		●	25			ns
t_3	SCK Low	$T_{CLK} = t_3 + t_4 \ge 1µs$	●	200			ns
t_4	SCK High	$T_{CLK} = t_3 + t_4 \ge 1µs$	●	200			ns
t_5	CSB Rising Edge to CSB Falling Edge		●	0.65			µs
t_6	SCK Rising Edge to CSB Rising Edge	(Note 4)	●	0.8			µs
t_7	CSB Falling Edge to SCK Rising Edge	(Note 4)	●	1			µs
t_8	SCK Falling Edge to SDO Valid	(Note 5)	●			60	ns
isoSPI Timing Specifications							
t_9	SCK Rising Edge to Short ±1 Transmit		●			50	ns
t_{10}	CSB Transition to Long ±1 Transmit		●			60	ns
t_{11}	CSB Rising Edge to SDO Rising	(Note 5)	●			200	ns
t_{RTN}	Data Return Delay		●	325	375	425	ns
$t_{DSY(CS)}$	Chip-Select Daisy-Chain Delay		●		120	180	ns

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full specified temperature range, otherwise specifications are at T_A = 25°C. The test conditions are V^+ = +5.0V unless otherwise noted. The ISOMD pin is tied to the V^- pin, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$t_{DSY(D)}$	Data Daisy-Chain Delay		●	200	250	300	ns
t_{LAG}	Data Daisy-Chain Lag (vs. Chip-Select)		●	0	35	70	ns
$t_{5(GOV)}$	Chip-Select High-to-Low Pulse Governor		●	0.6		0.82	µs
$t_{6(GOV)}$	Data to Chip-Select Pulse Governor		●	0.8		1.05	µs
t_{BLOCK}	isoSPI Port Reversal Blocking Window		●	2		10	µs

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime. C0 ABS MAX is tested at ±30V due to test equipment limitation. It is designed to be the same as C1 to C12.

Note 2: The ADC specifications are guaranteed by the Total Measurement Error specification.

Note 3: The ACTIVE state current is calculated from DC measurements. The ACTIVE state current is the additional supply current into V^+ when there is continuous communications on the isoSPI ports with 50% data 1's and 50% data 0's. The calculations are based on the test circuits #1 and #2 which use 2 isoSPI ports. The ACTIVE state current is 50% less when using 1 isoSPI port. See Applications Information section for additional details.

Note 4: These timing specifications are dependent on the delay through the cable, and include allowances for 50ns of delay each direction. 50ns corresponds to 10m of CAT5 cable (which has a velocity of propagation of 66% the speed of light). Use of longer cables would require derating these specs by the amount of additional delay.

Note 5: These specifications do not include rise or fall time of SDO. While fall time (typically 5ns due to the internal pull-down transistor) is not a concern, rising-edge transition time t_{RISE} is dependent on the pull-up resistance and load capacitance on the SDO pin. The time constant must be chosen such that SDO meets the setup time requirements of the MCU.

Note 6: These times vary inversely with f_S.

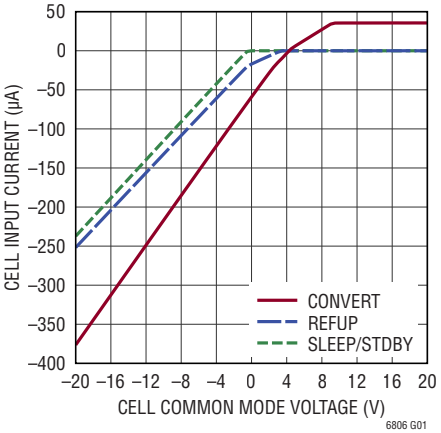
Note 7: TME is defined as the difference between the voltages at the pins and the cell measurements as reported by the LTC6806.

Note 8: VCx is the common mode voltage with respect to V^- at the measured input pins C(n) or C(n-1).

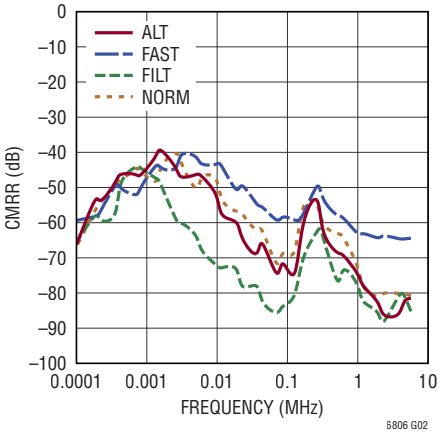
Note 9: A "72V Stack" configuration refers to 36 series fuel cells connected to the LTC6806 with an average cell voltage of 2V per cell.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

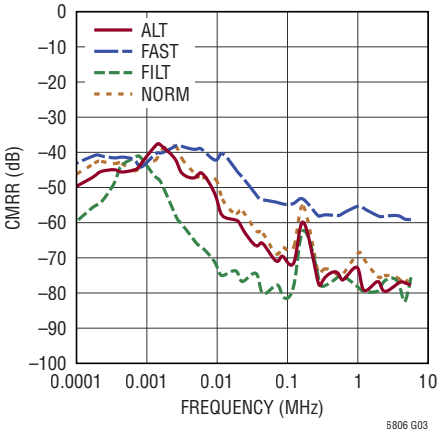
Input Current vs Cell Common Mode Voltage



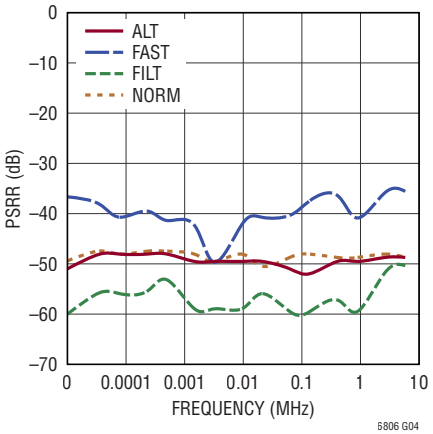
CMRR vs Frequency, LORNG Mode



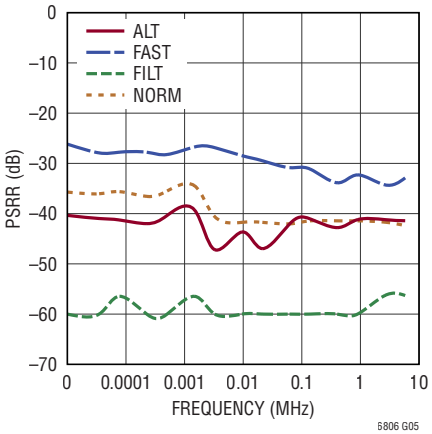
CMRR vs Frequency, HIRNG Mode



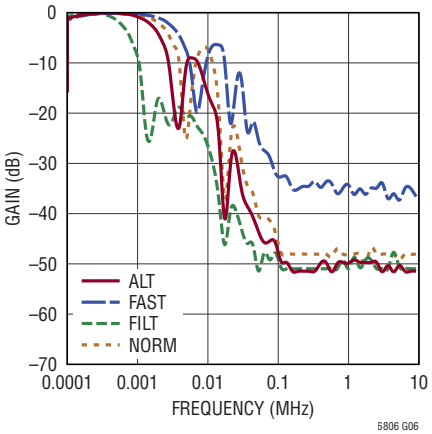
PSRR vs Frequency, LORNG Mode



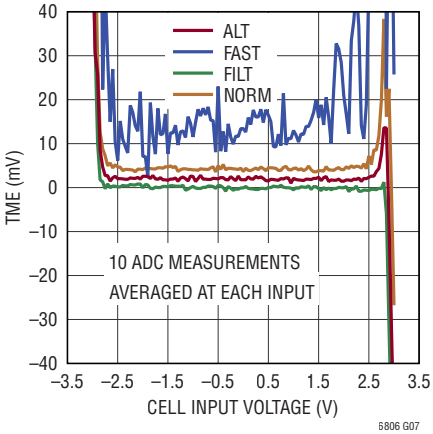
PSRR vs Frequency, HIRNG Mode



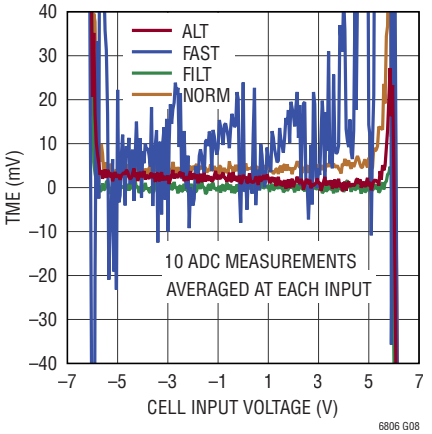
Filter Response



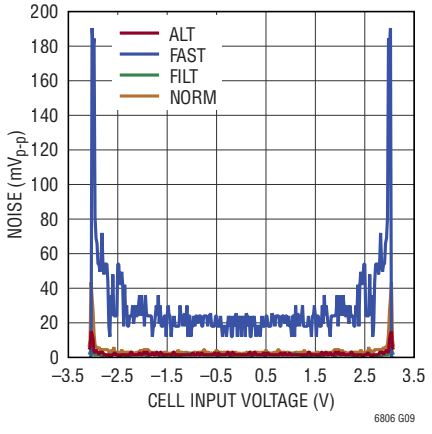
TME vs Cell Input Voltage, LORNG Mode



TME vs Cell Input Voltage, HIRNG Mode

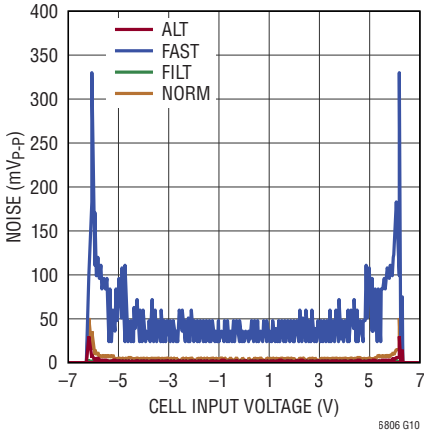


Peak-to-Peak Noise vs Cell Input Voltage, LORNG Mode

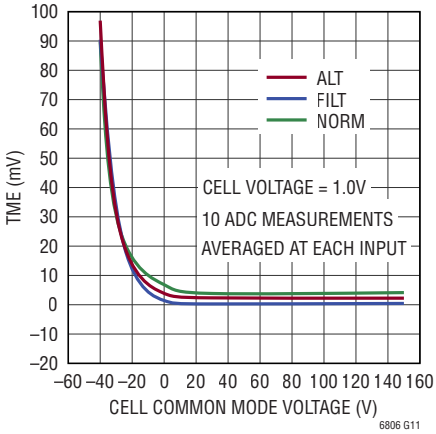


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

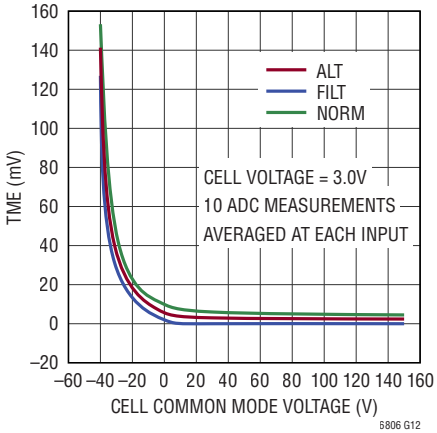
Peak-to-Peak Noise vs Cell Input Voltage, HIRNG Mode



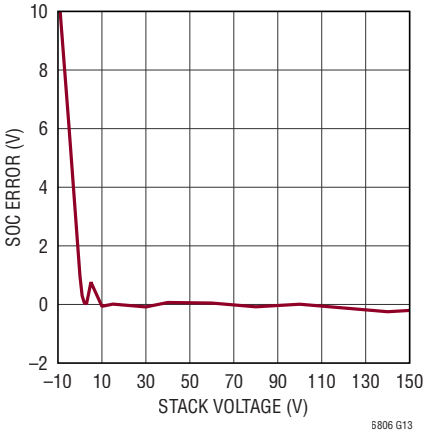
TME vs Cell Common Mode Voltage, LORNG Mode



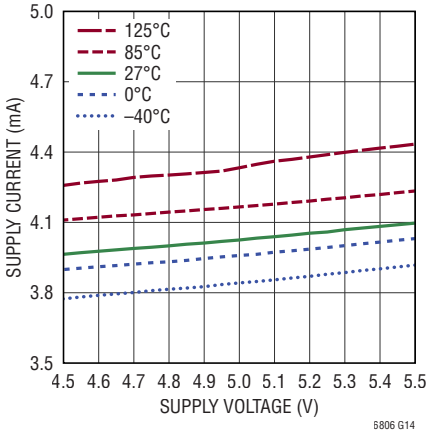
TME vs Cell Common Mode Voltage, HIRNG Mode



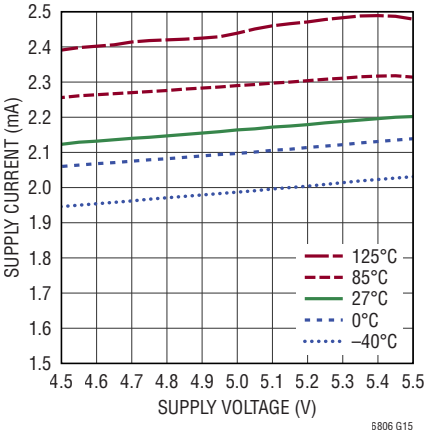
Sum of Cell Measurement Error vs Cell Stack Voltage (C36)



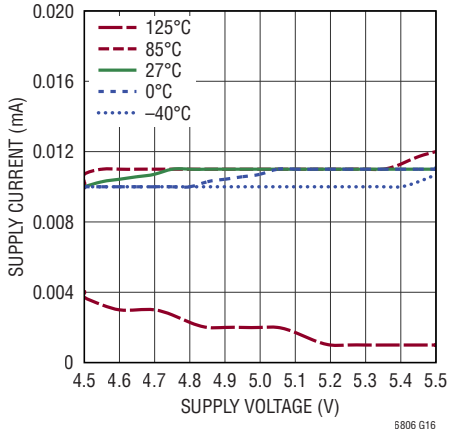
Supply Current vs Supply Voltage, MEASURE Mode



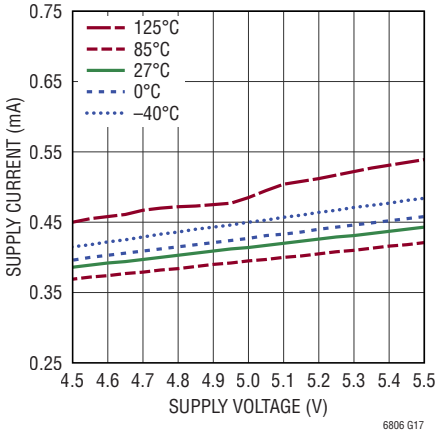
Supply Current vs Supply Voltage, REFUP Mode



Supply Current vs Supply Voltage, SLEEP Mode

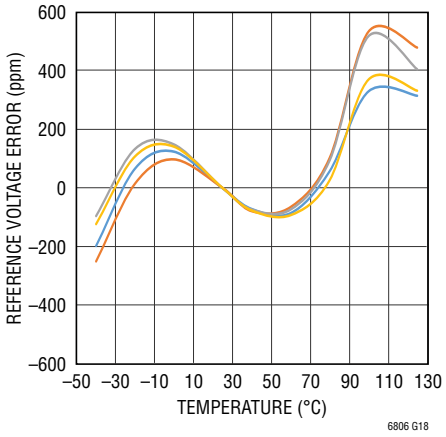


Supply Current vs Supply Voltage, STANDBY Mode

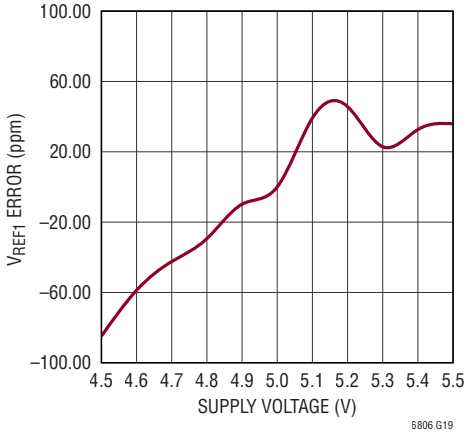


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

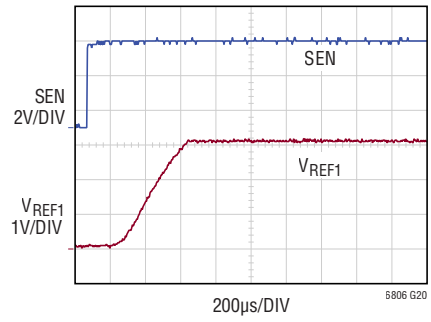
V_{REF1} Error vs Temperature



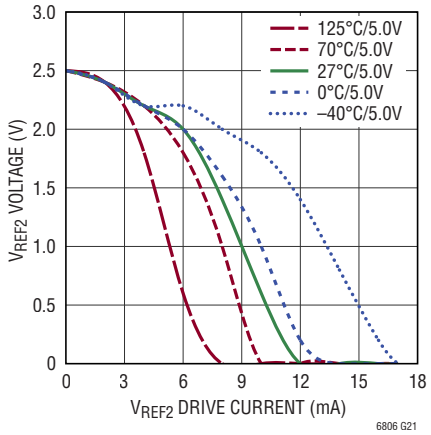
V_{REF1} Error vs Supply Voltage



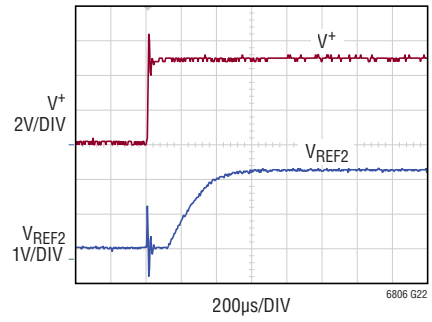
V_{REF1} Start-Up



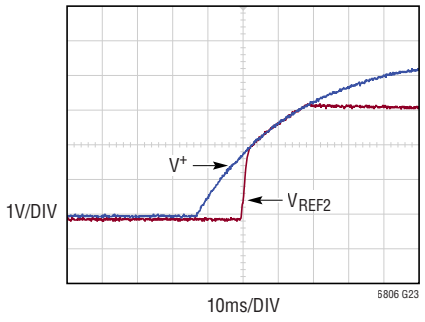
V_{REF2} Load Regulation



V_{REF2} Start-Up Fast V^+ Rise Time



V_{REF2} Start-Up Slow V^+ Rise Time



PIN FUNCTIONS

C0-C36: Cell input. When using fewer than 36 inputs, it is recommended to populate the highest cell channels first with unused lower C pins shorted to V^+. C0 must be connected to a supply voltage, and may be connected to any potential within its absolute maximum operating range including the V^+ and V^- pins. It is recommended that C0 be connected to V^+ in order to provide the best accuracy on inputs at lower common mode voltage. If the fuel cell input resistance is larger than 100 ohm, connecting C0 to V^+ will also prevent cell input leakage current from influencing bottom fuel cells' voltages. To allow very negative fuel cell stack voltage (< –80V), minimize cell input leakage current, and maximize cell measurement accuracy, it is recommended to connect a 10k resistor (or larger depending on application) in parallel with a schottky diode between C0 and V^+. The anode of the schottky diode is tied to V^+.

V^+: Positive Power Supply Input. Supply voltage should be between 4.75V and 5.50V with a bypass capacitor of at least 1µF connected to V^-, within 1cm of the supply leads.

V^-, V^{-*}: Negative supply pins. The V^{-*} pin must be shorted to the V^- pin external to the IC.

V_{REF2}: Secondary Voltage Reference. Buffered to drive up to 4 thermistors. Bypass with an external 1µF capacitor.

V_{REF1}: ADC Reference Voltage. Bypass with an external 1µF capacitor. No DC loads allowed.

GPIO[1:6]: General Purpose I/O. Can be used as digital inputs or digital outputs, or as analog inputs with a measurement range from V^- to 5V. Pin voltage may not exceed the positive supply voltage applied to V^+. When used as a digital output, these pins are open-drain outputs and a pull-up resistor of 1M should be connected between the GPIO pin and V^+.

ISOMD: Serial Interface Mode Pin. Connecting ISOMD to V^+ configures Pins 57 to 60 of the LTC6806 for 2-wire isolated interface (isoSPI) mode. Connecting ISOMD to V^- configures the LTC6806 for 4-wire SPI mode.

DCMD: Daisy-Chain Mode Pin. Connecting DCMD to V^+ configures the LTC6806 for daisy-chained multiple chip operation. Connecting DCMD to V^- configures the LTC6806 for parallel multiple chip operation.

Serial Port Pins: The serial port pins are configurable depending on the state of the DCMD and ISOMD pins as outlined in Table 1.

Table 1. Serial Port Pins

	DAISY-CHAIN MODE (DCMD = V^+)		PARALLEL MODE (DCMD = V^-)	
	ISOMD = V^+	ISOMD = V^-	ISOMD = V^+	ISOMD = V^-
PORT B (Pins 61 to 64)	IPB	IPB	A3	A3
	IMB	IMB	A2	A2
	ICMP	ICMP	A1	A1
	IBIAS	IBIAS	A0	A0
PORT A (Pins 57 to 60)	(NC)	SDO	IBIAS	SDO
	(NC)	SDI	ICMP	SDI
	IPA	SCK	IPA	SCK
	IMA	CSB	IMA	CSB

CSB, SCK, SDI, SDO: 4-Wire Serial Peripheral Interface (SPI). Active low chip select (CSB), serial clock (SCK) and serial data in (SDI) are digital inputs. Serial data out (SDO) is an open drain NMOS output pin. SDO requires a pull-up resistor. A less than 5k ohm resistor is recommended.

A0 to A3: Address Pins. These digital inputs must be connected to V^+ or V^- to set the chip address for addressable serial commands

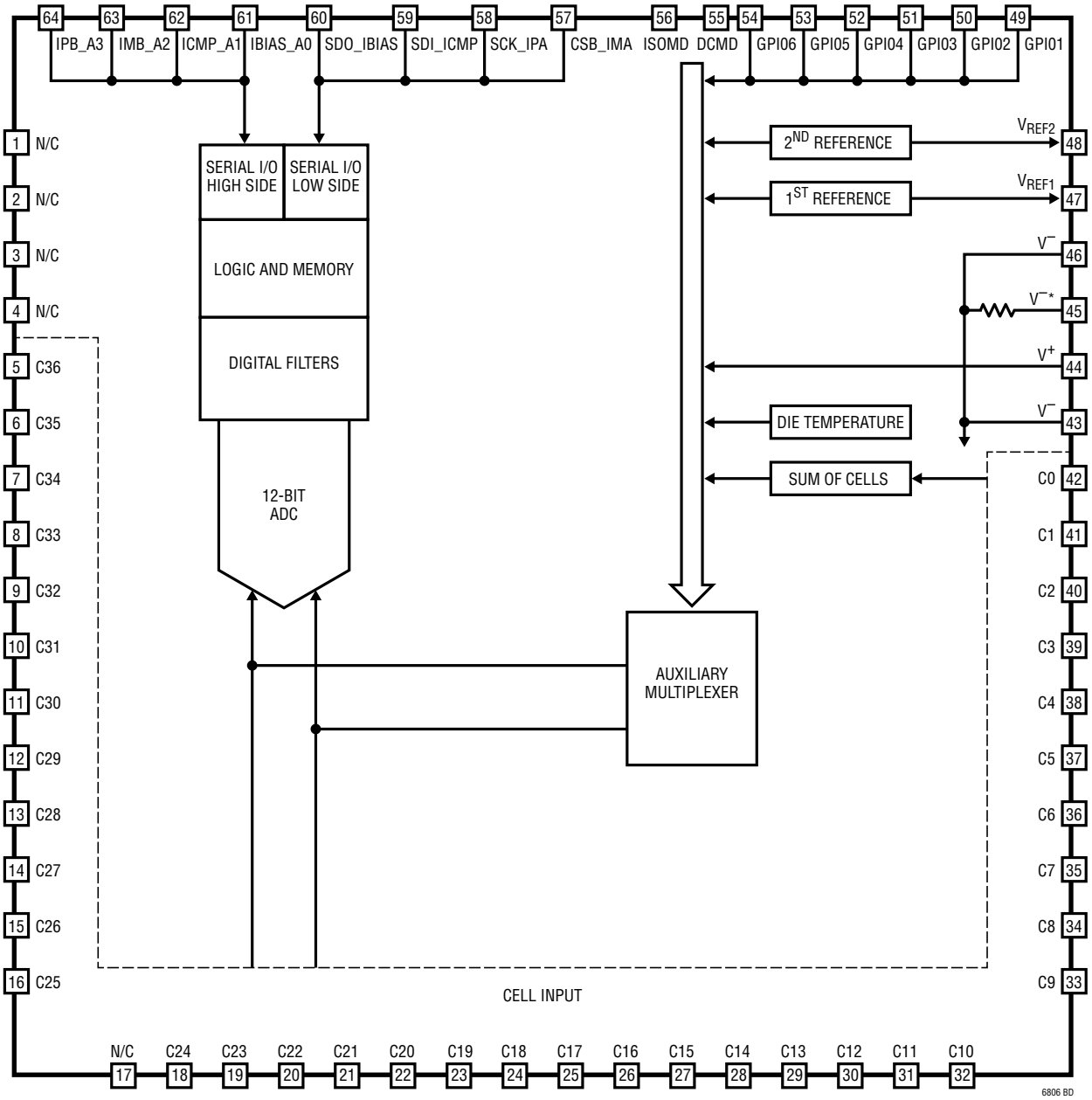
IPA, IMA: Isolated 2-Wire Serial Interface Port A. IPA (plus) and IMA (minus) are a differential input/output pair.

IPB, IMB: Isolated 2-Wire Serial Interface Port B. IPB (plus) and IMB (minus) are a differential input/output pair.

IBIAS: Isolated Interface Current Bias. Tie IBIAS to V^- through a resistor divider to set the interface output current level. When the isoSPI interface is enabled, the IBIAS pin voltage is 2V. The IPA/IMA or IPB/IMB output current drive is set to 20 times the current, I_B, sourced from the IBIAS pin.

ICMP: Isolated Interface Comparator Voltage Threshold Set. Tie this pin to the resistor divider between IBIAS and V^- to set the voltage threshold of the isoSPI receiver comparators. The comparator thresholds are set to half the voltage on the ICMP pin.

BLOCK DIAGRAM



OPERATION

STATE DIAGRAM

The operation of LTC6806 is divided into two separate sections: the core circuit and the isoSPI circuit. Both sections have an independent set of operating states, as well as a shutdown timeout.

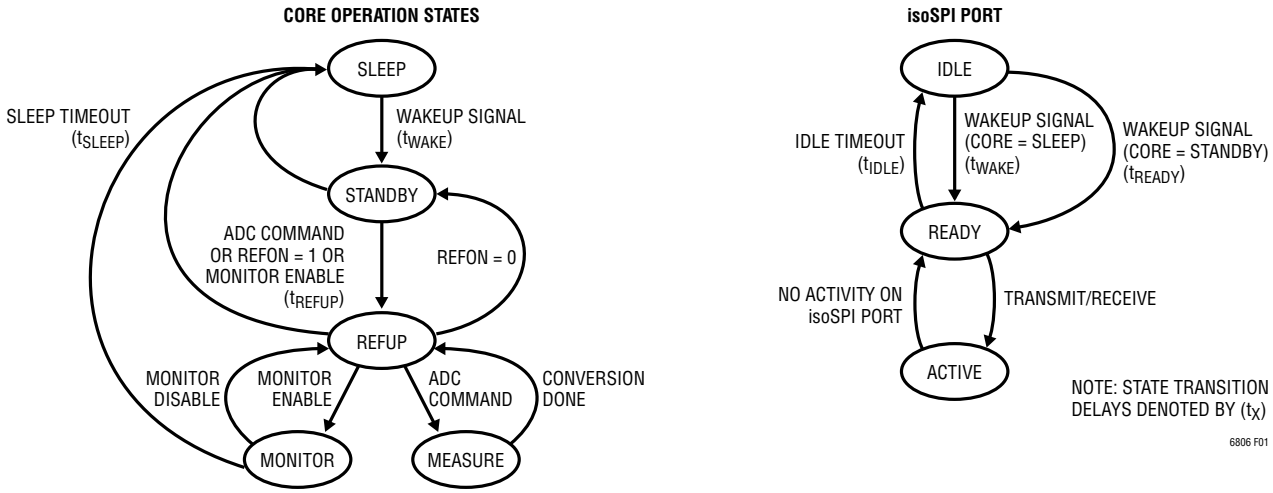


Figure 1. LTC6806 Operation State Diagram

LTC6806 CORE STATE DESCRIPTIONS

SLEEP State

The reference, oscillator and ADC modulator are off. The sleep timer has timed out. The isoSPI ports will be in the IDLE state. The supply currents are reduced to minimum levels. If a WAKEUP signal is received (see Waking Up the Serial Interface), the LTC6806 will enter the STANDBY state.

STANDBY State

The oscillator is turned on. The reference and ADC modulator are still off. The sleep timer is running. If the REFON bit is set, or a valid ADC command is received, or monitor mode is enabled, the IC goes to REFUP. Otherwise, if the serial interface remains idle, then the LTC6806 will return to SLEEP after t_{SLEEP}.

REFUP State

The IC is ready for ADC conversions. The reference is on. The ADC modulator is off. The sleep timer is running. If a valid ADC command is received, the IC will go to MEASURE to begin the conversion. If monitor mode is enabled, the IC will go to MONITOR to begin monitoring. Otherwise if the serial interface remains idle, then the LTC6806 will return to SLEEP after t_{SLEEP}.

MEASURE State

The IC is performing ADC conversions. The reference and ADC modulator are powered up. After the conversions are done, the IC will return to REFUP and if REFON bit is 0, the IC will then return to STANDBY.

MONITOR State

The IC is continuously performing ADC conversions and using GPIO[4:6] to indicate fault conditions. The reference and ADC modulator are on. Monitoring will continue until either the Sleep Timeout occurs or the MMD bits in the configuration register group are written to 00. In the MONITOR state the sleep timer may be disabled by driving GPIO3 to V^-.

OPERATION

isoSPI STATE DESCRIPTIONS

IDLE State

The isoSPI ports are powered down.

When isoSPI Port A or Port B receives a WAKEUP signal (see Waking Up the Serial Interface), the isoSPI enters the READY state. This transition happens quickly (within t_{READY}) if the Core is in the STANDBY state. If the Core is in the SLEEP state when the isoSPI receives a WAKEUP signal, then it transitions to the READY state within t_{WAKE}.

READY State

The isoSPI port(s) are ready for communication. Port B is enabled when DCMD is tied to V^+. The serial interface current in this state depends on the status of the DCMD pin, the status of the ISOMD pin and $R_{BIAS} = R_{B1} + R_{B2}$ (the external resistors tied to the IBIAS pin).

If there is no activity (i.e. no WAKEUP signal) on Port A or Port B for greater than t_{IDLE}, the LTC6806 goes to the IDLE state. When the serial interface is transmitting or receiving data, the LTC6806 goes to the ACTIVE state.

ACTIVE State

The LTC6806 is transmitting/receiving data using one or both of the isoSPI ports. The serial interface consumes maximum power in this state. The supply current increases with clock frequency as the density of isoSPI pulses increases.

SLEEP TIMER

When there are no WAKEUP signals on the SPI or isoSPI ports for more than 1.5 seconds, the Sleep Timeout expires.

The Sleep Timeout initializes the configuration register to its power-up default value. This will initialize the GPIOx pin control bits to logic 1's so that the LTC6806 will not drive the GPIO pins low. It will also clear the REFON, MMD and FCHNL bits. The core will transition to the SLEEP state and the serial ports will be in the IDLE state.

When the core is in the MONITOR state, the sleep timer can be disabled by tying GPIO3 to V^-. In this way, the device can continue monitoring indefinitely, without requiring serial communication to reset the sleep timer.

POWER CONSUMPTION

The power consumption varies according to the operational states. Table 2 and Table 3 provide equations to approximate the supply pin currents in each state.

Table 2. Core Supply Current

	I_{V+}
SLEEP	12µA
STANDBY	500µA
REFUP	2.25mA
MEASURE	4.25mA
MONITOR	4.25mA

Table 3. isoSPI Supply Current Equations

isoSPI STATE	DCMD	ISOMD	$I_{REG(isoSPI)}$
IDLE			0mA
READY	High	High	$2mA + 3 \bullet I_B$
		Low	$1.5mA + 3 \bullet I_B$
	Low	High	$1.5mA + 3 \bullet I_B$
		Low	0mA
ACTIVE	High	High	Write: $2mA + \left(3 + 20 \bullet \frac{100ns}{t_{CLK}}\right) \bullet I_B$ Read: $2mA + \left(3 + 20 \bullet \frac{100ns \bullet 1.5}{t_{CLK}}\right) \bullet I_B$
		Low	$1.5mA + \left(3 + 20 \bullet \frac{100ns}{t_{CLK}}\right) \bullet I_B$
	Low	High	Write: $1.5mA + 3 \bullet I_B$ Read: $1.5mA + \left(3 + 20 \bullet \frac{100ns \bullet 0.5}{t_{CLK}}\right) \bullet I_B$
		Low	0mA

OPERATION

ADC OPERATION

A single ADC inside the LTC6806 is used to convert all ADC channels.

ADC Input Stage

The input stage of the LTC6806 consists of a common-gate stage with 150kΩ series resistance leading to the cell input pins. To accommodate negative common mode measurement, various clamp circuits are implemented at the front end, as shown in Figure 2.

1. When a cell is being measured, all switches in Figure 2 are closed. If the cell common mode voltage is above V^+, all diodes are reverse biased and the cell input sinks approximately 35µA bias current. If the cell common mode drops below V^+, additional current is sourced into the cell input as diode paths to V^+ turn on.
2. When a cell is not being measured, and the part is in MEASURE/MONITOR/REFUP mode, switch NOT SLEEP is closed but all other switches are open. The cell input current is typically zero, unless the cell common mode voltage drops below V^+, causing additional current to be sourced through diodes D10, D11, D20, and D21. If the cell common mode voltage drops below V^-, additional current can be sourced through diode D12 and D22.
3. In SLEEP/STANDBY mode, all switches are open. The cell input current is typically zero, unless the cell common mode voltage drops below V^- turning on the current path through D12 and D22.

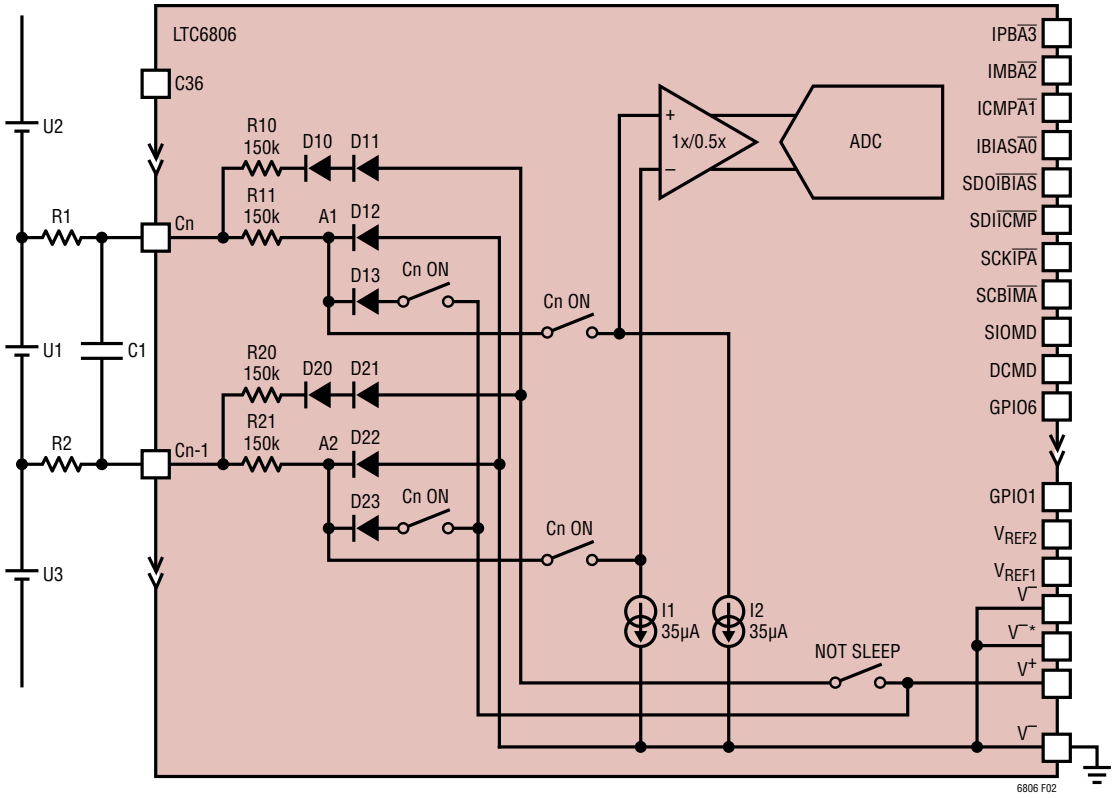


Figure 2. Input Stage Conceptual Block Diagram

OPERATION

ADC Modes

The ADC has four modes of operation. The accuracy and timing of these modes are summarized in Table 4. In each mode, the ADC first performs a single calibration measurement and then measures the inputs.

Normal Mode

In this mode, the ADC has high resolution and low TME (total measurement error) using an oversampling ratio of 128. This is considered the normal operating mode because of the optimum combination of speed and accuracy.

Alternate Mode

In this mode, the ADC –3dB frequency is lowered to 800Hz by increasing the oversampling ratio.

Filtered Mode

In this mode, the ADC –3dB frequency is lowered to 200Hz by increasing the oversampling ratio.

Fast Mode

In this mode, the ADC has maximum throughput.

The increase in speed comes from a reduction in the oversampling ratio with a resulting increase in noise and average TME (total measurement error).

The conversion times for these modes are provided in the Electrical Characteristics table. If the core is in the STANDBY state, an additional t_{REFUP} time is required to power up the reference before beginning the ADC conversions. The reference can remain powered up between ADC conversions, if the REFON bit in the Configuration Register Group is set to 1. This avoids having to wait for the t_{REFUP} delay before beginning additional ADC conversions.

Table 4. ADC Modes

MODE	OVERSAMPLING RATIO (OSR)	36-CELL MEASUREMENT TIME	–3dB FILTER BW	–40dB FILTER BW	TME SPEC[1]
Filtered	1024	43.45ms	0.2kHz	1.25kHz	±20.0mV
Alternate	256	15.04ms	0.8kHz	5kHz	±20.0mV
Normal	128	10.30ms	1.6kHz	10kHz	±20.0mV
Fast	32	6.75ms	6.4kHz	40kHz	±95mV

1. TME is the Total Measurement Error, which includes all error sources. This spec is taken from the Electrical Characteristics table for Cell Measurements with HIRNG =0, reading +1.25V.
2. OSR is the oversampling ratio selected.

OPERATION

ADC Range and Resolution

Delta-Sigma ADCs have quantization noise which depends on the input voltage, especially at low oversampling ratios (OSR), such as in FAST mode. In some of the ADC modes, the quantization noise increases as the input voltage approaches the upper and lower limits of the ADC range. For example, the quantization noise versus input voltage in normal and fast modes is shown in Figure 3.

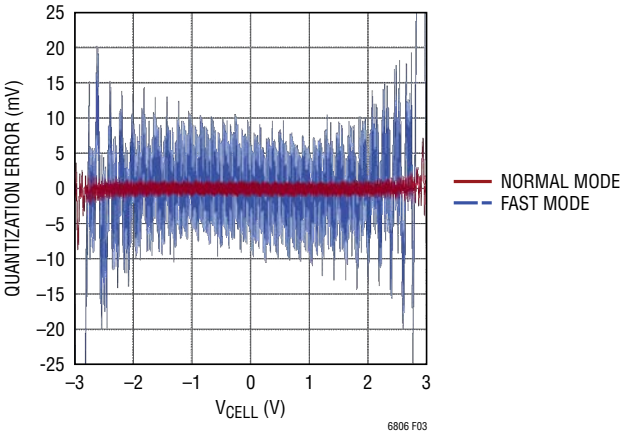


Figure 3. Quantization Noise vs Input Voltage

In Table 5, the precision range of the ADC is arbitrarily defined as the range where the quantization noise is relatively constant even in the lower OSR modes (see Figure 3). Table 5 summarizes the total noise in this range for different inputs.

ADC Range vs Voltage Reference Value

Typical ADCs have a range which is exactly twice the value of the voltage reference, and the ADC measurement error is directly proportional to the error in the voltage reference. The LTC6806 ADC is not typical. The absolute value of V_{REF1} is trimmed up/down to compensate for gain errors in the ADC. Therefore, the ADC total measurement error (TME) specifications are superior to the V_{REF1} specifications.

Measuring Cell Voltages (ADCV Command)

The ADCV command initiates the measurement of the cell inputs, pins C0 through C36. This command has options to select the channel(s) to measure and the ADC mode. See the section on Commands for the ADCV command format.

Figure 4 illustrates the timing of the ADCV command as it measures all 36 cells. The ADC is calibrated before

Table 5. ADC Range and Resolution

MEASUREMENT	FULL RANGE	PRECISION RANGE[1]	LSB	FORMAT	MAX NOISE	EFFECTIVE RESOLUTION[2]
Cells HIRNG = 1	–6.114V to +6.114V	–5V to 5V	3mV	2's Complement 12 Bits	$2mV_{P-P}$	12 Bits
Cells HIRNG = 0	–3.072V to +3.072V	–2.5V to 2.5V	1.5mV	2's Complement 12 Bits	$1mV_{P-P}$	12 Bits
GPIOs	0V to +5.572V	0V to 5V	1.5mV	Binary 12 Bits Readings < 0V Report 0V	$1mV_{P-P}$	12 Bits
V^+	n/a	4.5V to 5.5V	1.875mV	Binary 12 Bits Readings < 0V Report 0V	$2mV_{P-P}$	9 Bits
Sum of Cells	0V to 150V	10V to 150V	108mV	Binary 12 Bits Readings < 0V Report 0V	$144mV_{P-P}$	10 Bits
Internal Temperature	n/a	–40°C to 130°C	0.4K	Binary 12 Bits Please See Measuring Internal Device Parameters (ADSTAT Command) for Scaling Equation	0.3K	9 Bits

1. PRECISION RANGE is the range over which the V_{P-P} noise is less than MAX NOISE.

2. $\text{EFFECTIVE RESOLUTION} = \text{ROUND}\left(\text{LOG}\left[\frac{\text{PRECISION RANGE}}{\text{MAX NOISE}}\right] \Big/ \text{LOG}[2]\right)$.

OPERATION

measuring the cells to cancel offset errors. Table 6 shows the conversion times for the ADCV command measuring all 36 cells. Figure 5 illustrates the timing of the ADCV command as it measures one cell. Table 7 shows the conversion times for the ADCV command measuring one cell.

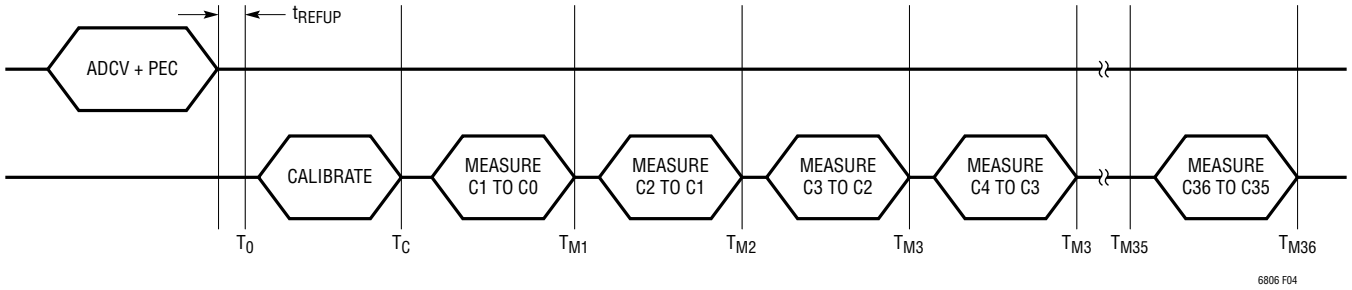


Figure 4. Timing for ADCV Command Measuring All 36 Cells

Table 6. Conversion Timing for ADCV Command Measuring All 36 Cells in Different Modes

CONVERSION TIMING (in µs)							
MODE	**T_0**	**T_C**	**T_{M1}**	**T_{M2}**	**T_{M3}**	**T_{M4}**	**T_{M36}**
Filtered	0	1168	1168 + 1174	1168 + 2 • 1174	1168 + 3 • 1174	1168 + 4 • 1174	1168 + 36 • 1174
Alternate	0	400	400 + 406	400 + 2 • 406	400 + 3 • 406	400 + 4 • 406	400 + 36 • 406
Normal	0	272	272 + 278	272 + 2 • 278	272 + 3 • 278	272 + 4 • 278	272 + 36 • 278
Fast	0	176	176 + 182	176 + 2 • 182	176 + 3 • 182	176 + 4 • 182	176 + 36 • 182

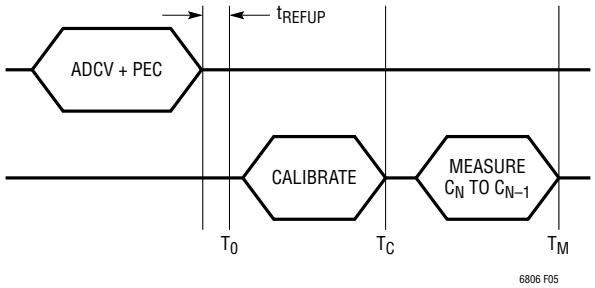


Figure 5. Timing for ADVC Command Measuring 1 Cell

Table 7. Conversion Times for ADCV Command Measuring 1 Cell in Different Modes

CONVERSION TIMING (in µs)			
MODE	**T_0**	**T_C**	**T_M**
Filtered	0	1168	1168 + 1174
Alternate	0	400	400 + 406
Normal	0	272	272 + 278
Fast	0	176	176 + 182

OPERATION

Under/Overvoltage Monitoring

Whenever the C inputs are measured, the results are compared to undervoltage and overvoltage thresholds stored in memory. A flag is set if the cell measurement is above the overvoltage limit. Similarly, a different flag is set if the cell measurement is below the undervoltage limit. In the MEASURE state (measurements are initiated by ADC commands), the undervoltage and overvoltage thresholds are applied with no hysteresis. When the LTC6806 is in the MONITOR state (continuous measurements), the thresholds are applied with 100.5mV (HIRNG = 0) or 201mV (HIRNG = 1) of hysteresis. The hysteresis is activated when any one or more of the monitored cells goes beyond the stored threshold value. The overvoltage and undervoltage thresholds are stored in the Configuration Register Group. The flags are stored in the Status Register Group A and B.

Auxiliary (GPIO) Measurements (ADAX Command)

The ADAX command initiates the measurement of the GPIO inputs. This command has options to select which GPIO input to measure (GPIO1-6) and which ADC mode. The ADAX command also measures the 2nd reference. There are options in the ADAX command to measure the 2nd reference and each GPIO separately or to measure the 2nd reference and all six GPIOs in a single command. See the section on Commands for the ADAX command format. All auxiliary measurements are relative to the V^- pin voltage. This command can be used to read external temperature by connecting the temperature sensors to the GPIOs. These sensors can be powered from the 2nd reference which is also measured by the ADAX command, resulting in precise ratiometric measurements. See Reading External Temperature Probes for more details.

Figure 6 illustrates the timing of the ADAX command as it measures all seven auxiliary channels. The ADC is calibrated before measuring the channels in order to cancel offset errors.

Measuring Sum of Cells and GPIOs (ADAXSC Command)

The ADAXSC command measures GPIO1, then sum of cells, then GPIO2. If GPIO1 and/or GPIO2 are used to measure a current sense element, then this command can be used for cell stack impedance measurements. The GPIO1 measurement occurs before the sum of cells measurement and the GPIO2 measurement occurs just after. If GPIO1 and GPIO2 are connected to the same sense element, then this command will report the current just before and just after the reported stack voltage. The GPIO1 and GPIO2

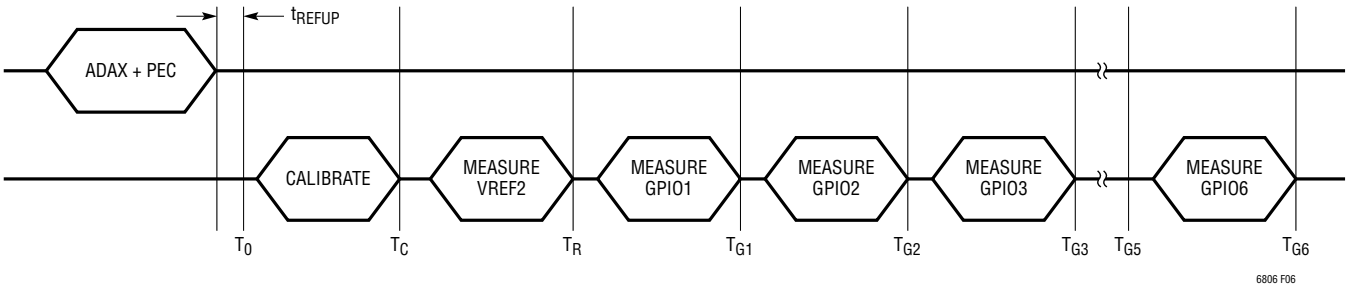


Figure 6. Timing for ADAX Command Measuring All GPIOs and 2nd Reference

Table 8. Conversion Times for ADAX Command Measuring All GPIOs and 2nd Reference in Different Modes

	CONVERSION TIMING (in µs)						
MODE	T_0	T_C	T_R	T_{G1}	T_{G2}	T_{G3}	T_{G6}
Filtered	0	1104	1104 + 1109.5	1104 + 2 • 1109.5	1104 + 3 • 1109.5	1104 + 4 • 1109.5	1104 + 7 • 1109.5
Alternate	0	336	336 + 341.5	336 + 2 • 341.5	336 + 3 • 341.5	336 + 4 • 341.5	336 + 7 • 341.5
Normal	0	208	208 + 213.5	208 + 2 • 213.5	208 + 3 • 213.5	208 + 4 • 213.5	208 + 7 • 213.5
Fast	0	112	112 + 117.5	112 + 2 • 117.5	112 + 3 • 117.5	112 + 4 • 117.5	112 + 7 • 117.5

OPERATION

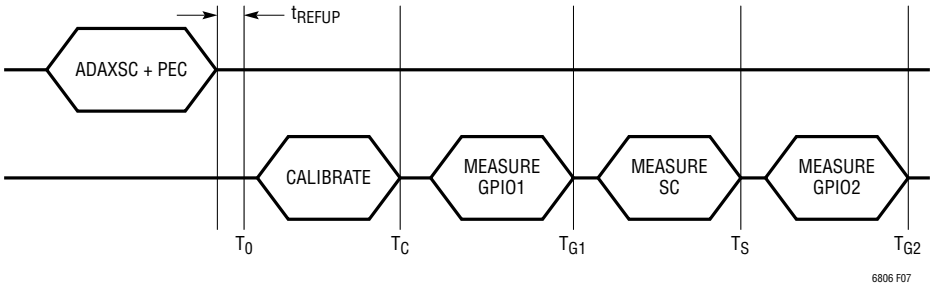


Figure 7. Timing for ADAXSC Command

Table 9. Conversion Times for ADAXSC Command in Different Modes

	CONVERSION TIMING (in µs)				
MODE	**T_0**	**T_C**	**T_{G1}**	**T_S**	**T_{G2}**
Filtered	0	1104	1104 + 1109.5	1104 + 2 • 1109.5	1104 + 3 • 1109.5
Alternate	0	336	336 + 341.5	336 + 2 • 341.5	336 + 3 • 341.5
Normal	0	208	208 + 213.5	208 + 2 • 213.5	208 + 3 • 213.5
Fast	0	112	112 + 117.5	112 + 2 • 117.5	112 + 3 • 117.5

results can then be averaged by the host to estimate the current during the sum of cells measurement.

Figure 7 illustrates the timing of ADAXSC command. The ADC is calibrated before measuring the cells in order to cancel offset errors.

CONTINUOUS MONITORING (MONITOR STATE)

The LTC6806 can be configured to continuously monitor two GPIO pins and a selected number of cell channels for specified fault conditions and issue interrupts on three of the GPIO pins. The IC will perform internal calibrations during each monitor cycle to cancel offsets. Monitoring is enabled by writing the MMD bits in the configuration register group to a non-zero value. The value of the MMD bits determines the ADC mode in which monitoring is performed. ADC commands are ignored while the IC is in the MONITOR state. Table 10 shows the available ADC modes for monitoring.

Table 10. ADC Modes for Monitoring

MMD BITS	ADC MODE	CYCLE TIME FOR MONITORING ALL CELLS PLUS GPIO1 AND GPIO2
00	N/A	Monitoring Is Disabled
01	Normal	11.2ms
10	Alternate	16.4ms
11	Filtered	47.9ms

While the LTC6806 is operating in the MONITOR state, the GPIO pins operate with fixed functions and the values stored in the GPIO[6:1] bits of the Configuration Register Group are ignored.

OPERATION

Table 11. GPIO Pin Functions for Monitoring

PIN	DIRECTION	PURPOSE
GPIO1	Analog Input	Monitoring an NTC thermistor for undertemperature faults.
GPIO2	Analog Input	Monitoring an NTC thermistor for overtemperature faults.
GPIO3	Digital Input	1 -> Enables the sleep timer. 0 -> Disables the sleep timer (prevents sleep timeout).
GPIO4	Digital Output	Outputs logic low when a temperature fault is detected on GPIO1 or GPIO2. External pull-up is required to indicate logic high.
GPIO5	Digital Output	Outputs logic low when an undervoltage fault is detected on a cell that is being monitored. External pull-up is required to indicate logic high.
GPIO6	Digital Output	Outputs logic low when an overvoltage fault is detected on a cell that is being monitored. External pull-up is required to indicate logic high.

Cell Monitoring

While operating in the MONITOR state, the host can limit which cells are to be monitored by writing the FCELL bits in the Configuration Register Group. The value of FCELL specifies the first cell in the stack to be monitored. The LTC6806 will begin monitoring from the FCELL channel and continue up through cell channel 36. Any system that uses fewer than 36 cells per LTC6806 should populate the highest cell channels and write the lowest populated cell count into the FCELL bits (see). The valid range of FCELL is 0x01 through 0x24 (decimal 1 through 36). If the FCELL value is outside of that range, the LTC6806 will monitor all 36 cells in the MONITOR state.

The cell measurements will be compared against the overvoltage and undervoltage thresholds, stored in the Configuration Register Group. If these comparisons indicate a fault condition, the fault will be indicated in the OV/UV bits in the Status Register Group A or B, and the GPIO5 or GPIO6 output will be asserted to logic low to indicate the fault. A hysteresis of 67LSBs is applied. This represents 100.5mV of hysteresis if HIRNG = 0 or 201mV of hysteresis if HIRNG = 1. Table 12 summarizes the MONITOR state fault indications.

Thermistor Monitoring

While operating in the MONITOR state, after measuring the selected cells, the LTC6806 will measure V_{REF2}, GPIO1 and GPIO2. If the GPIO1 measurement is greater than half of the V_{REF2} measurement, a fault will be indicated in the UT bit in the Status Register Group B and the GPIO4 output will be asserted to logic low. If the GPIO2 measurement is less than half of the V_{REF2} measurement, then the fault will be indicated in the OT bit in the Status Register Group B and the GPIO4 output will be asserted to logic low. A hysteresis of 100.5mV is applied. Table 12 summarizes the MONITOR state fault indications.

The thermal thresholds are designed so that GPIO1 and/or GPIO2 may be used to measure an NTC thermistor that is biased from the V_{REF2} pin. If GPIO1 is used to measure a current sense element instead, then choose devices such that the GPIO1 measurement will not be larger than half of the V_{REF2} measurement and the UT fault is not activated. Alternatively, choose a current sense element such that

Table 12. Fault Indications in the MONITOR State

FAULT CONDITION	HYSTERESIS	FAULT INDICATION IN MEMORY	FAULT PIN INDICATION
Any Monitored Cell Voltage ≥ VOV	100.5mV if HIRNG = 0 201mV if HIRNG = 1	Respective OV Bit(s) in Status Register Group A or B Is Set	GPIO6 = Low
Any Monitored Cell Voltage ≤ VUV	100.5mV if HIRNG = 0 201mV if HIRNG = 1	Respective UV Bit(s) in Status Register Group A or B Is Set	GPIO5 = Low
GPIO1 ≥ V_{REF2}/2	100.5mV	UT Bit in Status Register Group B Is Set	GPIO4 = Low
GPIO2 < V_{REF2}/2	100.5mV	OT Bit in Status Register Group B Is Set	GPIO4 = Low

OPERATION

half of the V_{REF2} voltage represents an appropriate overcurrent threshold. The GPIO1 comparison can be disabled by pulling GPIO1 to V^-. The GPIO2 comparison can also be disabled by pulling GPIO2 to V_{REF2}.

The OT and UT bits in the Status Register Group B default to logic high when the LTC6806 is not in the MONITOR state. Upon entering the MONITOR state, the OT and UT bits will remain unchanged until the end of the first monitoring cycle at which point, they will be updated according to the measured results.

Disabling the Sleep Timer in the MONITOR State

GPIO3 may be used to enable or disable the sleep timer while the LTC6806 is in the MONITOR state. If GPIO3 is externally driven logic low while the IC is in the MONITOR state, the sleep timer will be disabled and the IC will not transition to the SLEEP state. If GPIO3 is externally pulled to logic high, the sleep timer will be enabled and the IC will transition to the SLEEP state after 1.5 seconds without receiving a WAKEUP signal.

Register Handling While in the MONITOR State

The host should not modify the FCELL, VUV or VOV bits in the Configuration Register Group after the LTC6806 has entered the MONITOR state. The IC uses these values to control monitoring functions. If these values were written asynchronously, then the monitoring functions may operate incorrectly for the cycle during which the register was written.

The host should not read the cell voltage register groups or the Auxiliary Register Group A while the LTC6806 is in the MONITOR state. These registers contain multi-bit results which do not have double-buffers and arbitration to prevent collisions between result updates and read access. The host may instead read the flag values in Status Register Group A and B while the IC is in the MONITOR state to determine which type(s) of fault has occurred.

If the above types of memory access are required, terminate the MONITOR state, wait for monitoring to end, perform the needed memory access and then restart the monitoring.

Terminating the MONITOR State

When monitoring is no longer desired, the host can terminate monitoring by either asserting GPIO3 and waiting for the duration of the Sleep Timeout, or by writing the MMD bits to 0. After writing the MDD bits to 0, the LTC6806 will complete the last monitoring cycle in progress before returning to the REFUP or STANDBY state. The host can use the PLADC command to determine when this last cycle has completed or wait the duration of one complete monitor cycle as shown in Table 10.

DATA ACQUISITION SYSTEM DIAGNOSTICS

The fuel cell monitoring data acquisition system is comprised of the multiplexer, ADC, 1st reference, digital filters and memory. To ensure long term reliable performance there are several diagnostic commands which can be used to verify the proper operation of these circuits.

Measuring Internal Device Parameters (ADSTAT Command)

The ADSTAT command is a diagnostic command that measures the following internal device parameters: sum of cells (SC), internal die temperature (ITMP), and the V^+ power supply pin (V^+). These parameters are described in the section below. All the 4 ADC modes described earlier are available for these conversions. See the section on Commands for the ADSTAT command format. Figure 8 illustrates the timing of the ADSTAT command measuring all the three internal device parameters. Table 13 shows the conversion time of the ADSTAT command measuring all the three internal parameters.

Sum of Cells Measurement: The sum of cells measurement is the voltage between C36 and C0 with a 72:1 attenuation.

OPERATION

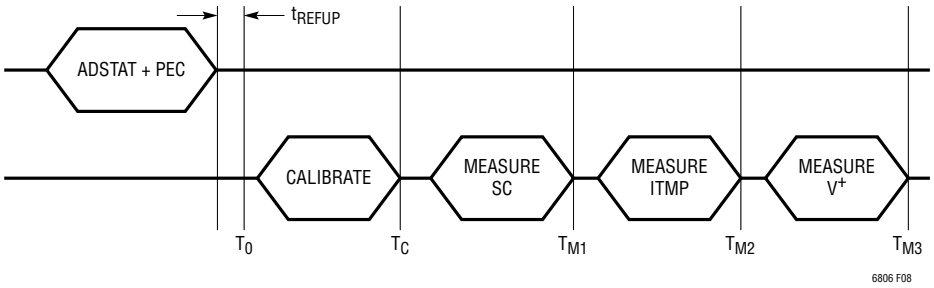


Figure 8. Timing for ADSTAT Command Measuring SC, ITMP, V+

Table 13. Conversion Times for ADSTAT Command Measuring SC, ITMP, V+

CONVERSION TIMING (in µs)					
MODE	**T0**	**T_C**	**T_{M1}**	**T_{M2}**	**T_{M3}**
Filtered	0	1104	1104 + 1109.5	1104 + 2 • 1109.5	1104 + 3 • 1109.5
Alternate	0	336	336 + 341.5	336 + 2 • 341.5	336 + 3 • 341.5
Normal	0	208	208 + 213.5	208 + 2 • 213.5	208 + 3 • 213.5
Fast	0	112	112 + 117.5	112 + 2 • 117.5	112 + 3 • 117.5

The 12-bit ADC value of sum of cells measurement (SC) is stored in Status Register Group C. From the SC value, the voltage from the sum of cell measurement can be determined using the expression:

Sum of Cells = SC • 72 • 1.5mV

Internal Die Temperature: The ADSTAT command can measure the internal die temperature. The 12-bit ADC value of the die temperature measurement (ITMP) is stored in Status Register Group C. From ITMP, the actual die temperature can be determined using the expression:

Internal Die Temperature (°C) = (ITMP/4.65) – 266K

Power Supply Measurement: The ADSTAT command is also used to measure the V+ Supply Pin (V+). The 12-bit ADC value of the analog power supply measurement (VA) is stored in Status Register Group C. The voltage from the power supply measurement can be determined using the expression:

Power Supply Measurement = V+ • 1.875mV

All Cells Plus Sum of Cells Measurement

The ADCVSC command is a diagnostic command that measures all of the cell voltages and the sum of all cells in a single command. The sum of cells measurement is executed in the middle of the sequence, after Cell 18 and before cell 19. This reduces latency between measurements compared to using the ADCV and ADSTAT commands separately. Note that in the ADCVSC timing diagram, the ADC performs a calibration every time there is a switch between cell conversions and SC conversions.

Accuracy Check

Measuring an independent voltage reference is the best means to verify the accuracy of a data acquisition system. The LTC6806 contains a 2nd reference for this purpose. The ADAX command will initiate the measurement of the 2nd reference, and place the results in Auxiliary Register Group A. The acceptable range of results will depend on the accuracy of the 2nd reference, which includes the thermal hysteresis and long term drift of the 2nd reference. Readings outside of the specified V_{REF2} range indicate that the system is out of its specified tolerance.

OPERATION

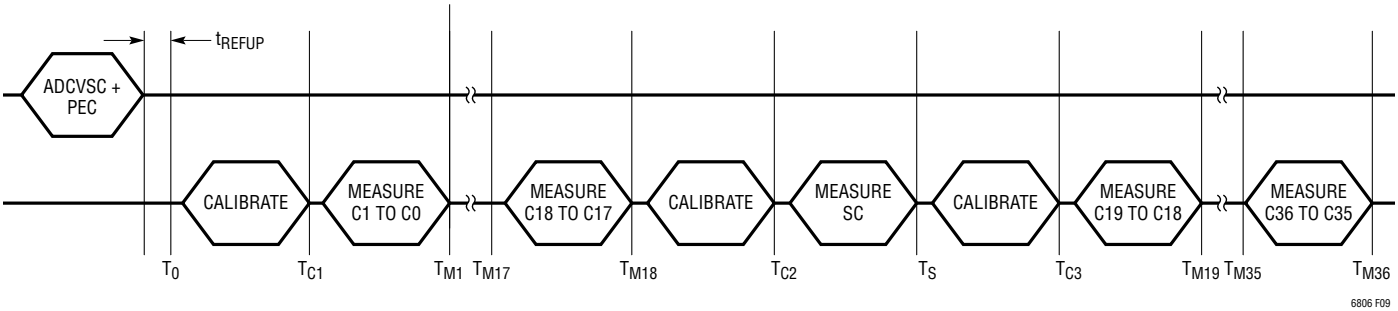


Figure 9. Timing for ADCVSC Command

Table 14. Conversion Times for ADCVSC Command in Different Modes

	CONVERSION TIMING (in µs)									
MODE	T_0	T_{C1}	T_{M1}	T_{M2}	T_{M18}	T_{C2}	T_S	T_{C3}	T_{M19}	T_{M36}
Filtered	0	1168	1168 + 1174	1168 + 2 • 1174	1168 + 18 • 1174	23,410	24,519	24,519 + 1174	24,519 + 2 • 1174	24,519 + 19 • 1174
Alternate	0	400	400 + 406	400 + 2 • 406	400 + 18 • 406	8050	8391	8391 + 406	8391 + 2 • 406	8391 + 19 • 406
Normal	0	272	272 + 278	272 + 2 • 278	272 + 18 • 278	5490	5703	5703 + 278	5703 + 2 • 278	5703 + 19 • 278
Fast	0	176	176 + 182	176 + 2 • 182	176 + 18 • 182	3570	3687	3687 + 182	3687 + 2 • 182	3687 + 19 • 182

MUX Decoder Check (DIAGN)

The diagnostic command DIAGN confirms the proper operation of each multiplexer channel. The command cycles through all channels and sets the MUXFAIL bit to 1 in the Configuration Register Group if any channel decoder fails. The MUXFAIL bit is set to 0 if the channel decoder passes the test. The MUXFAIL bit is also set to 1 upon power-up (POR) or after a CLRSTAT command.

The DIAGN command takes ~600µs to complete if the core is in REFUP state, and ~7.6ms to complete if the core is in STANDBY state. The polling methods described in the section Polling Methods can be used to determine the completion of the DIAGN command.

Digital Filter Check

The delta-sigma ADC is composed of a 1-bit pulse density modulator followed by a digital filter. A pulse density modulated bit stream has a higher percentage of 1s for higher analog input voltages. The digital filter converts this high frequency 1-bit stream into a single 12-bit word. This is why a delta-sigma ADC is often referred to as an oversampling converter.

The self-test commands verify the operation of the digital filters and memory. Figure 10 illustrates the operation of the ADC during self-test. The output of the 1-bit pulse density modulator is replaced by a 1-bit test signal. The test signal passes through the digital filter and is con-

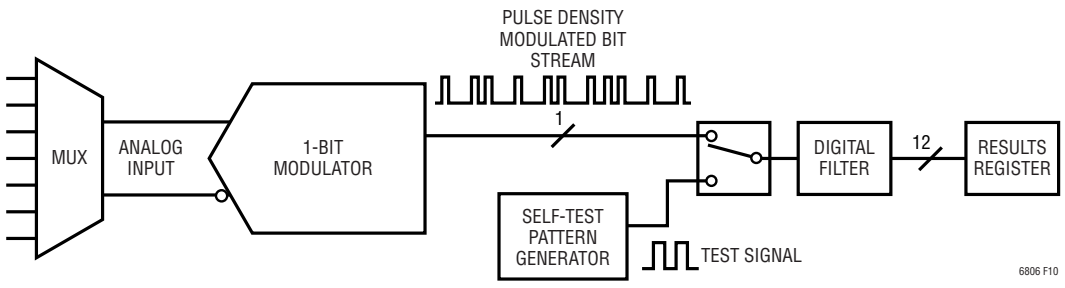


Figure 10. Operation of LTC6806 ADC Self-Test

OPERATION

verted to a 12-bit value. The 1-bit test signal undergoes the same digital conversion as the regular 1-bit pulse from the modulator, so the conversion time for any self-test command is exactly the same as the corresponding regular ADC conversion command. The 12-bit ADC value is stored in the same register groups as the regular ADC conversion command. The test signals are designed to place alternating one-zero patterns in the registers. Table 15 provides a list of the self-test commands. If the digital filters and memory are working properly, then the registers will contain the values shown in Table 15. For more details see the section Commands.

ADC Clear Commands

LTC6806 has three clear commands — CLRCELL, CLRAUX and CLRSTAT. These commands clear the registers that store all ADC conversion results.

The CLRCELL command clears Cell Voltage Register Group A, B, C, D, E, F, G, H and I. All bytes in these registers are set to 0xFF by CLRCELL command.

The CLRAUX command clears Auxiliary Register Group A and B. All bytes in these registers are set to 0xFF by CLRAUX command.

The CLRSTAT command clears Status Register Group A, B and C except the OT and UT in Status Register Group B. All OV and UV flags, MUXFAIL bit, STXFF bit, STXFS bit, and THSD bit in Status Register Group B are set to 1 by CLRSTAT command. The registers storing SC, ITMP and V^+ are all set to 0xFF by CLRSTAT command.

Open Wire Check (ADOW Command)

The LTC6806 draws a bias current from each cell as it is measured. When the cell voltage is above V^+, the ADC bias current is a positive current into the pin. When a C pin is open, the open pin will be pulled down by the bias current to around 1.5V below V^+ in REFUP/MEASURE/MONITOR modes. As a result of this bias current, an open wire on a majority of the C pins will produce a negative full-scale reading on the open C pin channel and a positive full-scale reading on the next cell above the open channel. For most C pins the combination of looking for a negative and positive full-scale measurement on the C(N) and C(N+1) pins is the best way to detect open wires. However, this detection method is insufficient if either the open wire impedance is too low or if the common mode voltage of the C pin is not high enough above V^+ to create negative/positive full-scale measurements. In these cases, the ADOW command is used to check for open wires.

This command performs ADC conversions on the C pin inputs identically to the ADCV command, except internal current sources sink current from all C pins for a set period of time before and during the measurement. For C pins biased near ground, internal current sources will

Table 15. Self-Test Command Summary

COMMAND	SELF-TEST OPTION	OUTPUT PATTERN IN DIFFERENT ADC MODES				RESULTS REGISTER GROUPS
		Fast	Normal	Alternate	Filtered	
CVST	ST[1:0] = 01	0x555	0x555	0x555	0x555	C1V to C36V
	ST[1:0] = 10	0xAAA	0xAAA	0xAAA	0xAAA	(CVA, CVB, CVC, CVD, CVE, CVF, CVG, CVH, CVI)
AXST	ST[1:0] = 01	0x554	0x555	0x555	0x555	G1V to G6V, REF
	ST[1:0] = 10	0xAA8	0xAAA	0xAAA	0xAAA	(AUXA, AUXB)
STATST	ST[1:0] = 01	0x554	0x555	0x555	0x555	SC, ITMP, V^+
	ST[1:0] = 10	0xAA8	0xAAA	0xAAA	0xAAA	(STATC)

OPERATION

instead source current into the pin. The pull-up (PUP) bit of the ADOW command determines whether the current sources are sinking.

The open wire checks should be run on an operating fuel cell stack.

The following simple algorithm can be used to check for an open wire on any of the 36 C pins:

1) Run the 36-cell command ADOW with PUP = 0 once. Read the cell voltages for cells 1 to 36 and store them in array $CELL_{PU(n)}$.
2) Run the 36-cell command ADOW with PUP = 1 once. Read the cell voltages for cells 1 to 36 and store them in array $CELL_{PD(n)}$.
3) Take the difference between the pull-up and pull-down measurements made in above steps for cells 1 to 36: $CELL_{\Delta(n)} = CELL_{PU(n)} – CELL_{PD(n)}$.
4) For all values of n from 1 to 36: If $CELL_{\Delta(n+1)} < –200mV$ then C(n) is open. Additionally, if $CELL_{PD(n)}$ *or* $CELL_{PU(n)}$ has a positive *or* negative full-scale value, then either C(n) or C(n–1) is open.

The OWPCH bits in the configuration register group configure the amount of precharge time that is allowed for the 20µA current sources to discharge pin capacitance on open cells before the ADC conversions begin. If the pin capacitance is large enough that 100ms is insufficient to adequately discharge it, then the host can send multiple ADOW commands to achieve further discharge. Use Table 16 to determine which configuration to use.

Table 16. Open Wire Precharge Configurations

EXTERNAL C PIN CAPACITANCE	OWPCH	PRECHARGE TIME
≤10nF	01	1ms
≤100nF	10	10ms
≤1µF	11	100ms
>1µF	Use Multiple ADOW Commands	

A difference of more than 200mV indicates an open wire. Adequate precharge time can be determined by using the following formula:

$$\text{Precharge Time} \geq (C_{FILTER} \bullet 200mV/20\mu A) = C_{FILTER} \bullet 1E+4$$

Revision Code

The configuration register group contains a 4-bit revision code. If software detection of device revision is necessary, then contact the factory for details. Otherwise, the code can be ignored. In all cases, however the values of all bits must be used when calculating the packet error code (PEC) on data reads.

SERIAL INTERFACE OVERVIEW

There are two types of serial ports on the LTC6806 , a standard 4-wire serial peripheral interface (SPI) and a 2-wire isolated interface (isoSPI). Pins 57 through 60 are configurable as a 2-wire or 4-wire serial port, based on the state of the ISOMD pin.

The state of the DCMD pin determines whether the pins 61 through 64 are a second 2-wire serial port. Connecting DCMD to V^+ configures the LTC6806 for use in a serial daisy chain. Connecting DCMD to $V^–$ configures the LTC6806 for use in a parallel addressable bus. In parallel mode, pins 61 through 64 are tied externally to $V^–$ or V^+ and set the address of the device.

OPERATION

4-WIRE SERIAL PERIPHERAL INTERFACE (SPI) PHYSICAL LAYER

External Connections

Connecting ISOMD to V^- configures serial port A for 4-wire SPI. The SDO pin is an open drain output which requires a pull-up resistor tied to the appropriate supply voltage (Figure 11).

Timing

The 4-wire serial port is configured to operate in a SPI system using CPHA = 1 and CPOL = 1. Consequently, data on SDI must be stable during the rising edge of SCK. The timing is depicted in Figure 12. The maximum data rate is 1Mbps; however, the device is tested at a higher data rate in production in order to guarantee operation at the maximum specified data rate.

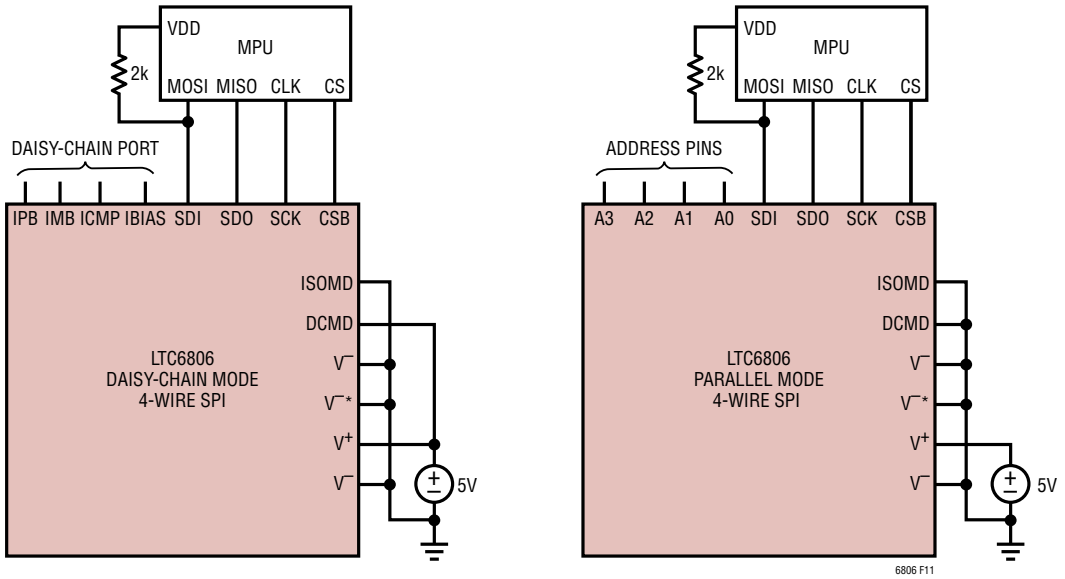


Figure 11. 4-Wire SPI Configuration

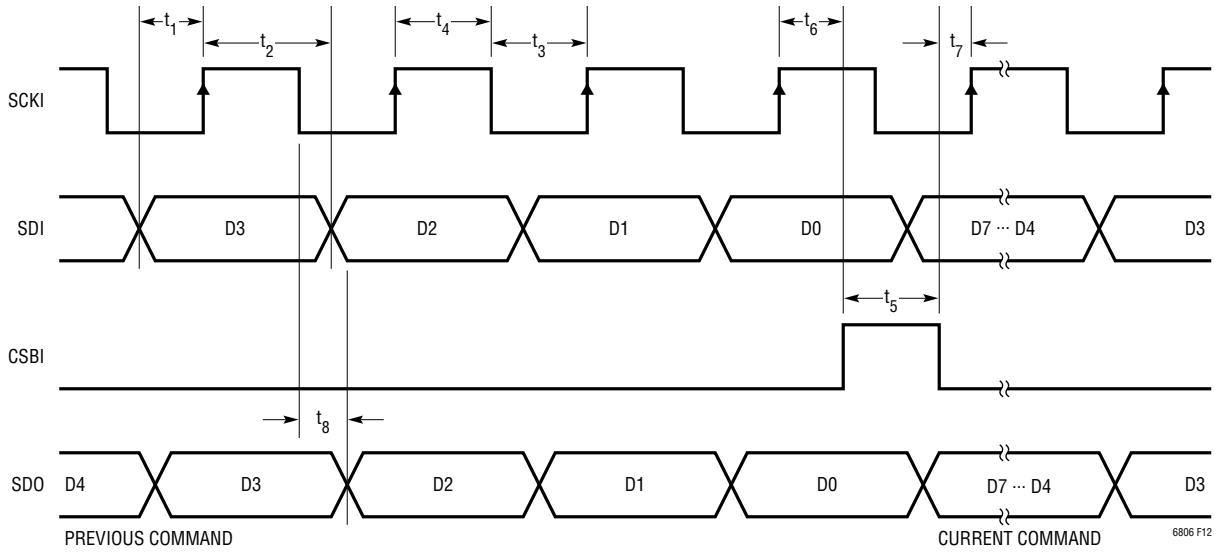


Figure 12. Timing Diagram of 4-Wire Serial Peripheral Interface

OPERATION

2-WIRE ISOLATED INTERFACE (isoSPI) PHYSICAL LAYER

The 2-wire interface provides a means to interconnect LTC6806 devices using simple twisted pair cabling. The interface is designed for low packet error rates when the cabling is subjected to high RF fields. Isolation is achieved through an external transformer.

Standard SPI signals are encoded into differential pulses. The strength of the transmission pulse and the threshold level of the receiver are set by two external resistors. The values of the resistors allow the user to trade off power dissipation for noise immunity.

Figure 13 shows an equivalent circuit. A 2V reference drives the IBIAS pin. External resistors R_{B1} and R_{B2} create the reference current I_B. This current sets the drive strength of the transmitter. R_{B1} and R_{B2} also form a voltage divider of the 2V reference at the ICMP pin. The receiver circuit threshold is half of the voltage at the ICMP pin.

External Connections

In daisy-chain mode, the LTC6806 has two serial ports which are called Port A and Port B. Port B is always configured as a 2-wire interface. Port A is either a 2-wire or 4-wire interface, depending on the connection of the ISOMD pin.

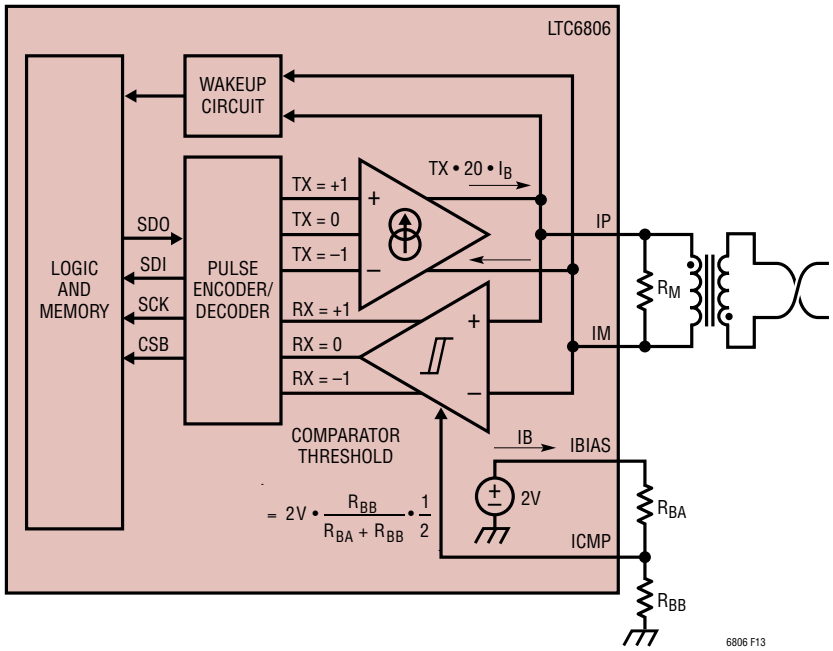


Figure 13. isoSPI Interface

OPERATION

When Port A is configured as a 4-wire interface, Port A is always the SLAVE port and Port B is the MASTER port. Communication is always initiated on Port A of the first device in the daisy-chain configuration. The final device in the daisy chain does not use Port B, and it should be terminated into R_M.

When Port A is configured as a 2-wire interface, communication can be initiated on either Port A or Port B. If communication is initiated on Port A, LTC6806 configures Port A as slave and Port B as master. Likewise, if communication is initiated on Port B, LTC6806 configures Port B as slave and Port A as master. See the section Reversible isoSPI for LTC6806 in daisy-chain mode for a detailed description on reversible isoSPI.

Figure 14 is an example of a robust interconnection of multiple identical PCBs, each containing one LTC6806 configured for operation in a daisy chain. The microprocessor is located on a separate PCB. To achieve 2-wire isolation between the microprocessor PCB and the 1st LTC6806 PCB, use the LTC6820 support IC. The LTC6820 converts between SPI and isoSPI. In this example, communication is initiated on Port A. So LTC6806 configures Port A as slave and Port B as master.

Figure 15 illustrates a daisy-chained configuration of LTC6806 using reversible isoSPI. Two LTC6820s are connected on either side of the daisy chain. Both LTC6820s

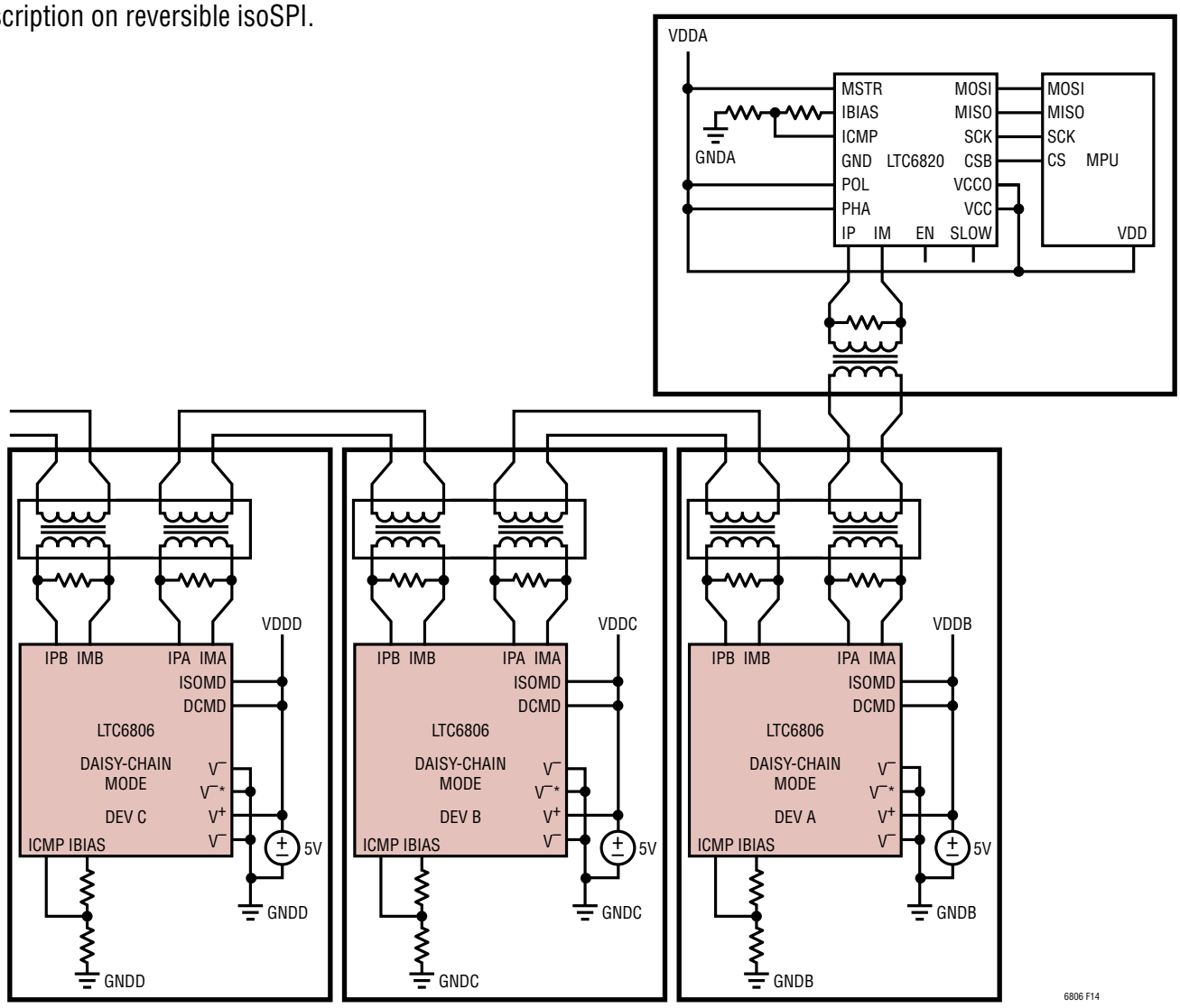


Figure 14. Simplified Transformer-Isolated Daisy Chain Configuration

OPERATION

are configured as Master and share the same SPI interface to connect to the MPU. The MPU uses two different CS signals to talk to one of the two LTC6820s.

For example, in Figure 15, if the bottom LTC6820 is addressed, then LTC6806 DEV A becomes the first device in the stack followed by DEV B and DEV C. Port A of each LTC6806 is configured as the slave and Port B is configured as the Master. On the other hand, if the top LTC6820 is addressed, then LTC6806 DEV C becomes the first device in the stack followed by DEV B and DEV A. Port B of each LTC6806 is configured as slave and Port A is configured as Master.

The reversible isoSPI provides a redundant communication path in the event of a single point failure in the 2-wire interface.

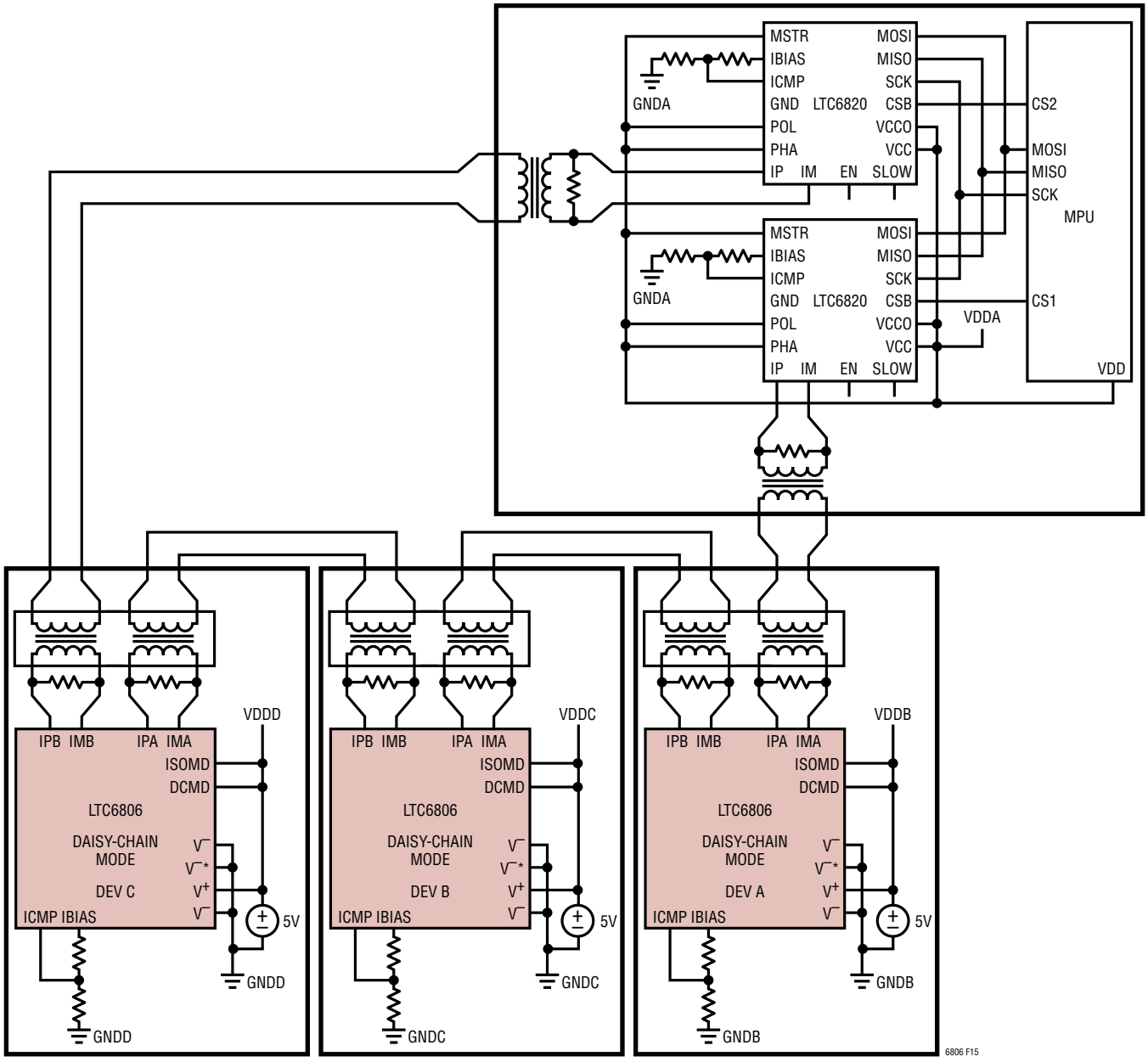


Figure 15. Simplified Transformer Isolated Daisy Chain Configuration with Reversible isoSPI

OPERATION

The LTC6806 in Parallel Mode has a single serial port (Port A) which can be 2-wire or 4-wire, depending on the state of the ISOMD pin. When configured for 2-wire communications, several devices can be connected in a multi-drop configuration, as shown in Figure 16. The LTC6820 IC is used to interface the MPU (master) to the LTC6806s (slaves).

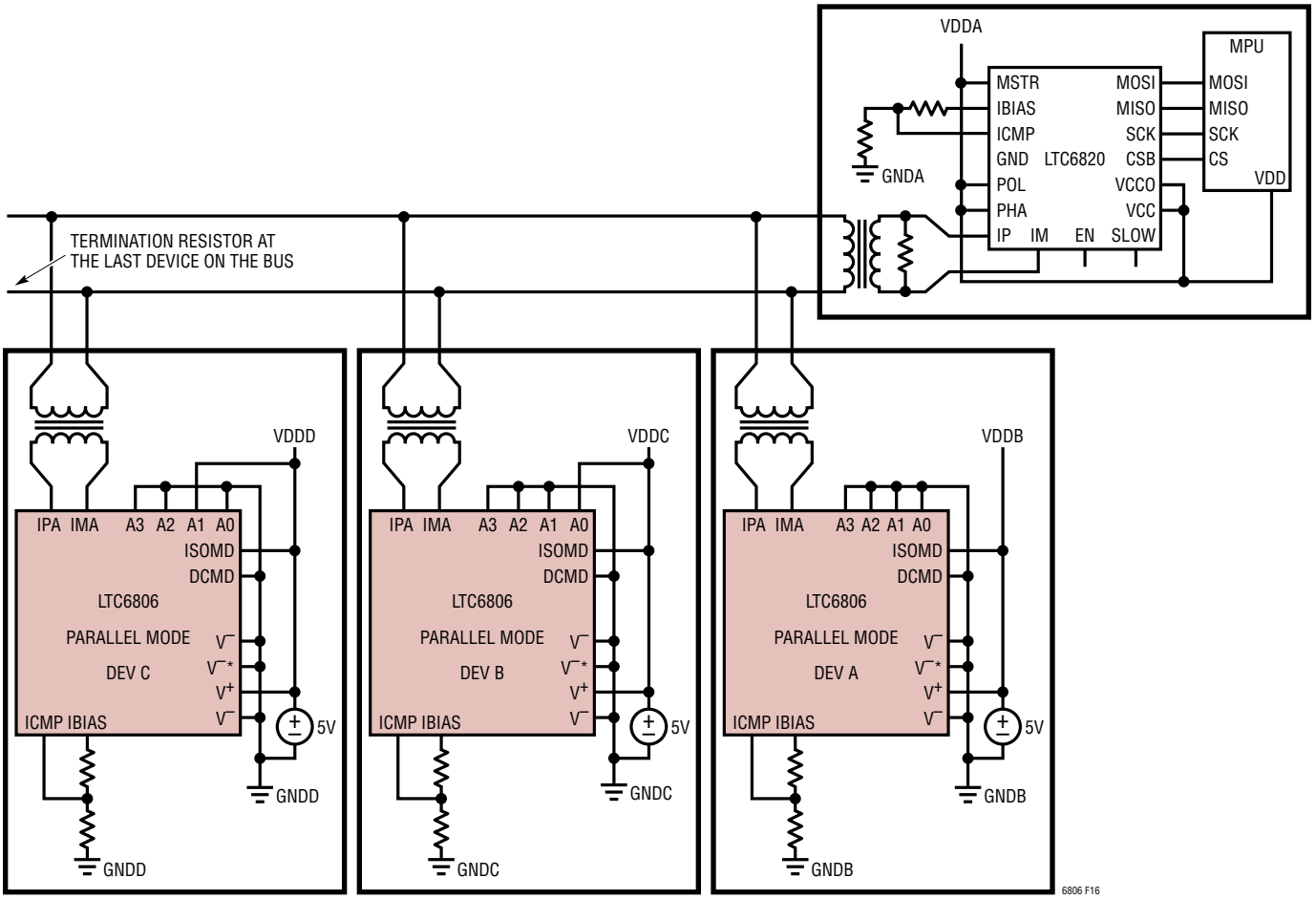


Figure 16. Simplified Multi-Drop Configuration

OPERATION

Selecting Bias Resistors

The adjustable signal amplitude allows the system to trade power consumption for communication robustness and the adjustable comparator threshold allows the system to account for signal losses.

The isoSPI transmitter drive current and comparator voltage threshold are set by a resistor divider ($R_{BIAS} = R_{B1} + R_{B2}$) between the IBIAS and V^-. The divided voltage is connected to the ICMP pin which sets the comparator threshold to 1/2 of this voltage (V_{ICMP}). When either isoSPI interface is enabled (not IDLE) IBIAS is held at 2V, causing a current I_B to flow out of the IBIAS pin. The IP and IM pin drive currents are $20 \bullet I_B$.

As an example, if divider resistor R_{B1} is 2.8kΩ and resistor R_{B2} is 1.21kΩ (so that R_{BIAS} = 4kΩ), then:

$$I_B = \frac{2V}{R_{B1} + R_{BS}} = 0.5mA$$

$$I_{DRV} = I_{IP} = I_{IM} = 20 \bullet I_B = 10mA$$

$$V_{ICMP} = 2V \bullet \frac{R_{B2}}{R_{B1} + R_{B2}} = I_B \bullet R_{B2} = 603mV$$

$$V_{TCMP} = 0.5 \bullet V_{ICMP} = 302mV$$

In this example, the pulse drive current I_{DRV} will be 10mA and the receiver comparators will detect pulses with IP – IM amplitudes greater than ±302mV.

If the isolation barrier uses 1:1 transformers connected by a twisted pair and terminated with 120Ω resistors on each end, then the transmitted differential signal amplitude (±) will be:

$$V_A = I_{DRV} \bullet \frac{R_M}{2} = 0.6V$$

(This result ignores transformer and cable losses, which may reduce the amplitude).

isoSPI Pulse Detail

Two LTC6806 devices can communicate by transmitting and receiving differential pulses back and forth through an isolation barrier. The transmitter can output three logic levels: $+V_A$, 0V and $–V_A$. A positive output results from IP sourcing current and IM sinking current across load resistor R_M. A negative voltage is developed by IP sinking and IM sourcing. When both outputs are off, the load resistance forces the differential output to 0V.

To eliminate the DC signal component and enhance reliability, the isoSPI uses two different pulse lengths. This allows for four types of pulses to be transmitted, as shown in Table 17. A –1 pulse will be transmitted as a negative pulse followed by a positive pulse. The duration of each pulse is defined as $t_{1/2PW}$, since each is half of the required symmetric pair. (The total isoSPI pulse duration is $2 \bullet t_{1/2PW}$).

Table 17. isoSPI Pulse Types

PULSE TYPE	FIRST LEVEL ($t_{½PW}$)	SECOND LEVEL ($t_{½PW}$)	ENDING LEVEL
Long +1	$+V_A$ (150ns)	$–V_A$ (150ns)	0V
Long –1	$–V_A$ (150ns)	$+V_A$ (150ns)	0V
Short +1	$+V_A$ (50ns)	$–V_A$ (50ns)	0V
Short –1	$–V_A$ (50ns)	$+V_A$ (50ns)	0V

The receiver is designed to detect each of these isoSPI pulse types. For successful detection, the incoming isoSPI pulses (CSB or data) should meet the following requirements:

1. $t_{½PW}$ of incoming pulse > t_{FILT} of the receiver and
2. t_{INV} of incoming pulse < t_{WNDW} of the receiver

The worst-case margin (margin 1) for the first condition is the difference between minimum $t_{½PW}$ of the incoming pulse and maximum t_{FILT} of the receiver. Likewise, the worst-case margin (margin 2) for the second condition is the difference between minimum t_{WNDW} of the receiver and maximum t_{INV} of the incoming pulse. These timing relations are illustrated in Figure 18.

A host microprocessor does not have to generate isoSPI pulses to use this 2-wire interface. The first LTC6806 in the system can communicate to the microprocessor using the 4-wire SPI interface on its Port A, then daisy-chain to other LTC6806s using the 2-wire isoSPI interface on its Port B. Alternatively, the LTC6820 can be used to translate the SPI signals into isoSPI pulses.

OPERATION

LTC6806 Operation in Daisy-Chain with Port A Configured for SPI

If LTC6806 is operating in a daisy chain configuration (DCMD = High), Port A of the first device in the stack can be configured for SPI (ISOMD = Low) or isoSPI (ISOMD = High). If port A is configured for SPI (ISOMD = Low), the SPI detects one of four communication events: CSB falling, CSB rising, SCK rising with SDI = 0, and SCK rising with SDI = 1. Each event is converted into one of the four pulse types for transmission through the LTC6806 daisy chain. Long pulses are used to transmit CSB changes and short pulses are use to transmit data, as explained in Table 18.

Table 18. Port B (Master) isoSPI Port Function

COMMUNICATION EVENT (Port A SPI)	TRANSMITTED PULSE (Port B isoSPI)
CSB Rising	Long +1
CSB Falling	Long –1
SCK Rising Edge, SDI = 1	Short +1
SCK Rising Edge, SDI = 0	Short –1

Table 19. Port A (Slave) isoSPI Port Function

RECEIVED PULSE (Port A isoSPI)	INTERNAL SPI PORT ACTION	RETURN PULSE
Long +1	Drive CSB High	None
Long –1	Drive CSB Low	
Short +1	1. Set SDI = 1 2. Pulse SCK	Short –1 Pulse if Reading a 0 Bit
Short –1	1. Set SDI = 0 2. Pulse SCK	(No Return Pulse if Not in READ Mode or if Reading a 1 Bit)

LTC6806 Operation in Daisy-Chain with Port A Configured for isoSPI

On the other side of the isolation barrier (i.e. at the other end of the cable), the 2nd LTC6806 will have ISOMD = V^+ so that its Port A is configured for isoSPI. The slave isoSPI port (Port A or B) receives each transmitted pulse and reconstructs the SPI signals internally, as shown in Table 19. In addition, during a READ command, this port may transmit return data pulses.

The slave isoSPI port never transmits long (CSB) pulses. Furthermore, a slave isoSPI port will only transmit short –1 pulses, never a +1 pulse. The master port recognizes a null response as a logic 1. This allows for multiple slave devices on a single cable without risk of collisions (Multi-drop).

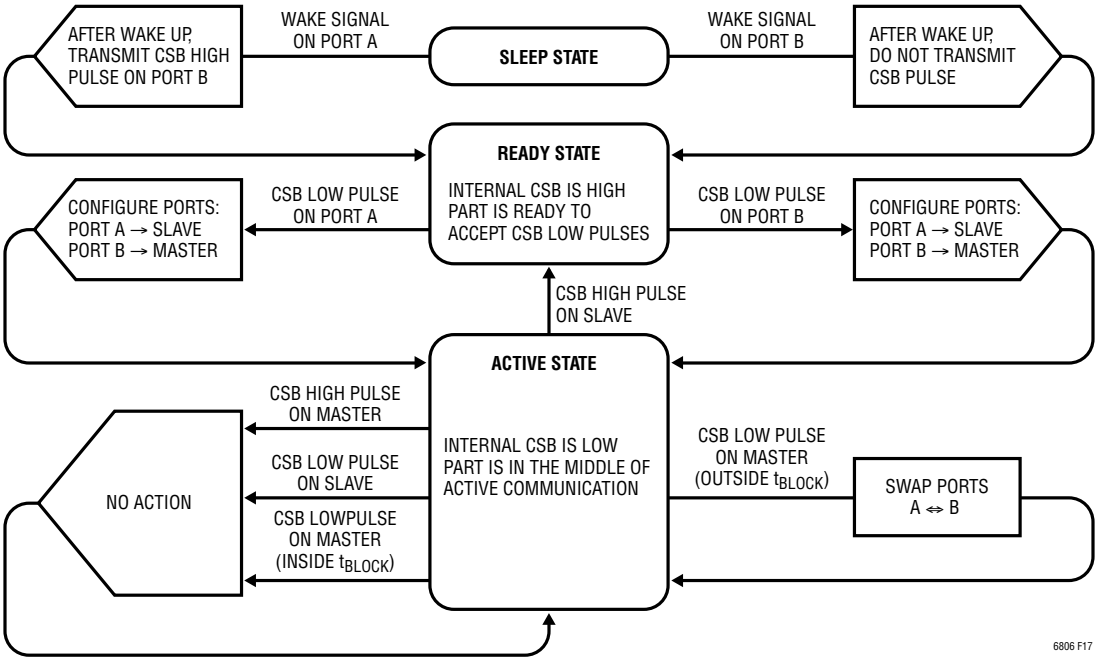


Figure 17. Reversible isoSPI State Diagram

OPERATION

Reversible isoSPI for LTC6806 in Daisy-Chain Mode

When LTC6806 is operating in daisy-chain mode with Port A configured for isoSPI, communication can be initiated from either Port A or Port B. In other words, LTC6806 can configure either Port A or Port B as slave or master, depending on the direction of communication. The reversible isoSPI feature permits communication from both directions in a stack of daisy-chained devices. Figure 17 illustrates the operation of reversible isoSPI.

When LTC6806 is in SLEEP state, it will respond to a valid wake up signal on either Port A or Port B. This is true for all configurations of DCMD and ISOMD pins.

In daisy-chain configurations, if the wake up signal was sent on Port A, LTC6806 transmits a long +1 isoSPI pulse (CSB rising) on Port B after the isoSPI is powered up. If the wake up signal was sent on Port B, LTC6806 powers up the isoSPI but does not transmit a long +1 isoSPI pulse on Port A.

When LTC6806 is in READY state, communication can be initiated by sending a long –1 isoSPI pulse (CSB falling) on either Port A or Port B. The LTC6806 automatically configures the port that receives the long –1 isoSPI pulse as the slave and the other port is configured as the master. The isoSPI pulses are transmitted through the master port to the rest of the devices in the daisy chain.

In ACTIVE state, the LTC6806 is in the middle of communication and CSB of the internal SPI port is low. At the end of communication, a long +1 pulse (CSB rising) on the SLAVE port returns the part to the READY state. Although it is not part of a normal communication routine, the LTC6806 allows ports A and B to be swapped inside the ACTIVE state. This feature is useful for the master controller to reclaim control of the slave port of LTC6806 irrespective of the current state of the ports. This can be done by sending a long –1 isoSPI pulse on the master port after a time delay of t_{BLOCK} from the last isoSPI signal that was transmitted by the part. Any long isoSPI pulse sent to the master port inside t_{BLOCK} is rejected by the part. This ensures the LTC6806 cannot switch ports because of signal reflections from poorly terminated cables (< 100m cable length).

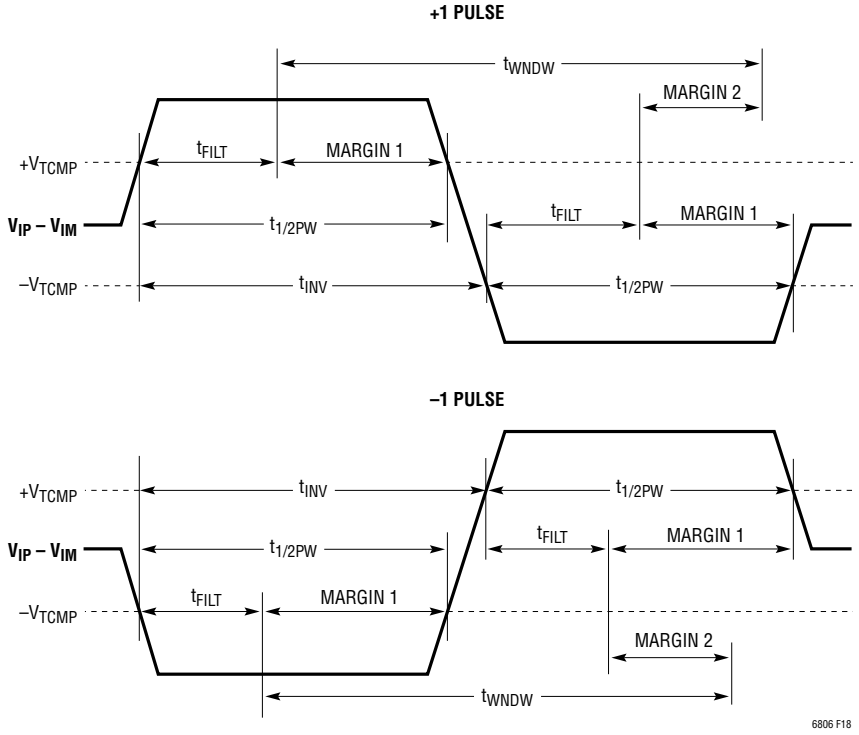


Figure 18. isoSPI Pulse Detail

OPERATION

Timing Diagrams

Figure 19 shows the isoSPI timing diagram for a READ command to daisy-chained LTC6806 parts. The ISOMD pin is tied to V^- on the bottom part so its Port A is configured as a SPI port (CSB, SCK, SDI and SDO). The isoSPI signals of three stacked devices are shown, labeled with the port (A or B) and part number. Note that ISO B1 and ISO A2 are actually the same signal, but shown on each end of the transmission cable that connects parts 1 and 2. Likewise, ISO B2 and ISO A3 are the same signal, but with the cable delay shown between parts 2 and 3.

Bits W_n-W_0 refers to the 16-bit command code and the 16-bit PEC of a READ command. At the end of bit W_0 the three parts decode the READ command and begin shifting out data which is valid on the next rising edge of clock SCK. Bits Xn-X0 refer to the data shifted out by Part 1. Bits Y_n-Y_0 refer to the data shifted out by Part 2 and bits Z_n-Z_0 refer to the data shifted out by Part 3. All this data is read back from the SDO port on Part 1 in a daisy-chained fashion.

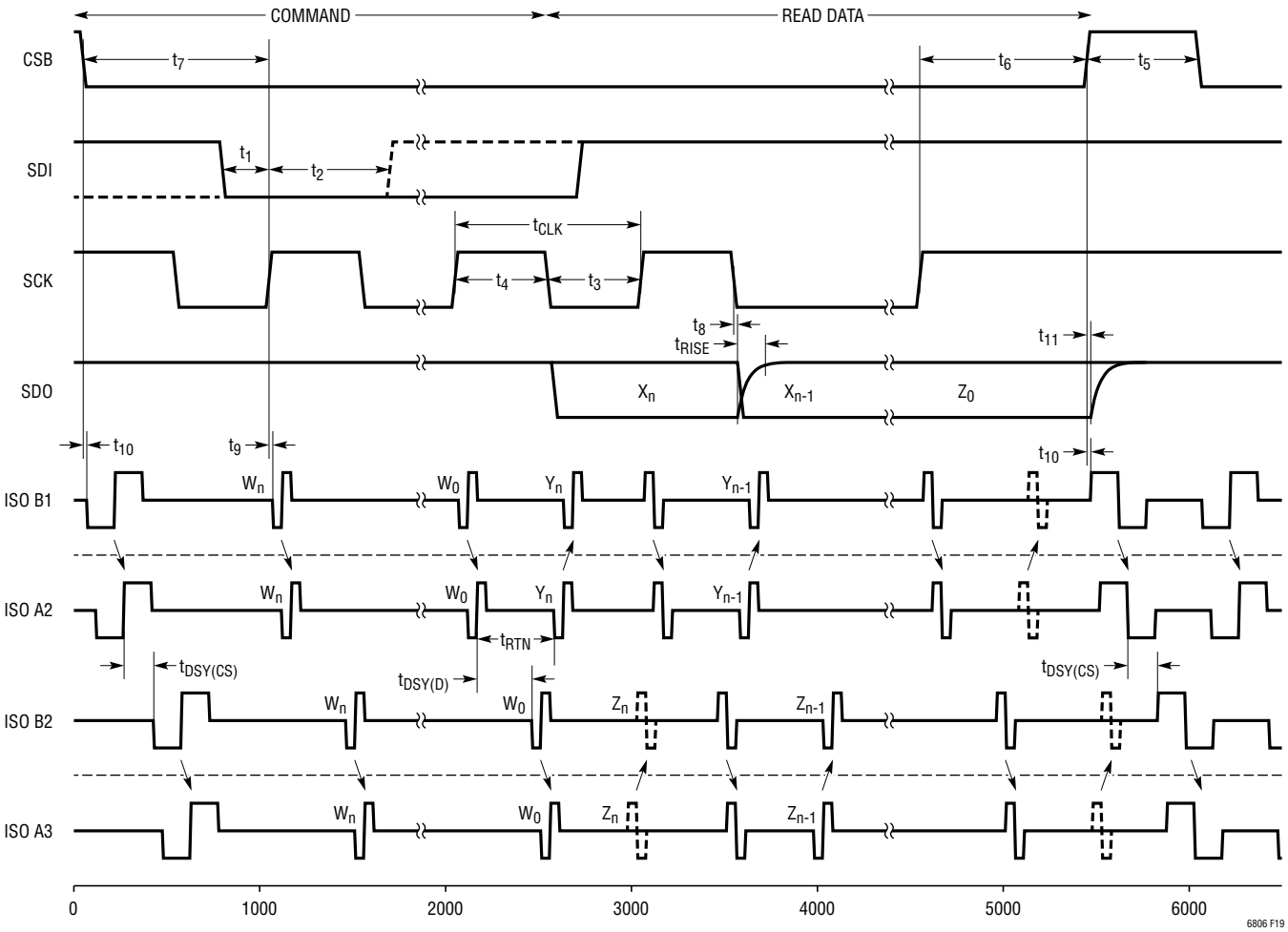


Figure 19. isoSPI Timing Diagram

OPERATION

Waking Up the Serial Interface

The serial ports (SPI or isoSPI) will enter the low power IDLE state if there is no activity on Port A or Port B for a time of t_{IDLE}. LTC6806 has two wake-up circuits monitoring pins CSB_IMA, SCK_IPA and pins IMB_A2, IPB_A3.

Differential activity on pins CSB_IMA, SCK_IPA or pins IMB_A2, IPB_A3 wakes up the serial interface. The LTC6806 will be ready to communicate when the isoSPI state changes to READY within t_{WAKE} or t_{READY}, depending on the core state (see LTC6806 Core State Descriptions for details.)

In daisy-chain mode (DCMD = High), if the LTC6806 wakes up due to differential activity on Port A, it sends a long +1 pulse on Port B after it is ready to communicate. This pulse wakes up the next device in the stack which will, in turn, wake up the next device. If there are N devices in the stack, all the devices are powered up within the time N • t_{WAKE} or N • t_{READY}, depending on the core state. For large stacks, the time N • t_{WAKE} may be equal to or larger than t_{IDLE}. In this case, after waiting longer than the time of N • t_{WAKE}, the host may send another dummy byte and wait for the time N • t_{READY}, in order to ensure that all devices are in the READY state.

If the LTC6806 wakes up due to differential activity on Port B, it will not send a long +1 pulse on Port A after it is ready. So, to wake up all devices in the stack, the host needs to send a series of wake-up pulses spaced no longer than t_{IDLE}.

Figure 20 illustrates the timing and the functionally equivalent circuit for the wake-up circuit on Port A. The wake-up circuit responds to the difference between CSB_IMA and SCK_IPA pins. Common mode signals will not wake up the serial interface. The interface is designed to wake up after receiving a large signal single-ended pulse, or a low amplitude symmetric pulse. The differential signal |SCK_IPA – CSB_IMA|, must be at least V_{WAKE} = 250mV for a minimum duration of t_{DWELL} = 240ns to qualify as a wake-up signal that powers up the serial interface. The wake-up detect circuit on Port B is identical to this circuit with IPB_A3 and IMB_A2 as its inputs.

DATA LINK LAYER

All data transfers on LTC6806 occur in byte groups. Every byte consists of 8 bits. Bytes are transferred with the most significant bit (MSB) first. CSB must remain low for the entire duration of a command sequence, including between a command byte and subsequent data. On a write command, data is latched in on the rising edge of CSB.

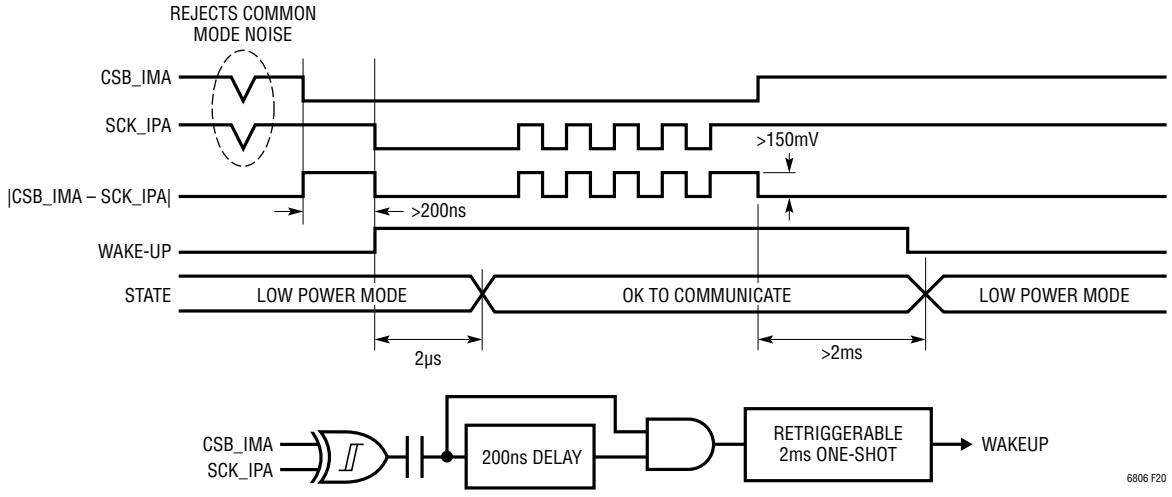


Figure 20. Wake-Up Detection and IDLE Timer

OPERATION

NETWORK LAYER

Packet Error Code

The packet error code (PEC) is a 15-bit cyclic redundancy check (CRC) value calculated for all of the bits in a register group in the order they are passed, using the initial PEC value of 000000000010000 and the following characteristic polynomial: $X^{15} + X^{14} + X^{10} + X^8 + X^7 + X^4 + X^3 + 1$. To calculate the 15-bit PEC value, a simple procedure can be established:

1. Initialize the PEC to 000000000010000 (PEC is a 15-bit register group)
2. For each bit DIN coming into the PEC register group, set

   IN0 = DIN XOR PEC [14]

   IN3 = IN0 XOR PEC [2]

   IN4 = IN0 XOR PEC [3]

   IN7 = IN0 XOR PEC [6]

   IN8 = IN0 XOR PEC [7]

   IN10 = IN0 XOR PEC [9]

   IN14 = IN0 XOR PEC [13]

3. Update the 15-bit PEC as follows

   PEC [14] = IN14,

   PEC [13] = PEC[12],

   PEC [12] = PEC[11],

   PEC [11] = PEC[10],

   PEC [10] = IN10,

   PEC [9] = PEC[8],

   PEC [8] = IN8,

   PEC [7] = IN7,

   PEC [6] = PEC[5],

   PEC [5] = PEC[4],

   PEC [4] = IN4,

   PEC [3] = IN3,

   PEC[2] = PEC[1],

   PEC[1] = PEC[0],

   PEC[0] = IN0.

4. Go back to Step 2 until all the data is shifted. The final PEC (16 bits) is the 15-bit value in the PEC register with a 0 bit appended to its LSB.

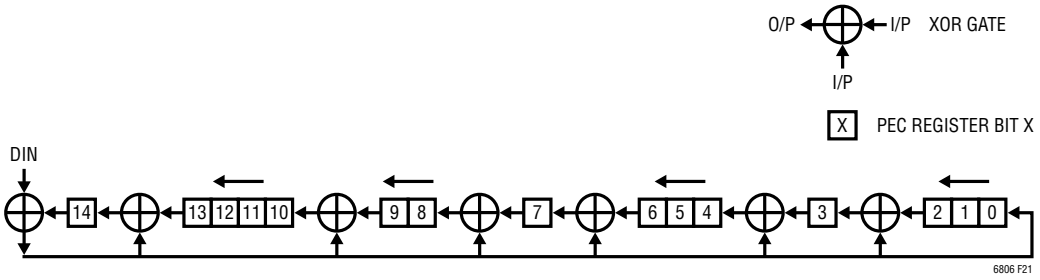


Figure 21. 15-Bit PEC Computation Circuit

OPERATION

Figure 21 illustrates the algorithm described above. An example to calculate the PEC for a 16-bit word (0x0001) is listed in Table 20. The PEC for 0x0001 is computed as 0x3D6E after stuffing a 0 bit at the LSB. For longer data streams, the PEC is valid at the end of the last bit of data sent to the PEC register.

LTC6806 calculates PEC word for any command or data received and compares it with the PEC following the command or data. The command or data is regarded as valid only if the PEC matches. LTC6806 also attaches the calculated PEC word at the end of the data it shifts out. Table 21 shows the format of PEC while writing to or reading from LTC6806.

Table 20. PEC Calculation for 0x0001

PEC[14]	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	0	**0**
PEC[13]	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	1	0	**0**
PEC[12]	0	0	0	0	0	0	0	0	1	0	0	0	0	1	1	0	1	**1**
PEC[11]	0	0	0	0	0	0	0	1	0	0	0	0	1	1	0	1	1	**1**
PEC[10]	0	0	0	0	0	0	1	0	0	0	0	1	1	0	1	1	1	**1**
PEC[9]	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	1	**1**
PEC[8]	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	1	0	**0**
PEC[7]	0	0	0	1	0	0	0	0	0	0	0	1	1	1	0	1	1	**1**
PEC[6]	0	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	**0**
PEC[5]	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	**1**
PEC[4]	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	1	**1**
PEC[3]	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	**0**
PEC[2]	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	**1**
PEC[1]	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	**1**
PEC[0]	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	**1**
IN14	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	0		**0**
IN10	0	0	0	0	0	1	0	0	0	0	1	1	0	1	1	1		**PEC Word**
IN8	0	0	0	1	0	0	0	0	0	0	1	0	0	0	1	0		
IN7	0	0	1	0	0	0	0	0	0	0	1	1	1	0	1	1		
IN4	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	1		
IN3	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0		
IN0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1		
DIN	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1		
Clock Cycle	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

Table 21. Write/Read PEC Format

NAME	RD/WR	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PEC0	RD/WR	PEC[14]	PEC[13]	PEC[12]	PEC[11]	PEC[10]	PEC[9]	PEC[8]	PEC[7]
PEC1	RD/WR	PEC[6]	PEC[5]	PEC[4]	PEC[3]	PEC[2]	PEC[1]	PEC[0]	0

OPERATION

While writing any command to LTC6806, the command bytes CMD0 and CMD1 (see Table 28 and Table 29) and the PEC bytes PEC0 and PEC1 are sent on Port A in the following order:

CMD0, CMD1, PEC0, PEC1

After a broadcast write command to daisy-chained LTC6806 devices, data is sent to each device followed by the PEC. For example, when writing the configuration register group to two daisy-chained devices (primary device P, stacked device S), the data will be sent to the primary device on Port A in the following order:

CFGR0(S), ..., CFGR5(S), PEC0(S), PEC1(S), CFGR0(P), ..., CFGR5(P), PEC0(P), PEC1(P)

After a READ command for daisy-chained devices, each device shifts out its data and the PEC that it computed for its data on Port A followed by the data received on Port B. For example, when reading Status Register Group B from two daisy-chained devices (primary device P, stacked device S), the primary device sends out data on Port A in the following order:

STBR0(P), STBR1(P), …, STBR5(P), PEC0(P),PEC1(P), STBR0(S), STBR1(S), … , STBR5(S), PEC0(S),PEC1(S)

Broadcast Commands

A broadcast command is one to which all devices on the bus will respond, regardless of device address. This command can be used with in either daisy-chained or parallel modes. See Bus Protocols for broadcast command format. With broadcast commands, all devices can be sent commands simultaneously.

In parallel configurations, this is useful for ADC conversion and polling commands. It can also be used with write commands when all parts are being written with the same data. Broadcast read commands should not be used in the parallel configuration.

Daisy-chained configurations only support broadcast commands. All devices in the chain receive the command bytes simultaneously. For example, to initiate ADC conversions in a stack of devices, a single ADCV command is sent, and all devices will start conversions at the same time. For read and write commands, a single command is sent, and then the stacked devices effectively turn into a cascaded shift register, in which data is shifted through each device to the next device in the stack. See the Serial Programming Examples section.

Address Commands

An address command is one in which only the addressed device on the bus responds. Address commands are used only with LTC6806 configured in parallel mode. See Bus Protocols for address command format.

Automatic Incrementing for Address commands

When using an address read command (RDCVA, RDCVB, RDCVC, RDCVD, RDCVE, RDCVF, RDCVG, RDCVG, RDCVH, RDCVI, RDAUXA, RDAUXB, RDSTATA, RDSTATB, RDSTATC), the LTC6806 will send the requested register group data and PEC, then automatically increment to the next related register group. In this way, the host may, for instance, send a RDCVA command and read through all of the cell voltage register groups in a single command. After sending the Cell Voltage Register Group I data and PEC, the LTC6806 will send all 1's.

Polling Methods

The simplest method to determine ADC completion is for the controller to start an ADC conversion and wait for the specified conversion time to pass before reading the results.

In parallel configurations that communicate in SPI mode (ISOMD pin tied low), there are two methods of polling. The first method is to hold CSB low after an ADC conversion command is sent. After entering a conversion command, the SDO line is driven low when the device is busy performing conversions (Figure 22). SDO is pulled high

OPERATION

when the device completes conversions. However, the SDO will also go back high when CSB goes high even if the device has not completed the conversion. An addressed device drives the SDO line based on its status alone. A problem with this method is that the controller is not free to do other serial communication while waiting for ADC conversions to complete. The next method overcomes this limitation. The controller can send an ADC start command, perform other tasks, and then send a poll ADC converter status(PLADC) command to determine the status of the ADC conversions (Figure 23). After entering the PLADC command, SDO will go low if the device is busy performing conversions. SDO is pulled high at the end of conversions. However, the SDO will also go high when CSB goes high even if the device has not completed the conversion. See Programming Examples on how to use the PLADC command with devices in parallel configuration.

In parallel configurations that communicate in isoSPI mode, the low side port transmits a data pulse only in response to a master isoSPI pulse received by it. So, after entering the command in either method of polling described above, isoSPI data pulses are sent to the part to update the conversion status. These pulses can be sent using LTC6820 by simply clocking its SCK pin. In response to this pulse, the device sends back an isoSPI pulse if it is still busy performing conversions and does not return a pulse if it has completed the conversions. If a CSB high isoSPI pulse is sent to the device, it exits the polling command.

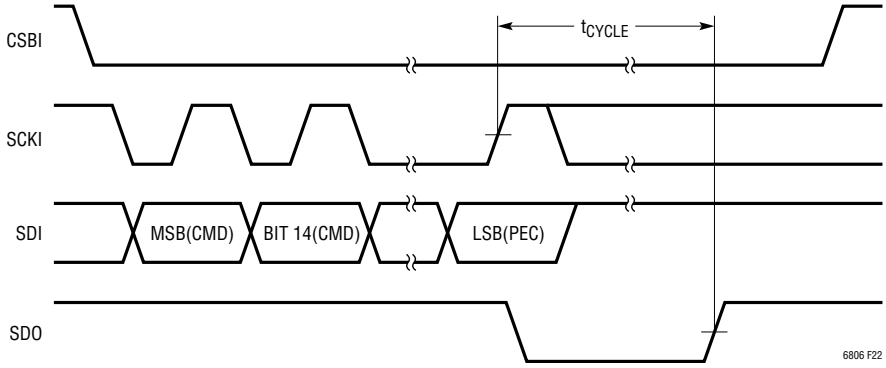


Figure 22. SDO Polling After an ADC Command

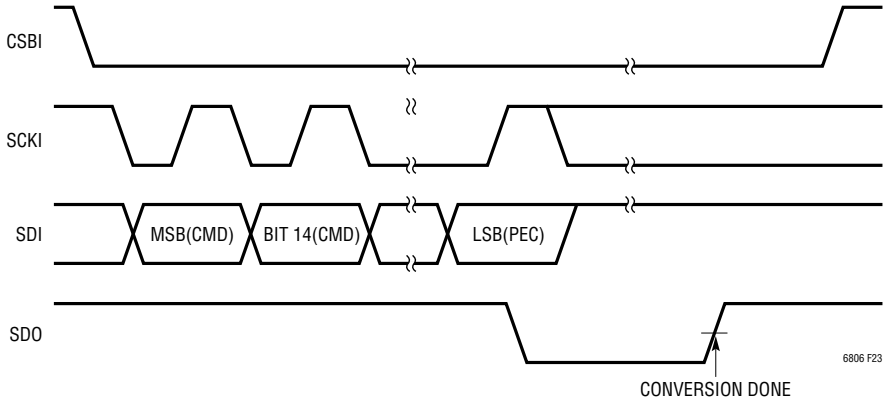


Figure 23. SDO Polling Using PLADC Command

OPERATION

In a daisy-chained configuration of N stacked devices, the same two polling methods can be used. If the bottom device communicates in SPI mode, the SDO of the bottom device indicates the conversion status of the entire stack i.e. SDO will remain low until all the devices in the stack have completed the conversions. In the first method of polling, after an ADC conversion command is sent, clock pulses are sent on SCKI while keeping CSBI low. The SDO status becomes valid only at the end of N clock pulses on SCKI and gets updated for every clock pulse that follows (Figure 24). In the second method, the PLADC command is sent followed by clock pulses on SCKI while keeping CSBI low. Similar to the first method, the SDO status is valid only after N clock cycles on SCKI and gets updated after every clock cycle that follows (Figure 25). See Programming Examples on how to use the PLADC command with N stacked devices.

If the bottom device communicates in isoSPI mode, isoSPI data pulses are sent to the device to update the conversion status. Using LTC6820, this can be achieved by just clocking its SCK pin. The conversion status is valid only after the bottom LTC6806 device receives N isoSPI data pulses and the status gets updated for every isoSPI data pulse that follows. The device returns a low data pulse if any of the devices in the stack is busy performing conversions and returns a high data pulse if all the devices are free.

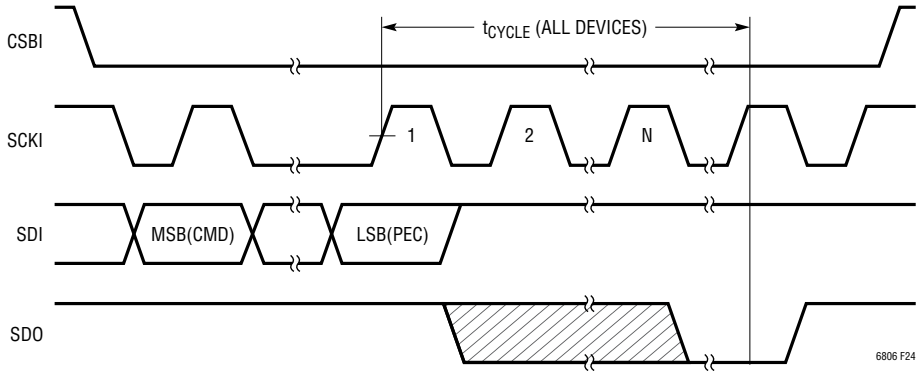


Figure 24. SDO Polling After an ADC Command in a Daisy Chain

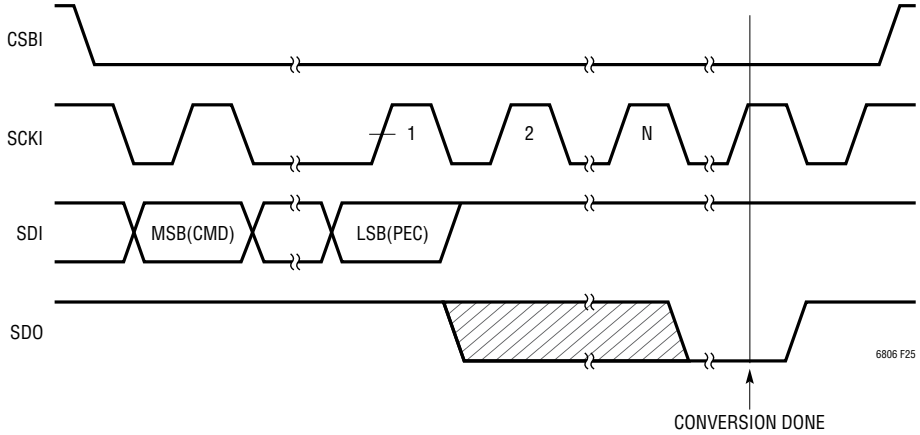


Figure 25. SDO Polling Using the PLADC Command in a Daisy Chain

OPERATION

Bus Protocols

Protocol Format: The protocol formats for both broadcast and address commands are depicted in Table 23 through Table 27. Table 22 is the key for reading the protocol diagrams.

Table 22. Protocol Key

CMD0	First Command Byte (See Table 28 and Table 29)
CMD1	Second Command Byte (See Table 28 and Table 29)
PEC0	First PEC Byte (See Table 21)
PEC1	Second PEC Byte (See Table 21)
n	Number of Bits
…	Continuation of Protocol
	Master to Slave
	Slave to Master

Table 23. Broadcast/Address Poll Command

8	8	8	8	
CMD0	CMD1	PEC0	PEC1	Poll Data

Table 24. Broadcast Write Command

				Data to Device N						Data to Device 1				
8	8	8	8	8		8	8	8		8		8	8	8
CMD0	CMD1	PEC0	PEC1	Data Byte Low	…	Data Byte High	PEC0	PEC1	…	Data Byte Low	…	Data Byte High	PEC0	PEC1

Table 25. Address Write Command

8	8	8	8	8		8	8	8
CMD0	CMD1	PEC0	PEC1	Data Byte Low	…	Data Byte High	PEC0	PEC1

Table 26. Broadcast Read Command

				Data from Device 1						Data from Device N				
8	8	8	8	8		8	8	8		8		8	8	8
CMD0	CMD1	PEC0	PEC1	Data Byte Low	…	Data Byte High	PEC0	PEC1	…	Data Byte Low	…	Data Byte High	PEC0	PEC1

Table 27. Address Read Command

8	8	8	8	8		8	8	8
CMD0	CMD1	PEC0	PEC1	Data Byte Low	…	Data Byte High	PEC0	PEC1

OPERATION

Command Format: The formats for the broadcast and address commands are shown in Table 28 and Table 29 respectively. The 11-bit command code CC[10:0] is the same for a broadcast or an address command. A list of all the command codes is shown in Table 30. A broadcast command has a value 0 for CMD0[7] through CMD0[3]. An address command has a value 1 for CMD0[7] followed by the 4-bit address of the device (a3, a2, a1, a0) in bits CMD0[6:3]. An addressed device will respond to an address command only if the physical address of the device on pins A3 to A0 match the address specified in the address command. The PEC for broadcast and address commands must be computed on the entire 16-bit command (CMD0 and CMD1).

Table 28. Broadcast Command Format

NAME	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CMD0	WR	0	0	0	0	0	CC[10]	CC[9]	CC[8]
CMD1	WR	CC[7]	CC[6]	CC[5]	CC[4]	CC[3]	CC[2]	CC[1]	CC[0]

Table 29. Address Command Format

NAME	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CMD0	WR	1	a3*	a2*	a1*	a0*	CC[10]	CC[9]	CC[8]
CMD1	WR	CC[7]	CC[6]	CC[5]	CC[4]	CC[3]	CC[2]	CC[1]	CC[0]

*ax is Address Bit x

Commands

Table 30 lists all the commands and their options for the LTC6806.

Table 30. Command Codes

		11 BIT COMMAND CODE										
COMMAND DESCRIPTION	NAME	10	9	8	7	6	5	4	3	2	1	0
Write Configuration Register Group	WRCFG	0	0	0	0	0	0	0	0	0	0	1
Read Configuration Register Group	RDCFG	0	0	0	0	0	0	0	0	0	1	0
Read Cell Voltage Register Group A	RDCVA	0	0	0	0	0	0	0	0	1	0	0
Read Cell Voltage Register Group B	RDCVB	0	0	0	0	0	0	0	0	1	0	1
Read Cell Voltage Register Group C	RDCVC	0	0	0	0	0	0	0	0	1	1	0
Read Cell Voltage Register Group D	RDCVD	0	0	0	0	0	0	0	0	1	1	1
Read Cell Voltage Register Group E	RDCVE	0	0	0	0	0	0	0	1	0	0	0
Read Cell Voltage Register Group F	RDCVF	0	0	0	0	0	0	0	1	0	0	1
Read Cell Voltage Register Group G	RDCVG	0	0	0	0	0	0	0	1	0	1	0
Read Cell Voltage Register Group H	RDCVH	0	0	0	0	0	0	0	1	0	1	1

OPERATION

Table 30. Command Codes

COMMAND DESCRIPTION	NAME	11 BIT COMMAND CODE										
		10	9	8	7	6	5	4	3	2	1	0
Read Cell Voltage Register Group I	RDCVI	0	0	0	0	0	0	0	1	1	0	0
Read Auxiliary Register Group A	RDAUXA	0	0	0	0	0	0	1	0	0	0	0
Read Auxiliary Register Group B	RDAUXB	0	0	0	0	0	0	1	0	0	0	1
Read Status Register Group A	RDSTATA	0	0	0	0	0	0	1	0	1	0	0
Read Status Register Group B	RDSTATB	0	0	0	0	0	0	1	0	1	0	1
Read Status Register Group C	RDSTATC	0	0	0	0	0	0	1	0	1	1	0
Start Cell Voltage ADC Conversion and Poll Status	ADCV	1	0	0	MD [1]	MD [0]	CH [5]	CH [4]	CH [3]	CH [2]	CH [1]	CH [0]
Start Open Wire ADC Conversion and Poll Status	ADOW	1	1	PUP	MD [1]	MD [0]	CH [5]	CH [4]	CH [3]	CH [2]	CH [1]	CH [0]
Start Cell Voltage Plus Sum of Cells ADC Conversion and Poll Status	ADCVSC	1	0	0	MD [1]	MD [0]	1	1	0	0	0	0
Start Self-Test Cell Voltage Conversion and Poll Status	CVST	1	ST [1]	ST [0]	MD [1]	MD [0]	1	1	1	1	1	1
Stat GPIOs ADC Conversion and Poll Status	ADAX	0	1	1	MD [1]	MD [0]	1	0	0	AX [2]	AX [1]	AX [0]
Start GPIOs Plus Sum of Cells ADC Conversion and Poll Status	ADAXSC	0	1	1	MD [1]	MD [0]	1	1	0	0	0	0
Start Self-Test GPIOs Conversion and Poll Status	AXST	0	ST [1]	ST [0]	MD [1]	MD [0]	1	1	0	1	1	1
Start Status Group ADC Conversion and Poll Status	ADSTAT	0	1	1	MD [1]	MD [0]	1	0	1	CHST [2]	CHST [1]	CHST [0]
Start Self-Test Status Group Conversion and Poll Status	STATST	0	ST [1]	ST [0]	MD [1]	MD [0]	1	1	1	1	1	1
Clear Cell Voltage Register Group	CLRCELL	0	0	0	0	0	0	1	1	0	0	1
Clear Auxiliary Register Group	CLRAUX	0	0	0	0	0	0	1	1	0	1	0
Clear Status Register Group	CLRSTAT	0	0	0	0	0	0	1	1	0	1	1
Poll ADC Conversion Status	PLADC	0	0	0	0	0	0	1	1	1	0	0
Diagnose MUX and Poll Status	DIAGN	0	0	0	0	0	0	1	1	1	0	1

OPERATION

Table 31. Command Bit Descriptions

NAME	DESCRIPTION	VALUES	
MD[1:0]	ADC Mode	MD	
		00	Fast Mode
		01	Normal Mode
		10	Alternate Mode
		11	Filtered Mode
CH[5:0]	Cell Selection for ADC Conversion	CH	
		000000	All Cells
		000001	Cell 1
		***	
		100100	Cell 36
		> 100100	Invalid Selection
PUP	Pull-Up/Pull-Down Current for Open Wire Conversions	PUP	
		1	Pull-Down Current
		0	Pull-Up Current
ST[1:0]	Self-Test Mode Selection	ST	
		01	Self-Test 1
		10	Self-Test 2
AX[2:0]	AUX Channel Selection	AX	
		000	2^{nd} Reference + GPIO1 – GPIO6
		001	2^{nd} Reference
		010	GPIO1
		011	GPIO2
		100	GPIO3
		101	GPIO4
		110	GPIO5
		111	GPIO6
CHST[2:0]	Status Group Channel Selection	CHST	
		000	SC + ITMP + V^+
		001	SC (Sum of Cells Measurement)
		010	ITMP (Internal Temperature)
		011	V^+ (5V Power Supply)
		>011	Invalid Selection

OPERATION

Memory Map

Table 32. Configuration Register Group

REGISTER	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CFGR0	RD/WR	RSVD	RSVD	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1
CFGR1	RD/WR	HIRNG	REFON	OWPCH[1]	OWPCH[0]	REV[3]	REV[2]	REV[1]	REV[0]
CFGR2	RD/WR	MMD[1]	MMD[0]	FCHNL[5]	FCHNL[4]	FCHNL[3]	FCHNL[2]	FCHNL[1]	FCHNL[0]
CFGR3	RD/WR	VUV[11]	VUV[10]	VUV[9]	VUV[8]	VUV[7]	VUV[6]	VUV[5]	VUV[4]
CFGR4	RD/WR	VUV[3]	VUV[2]	VUV[1]	VUV[0]	VOV[11]	VOV[10]	VOV[9]	VOV[8]
CFGR5	RD/WR	VOV[7]	VOV[6]	VOV[5]	VOV[4]	VOV[3]	VOV[2]	VOV[1]	VOV[0]

Table 33. Cell Voltage Register Group A

REGISTER	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CVAR0	RD	C1V[11]	C1V[10]	C1V[9]	C1V[8]	C1V[7]	C1V[6]	C1V[5]	C1V[4]
CVAR1	RD	C1V[3]	C1V[2]	C1V[1]	C1V[0]	C2V[11]	C2V[10]	C2V[9]	C2V[8]
CVAR2	RD	C2V[7]	C2V[6]	C2V[5]	C2V[4]	C2V[3]	C2V[2]	C2V[1]	C2V[0]
CVAR3	RD	C3V[11]	C3V[10]	C3V[9]	C3V[8]	C3V[7]	C3V[6]	C3V[5]	C3V[4]
CVAR4	RD	C3V[3]	C3V[2]	C3V[1]	C3V[0]	C4V[11]	C4V[10]	C4V[9]	C4V[8]
CVAR5	RD	C4V[7]	C4V[6]	C4V[5]	C4V[4]	C4V[3]	C4V[2]	C4V[1]	C4V[0]

Table 34. Cell Voltage Register Group B

REGISTER	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CVBR0	RD	C5V[11]	C5V[10]	C5V[9]	C5V[8]	C5V[7]	C5V[6]	C5V[5]	C5V[4]
CVBR1	RD	C5V[3]	C5V[2]	C5V[1]	C5V[0]	C6V[11]	C6V[10]	C6V[9]	C6V[8]
CVBR2	RD	C6V[7]	C6V[6]	C6V[5]	C6V[4]	C6V[3]	C6V[2]	C6V[1]	C6V[0]
CVBR3	RD	C7V[11]	C7V[10]	C7V[9]	C7V[8]	C7V[7]	C7V[6]	C7V[5]	C7V[4]
CVBR4	RD	C7V[3]	C7V[2]	C7V[1]	C7V[0]	C8V[11]	C8V[10]	C8V[9]	C8V[8]
CVBR5	RD	C8V[7]	C8V[6]	C8V[5]	C8V[4]	C8V[3]	C8V[2]	C8V[1]	C8V[0]

Table 35. Cell Voltage Register Group C

REGISTER	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CVCR0	RD	C9V[11]	C9V[10]	C9V[9]	C9V[8]	C9V[7]	C9V[6]	C9V[5]	C9V[4]
CVCR1	RD	C9V[3]	C9V[2]	C9V[1]	C9V[0]	C10V[11]	C10V[10]	C10V[9]	C10V[8]
CVCR2	RD	C10V[7]	C10V[6]	C10V[5]	C10V[4]	C10V[3]	C10V[2]	C10V[1]	C10V[0]
CVCR3	RD	C11V[11]	C11V[10]	C11V[9]	C11V[8]	C11V[7]	C11V[6]	C11V[5]	C11V[4]
CVCR4	RD	C11V[3]	C11V[2]	C11V[1]	C11V[0]	C12V[11]	C12V[10]	C12V[9]	C12V[8]
CVCR5	RD	C12V[7]	C12V[6]	C12V[5]	C12V[4]	C12V[3]	C12V[2]	C12V[1]	C12V[0]

OPERATION

Table 36. Cell Voltage Register Group D

REGISTER	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CVDR0	RD	C13V[11]	C13V[10]	C13V[9]	C13V[8]	C13V[7]	C13V[6]	C13V[5]	C13V[4]
CVDR1	RD	C13V[3]	C13V[2]	C13V[1]	C13V[0]	C14V[11]	C14V[10]	C14V[9]	C14V[8]
CVDR2	RD	C14V[7]	C14V[6]	C14V[5]	C14V[4]	C14V[3]	C14V[2]	C14V[1]	C14V[0]
CVDR3	RD	C15V[11]	C15V[10]	C15V[9]	C15V[8]	C15V[7]	C15V[6]	C15V[5]	C15V[4]
CVDR4	RD	C15V[3]	C15V[2]	C15V[1]	C15V[0]	C16V[11]	C16V[10]	C16V[9]	C16V[8]
CVDR5	RD	C16V[7]	C16V[6]	C16V[5]	C16V[4]	C16V[3]	C16V[2]	C16V[1]	C16V[0]

Table 37. Cell Voltage Register Group E

REGISTER	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CVER0	RD	C17V[11]	C17V[10]	C17V[9]	C17V[8]	C17V[7]	C17V[6]	C17V[5]	C17V[4]
CVER1	RD	C17V[3]	C17V[2]	C17V[1]	C17V[0]	C18V[11]	C18V[10]	C18V[9]	C18V[8]
CVER2	RD	C18V[7]	C18V[6]	C18V[5]	C18V[4]	C18V[3]	C18V[2]	C18V[1]	C18V[0]
CVER3	RD	C19V[11]	C19V[10]	C19V[9]	C19V[8]	C19V[7]	C19V[6]	C19V[5]	C19V[4]
CVER4	RD	C19V[3]	C19V[2]	C19V[1]	C19V[0]	C20V[11]	C20V[10]	C20V[9]	C20V[8]
CVER5	RD	C20V[7]	C20V[6]	C20V[5]	C20V[4]	C20V[3]	C20V[2]	C20V[1]	C20V[0]

Table 38. Cell Voltage Register Group F

REGISTER	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CVFR0	RD	C21V[11]	C21V[10]	C21V[9]	C21V[8]	C21V[7]	C21V[6]	C21V[5]	C21V[4]
CVFR1	RD	C21V[3]	C21V[2]	C21V[1]	C21V[0]	C22V[11]	C22V[10]	C22V[9]	C22V[8]
CVFR2	RD	C22V[7]	C22V[6]	C22V[5]	C22V[4]	C22V[3]	C22V[2]	C22V[1]	C22V[0]
CVFR3	RD	C23V[11]	C23V[10]	C23V[9]	C23V[8]	C23V[7]	C23V[6]	C23V[5]	C23V[4]
CVFR4	RD	C23V[3]	C23V[2]	C23V[1]	C23V[0]	C24V[11]	C24V[10]	C24V[9]	C24V[8]
CVFR5	RD	C24V[7]	C24V[6]	C24V[5]	C24V[4]	C24V[3]	C24V[2]	C24V[1]	C24V[0]

Table 39. Cell Voltage Register Group G

REGISTER	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CVGR0	RD	C25V[11]	C25V[10]	C25V[9]	C25V[8]	C25V[7]	C25V[6]	C25V[5]	C25V[4]
CVGR1	RD	C25V[3]	C25V[2]	C25V[1]	C25V[0]	C26V[11]	C26V[10]	C26V[9]	C26V[8]
CVGR2	RD	C26V[7]	C26V[6]	C26V[5]	C26V[4]	C26V[3]	C26V[2]	C26V[1]	C26V[0]
CVGR3	RD	C27V[11]	C27V[10]	C27V[9]	C27V[8]	C27V[7]	C27V[6]	C27V[5]	C27V[4]
CVGR4	RD	C27V[3]	C27V[2]	C27V[1]	C27V[0]	C28V[11]	C28V[10]	C28V[9]	C28V[8]
CVGR5	RD	C28V[7]	C28V[6]	C28V[5]	C28V[4]	C28V[3]	C28V[2]	C28V[1]	C28V[0]

OPERATION

Table 40. Cell Voltage Register Group H

REGISTER	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CVHR0	RD	C29V[11]	C29V[10]	C29V[9]	C29V[8]	C29V[7]	C29V[6]	C29V[5]	C29V[4]
CVHR1	RD	C29V[3]	C29V[2]	C29V[1]	C29V[0]	C30V[11]	C30V[10]	C30V[9]	C30V[8]
CVHR2	RD	C30V[7]	C30V[6]	C30V[5]	C30V[4]	C30V[3]	C30V[2]	C30V[1]	C30V[0]
CVHR3	RD	C31V[11]	C31V[10]	C31V[9]	C31V[8]	C31V[7]	C31V[6]	C31V[5]	C31V[4]
CVHR4	RD	C31V[3]	C31V[2]	C31V[1]	C31V[0]	C32V[11]	C32V[10]	C32V[9]	C32V[8]
CVHR5	RD	C32V[7]	C32V[6]	C32V[5]	C32V[4]	C32V[3]	C32V[2]	C32V[1]	C32V[0]

Table 41. Cell Voltage Register Group I

REGISTER	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CVIR0	RD	C33V[11]	C33V[10]	C33V[9]	C33V[8]	C33V[7]	C33V[6]	C33V[5]	C33V[4]
CVIR1	RD	C33V[3]	C33V[2]	C33V[1]	C33V[0]	C34V[11]	C34V[10]	C34V[9]	C34V[8]
CVIR2	RD	C34V[7]	C34V[6]	C34V[5]	C34V[4]	C34V[3]	C34V[2]	C34V[1]	C34V[0]
CVIR3	RD	C35V[11]	C35V[10]	C35V[9]	C35V[8]	C35V[7]	C35V[6]	C35V[5]	C35V[4]
CVIR4	RD	C35V[3]	C35V[2]	C35V[1]	C35V[0]	C36V[11]	C36V[10]	C36V[9]	C36V[8]
CVIR5	RD	C36V[7]	C36V[6]	C36V[5]	C36V[4]	C36V[3]	C36V[2]	C36V[1]	C36V[0]

Table 42. Auxiliary Register Group A

REGISTER	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
AVAR0	RD	VREF2[11]	VREF2[10]	VREF2[9]	VREF2[8]	VREF2[7]	VREF2[6]	VREF2[5]	VREF2[4]
AVAR1	RD	VREF2[3]	VREF2[2]	VREF2[1]	VREF2[0]	G1V[11]	G1V[10]	G1V[9]	G1V[8]
AVAR2	RD	G1V[7]	G1V[6]	G1V[5]	G1V[4]	G1V[3]	G1V[2]	G1V[1]	G1V[0]
AVAR3	RD	G2V[11]	G2V[10]	G2V[9]	G2V[8]	G2V[7]	G2V[6]	G2V[5]	G2V[4]
AVAR4	RD	G2V[3]	G2V[2]	G2V[1]	G2V[0]	G3V[11]	G3V[10]	G3V[9]	G3V[8]
AVAR5	RD	G3V[7]	G3V[6]	G3V[5]	G3V[4]	G3V[3]	G3V[2]	G3V[1]	G3V[0]

Table 43. Auxiliary Register Group B

REGISTER	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
AVBR0	RD	G4V[11]	G4V[10]	G4V[9]	G4V[8]	G4V[7]	G4V[6]	G4V[5]	G4V[4]
AVBR1	RD	G4V[3]	G4V[2]	G4V[1]	G4V[0]	G5V[11]	G5V[10]	G5V[9]	G5V[8]
AVBR2	RD	G5V[7]	G5V[6]	G5V[5]	G5V[4]	G5V[3]	G5V[2]	G5V[1]	G5V[0]
AVBR3	RD	G6V[11]	G6V[10]	G6V[9]	G6V[8]	G6V[7]	G6V[6]	G6V[5]	G6V[4]
AVBR4	RD	G6V[3]	G6V[2]	G6V[1]	G6V[0]	RSVD	RSVD	RSVD	RSVD
AVBR5	RD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD

OPERATION

Table 44. Status Register Group A

REGISTER	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
STAR0	RD	C40V	C4UV	C30V	C3UV	C20V	C2UV	C10V	C1UV
STAR1	RD	C80V	C8UV	C70V	C7UV	C60V	C6UV	C50V	C5UV
STAR2	RD	C120V	C12UV	C110V	C11UV	C100V	C10UV	C90V	C9UV
STAR3	RD	C160V	C16UV	C150V	C15UV	C140V	C14UV	C130V	C13UV
STAR4	RD	C200V	C20UV	C190V	C19UV	C180V	C18UV	C170V	C17UV
STAR5	RD	C240V	C24UV	C230V	C23UV	C220V	C22UV	C210V	C21UV

Table 45. Status Register Group B

REGISTER	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
STBR0	RD	C280V	C28UV	C270V	C27UV	C260V	C26UV	C250V	C25UV
STBR1	RD	C320V	C32UV	C310V	C31UV	C300V	C30UC	C290V	C29UV
STBR2	RD	C360V	C36UV	C350V	C35UV	C340V	C34UV	C330V	C33UV
STBR3	RD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD
STBR4	RD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD
STBR5	RD	OT	UT	RSVD	RSVD	RSVD	STXFF	STXFS	MUXFAIL

Table 46. Status Register Group C

REGISTER	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
STCR0	RD	SC[11]	SC[10]	SC[9]	SC[8]	SC[7]	SC[6]	SC[5]	SC[4]
STCR1	RD	SC[3]	SC[2]	SC[1]	SC[0]	ITMP[11]	IMTP[10]	ITMP[9]	ITMP[8]
STCR2	RD	ITMP[7]	ITMP[6]	ITMP[5]	ITMP[4]	ITMP[3]	ITMP[2]	ITMP[1]	ITMP[0]
STCR3	RD	V^+[11]	V^+[10]	V^+[9]	V^+[8]	V^+[7]	V^+[6]	V^+[5]	V^+[4]
STCR4	RD	V^+[3]	V^+[2]	V^+[1]	V^+[0]	RSVD	RSVD	RSVD	RSVD
STCR5	RD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD

Table 47. Memory Bit Descriptions

NAME	DESCRIPTION	VALUES
RSVD	Reserved Bit	
GPIOx	GPIOx Pin Control	x = 1 to 6 Write: 0 -> GPIOx Pin Pull-Down ON; 1-> GPIOx Pin Pull-Down OFF Read: 0 -> GPIOx Pin at Logic 0; 1 -> GPIOx Pin at Logic 1 Default: GPIOx = 1
HIRNG	Cell Measurement Range Selection	1 -> Cell Precision Range = –5V to 5V 0 -> Cell Precision Range = –2.5V to 2.5V Default: HIRNG = 0
REFON	Reference Powered Up	1 -> Reference Remains Powered 0 -> Reference Shuts Down after Conversions Default: REFON = 0

OPERATION

Table 47. Memory Bit Descriptions

NAME	DESCRIPTION	VALUES
OWPCH	Open Wire Precharge Time	00 -> 0.1ms 01 -> 1ms 10 -> 10ms 11 -> 100ms Default: OWPCH = 00
REV	Revision Code	Device Revision Code
MMD	Monitor Mode Selection	00 -> Monitoring Disabled 01 -> Monitor in Normal ADC Mode 10 -> Monitor in Alternate ADC Mode 11 -> Monitor in Filtered ADC Mode Default: MMD = 00
FCHNL	First Channel for Monitoring	Specifies First Cell Channel for Monitoring. During the monitor cycle the IC will monitor cell channels from FCHNL to 36, then V_{REF2}, GPIO1 and GPIO2 channels. Valid Range = 1 to 36 Else All Cell Channels Will Be Monitored Default: FCHNL = 0x00
VUV	Undervoltage Comparison Voltage*	Comparison Voltage = VUV • 1.5mV when HIRNG = 0 Comparison Voltage = VUV • 3mV when HIRNG = 1 100mV Hysteresis Is Applied During Monitoring Default: VUV = 0x000
VOV	Overvoltage Comparison Voltage*	Comparison Voltage = VUV • 1.5mV, Cell Measurements with HIRNG = 0 Comparison Voltage = VUV • 3mV, Cell Measurements with HIRNG = 1 100mV Hysteresis Is Applied During Monitoring Default: VOV = 0x000
CxV	Cell ‘x’ Voltage*	x = 1 to 36 12-Bit ADC Measurement Value for Cell ‘x’ Cell Voltage for Cell ‘x’ = CxV • 1.5mV (HIRNG = 0) or 3.0mV (HIRNG = 1) CxV Is Reset To 0XFFF on Power-Up and After Clear Command
AxV	Auxiliary Channel ‘x’ Voltage*	x = 1 to 6 12-Bit ADC Measurement Value for GPIO Channel ‘x’ Voltage for Aux Channel ‘x’ = AxV • 1.5mV AxV Is Reset to 0xFFF on Power-Up and After Clear Command
REF	2nd Reference Voltage*	12-Bit ADC Measurement Value for 2nd Reference Voltage for 2nd Reference = REF • 1.5mV Normal Range Is Within 2.4V to 2.6V REF Is Reset to 0xFFF on Power-Up and After Clear Command
CxOV	Cell ‘x’ Overvoltage Flag	x = 1 to 36 Cell Voltage Compared to VOV Comparison Voltage 0 -> Cell x Not Flagged for Overvoltage Condition. 1 -> Cell x Flagged
CxUV	Cell ‘x’ Undervoltage Flag	x = 1 to 36 Cell Voltage Compared to VUV Comparison Voltage 0 -> Cell x Not Flagged for Undervoltage Condition. 1 -> Cell x Flagged
OT	Over Temperature Flag	Read: 1 -> GPIO2 < V_{REF2}/2 with 100mV Hysteresis Read: 0 -> GPIO2 ≥ V_{REF2}/2 with 100mV Hysteresis Defaults to 1 when Not Monitoring
UT	Under Temperature Flag	Read: 1 -> GPIO1 ≥ V_{REF2}/2 with 100mV Hysteresis Read: 0 -> GPIO1 < V_{REF2}/2 with 100mV Hysteresis Defaults to 1 when Not Monitoring
STXFF	Serial Transfer Self-Test Flag	Read: 0 -> All Previous ADC Commands Since the Last DIAGN Command Have Passed the Serial Transfer Self-Test Read: 1 -> At Least One of the ADC Commands Since the Last DIAGN Command Has Failed the Serial Transfer Self-Test This bit can be asserted by sending the CLRSTAT command.
STXFS	Serial Transfer Self-Test Status	Read: 0 -> The Previous ADC Command Passed the Serial Transfer Self-Test Read: 1 -> The Previous ADC Command Failed the Serial Transfer Self-Test This bit can be asserted by sending the CLRSTAT command.

OPERATION

Table 47. Memory Bit Descriptions

NAME	DESCRIPTION	VALUES
MUXFAIL	Multiplexer Self-Test Result	Read: 0 -> Multiplexer Passed Self-Test Read: 1 -> Multiplexer Failed Self-Test
SC	Sum of Cells Measurement*	12-Bit ADC Measurement Value of the Sum of All Cell Voltages Sum of All Cells Voltage = SC • 1.5mV • 72 SC Is Reset to 0xFFF on Power-Up and After Clear Command
ITMP	Internal Die Temperature*	12-Bit ADC Measurement Value of Internal Die Temperature Temperature Measurement = ITMP • 1.5mV/(4.65mV/K) – 266K ITMP Is Reset to 0xFFF on Power-Up and After Clear Command
V^+	5V Power Supply Voltage*	12-Bit ADC Measurement Value of 5V Power Supply Voltage Analog Power Supply Voltage = V^+ • 1.875mV Normal Range Is within 4.75V to 5.5V V^+ Is Reset to 0xFFF on Power-Up and After Clear Command

* Voltage equations use the decimal value of registers, 0 to 4095 for 12 bits.

PROGRAMMING EXAMPLES

The following examples use a configuration of three stacked LTC6806 devices in daisy-chain mode : bottom (B), middle (M) and top (T). The low side port on the bottom device is configured in SPI mode.

Write Configuration Registers

1. Pull CSBI low.
2. Send WRCFG command (0x0001) and its PEC word (0x3D6E).
3. Send CFGR0 byte of top device, then CFGR1(T), … CFGR5(T), PEC of CFGR0(T) to CFGR5(T).
4. Send CFGR0 byte of middle device, then CFGR1(M), …CFGR5(M), PEC of CFGR0(M) to CFGR5(M).
5. Send CFGR0 byte of bottom device, then CFGR1(B), … CFGR5(B), PEC of CFGR0(B) to CFGR5(B).
6. Pull CSBI high, data latched into all devices on rising edge of CSBI.

Calculation of serial interface time for sequence above:

Number of devices in stack = N

Number of bytes in sequence (B):

Command: 2 (command byte) + 2 (command PEC) = 4

Data: 6 (Data bytes) + 2 (Data PEC) per device = 8 per device

B = 4 + 8 • N

Serial port frequency per bit = F

Time = (1/F) • B • 8 bits/byte = (1/F) • [4 + 8 • N] • 8

Time for 3 cell example above, with 1MHz serial port = (1/1e6) • (4 + 8 • 3) • 8 = 224µs

Note: This time will remain the same for all write and read commands.

Read Cell Voltage Register Group A

1. Pull CSBI low.
2. Send RDCVA command (0x0004) and its PEC word (0x07C2).
3. Read CVAR0 byte of bottom device, then CVAR1(B), … CVAR5(B), PEC of CVAR0(B) to CVAR5(B).
4. Read CVAR0 byte of middle device, then CVAR1(M), …CVAR5(M), PEC of CVAR0(M) to CVAR5(M).
5. Read CVAR0 byte of top device, then CVAR1(T), … CVAR5(T), PEC of CVAR0(T) to CVAR5(T).
6. Pull CSBI high.

OPERATION

Start Cell Voltage ADC Conversion

(All cells, normal mode and poll status)

1. Pull CSBI low.
2. Send ADCV command with MD = 1 and i.e. 0x0440 and its PEC word (0xEDB0).
3. SDO output of the bottom device is pulled for the duration of the conversion (~ 10.3ms).
4. SDO output goes high indicating conversions are complete for all devices in the daisy chain.
5. Pull CSBI high to exit polling.

Clear Cell Voltage Registers

1. Pull CSBI low.
2. Send CLRCELL command (0x0011) and its PEC word (0x6640).
3. Pull CSBI high.

Poll ADC Status

(Daisy-chained configuration, 3 stacked devices)

1. Pull CSBI low.
2. Send PLADC command (0x001C) and its PEC word (0xB4E2).
3. Continue to send clock pulses on SCK.
4. SDO output of bottom device is valid after the 3rd clock pulse (for 3 stacked devices).
5. SDO is updated after every clock pulse after the 3rd pulse.
6. SDO is low if ADC conversions are not complete and goes high if conversions are complete for all devices in the daisy chain.
7. Pull CSBI high to exit polling.

Poll ADC Status

(Parallel configuration)

This example uses an addressed LTC6806 device with address A [3:0] = 0011.

1. Pull CSBI low.
2. Send PLADC command (0x981C) and its PEC word (0x5BC6).
3. SDO output is pulled low if the device is busy.
4. SDO output is high if the device has completed conversions.
5. Pull CSBI high to exit polling.

APPLICATIONS INFORMATION

PROVIDING DC POWER

Power Supply Connections

The LTC6806 draws its power from the V^+ pin. 4.75V to 5.5V should be supplied to V^+. A DC to DC converter can drive V^+. V^- and V^{-*} pins should be shorted together externally. V^+ should be bypassed by a quality 1µF capacitor, located close to the supply pins of the IC.

When using the 4-wire SPI mode, port A may be connected directly to a microprocessor. This connection will require that the processor share its logic ground with the V^- of the LTC6806, and pass its 5V power to V^+. This is not an isolated circuit, so the processor will operate at the potential of the cell group, possibly at a dangerous potential. In many cases the processor is powered and interfaced to other equipment with isolated circuitry that can make this a safe practice.

Generating an Isolated Supply

A DC to DC converter and a data isolator can be used in the SPI path to the microprocessor as shown in Figure 26, which features the integrated power and data isolation µModule®, the LTC2883-5S. This arrangement allows the microprocessor to operate at a safe potential and avoid ground noise coupling as well. Note that the 4-wire SPI is not intended for transmission over a significant distance, so it is best for circuits that share a circuit board.

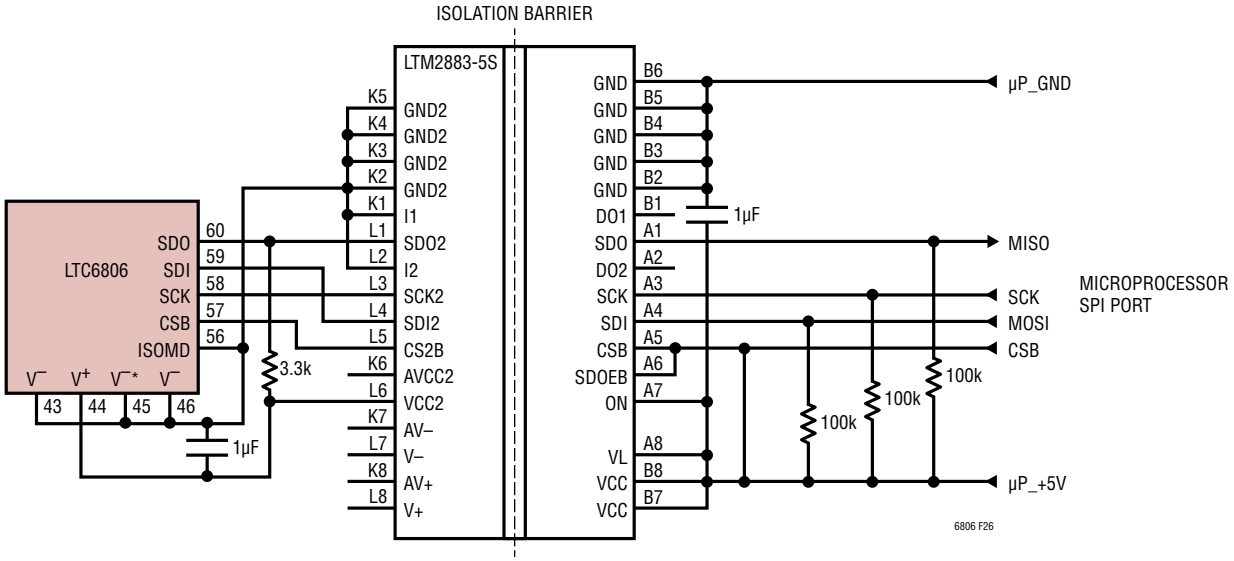


Figure 26. Providing Fully Isolated Power and 4-Wire SPI Communication.

APPLICATIONS INFORMATION

Designs that use the isoSPI interface will need to implement an isolated supply to power the LTC6806. Figure 27 shows an example of a fully isolated power supply that can be used. The isolated power supply uses a no-opto isolated flyback converter that requires only a single 210k resistor to program the output voltage. on the isolated side, a Zener diode is required to regulate the supply voltage in low load situations, such as when the LTC6806 is in STANDBY or IDLE mode. For the lowest power consumption, the isolated supply can be disabled either by removing the 7V-12V supply or disabling the part via the EN pin.

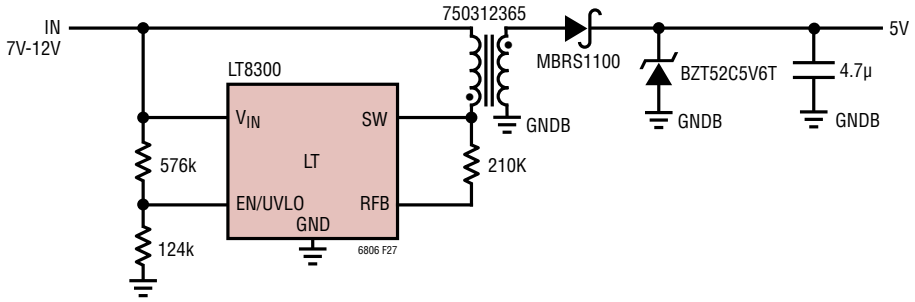


Figure 27. Providing Fully Isolated Data Link and Power Over Long Interconnections.

DIGITAL COMMUNICATIONS

PEC Calculation

The Packet Error Code(PEC) provides confidence that the serial data read from the LTC6806 is valid and has not been corrupted by any external noise source. This checking feature is critical for reliable communication; the part requires that a PEC be calculated for all data being read from and written to the LTC6806. For this reason it is important to have an efficient method for calculating the PEC. The C code below demonstrates a simple implementation of a lookup table derived PEC calculation method. There are two functions. The first function init_PEC15_Table() should only be called once when the microprocessor starts; the function will initialize a PEC15 table array called pec15Table[]. This table will be used in all future PEC calculations. The PEC15 table can also be hard coded into the microprocessor rather than running the init_PEC15_Table() function at startup. The pec15() function calculates the PEC and will return the correct 15-bit PEC for byte arrays of any given length.

APPLICATIONS INFORMATION

```
/*****************************************
Copyright 2012 Linear Technology Corp. (LTC)
Permission to freely use, copy, modify, and distribute this software for any
purpose with or without fee is hereby granted, provided that the above
copyright notice and this permission notice appear in all copies:
THIS SOFTWARE IS PROVIDED "AS IS" AND LTC DISCLAIMS ALL WARRANTIES
INCLUDING ALL IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS. IN NO
EVENT SHALL LTC BE LIABLE FOR ANY SPECIAL, DIRECT, INDIRECT, OR CONSEQUENTIAL
DAMAGES OR ANY DAMAGES WHATSOEVER RESULTING FROM ANY USE OF SAME, INCLUDING
ANY LOSS OF USE OR DATA OR PROFITS, WHETHER IN AN ACTION OF CONTRACT, NEGLIGENCE
OR OTHER TORTUOUS ACTION, ARISING OUT OF OR IN CONNECTION WITH THE USE OR
PERFORMANCE OF THIS SOFTWARE.
*****************************************************/
int16 pec15Table[256];
int16 CRC15_POLY = 0x4599;
void init_PEC15_Table()
{
      for (int i = 0; i < 256; i++)
      {
            remainder = i << 7;
            for (int bit = 8; bit > 0; --bit)
            {
                  if (remainder & 0x4000)
                  {
                        remainder = ((remainder << 1));
                        remainder = (remainder ^ CRC15_POLY)
                  }
                  else
                  {
                        remainder = ((remainder << 1));
                  }
            }
      pec15Table[i] = remainder&0xFFFF;
      }
}
unsigned int16 pec15 (char *data , int len)
{
      int16 remainder,address;
      remainder = 16;//PEC seed
      for (int i = 0; i < len; i++)
      {
            address = ((remainder >> 7) ^ data[i]) & 0xff;//calculate PEC table address
            remainder = (remainder << 8 ) ^ pec15Table[address];
      }
      return (remainder*2);//The CRC15 has a 0 in the LSB so the final value must be multiplied by 2
}
```

APPLICATIONS INFORMATION

CONFIGURING isoSPI HARDWARE

isoSPI I_{BIAS} and I_{CMP} Setup

The LTC6806 allows the isoSPI links of each application to be optimized for power consumption or for noise immunity. The power and noise immunity of an isoSPI system is determined by the programmed I_B current, which controls the isoSPI signaling currents. Bias current I_B can range from 100µA to 1mA. Internal circuitry scales up this bias current to create the isoSPI signal currents equal to be 20 • I_B. A low I_B reduces the isoSPI power consumption in the READY and ACTIVE states, while a high I_B increases the amplitude of the differential signal voltage V_A across the matching termination resistor, R_M. The I_B current is programmed by the sum of the R_{B1} and R_{B2} resistors connected between the 2V IBIAS pin and GND as shown in Figure 28. The receiver input threshold is set by the ICMP voltage that is programmed with the resistor divider created by the R_{B1} and R_{B2} resistors. The receiver differential threshold will be half of the voltage present on the ICMP pin.

The following guidelines should be used when setting the bias current (100µA to 1mA) I_B and the receiver comparator threshold voltage $V_{ICMP}/2$:

R_M = Transmission Line Characteristic Impedance Z_0

Signal Amplitude $V_A = (20 • I_B) • (R_M/2)$

V_{TCMP} (Receiver Comparator Threshold) = K • V_A

V_{ICMP} (Voltage on ICMP pin) = 2 • V_{TCMP}

$R_{B2} = V_{ICMP}/I_B = 20 • K • R_M$

$R_{B1} = (2/I_B) – R_{B2}$

Select I_B and K (ratio of Receiver Comparator to Signal Amplitude V_A) according to the application:

For lower power links: I_B = 0.5mA and K = 0.5

For full power links: I_B = 1mA and K = 0.5

For long links (>50m): I_B = 1mA and K = 0.25

For addressable multidrop: I_B = 1mA and K = 0.4

For applications with little system noise, setting I_B to 0.5mA is a good compromise between power consumption and noise immunity. Using this I_B setting with a 1:1 transformer and R_M = 100Ω, R_{B1} should be set to 3.01k and R_{B2} set to 1k. With typical CAT5 twisted pair, these settings will allow for communication up to 50m. Applications in very noisy environments or with cables longer than 50m should increase the I_B to 1mA. Higher drive current compensates for the increased insertion loss in the cable and provides high noise immunity. When using cables over 50m and a transformer with a 1:1 turns ratio and R_M = 100Ω, R_{B1} would be 1.5k and R_{B2} would be 499Ω.

The length of the cable determines the maximum clock rate of an isoSPI link. For cables 10 meters or less, the maximum 1MHz SPI clock frequency is possible. As the length of the cable increases, the maximum possible SPI clock rate decreases. This dependence is a result of the increased propagation delays that can create possible timing violations. Figure 29 shows how the maximum data rate reduces as the cable length increases when using a CAT5 twisted pair.

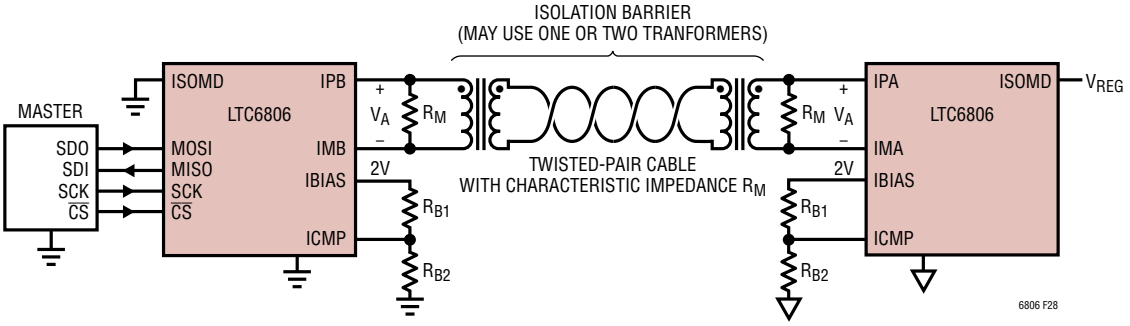


Figure 28. isoSPI Circuit

APPLICATIONS INFORMATION

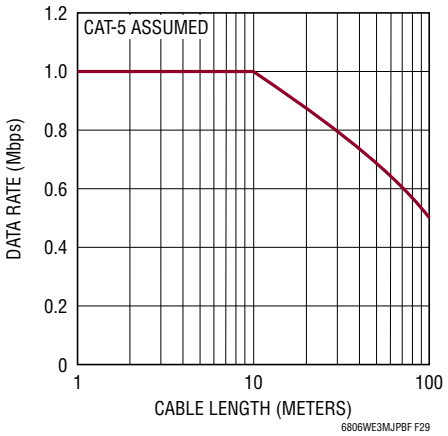


Figure 29. Data Rate vs Cable Length

Cable delay affects three timing specifications, t_{CLK}, t6 and t7. In the Electrical Characteristics table, each is derated by 100ns to allow for 50ns of cable delay. For longer cables, the minimum timing parameters obey the following relationship:

t_{CLK}, t_6 and $t_7 > 0.9\mu s + 2 \bullet t_{CABLE}$ (0.2m per ns)

Implementing a Modular isoSPI Daisy Chain

The hardware design of a daisy-chain isoSPI bus is identical for each device in the network due to the daisy-chain point to point architecture. Basic circuitry in Figure 28 shows a nominally functional, but not optimized configuration. The termination resistor R_M should be split and bypassed with a capacitor as shown in Figure 30. This change provides both a differential and common mode termination, and as such increases the system noise immunity. The use of cables between fuel cell modules, particularly in automotive applications, can lead to increased noise susceptibility in the communication lines. For high levels of electromagnetic interference (EMC), additional filtering is recommended. The circuit example in Figure 30 shows the use of common-mode chokes (CMC). The CMC provides the best common-mode noise rejection from transients present on the lines. Center tapped transformers will also provide additional noise performance. A bypass capacitor connected to the center tap creates a low impedance to the common mode noise (Figure 30a). Typically, center tapped transformers are more expensive than transformers without a center tap. Noise rejection of transformers without a center tap can be enhanced by adding ~100pF bypass capacitance at the IC (Figure 30b). Large center tap capacitors greater than 10nF should be avoided as they may prevent the isoSPI common mode voltage from settling. Common mode chokes similar to what are used in Ethernet or CAN bus applications are recommended, with some particular types suggested in Table 49.

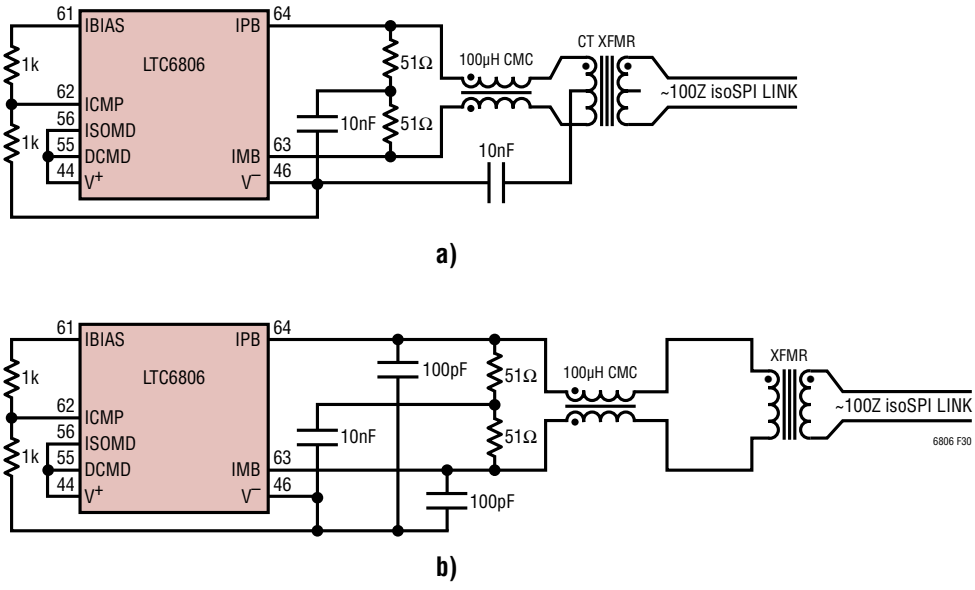


Figure 30. Daisy Chain Interface Components

APPLICATIONS INFORMATION

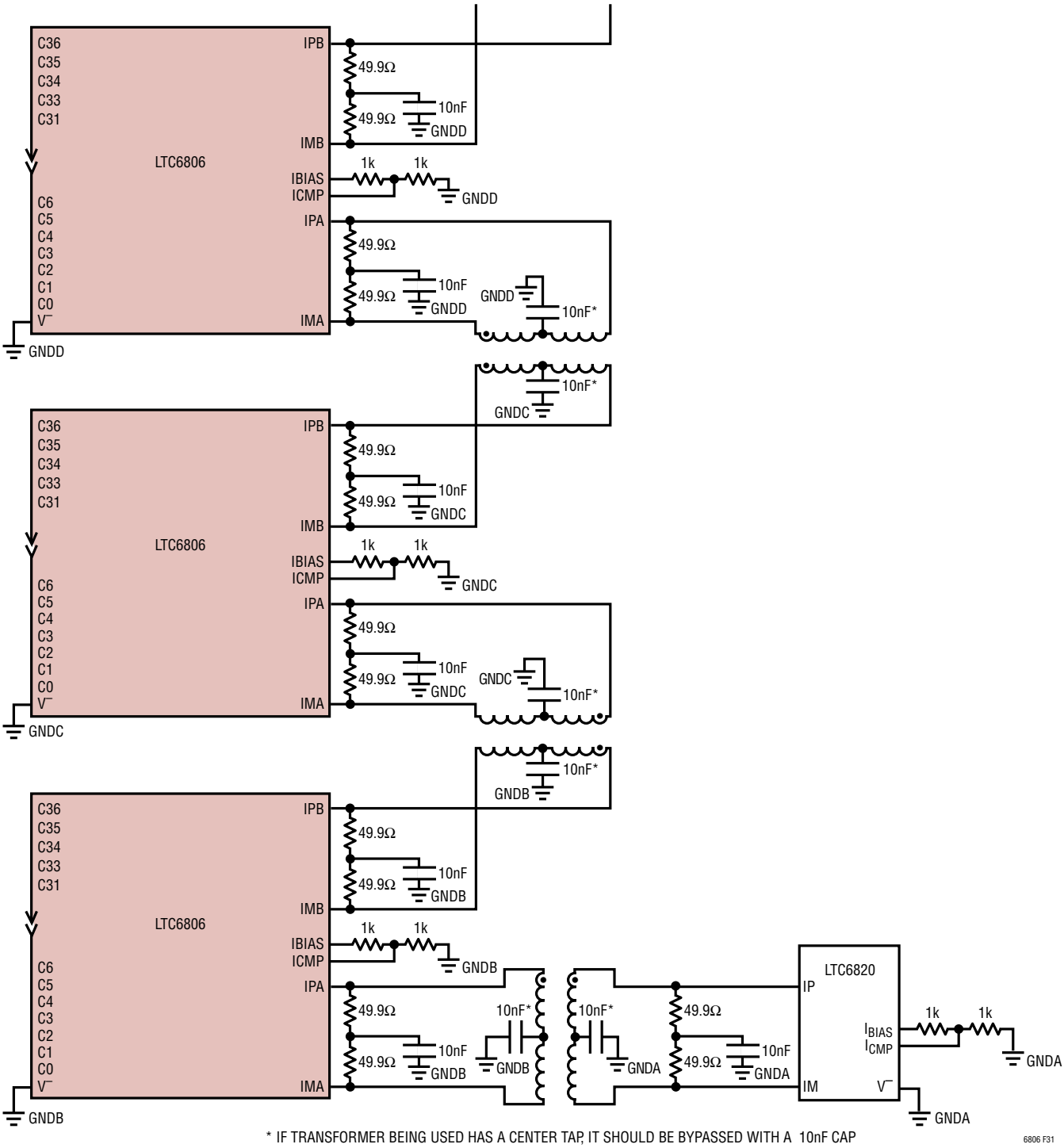


Figure 31. Daisy Chain Interface Components on Single Board

APPLICATIONS INFORMATION

The other main design consideration for a daisy chain is the number of devices in the network. The length of the chain will determine the serial timing as well as affect the data latency and throughput of the isoSPI network. The number of devices in a daisy chain has no limit as long as all serial timing requirements are met. The main limitations are the serial read back times and increased current consumption. For a daisy chain, two timing considerations for proper operation dominate (see Figure 19):

1. T6, the time between the last clock and the rising chip select must be long enough.
2. T5, the time between commands, so the time from a rising chip select to the next falling chip select must be long enough.

Both T5 and T6 must be lengthened as the number of LTC6806 devices in the daisy chain increase. The equations for these times are below:

T5 > (#Devices • 70ns) + 900nS

T6 > (#Devices • 70ns) + 950nS

Connecting a MCU to an LTC6806 with an isoSPI Data Link

The LTC6820 will convert standard 4-wire SPI into a 2-wire isoSPI link that can communicate directly with the LTC6806. An example is shown in Figure 32. The LTC6820 can be used in applications to provide isolation between the microprocessor and the stack of LTC6806s. The LTC6820 also enables system configurations that have the BMS controller at a remote location relative to the LTC6806 devices and the fuel cell pack.

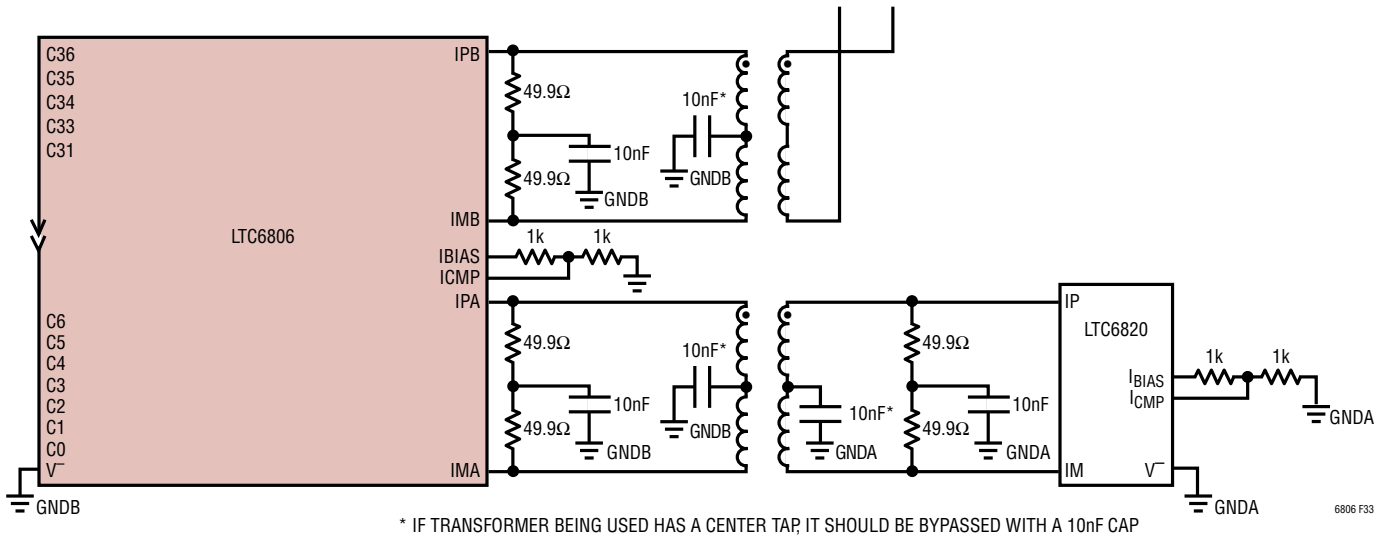


Figure 32. Interfacing an LTC6806 with a µP Using a LTC6820 for Isolated SPI Control

APPLICATIONS INFORMATION

Connecting Multiple LTC6806s on the Same PCB in a Daisy Chain

When connecting multiple LTC6806 devices on the same PCB, only a single transformer needs to connect LTC6806 daisy-chain isoSPI ports. The absence of the cable also reduces the noise levels on the communication lines and often only a split termination is required. Figure 31 shows an example application that has multiple LTC6806s on the same PCB with communication to the bottom MCU through a LTC6820 isoSPI driver. While no center tap is required, if a transformer with a center tap is being used, a capacitor can be added for better noise rejection. If additional noise filtering is required, the noise filters shown in Figure 30 can be implemented and discrete common mode chokes can be added to either side of the single transformer.

On single board designs with low noise requirements, it is possible for a simplified capacitor-isolated coupling as shown in Figure 33 to replace the transformer. Dual Zeners are used at each IC to clamp the common mode voltage to stay within the receivers input range. The common mode choke (CMC) provides high frequency noise rejection with the split terminations. The 590Ω resistor serves to create a resistor divider with the termination resistors to attenuate low frequency common mode noise.

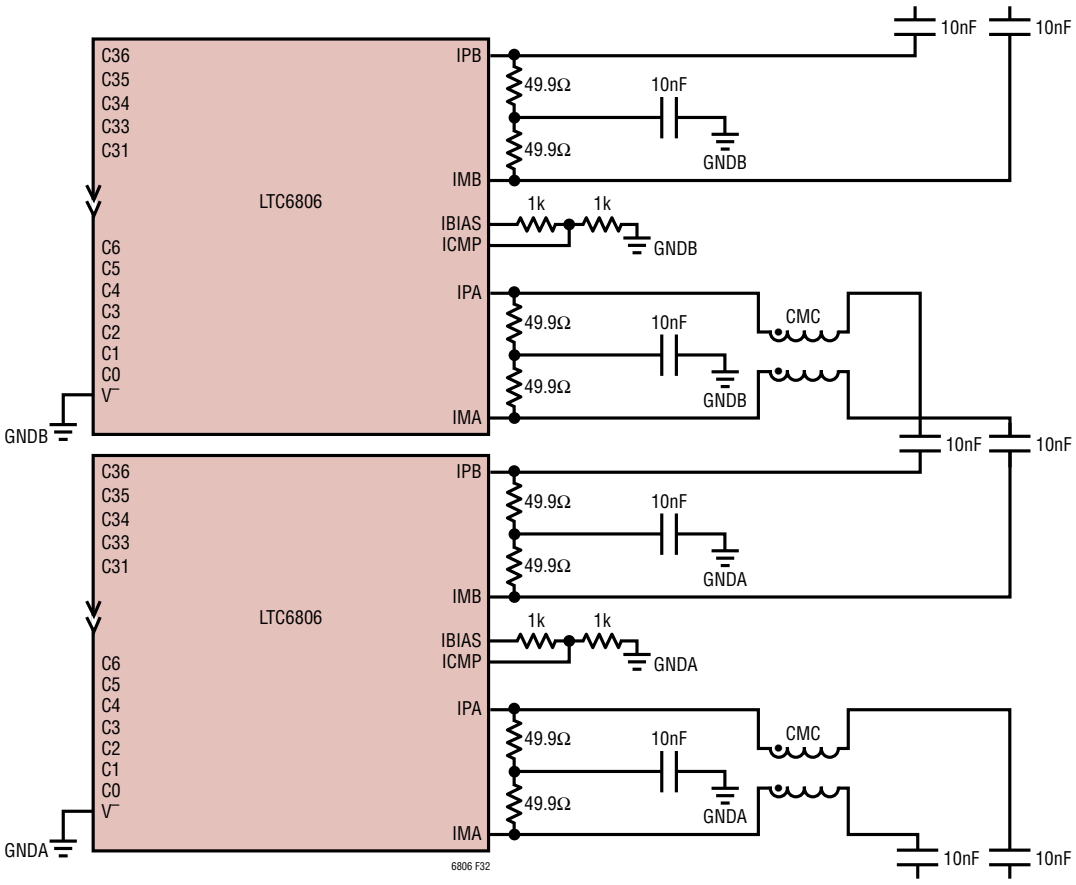


Figure 33. Capacitive Isolation Coupling for LTC6806s on the Same PCB.

APPLICATIONS INFORMATION

Configuring the LTC6806 in a Multi–Drop isoSPI Link

The addressing feature of the LTC6806 allows multiple devices to be connected to a single isoSPI master by distributing them along one twisted pair, essentially creating a large parallel SPI network. Figure 34 shows a basic multidrop system with the twisted pair being terminated only at the beginning (master) and the end. In between, the additional LTC6806s connect to short stubs on the twisted pair. These stubs should be kept short, with as little capacitance as possible, to avoid degrading the termination along the isoSPI wiring. When an LTC6806 is not addressed, it will not transmit data pulses. This scheme eliminates the possibility for collisions, as only the addressed device will ever be returning data to the master. Generally, multidrop systems are best confined to compact assemblies to avoid excessive isoSPI pulse-distortion and EMC pickup.

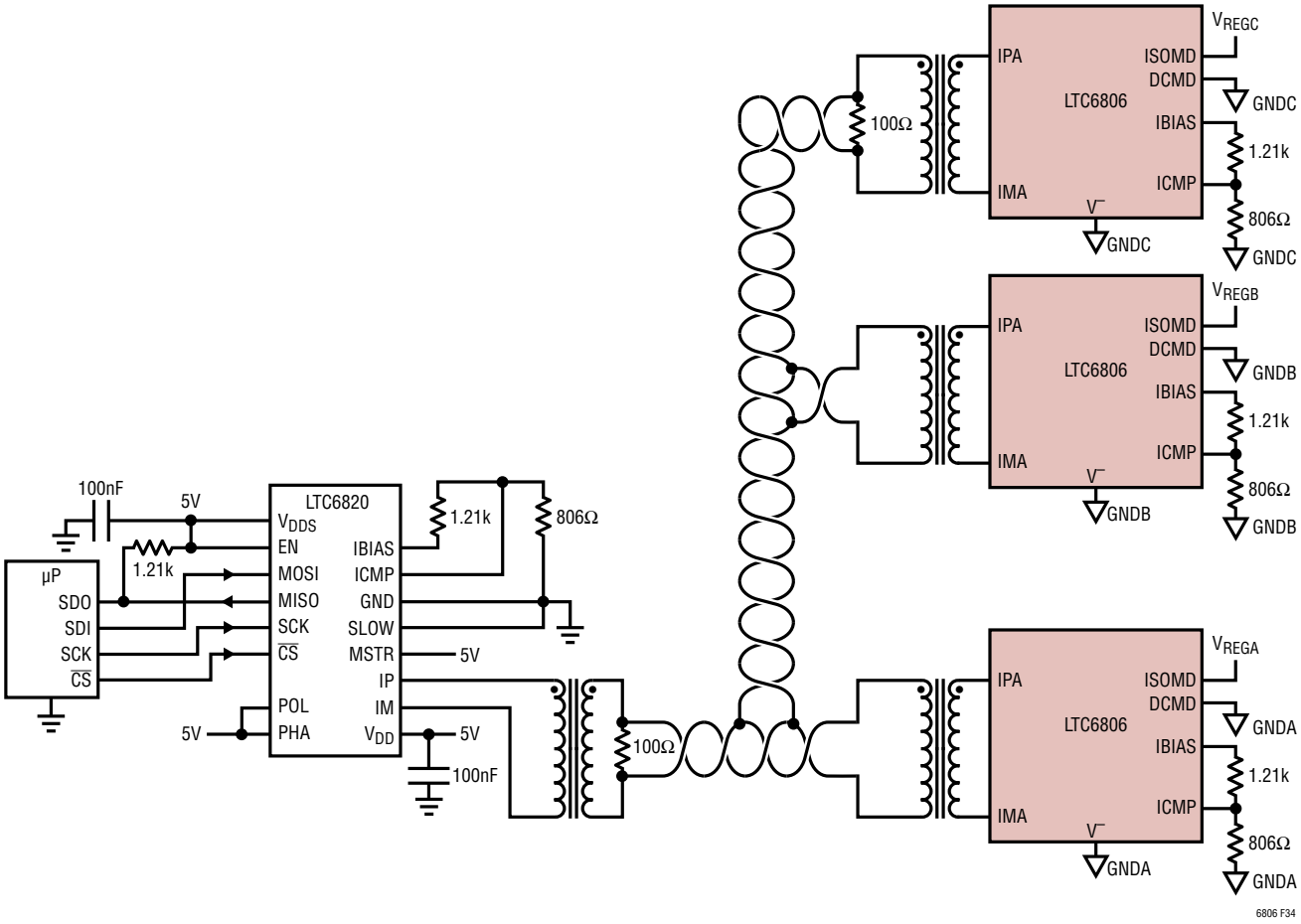


Figure 34. A Simplified Multi-Drop Implementation with a LTC6806 Array

APPLICATIONS INFORMATION

Basic Connection of the LTC6806 in a Multi-Drop Configuration

In a multi-drop isoSPI bus, placing the termination at the ends of the live transmission line will have the best performance (with 100Ω typically). Each of the LTC6806 and LTC6820 isoSPI ports should couple to the bus with through networks as shown in Figure 35. With center-tapped transformers, Figure 35 a offers the best performance; a common-mode-choke is increase the noise rejection further. Figure 35 also shows the used of an RC snubber at the IC connections as a means to suppress resonances (the IC capacitance provides sufficient out-of-band rejection). When using a non-center-tapped transformer, a virtual CT can be generated by connecting a CMC as a voltage-splitter as indicated in Figure 35b. In both configurations, series resistors are used to tap the actual isoSPI bus transmission lines to decouple the IC and board parasitic capacitances from the transmission line. Reducing parasitics on the transmission line minimizes reflections and pulse distortion. Note resistances and pin connections of the isoSPI programming resistors in this mode.

Transformer Selection Guide

As shown in Figure 28, a transformer or pair of transformers isolate the isoSPI signals between two isoSPI ports. The isoSPI signals have programmable pulse amplitudes up to $1.6V_{P-P}$ and pulse widths of 50nS and 150nS. To be able to transmit these pulses with the necessary fidelity, the system requires that the transformers have primary inductances above 60µH and a 1:1 turns ratio. It is also necessary to use a transformer with less than 2.5µH of leakage inductance. In terms of pulse shape the primary inductance mostly affects the pulse droop of the short isoSPI pulses. If the primary inductance is too low, the pulse amplitude will begin to droop and decay over the pulse period. When the pulse droop is severe enough, the effective pulse width seen by the receiver will drops substantially, reducing noise margin. Some droop is acceptable as long as it is a relatively small percentage of the total pulse amplitude. The leakage inductance primarily affects the rise and fall times of the pulses. Slower rise and fall times reduce the pulse width. Pulse width is determined by the receiver as the time the signal is above the threshold set by the ICMP pin. Slow rise and

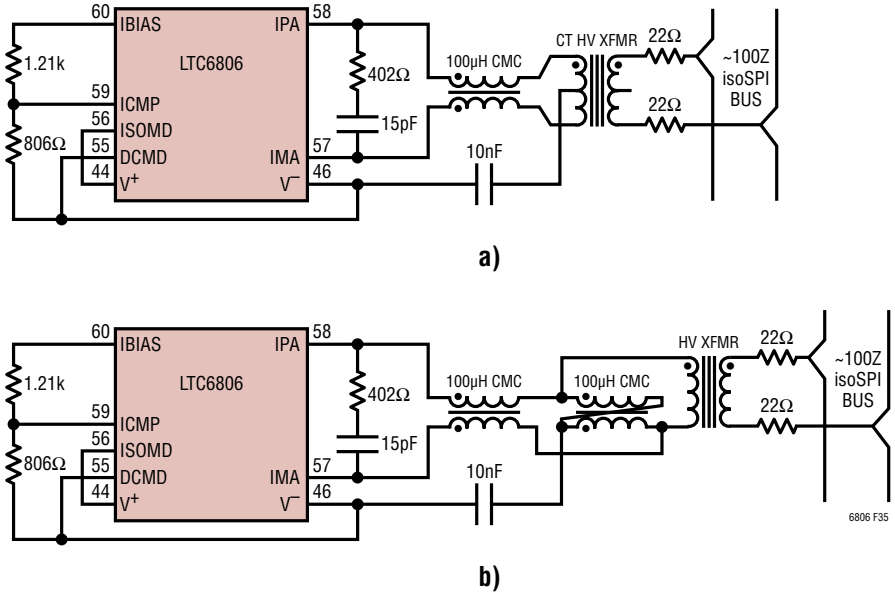


Figure 35. Preferred isoSPI Bus Couplings for Use with LTC6806 and LTC6820

APPLICATIONS INFORMATION

Table 48. Recommended Transformers

Supplier	Part Number	Temp Range	Vworking	Vhipot/60s	CT	CMC	H	L	W (w/ leads)	Pins	AEC-Q200
Bourns	SM91501AL	–40°C to 125°C	1000V	4.3kVdc	●	●	5.0mm	15.0mm	14.7mm	12SMT	●
Bourns	SM13105L (AS4562)	–40°C to 125°C	1600V	4.3kVrms	●	●	5.0mm	15.0mm	27.9mm	12SMT	-
Bourns	US4374	–40°C to 125°C	950V	4.3kVdc	●	●	4.9mm	15.6mm	24.0mm	12SMT	●
Jingweida	S12502BA	–40°C to 125°C	1000V	4.3kVdc	●	●	5.0mm	14.8mm	14.8mm	12SMT	●
Halo	TG110-AE050N5LF	–40°C to 85/125°C	60V (est)	1.5kVrms	●	●	6.4mm	12.7mm	9.5mm	16SMT	●
Sumida	CLP178-C20114	–40°C to 125°C	1000V (est)	3.75kVrms	●	●	9mm	17.5mm	15.1mm	12SMT	-
Sumida	CLP0612-C20115		600Vrms	3.75kVrms	●	-	5.7mm	12.7mm	9.4mm	16SMT	-
Pulse	HM2100NL	–40°C to 105°C	1000V	4.3kVdc	-	●	3.5mm	14.7mm	15.0mm	10SMT	●
Pulse	HM2112ZNL	–40°C to 125°C	1600V	4.3kVdc	●	●	3.5mm	14.7mm	15.5mm	12SMT	●
Pulse	HX1188FNL	–40°C to 85°C	60V (est)	1.5kVrms	●	●	6.0mm	12.7mm	9.7mm	16SMT	-
Pulse	HX0068ANL	–40°C to 85°C	60V (est)	1.5kVrms	●	●	2.1mm	12.7mm	9.7mm	16SMT	-
Wurth	7490140110	–40°C to 85°C	250Vrms	4kVrms	●	●	10.9mm	24.6mm	17.0mm	16SMT	-
Wurth	7490140111	0°C to 70°C	1000V (est)	4.5kVrms	●	-	8.4mm	17.1mm	15.2mm	12SMT	-
Wurth	749014018	0°C to 70°C	250Vrms	4kVrms	●	●	8.4mm	17.1mm	15.2mm	12SMT	-

Recommended Single Transformers

Supplier	Part Number	Temp Range	Vworking	Vhipot/60s	CT	CMC	H	L	W (w/ leads)	Pins	AEC-Q200
Bourns	SM91502AL	–40°C to 125°C	1000V	4.3kVdc	●	●	6.5mm	8.5mm	8.9mm	6SMT	●
Bourns	SM13102AL (US4195)	–40°C to 125°C	800V	4kVrms	●	●	3.8mm	11.6mm	21.1mm	6SMT	-
Halo	TD04-QXLTAW	–40°C to 85°C	1000V (est)	5kVrms	●	-	8.6mm	8.9mm	16.6mm	6TH	-
Halo	TGR04-6506V6LF	–40°C to 125°C	300V	3kVrms	●	-	10mm	9.5mm	12.1mm	6SMT	-
Halo	TGR04-A6506NA6NL	–40°C to 125°C	300V	3kVrms	●	-	9.4mm	8.9mm	12.1mm	6SMT	●
Halo	TDR04-A550ALLF	–40°C to 105°C	1000V	5kVrms	●	-	6.4mm	8.9mm	16.6mm	6TH	●
Jingweida	S06107BA	–40°C to 125°C	1000V (est)	4.3kVdc	●	●	6.3mm	7.6mm	9.9mm	6SMT	-
Pulse	HM2101NL	–40°C to 105°C	1000V	4.3kVdc	-	●	5.7mm	7.6mm	9.3mm	6SMT	●
Pulse	HM2113ZNL	–40°C to 125°C	1600V	4.3kVdc	●	●	3.5mm	9mm	15.5mm	6SMT	●
Sumida	CEEH96BNP-LTC6804/11	–40°C to 125°C	600V	2.5kVrms	-	-	7mm	9.2mm	12.0mm	4SMT	-
Sumida	CEP99NP-LTC6804	–40°C to 125°C	600V	2.5kVrms	●	-	10mm	9.2mm	12.0mm	8SMT	-
Sumida	ESMIT-4180/A	–40°C to 105°C	250Vrms	3kVrms	-	-	3.5mm	5.2mm	9.1mm	4SMT	●
Sumida	ESMIT-4187	–40°C to 105°C	>400Vrms (est)	2.5kVrms	-	-	3.5mm	7.5mm	12.8mm	4SMT	●
TDK	VMT40DR-201S2P4	–40°C to 125°C	600V (est)	3.4kVdc	●	-	4.0mm	8.5mm	13.8mm	6SMT	●
TDK	ALT4532V-201-T001	–40°C to 105°C	80V	~1kV	●	-	2.9mm	3.2mm	4.5mm	6SMT	●
TDK	VGT10/9EE-204S2P4	–40°C to 125°C	700V	2.8kVrms	●	-	10.6mm	10.4mm	12.6mm	8SMT	●
Sunlord	ALTW0806C-C03	–40°C to 125°C	300V (est)	3kVrms	●	-	8.8mm	6.3mm	8.9mm	6SMT	●
Wurth	750340848	–40°C to 105°C	250V	3kVrms	-	-	2.2mm	4.4mm	9.1mm	4SMT	-
XFMRS	XFBMC29-BA09	–40°C to 85°C	1600V (est)	2.9kVrms	●	●	5.0mm	10.0mm	19.5mm	6SMT	●

APPLICATIONS INFORMATION

fall times cut into the timing margins. Generally it is best to keep pulse edges as fast as possible. When evaluating transformers, it is also worth noting the parallel winding capacitance. While transformers have very good CMRR at low frequency, this rejection will degrade at higher frequencies due to the winding to winding capacitance. When choosing a transformer, it is best to pick one with minimal winding capacitance.

When choosing a transformer, it is equally important to pick a part that has an adequate isolation rating for the application. The working voltage rating of a transformer is a key spec when selecting a part for an application. Interconnecting daisy-chain links between LTC6806 daisy-chain devices see <60V stress in typical applications; ordinary pulse and LAN type transformers will suffice. Multi-drop connections and connections to the LTC6820 in general may need much higher working voltage ratings for good long term reliability. Usually matching the working voltage to the voltage of the entire fuel cell stack is conservative. Unfortunately, transformer vendors often specify only one-second HV testing. This rating is not equivalent to the long term (permanent) rating of the part. For example, according to most safety standards a 1.5kV rated transformer is expected to handle 230V continuously, and a 3kV device is capable of 1100V long term, though manufacturers may not always certify to those levels (refer to actual vendor data for specifics). Usually the higher voltage transformers are called high isolation or reinforced insulation types by the suppliers. Table 48 shows a list of transformers that have been evaluated in isoSPI links.

In most applications a common mode choke (CMC) is also necessary for noise rejection. Table 49 includes a list of suitable CMCs if the CMC is not already integrated into the transformer being used.

Table 49. Recommended Common Mode Chokes

MANUFACTURER	PART NUMBER
TDK	ACT45B-101-2P
Murata	DLW43SH101XK2

APPLICATIONS INFORMATION

isoSPI Layout Guidelines

Layout of the isoSPI signal lines also plays a significant role in maximizing the noise immunity of a data link. The following layout guidelines are recommended:

1. The transformer should be placed as close to the isoSPI cable connector as possible. The distance should be kept less than 2cm. The LTC6806 should be placed close to the transformer to minimize loss. However, leave at least 1cm to 2cm between the transformer and LTC6806 to isolate the IC from magnetic field coupling.
2. A V^- ground plane should not extend under the transformer, the isoSPI connector, nor in between the transformer and the connector.
3. The isoSPI signal traces should be as direct as possible while isolated from adjacent circuitry by ground metal or space. No traces should cross the isoSPI signal lines, unless separated by a ground plane on an inner layer.

Calculating Serial Throughput

For any given LTC6806 the calculation to determine communication time is simple: it is the number of bits in the transmission multiplied by the SPI clock period being used. The control protocol of the LTC6806 can be organized in such as way that almost all commands can be categorized as a write, read or an operation. The tables below can be used to determine the number of bits in a given LTC6806 command. Table 50 can be used for daisy chains and Table 51 for multi-drop networks.

Table 50. Daisy-Chain Serial Equations

COMMAND TYPE	CMD BYTES + CMD PEC	DATA BYTES + DATA PEC PER IC	TOTAL BITS	COMMUNICATION TIME
Read	4	8	(4 + (8 • #ICs)) • 8	Total Bits • Clock Period
Write	4	8	(4 + (8 • #ICs)) • 8	Total Bits • Clock Period
Operation	4	0	4 • 8 = 32	32 • Clock Period

Table 51. Multi-Drop Serial Time Equations

COMMAND TYPE	CMD BYTES + CMD PEC	DATA BYTES + DATA PEC PER IC	TOTAL BITS	COMMUNICATION TIME
Read	4	8	((4 + 8) • #ICs) • 8	Total Bits • Clock Period
Write	4	8	((4 + 8) • #ICs) • 8	Total Bits • Clock Period
Operation	4	0	4 • 8 = 32	32 • Clock Period

APPLICATIONS INFORMATION

Protection Components Between the Cell Stack and the C Inputs

ESD protection in the LTC6806 on the cell channels arises from bidirectional SCR devices from each C pin directly to V^-. The positive SCR voltages are graduated, starting at 80V on the lower C inputs and rising to 150V on the upper C inputs as shown in Figure 36. Negative SCR voltages vary, but are all in excess of the abs max rating of –20V. Internal 150kΩ series resistance between the C pins and internal circuitry provides robust ESD performance and limits input current.

System design must take into account the absolute maximum voltage ratings on each pin and provide external clamps and series resistance if there is a chance that electrical overstress above the absolute maximum ratings will be applied to any pin.

FILTERING OF CELL AND GPIO INPUTS

The LTC6806 uses a delta-sigma ADC with a delta sigma modulator followed by a SINC2 finite impulse response (FIR) digital filter. This ADC method greatly reduces input filtering requirements. Furthermore, the programmable oversampling ratio allows the user to determine the best trade-off between measurement speed and filter cutoff frequency. Even with this high order low pass filter, however, fast transients can still induce some residual noise in measurements, especially in the faster conversion modes. Addition of an RC low pass filter at each ADC input can reduce noise sensitivity and help to reject potentially damaging high energy transients.

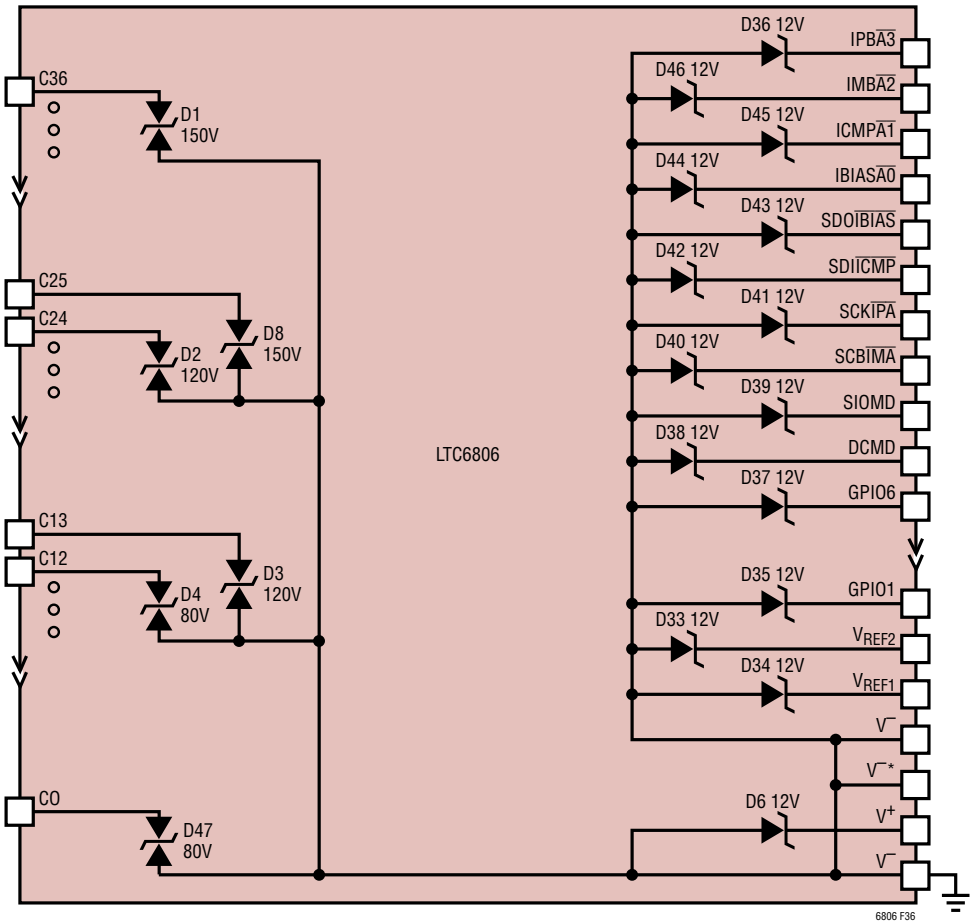


Figure 36. Internal ESD Protection Diagram

APPLICATIONS INFORMATION

For applications that demand the highest level of voltage ripple rejection, grounded capacitor filtering is recommended. This configuration uses a series resistors and capacitors that decouple HF noise to V–. The capacitors in this circuit require adequate voltage rating inasmuch as they directly connect between C pins and ground.

In systems where noise is less periodic or higher oversample rates are in use, a differential capacitor filter structure is adequate. In this configuration, there are series resistors to each input, but the capacitors connect between the adjacent C pins. However, the differential capacitor sections interact. As a result, the filter response is less consistent and results in less attenuation than predicted by the RC, by approximately a decade. Note that the capacitors only see one cell of applied voltage (thus smaller and lower cost) and tend to distribute transient energy uniformly across the IC (reducing stress events on the internal protection structures).

The LTC6806 can accommodate a wide range of external filter components on both the C and GPIO pins if a few simple principles are followed.

C Pins

Adjacent C pins combine to present approximately 300k differential resistance, and sink approximately 35µA per pin when a cell voltage is being measured. When the device is in standby or sleep modes, C pins held at 0V or higher common mode voltage will leak less than 1.6µA. C pins held below 0V common mode may source up to 550µA depending on the cell voltage and mode. Please refer to the I_{LM} and I_{LO} parameters in the specification table, and the graph showing LTC6806 Typical Input Current vs Cell Common Mode Voltage in the Typical Performance Characteristics section for more information.

The LTC6806 is designed to accommodate a wide range of series resistance between each fuel cell connection and the corresponding C pin for signal filtering and input protection. If values 1k or greater are used, it may be necessary for the user to make an accuracy correction to the gain based on the voltage divider ratio $1+R_{IN}/150k$ where R_{IN} is the differential resistance in series with the C pin.

A capacitance of up to 1µF may be used across adjacent C pins for noise filtering purposes. During Open Wire Detection, this capacitance must be charged in order to sense an open circuit, making it necessary to activate open wire detect for some time period before performing cell readings. With a 0.1µF filter capacitor, this time is approximately 10ms. Refer to Table 16 (Open Wire Pre-charge Configurations) as a guide for how much time should be chosen in open wire detection as a function of capacitance.

Input filter capacitance can also effect accuracy, depending on the RC time constant (t_{RC}). Small input filter capacitance values where t_{RC} is significantly less than the sampling time will converge toward the calculated error factor. Larger input filter capacitance values where t_{RC} is significantly larger than the sampling time will converge toward the uncorrected result.

GPIO Pins

Because the GPIO pins are not measured during open wire detection, filter capacitance is not limited. There is an equivalent input impedance of about 600kΩ when the GPIO pins are being read by the ADC. Accuracy depends on the source impedance of circuitry driving the GPIO pins in relation to 600k.

Correcting Filter Resistor Induced Gain Error

RC filters connecting to C pins are frequently used for noise rejection and overvoltage protection, as shown in Figure 37. Because LTC6806 sinks or sources currents from C pins during cell measurement, the IR drops across the filter resistor will affect the system gain. The gain error introduced by the external resistor can be corrected by simply multiplying the cell measurement data with a gain correction factor:

$$G = \frac{150k\Omega + R}{150k\Omega}$$

where R stands for the total resistance between a battery node and the C pin the node connects to. For example, when choosing 1kΩ filter resistor as shown in Figure 37, the gain correction factor will be:

APPLICATIONS INFORMATION

$$G = \frac{150k\Omega + 1k\Omega}{150k\Omega} \approx 1.0067$$

The 150kΩ represents the internal resistor connected to each C pin. Notice that the gain error correcting scheme applies to both HiRng and LoRng mode. The above gain correction should be applied when using little or no filter capacitance at the C pins. When using large filter capacitance, such as ≥ 22nF, the error is negligible and gain correction may not be necessary.

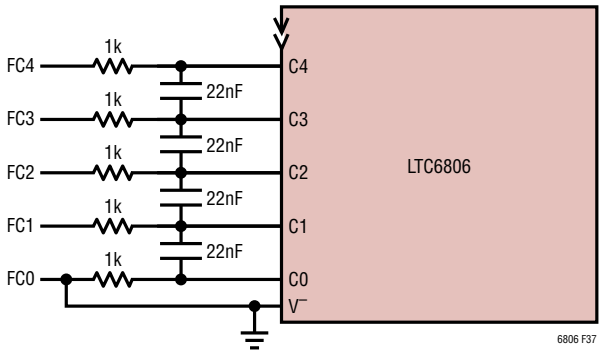


Figure 37.

Using the LTC6806 with Fewer than 36 Cells

The LTC6806 may be used with fewer than 36 inputs; however, care should be exercised to ensure that all cell pin voltage restrictions are followed. It is recommended that the upper C pins should be populated and the unused C pins be shorted to V^+.

The maximum voltage applied between the C pins and V^- is graduated, with higher numbered C pins having a higher limit. Please refer to the Electrical Characteristic table and Absolute Maximum Ratings tables for more information.

The LTC6806 measurement cycle will continue to measure voltages on the unused C pins; unused pins may NOT be left floating. In the MONITOR state the LTC6806 will start each monitor cycle by measuring the cell specified by FCHNL in the Configuration Register Group and continue measuring all cells up to cell 36.

ENHANCED APPLICATIONS

Reading External Temperature Probes

The V_{REF2} pin of the LTC6806 can be used to provide currents of up to 1mA in order to drive thermistors or diodes used for external temperature sensing, which may then be monitored through the GPIO pins.

Because V_{REF2} is not as accurate as V_{REF1}, these temperature measurements are most accurately made by reading both the GPIO pin and the internally monitored V_{REF2} voltage, and deriving the temperature reading from the ratio of the two measurements.

Figure 38 shows the typical biasing circuit for a negative-temperature-coefficient (NTC) thermistor. The 10kΩ at 25°C is the most popular sensor value and the V_{REF2} output stage is designed to provide the current required to bias several of these probes. The biasing resistor is selected to correspond to the NTC value so the circuit will provide 1.25V at 25°C (V_{REF2} is 2.5V nominal). The overall circuit response is approximately –1%/°C in the range of typical cell temperatures, as shown in the chart of Figure 38.

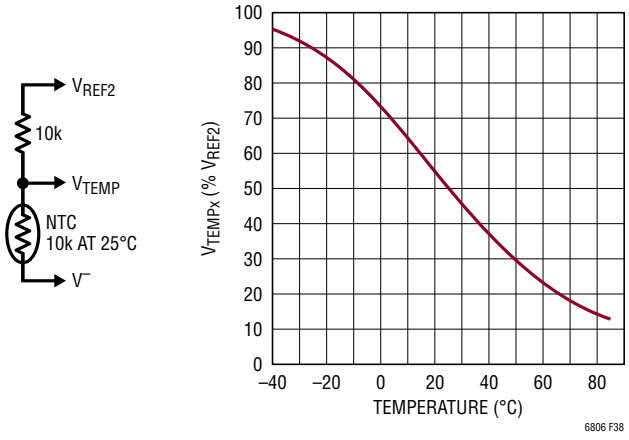


Figure 38. Typical Temperature Probe Circuit and Relative Output

APPLICATIONS INFORMATION

Current Measurement with a Hall Effect Sensor

The LTC6806 auxiliary ADC inputs (GPIO pins) may be used for any analog signal measurement, including those from various active sensors that have 0V to 5V analog outputs. One classic example is sensing of fuel cell stack current. Hall-effect sensors are popular for measuring large currents since the technology provides an isolated, low power dissipation solution.Figure 39 shows schematically a typical Hall sensor that produces two outputs that proportion to the V_{CC} provided. The sensor in the figure has two bidirectional outputs centered at half of supply, CH1 is a 0A to 50A low range and CH2 is a 0A to 200A high range. The sensor is powered from a 5V source and produces analog outputs that are connected to GPIO pins. The use of GPIO1 and GPIO2 as the ADC inputs has the possibility of being digitized within the same conversion sequence as the sum-of-cells (using the ADAXSC command), thus synchronizing cell voltage and cell current measurements.

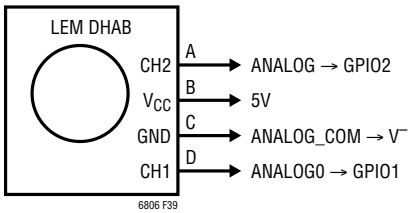


Figure 39. Interfacing a Typical Hall-Effect Current Sensor to Auxiliary ADC Inputs

Monitoring Multiple Fuel Cells on a Single Channel

The LTC6806 is capable of monitoring multiple fuel cells per cell channel. This capability allows the system to monitor more than 36 fuel cells per IC. Monitoring multiple fuel cells per channel reduces the system's ability to determine the exact voltage of the individual fuel cells. However, the system will still be able to determine whether any fuel cell is operating within its expected voltage range. The LTC6806 has two measurement ranges: a low range that measures from –2.5V to 2.5V and a high range that measures from –5V to 5V. In low range the LTC6806 is capable of monitoring up to two 1.2V fuel cells, while in high range (HIRNG = 1) the part is capable of monitoring up to four 1.2V fuel cells. Figure 40 show the LTC6806 monitoring 4 cells per channel. Setting the correct ADC measurement range is the only design action required. The C pin filter and protection circuits are identical when monitoring single fuel cell or multiple fuel cells.

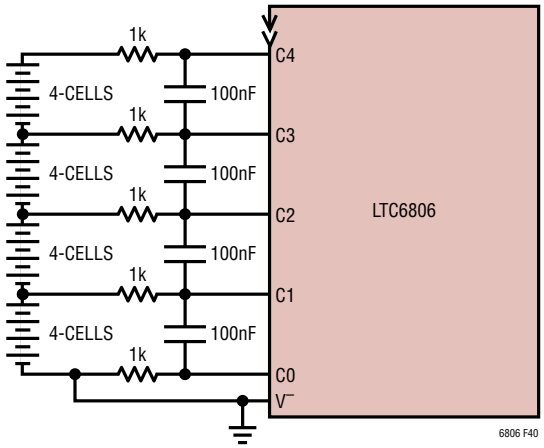


Figure 40. Monitoring Up to Four Cells per Channel

APPLICATIONS INFORMATION

Using the LTC6806 in Monitor Mode

The LTC6806 can be programmed to independently monitor the C pins for under and overvoltage faults without constant interaction with the controlling MCU. In monitor mode GPIO1 and GPIO2 can be used as general purpose analog fault flags. In the independent monitor mode, faults can be detected either by reading the device registers or by monitoring the GPIO pins. Figure 41 shows the GPIOs interfacing with opto-couplers so that an isolated MCU can monitor the fuel cells state independently of the isoSPI port. Figure 41 also shows GPIO1 and GPIO2 configured to monitor the fuel cell system for overtemperature conditions. Two standard 10k thermistors are used and the second resistor is chosen so that the voltage on the GPIO pin will be $V_{REF}/2$ at the overtemperature threshold.

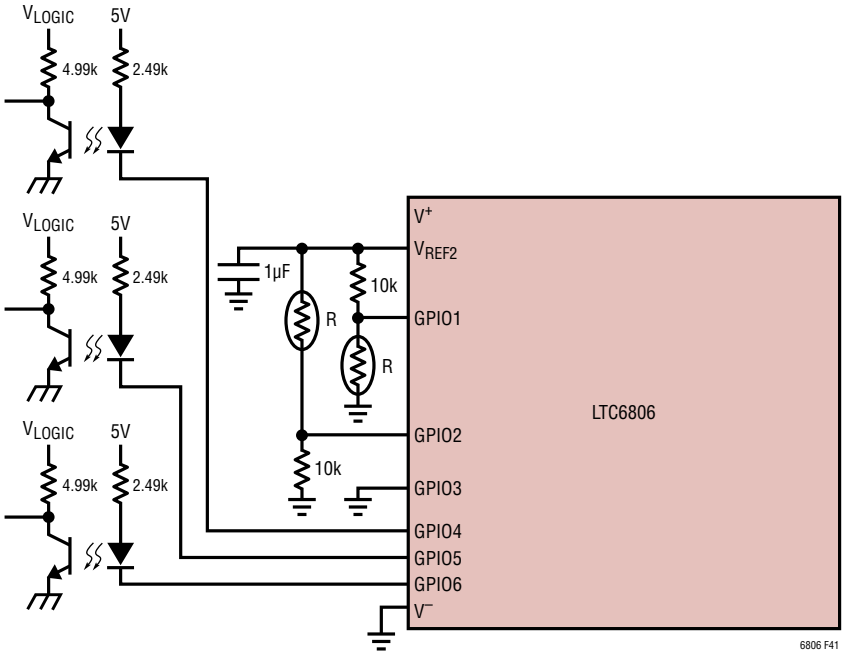
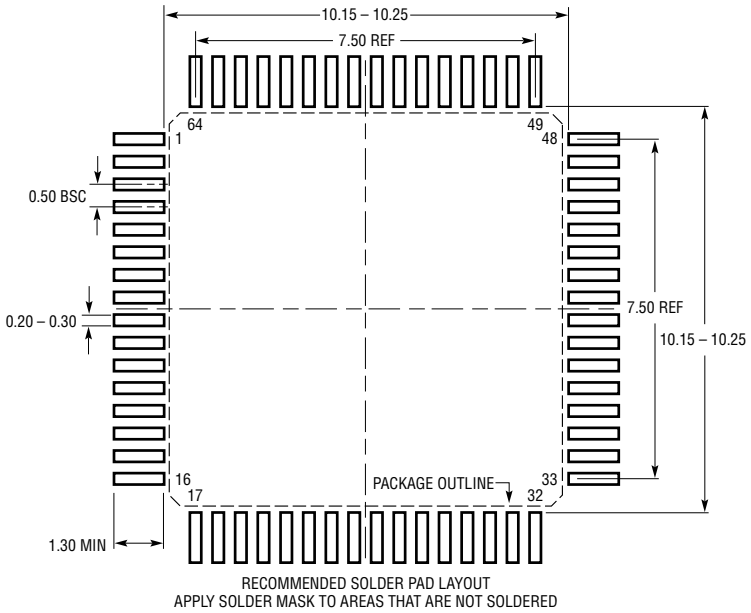
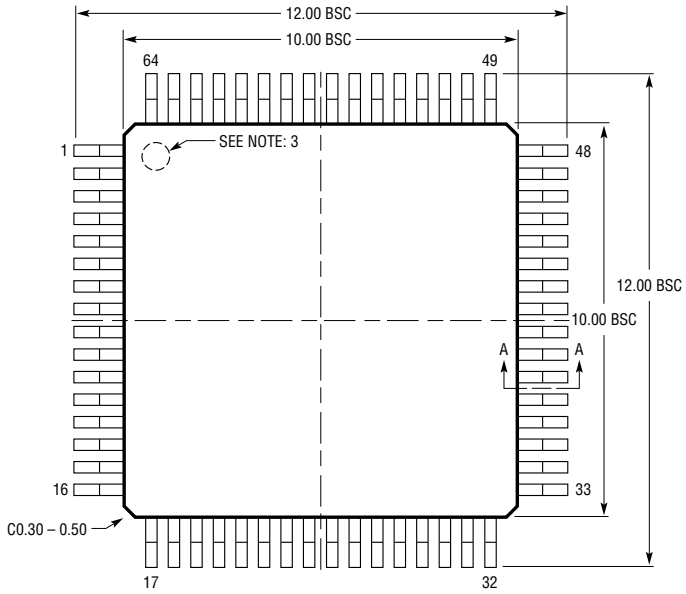


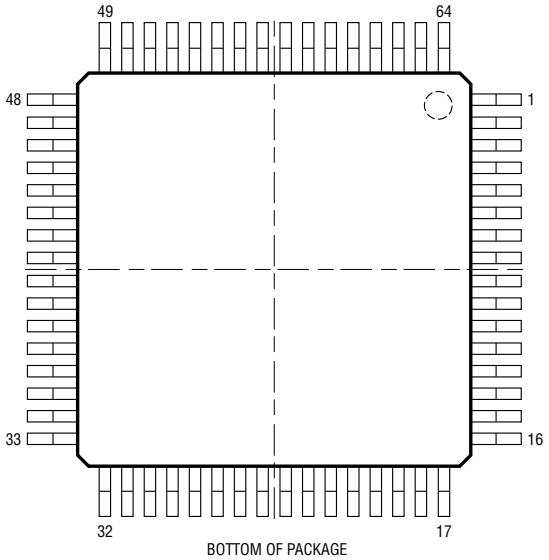
Figure 41. Monitor Mode Connections

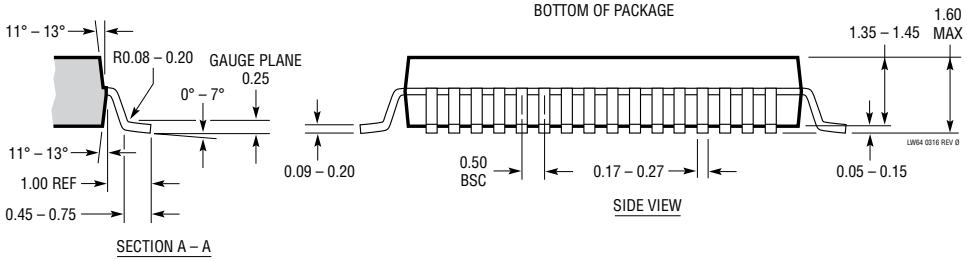
PACKAGE DESCRIPTION

LW Package
64-Lead Plastic LQFP (10mm × 10mm)
(Reference LTC DWG #05-08-1539 Rev Ø)









NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DIMENSIONS OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.25mm ON ANY SIDE. IF PRESENT
3. PIN-1 INDENTIFIER IS A MOLDED INDENTATION, 0.50mm DIAMETER
4. DRAWING IS NOT TO SCALE

Rev 0

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC6810	4th Generation 6-Cell Battery Stack Monitor and Balancing IC	Measures Cell Voltages for Up to 6 Series Battery Cells. The isoSPI Daisy-Chain Capability Allows Multiple Devices to be Interconnected for Measuring Many Battery Cells Simultaneously. The isoSPI Bus can Operate Up to 1MHz and can be Operated Bidirectionally for Fault Conditions, such as a Broken Wire or Connector. Includes Internal Passive CellBalancing Capability of up to 150mA.
LTC6811	4th Generation 12-Cell Battery Stack Monitor and Balancing IC	Measures Cell Voltages for Up to 12 Series Battery Cells. The isoSPI Daisy-Chain Capability Allows Multiple Devices to be Interconnected for Measuring Many Battery Cells Simultaneously. The isoSPI Bus can Operate Up to 1MHz. Includes Internal Passive CellBalancing Capability of up to 30mA.
LTC6812	4th Generation 15-Cell Battery Stack Monitor and Balancing IC	Measures Cell Voltages for Up to 15 Series Battery Cells. The isoSPI Daisy-Chain Capability Allows Multiple Devices to be Interconnected for Measuring Many Battery Cells Simultaneously. The isoSPI Bus can Operate Up to 1MHz and can be Operated Bidirectionally for Fault Conditions, such as a Broken Wire or Connector. Includes Internal Passive CellBalancing Capability of up to 200mA.
LTC6813	4th Generation 18-Cell Battery Stack Monitor and Balancing IC	Measures Cell Voltages for Up to 18 Series Battery Cells. The isoSPI Daisy-Chain Capability Allows Multiple Devices to be Interconnected for Measuring Many Battery Cells Simultaneously. The isoSPI Bus can Operate Up to 1MHz and can be Operated Bidirectionally for Fault Conditions, such as a Broken Wire or Connector. Includes Internal Passive CellBalancing Capability of up to 200mA.
LTC6820	isoSPI Isolated Communications Interface	Provides an Isolated Interface for SPI Communication Up to 100 Meters Using a Twisted Pair Companion to the LTC6804