# LM5104 High-Voltage Half-Bridge Gate Driver With Adaptive Delay

## 1 Features

- Drives Both a High-Side and Low-Side N-Channel MOSFET
- Adaptive Rising and Falling Edges With Programmable Additional Delay
- Single Input Control
- Bootstrap Supply Voltage Range up to 118-V DC
- Fast Turnoff Propagation Delay (25 ns Typical)
- Drives 1000-pF Loads With 15-ns Rise and Fall Times
- Supply Rail Undervoltage Lockout
- SOIC and WSON-10 4-mm × 4-mm Package

## 2 Applications

- Current Fed Push-Pull Power Converters
- High Voltage Buck Regulators
- Active Clamp Forward Power Converters
- Half-Bridge and Full-Bridge Converters

## 3 Description

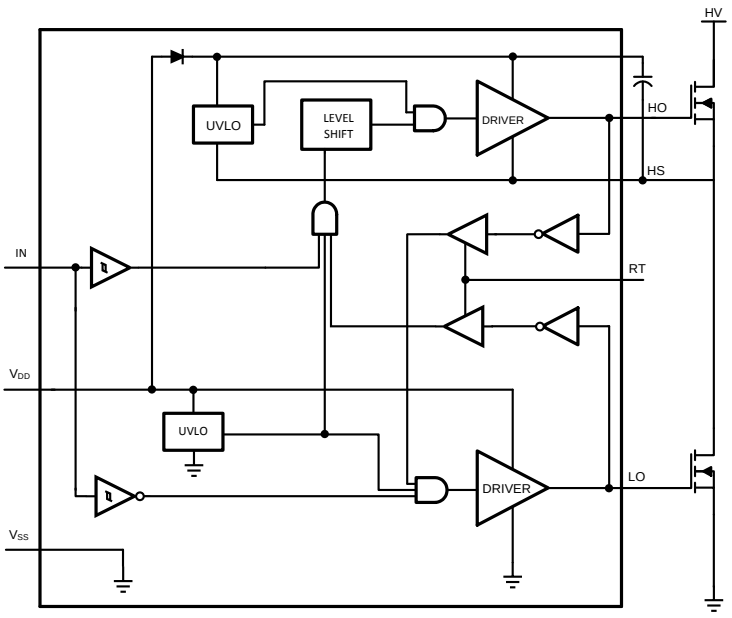
The LM5104 High-Voltage Gate Driver is designed to drive both the high-side and the low-side N-channel MOSFETs in a synchronous buck configuration. The floating high-side driver can work with supply voltages up to 100 V. The high-side and low-side gate drivers are controlled from a single input. Each change in state is controlled in an adaptive manner to prevent shoot-through issues. In addition to the adaptive transition timing, an additional delay time can be added, proportional to an external setting resistor. An integrated high-voltage diode is provided to charge high-side gate drive bootstrap capacitor. A robust level shifter operates at high speed while consuming low power and providing clean level transitions from the control logic to the high-side gate driver. Undervoltage lockout is provided on both the low-side and the high-side power rails. This device is available in the standard SOIC and the WSON packages.

**Device Information(1)**

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| LM5104 | SOIC (8) | 4.90 mm × 3.91 mm |
| | WSON (10) | 4.00 mm × 4.00 mm |

(1) For all available packages, see the orderable addendum at the end of the datasheet.

**Simplified Block Diagram**



# Table of Contents

**1 Features** ... 1
**2 Applications** ... 1
**3 Description** ... 1
**4 Revision History** ... 2
**5 Pin Configuration and Functions** ... 3
**6 Specifications** ... 4
6.1 Absolute Maximum Ratings ... 4
6.2 ESD Ratings ... 4
6.3 Recommended Operating Conditions ... 4
6.4 Thermal Information ... 4
6.5 Electrical Characteristics ... 5
6.6 Switching Characteristics ... 6
6.7 Typical Characteristics ... 6
**7 Detailed Description** ... 9
7.1 Overview ... 9
7.2 Functional Block Diagram ... 9
7.3 Feature Description ... 9
7.4 Device Functional Modes ... 10
**8 Application and Implementation** ... 11
8.1 Application Information ... 11
8.2 Typical Application ... 11
**9 Power Supply Recommendations** ... 14
9.1 Power Dissipation Considerations ... 14
**10 Layout** ... 15
10.1 Layout Guidelines ... 15
10.2 Layout Example ... 16
**11 Device and Documentation Support** ... 16
11.1 Trademarks ... 16
11.2 Electrostatic Discharge Caution ... 16
11.3 Glossary ... 16
**12 Mechanical, Packaging, and Orderable Information** ... 16

## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**Changes from Revision C (March 2013) to Revision D** **Page**

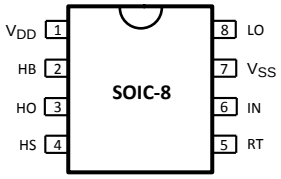
- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

**Changes from Revision B (March 2013) to Revision C** **Page**

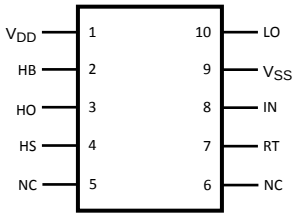
- Changed layout of National Data Sheet to TI format ... 11

# 5 Pin Configuration and Functions

**D Package**
**8-Pin SOIC**
**Top View**




**DPR Package**
**10-Pin WSON**
**Top View**




**Pin Functions**

| PIN | | NAME | DESCRIPTION | APPLICATION INFORMATION |
|---|---|---|---|---|
| SOIC | WSON | | | |
| 1 | 1 | $V_{DD}$ | Positive gate drive supply | Locally decouple to $V_{SS}$ using ESR/ESL capacitor, located as close to IC as possible. |
| 2 | 2 | HB | High-side gate driver bootstrap rail | Connect the positive terminal to bootstrap capacitor to the HB pin and connect negative terminal to HS. The Bootstrap capacitor should be placed as close to IC as possible |
| 3 | 3 | HO | High-side gate driver output | Connect to gate of high-side MOSFET with short low inductance path. |
| 4 | 4 | HS | High-side MOSFET source connection | Connect to bootstrap capacitor negative terminal and source of high-side MOSFET. |
| 5 | 7 | RT | Deadtime programming pin | Resistor from RT to ground programs the deadtime between high- and low-side transitions. The resistor should be located close to the IC to minimize noise coupling from adjacent traces. |
| 6 | 8 | IN | Control input | Logic 1 equals High-side ON and Low-side OFF. Logic 0 equals High-side OFF and Low-side ON. |
| 7 | 9 | $V_{SS}$ | Ground return | All signals are referenced to this ground. |
| 8 | 10 | LO | Low-side gate driver output | Connect to the gate of the low-side MOSFET with a short low inductance path. |

# 6 Specifications

## 6.1 Absolute Maximum Ratings (1)(2)

| | MIN | MAX | UNIT |
|---|---|---|---|
| $V_{DD}$ to $V_{SS}$ | –0.3 | 18 | V |
| $V_{HB}$ to $V_{HS}$ | –0.3 | 18 | V |
| IN to $V_{SS}$ | –0.3 | $V_{DD}$ + 0.3 | V |
| LO Output | –0.3 | $V_{DD}$ + 0.3 | V |
| HO Output | $V_{HS}$ – 0.3 | $V_{HB}$ + 0.3 | V |
| $V_{HS}$ to $V_{SS}$ | −1 | 100 | V |
| $V_{HB}$ to $V_{SS}$ | | 118 | V |
| RT to $V_{SS}$ | –0.3 | 5 | V |
| Junction Temperature | | 150 | °C |
| Storage temperature range, $T_{stg}$ | –55 | 150 | °C |

(1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. *Recommended Operating Conditions* under which operation of the device is specified. Recommended Operating Conditions do not imply performance limits. For performance limits and associated test conditions, see *Electrical Characteristics*.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.

## 6.2 ESD Ratings

| | | VALUE | UNIT |
|---|---|---|---|
| $V_{(ESD)}$ Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1) | ±2000 | V |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

| | MIN | MAX | UNIT |
|---|---|---|---|
| $V_{DD}$ | 9 | 14 | V |
| HS | –1 | 100 | V |
| HB | $V_{HS}$ + 8 | $V_{HS}$ + 14 | V |
| HS Slew Rate | | < 50 | V/ns |
| Junction Temperature | –40 | 125 | °C |

## 6.4 Thermal Information

| THERMAL METRIC (1) | | LM5104 | | UNIT |
|---|---|---|---|---|
| | | D | DPR | |
| | | 8 PINS | 10 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 114.5 | 37.9 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 61.1 | 38.1 | |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 55.6 | 14.9 | |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 9.7 | 0.4 | |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 54.9 | 15.2 | |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | n/a | 4.4 | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

## 6.5 Electrical Characteristics

MIN and MAX limits apply over the full operating junction temperature range. Unless otherwise specified, $T_J$ = +25°C, $V_{DD}$ = $V_{HB}$ = 12 V, $V_{SS}$ = $V_{HS}$ = 0 V, RT = 100kΩ. No Load on LO or HO.

| | PARAMETER | TEST CONDITIONS | MIN(1) | TYP | MAX(1) | UNIT |
|---|---|---|---|---|---|---|
| **SUPPLY CURRENTS** | | | | | | |
| $I_{DD}$ | $V_{DD}$ Quiescent Current | LI = HI = 0 V | | 0.4 | 0.6 | mA |
| $I_{DDO}$ | $V_{DD}$ Operating Current | f = 500 kHz | | 1.9 | 3 | mA |
| $I_{HB}$ | Total HB Quiescent Current | LI = HI = 0 V | | 0.06 | 0.2 | mA |
| $I_{HBO}$ | Total HB Operating Current | f = 500 kHz | | 1.3 | 3 | mA |
| $I_{HBS}$ | HB to $V_{SS}$ Current, Quiescent | $V_{HS}$ = $V_{HB}$ = 100 V | | 0.05 | 10 | µA |
| $I_{HBSO}$ | HB to $V_{SS}$ Current, Operating | f = 500 kHz | | 0.08 | | mA |
| **INPUT PINS** | | | | | | |
| $V_{IL}$ | Low Level Input Voltage Threshold | | 0.8 | 1.8 | | V |
| $V_{IH}$ | High Level Input Voltage Threshold | | | 1.8 | 2.2 | V |
| $R_I$ | Input Pulldown Resistance | | 100 | 200 | 500 | kΩ |
| **TIME DELAY CONTROLS** | | | | | | |
| $V_{RT}$ | Nominal Voltage at RT | | 2.7 | 3 | 3.3 | V |
| $I_{RT}$ | RT Pin Current Limit | RT = 0 V | 0.75 | 1.5 | 2.25 | mA |
| $T_{D1}$ | Delay Timer, RT = 10 kΩ | | 58 | 90 | 130 | ns |
| $T_{D2}$ | Delay Timer, RT = 100 kΩ | | 140 | 200 | 270 | ns |
| **UNDER VOLTAGE PROTECTION** | | | | | | |
| $V_{DDR}$ | $V_{DD}$ Rising Threshold | | 6.0 | 6.9 | 7.4 | V |
| $V_{DDH}$ | $V_{DD}$ Threshold Hysteresis | | | 0.5 | | V |
| $V_{HBR}$ | HB Rising Threshold | | 5.7 | 6.6 | 7.1 | V |
| $V_{HBH}$ | HB Threshold Hysteresis | | | 0.4 | | V |
| **BOOT STRAP DIODE** | | | | | | |
| $V_{DL}$ | Low-Current Forward Voltage | $I_{VDD-HB}$ = 100 µA | | 0.60 | 0.9 | V |
| $V_{DH}$ | High-Current Forward Voltage | $I_{VDD-HB}$ = 100 mA | | 0.85 | 1.1 | V |
| $R_D$ | Dynamic Resistance | $I_{VDD-HB}$ = 100 mA | | 0.8 | 1.5 | Ω |
| **LO GATE DRIVER** | | | | | | |
| $V_{OLL}$ | Low-Level Output Voltage | $I_{LO}$ = 100 mA | | 0.25 | 0.4 | V |
| $V_{OHL}$ | High-Level Output Voltage | $I_{LO}$ = –100 mA<br>$V_{OHL}$ = $V_{DD}$ – $V_{LO}$ | | 0.35 | 0.55 | V |
| $I_{OHL}$ | Peak Pullup Current | $V_{LO}$ = 0 V | | 1.6 | | A |
| $I_{OLL}$ | Peak Pulldown Current | $V_{LO}$ = 12 V | | 1.8 | | A |
| **HO GATE DRIVER** | | | | | | |
| $V_{OLH}$ | Low-Level Output Voltage | $I_{HO}$ = 100 mA | | 0.25 | 0.4 | V |
| $V_{OHH}$ | High-Level Output Voltage | $I_{HO}$ = –100 mA,<br>$V_{OHH}$ = $V_{HB}$ – $V_{HO}$ | | 0.35 | 0.55 | V |
| $I_{OHH}$ | Peak Pullup Current | $V_{HO}$ = 0 V | | 1.6 | | A |
| $I_{OLH}$ | Peak Pulldown Current | $V_{HO}$ = 12 V | | 1.8 | | A |

(1) Min and Max limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate Average Outgoing Quality Level (AOQL).

## 6.6 Switching Characteristics

MAX limits apply over the full operating junction temperature range. Unless otherwise specified, $T_J$ = +25°C, $V_{DD}$ = $V_{HB}$ = 12 V, $V_{SS}$ = $V_{HS}$ = 0 V, No Load on LO or HO .

| | PARAMETER | TEST CONDITIONS | MIN(1) | TYP | MAX(1) | UNIT |
|---|---|---|---|---|---|---|
| $t_{LPHL}$ | Lower Turn-Off Propagation Delay (IN Rising to LO Falling) | | | 25 | 56 | ns |
| $t_{HPHL}$ | Upper Turn-Off Propagation Delay (IN Falling to HO Falling) | | | 25 | 56 | |
| $t_{RC}$, $t_{FC}$ | Either Output Rise/Fall Time | $C_L$ = 1000 pF | | 15 | | |
| $t_R$, $t_F$ | Either Output Rise/Fall Time (3V to 9V) | $C_L$ = 0.1 µF | | 0.6 | | µs |
| $t_{BS}$ | Bootstrap Diode Turn-Off Time | $I_F$ = 20 mA, $I_R$ = 200 mA | | 50 | | ns |

(1) Min and Max limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate Average Outgoing Quality Level (AOQL).

## 6.7 Typical Characteristics

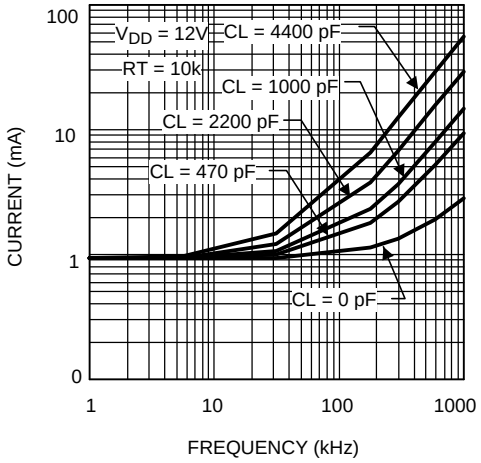



**Figure 1. $I_{DD}$ vs Frequency**

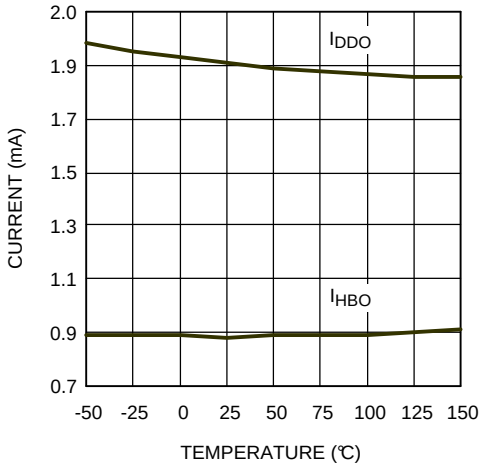



**Figure 2. Operating Current vs Temperature**

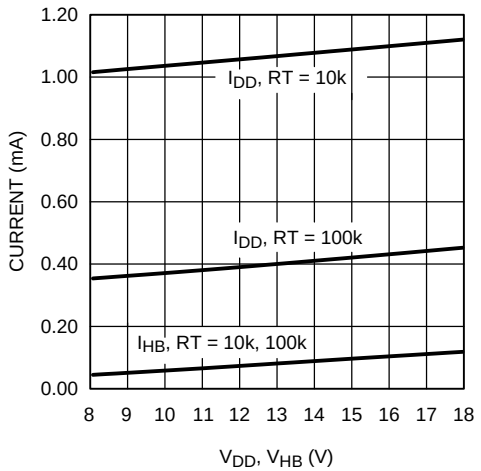



**Figure 3. Quiescent Current vs Supply Voltage**

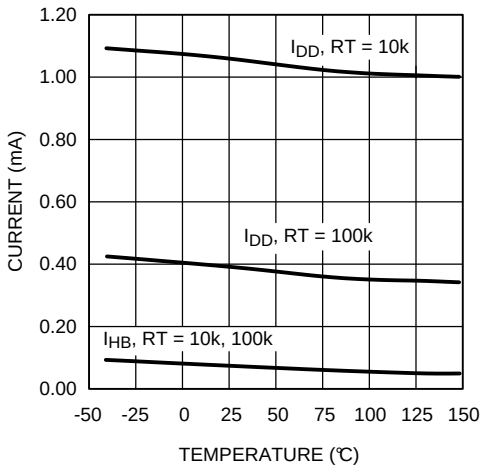



**Figure 4. Quiescent Current vs Temperature**

## Typical Characteristics (continued)

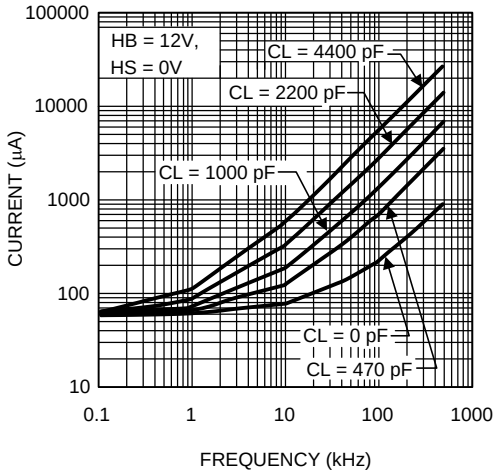



**Figure 5. $I_{HB}$ vs Frequency**

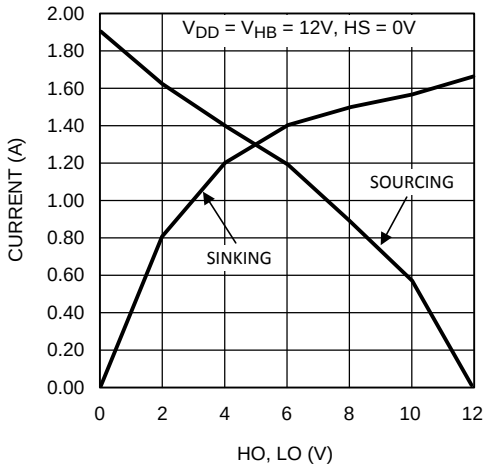



**Figure 6. HO & LO Peak Output Current vs Output Voltage**

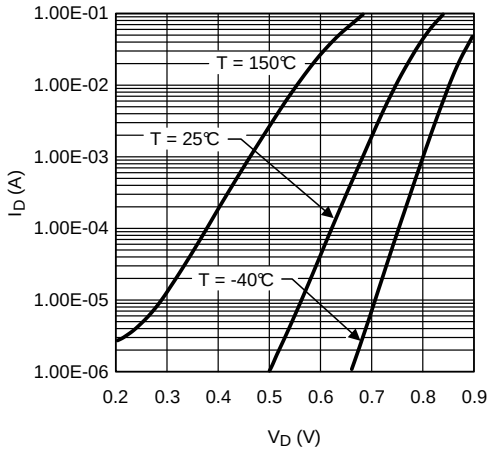



**Figure 7. Diode Forward Voltage**

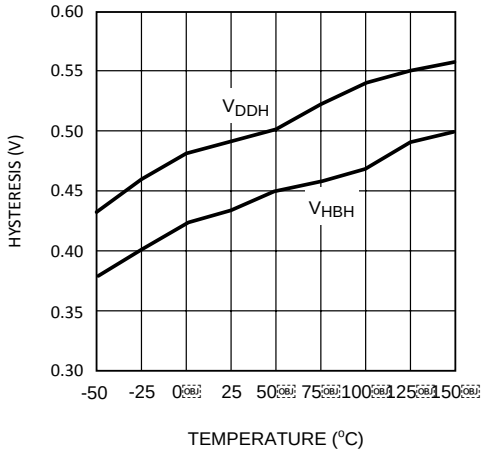



**Figure 8. Undervoltage Threshold Hysteresis vs Temperature**

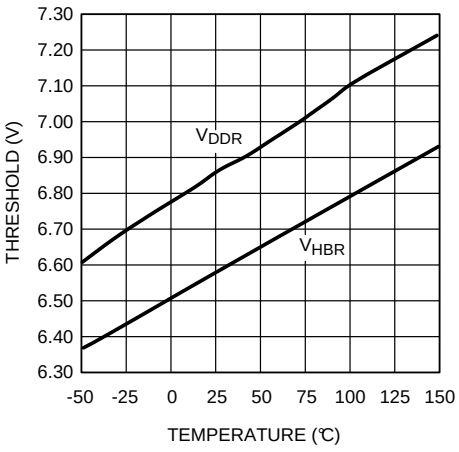



**Figure 9. Undervoltage Rising Threshold vs Temperature**

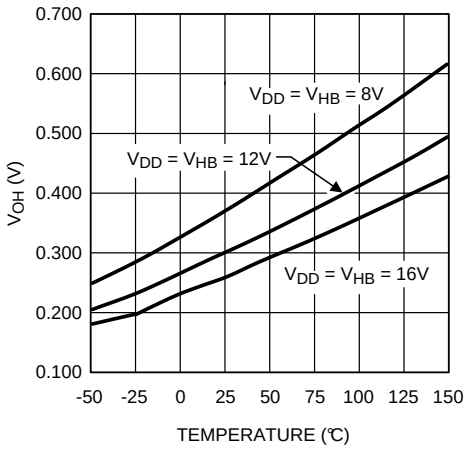



**Figure 10. LO and HO Gate Drive—High-Level Output Voltage vs Temperature**

## Typical Characteristics (continued)

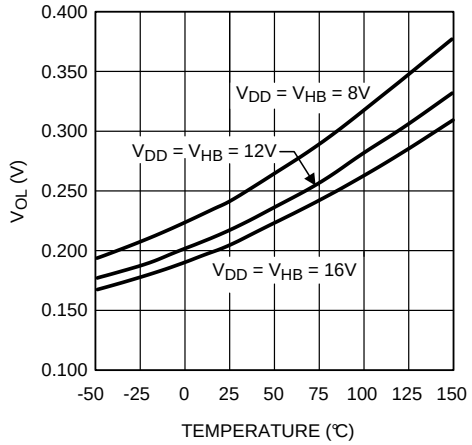



**Figure 11. LO and HO Gate Drive—Low-Level Output Voltage vs Temperature**

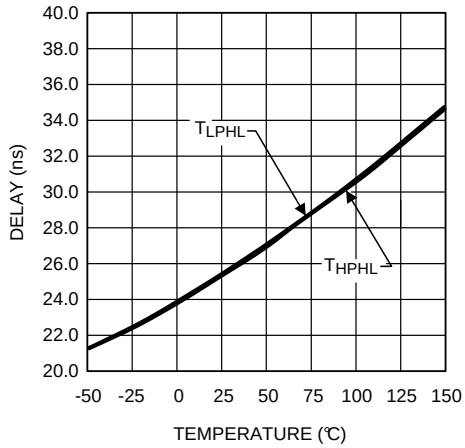



**Figure 12. Turn Off Propagation Delay vs Temperature**

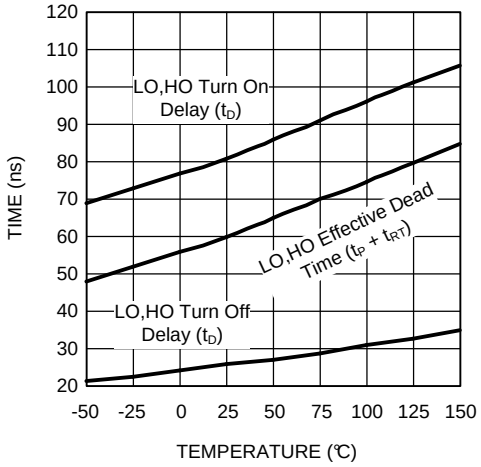



**Figure 13. Timing vs Temperature RT = 10K**

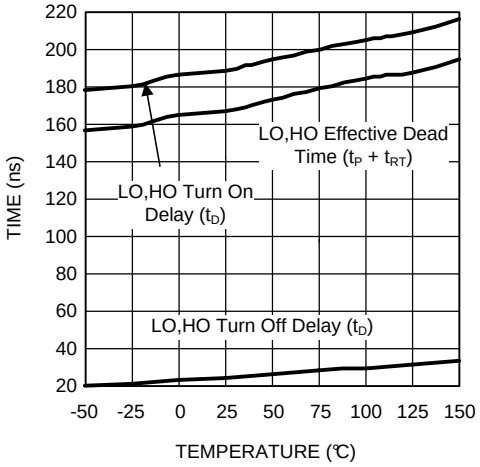


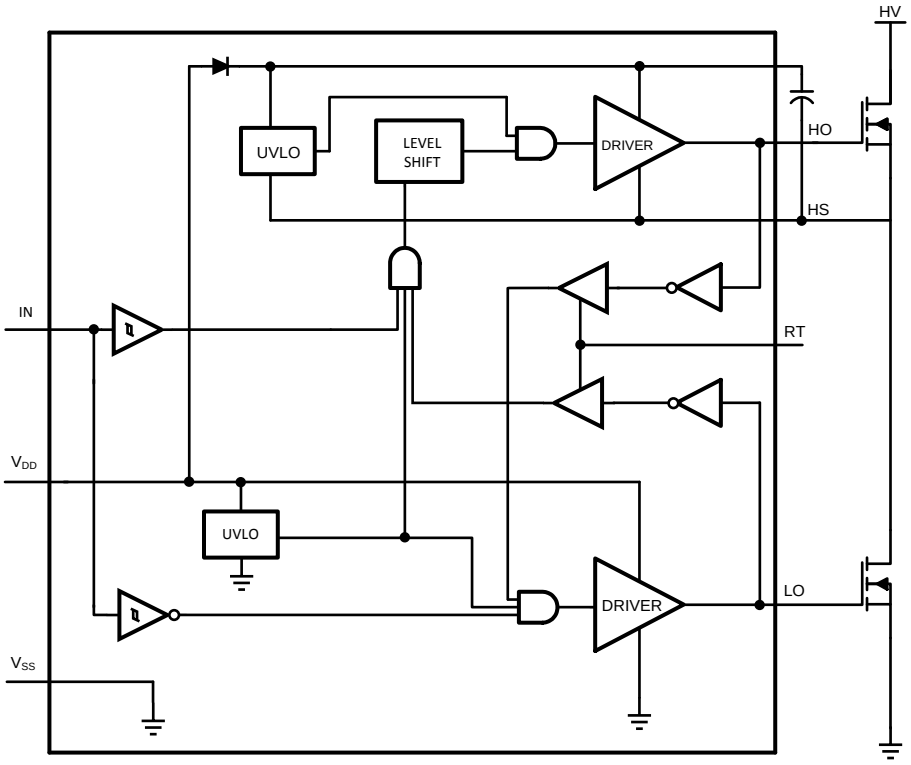

**Figure 14. Timing vs Temperature RT = 100K**

# 7 Detailed Description

## 7.1 Overview

The LM5104 High Voltage gate driver is designed to drive both the high side and the low side N-Channel MOSFETs in a synchronous buck configuration. The floating high-side driver is capable of working with supply voltages up to 100 V. The high side and low side gate drivers are controlled from a single input. Each change in state is controlled in an adaptive manner to prevent shoot-through issues. In addition to the adaptive transition timing, an additional delay time can be added, proportional to an external setting resistor. An integrated high voltage diode is provided to charge high side gate drive bootstrap capacitor. A robust level shifter operates at high speed while consuming low power and providing clean level transitions from the control logic to the high side gate driver. Under-voltage lockout is provided on both the low side and the high side power rails.

## 7.2 Functional Block Diagram




## 7.3 Feature Description

### 7.3.1 Adaptive Shoot-Through Protection

LM5104 is a high voltage, high speed dual output driver designed to drive top and bottom MOSFET's connected in synchronous buck or half-bridge configuration, from one externally provided PWM signal. LM5104 features adaptive delay to prevent shoot-through current through top and bottom MOSFETs during switching transitions. Referring to the timing diagram Figure 16, the rising edge of the PWM input (IN) turns off the bottom MOSFET (LO) after a short propagation delay ($t_P$). An adaptive circuit in the LM5104 monitors the bottom gate voltage (LO) and triggers a programmable delay generator when the LO pin falls below an internally set threshold (≈ $V_{dd}/2$). The gate drive of the upper MOSFET (HO) is disabled until the deadtime expires. The upper gate is enabled after the TIMER delay ($t_P$+$T_{RT}$), and the upper MOSFET turns-on. The additional delay of the timer prevents lower and upper MOSFETs from conducting simultaneously, thereby preventing shoot-through.

## Feature Description (continued)

A falling transition on the PWM signal (IN) initiates the turn-off of the upper MOSFET and turn-on of the lower MOSFET. A short propagation delay ($t_P$) is encountered before the upper gate voltage begins to fall. Again, the adaptive shoot-through circuitry and the programmable deadtime TIMER delays the lower gate turn-on time. The upper MOSFET gate voltage is monitored and the deadtime delay generator is triggered when the upper MOSFET gate voltage with respect to ground drops below an internally set threshold (≈ $V_{dd}$/2). The lower gate drive is momentarily disabled by the timer and turns on the lower MOSFET after the deadtime delay expires ($t_P$+$T_{RT}$).

The RT pin is biased at 3V and current limited to 1mA. It is designed to accommodate a resistor between 5K and 100K, resulting in an effective dead-time proportional to RT and ranging from 90ns to 200ns. RT values below 5K will saturate the timer and are not recommended.

### 7.3.2 Start-up and UVLO

Both top and bottom drivers include undervoltage lockout (UVLO) protection circuitry which monitors the supply voltage ($V_{DD}$) and bootstrap capacitor voltage ($V_{HB}$ – $V_{HS}$) independently. The UVLO circuit inhibits each driver until sufficient supply voltage is available to turn-on the external MOSFETs, and the built-in hysteresis prevents chattering during supply voltage transitions. When the supply voltage is applied to $V_{DD}$ pin of LM5104, the top and bottom gates are held low until $V_{DD}$ exceeds UVLO threshold, typically about 6.9 V. Any UVLO condition on the bootstrap capacitor will disable only the high-side output (HO).

## 7.4 Device Functional Modes

| IN Pin | LO Pin | HO Pin |
|---|---|---|
| L | H | L |
| H | L | H |

# 8 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 8.1 Application Information

The LM5104 is one of the latest generation of high-voltage gate drivers which are designed to drive both the high-side and low-side N-channel MOSFETs in a half-bridge/full bridge configuration or in a synchronous buck circuit. The floating high-side driver can operate with supply voltages up to 100 V. This allows for N-channel MOSFET control in half-bridge, full-bridge, push-pull, two switch forward and active clamp topologies.

**Table 1. Highlights**

| FEATURE | BENEFIT |
|---|---|
| Adaptive Rising and Falling Edges with Programmable Additional Delay | Allows optimization of gate drive timings to account for device differences between high-side and low-side positions. |
| Single Input Control | Direct drive from lower cost PWM controllers |
| Internal Bootstrap Diode | Reduces parts count and PCB real estate |

## 8.2 Typical Application

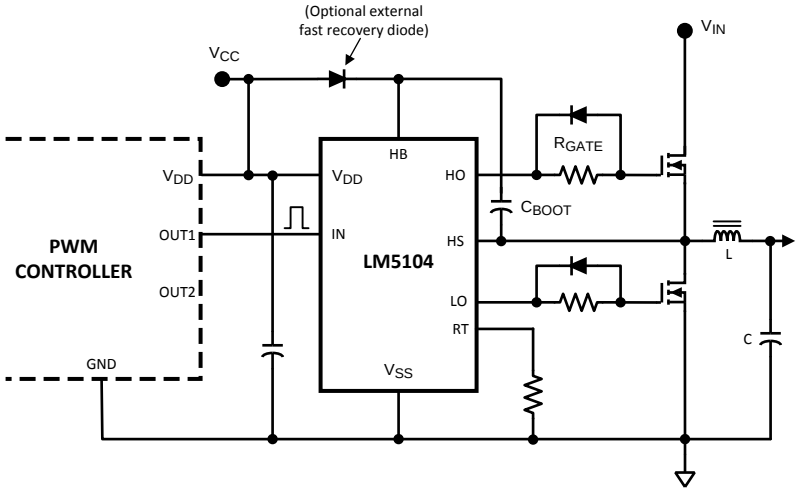



**Figure 15. LM5104 Driving MOSFETs Connected in Synchronous Buck Configuration**

## Typical Application (continued)

### 8.2.1 Design Requirements

| PARAMETER | VALUE |
|---|---|
| Gate Driver IC | LM5104 |
| Mosfet | CSD18531Q5A |
| $V_{DD}$ | 10 V |
| $Q_{gmax}$ | 43 nC |
| $F_{sw}$ | 200 kHz |
| $D_{Max}$ | 95% |
| $I_{HBO}$ | 10 µA |
| $V_{DH}$ | 1.1 V |
| $V_{HBR}$ | 7.1 V |
| $V_{HBH}$ | 0.4 V |

### 8.2.2 Detailed Design Procedure

$\Delta V_{HB} = V_{DD} - V_{DH} - V_{HBL}$

where

- $V_{DD}$ = Supply voltage of the gate drive IC
- $V_{DH}$ = Bootstrap diode forward voltage drop
- $V_{gsmin}$ = Minimum gate source threshold voltage (1)

$$C_{BOOT} = \frac{Q_{TOTAL}}{\Delta V_{HB}} \quad (2)$$

$$Q_{TOTAL} = Q_{gmax} + I_{HBO} \times \frac{D_{Max}}{F_{SW}} \quad (3)$$

The quiescent current of the bootstrap circuit is 10 µA which is negligible compared to the Qgs of the MOSFET.

$$Q_{TOTAL} = 43nC + 10\mu A \times \frac{0.95}{100kHz} \quad (4)$$

$Q_{TOTAL}$ = 43.01 nC (5)

In practice the value for the $C_{BOOT}$ capacitor should be greater than that calculated to allow for situations where the power stage may skip pulse due to load transients. In this circumstance the boot capacitor must maintain the HB pin voltage above the UVLO voltage for the HB circuit.

As a general rule the local $V_{DD}$ bypass capacitor should be 10 times greater than the value of $C_{BOOT}$.

$V_{HBL} = V_{HBR} - V_{HBH}$ (6)

$V_{HBL}$ = 6.7 V (7)

$\Delta V_{HB}$ = 10 V – 1.1 V – 6.7 V (8)

$\Delta V_{HB}$ = 2.2 V (9)

$$C_{BOOT} = \frac{43.01nc}{2.2V} \quad (10)$$

$C_{BOOT}$ = 19.54 nF (11)

The bootstrap and bias capacitors should be ceramic types with X7R dielectric. The voltage rating should be twice that of the maximum $V_{DD}$ to allow for loss of capacitance once the devices have a DC bias voltage across them and to ensure long-term reliability of the devices.

An additional delay turn-on delay can be programmed using an external resistor, RT. Figure 17 shows the relationship between the turnon delay time and the resistor value for RT.

### 8.2.3 Application Curves

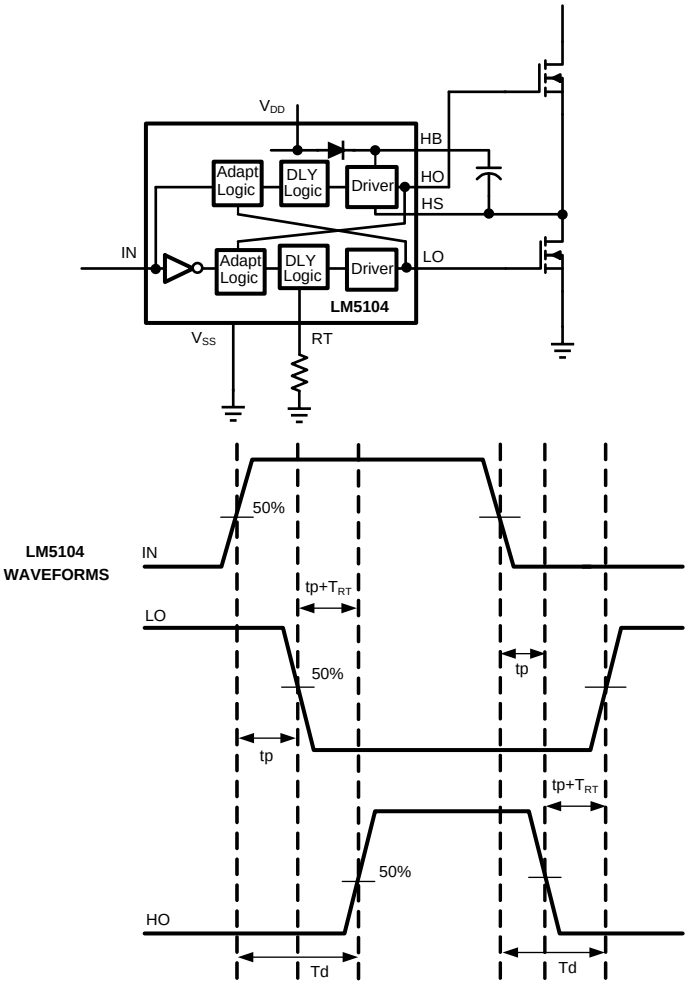



**Figure 16. Application Timing Waveforms**

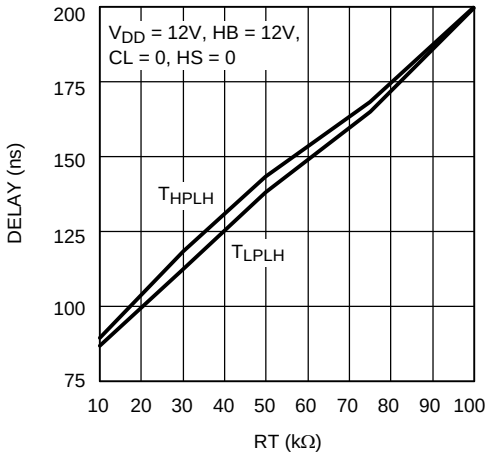



**Figure 17. Turn On Delay vs RT Resistor Value**

# 9 Power Supply Recommendations

## 9.1 Power Dissipation Considerations

The total IC power dissipation is the sum of the gate driver losses and the bootstrap diode losses. The gate driver losses are related to the switching frequency (f), output load capacitance on LO and HO ($C_L$), and supply voltage ($V_{DD}$) and can be roughly calculated as:

$$P_{DGATES} = 2 \bullet f \bullet C_L \bullet V_{DD}^2 \quad (12)$$

There are some additional losses in the gate drivers due to the internal CMOS stages used to buffer the LO and HO outputs. The plot in Figure 18 shows the measured gate driver power dissipation versus frequency and load capacitance. At higher frequencies and load capacitance values, the power dissipation is dominated by the power losses driving the output loads and agrees well with Equation 12. This plot can be used to approximate the power losses due to the gate drivers.

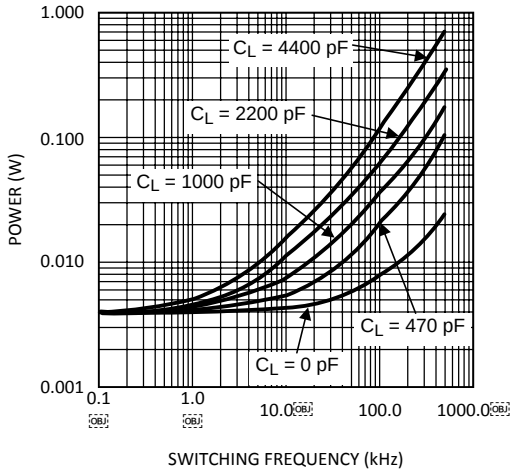



**Figure 18. Gate Driver Power Dissipation (LO + HO)**
**$V_{CC}$ = 12V, Neglecting Diode Losses**

The bootstrap diode power loss is the sum of the forward bias power loss that occurs while charging the bootstrap capacitor and the reverse bias power loss that occurs during reverse recovery. Since each of these events happens once per cycle, the diode power loss is proportional to frequency. Larger capacitive loads require more current to recharge the bootstrap capacitor resulting in more losses. Higher input voltages ($V_{IN}$) to the half bridge result in higher reverse recovery losses. The following plot was generated based on calculations and lab measurements of the diode recovery time and current under several operating conditions. This can be useful for approximating the diode power dissipation.

### Power Dissipation Considerations (continued)

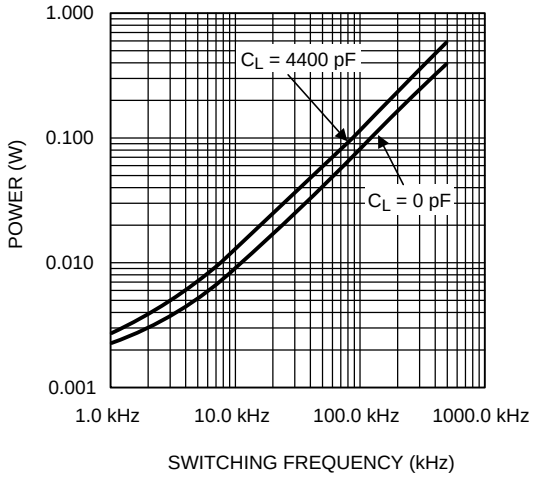



**Figure 19. Diode Power Dissipation $V_{IN}$ = 80V**

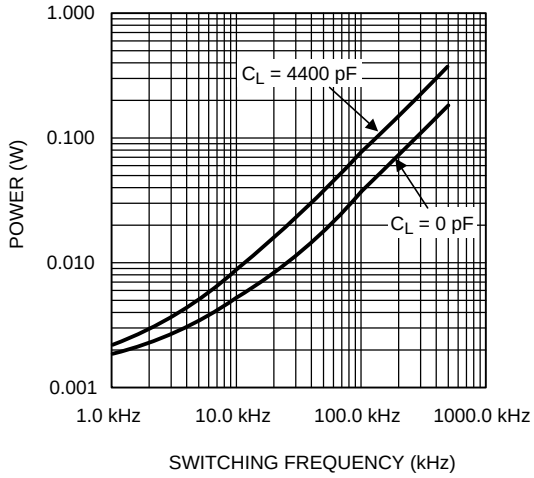



**Figure 20. Diode Power Dissipation $V_{IN}$ = 40V**

The total IC power dissipation can be estimated from the above plots by summing the gate drive losses with the bootstrap diode losses for the intended application. Because the diode losses can be significant, an external diode placed in parallel with the internal bootstrap diode (refer to Figure 15) can be helpful in removing power from the IC. For this to be effective, the external diode must be placed close to the IC to minimize series inductance and have a significantly lower forward voltage drop than the internal diode.

## 10 Layout

### 10.1 Layout Guidelines

The optimum performance of high- and low-side gate drivers cannot be achieved without taking due considerations during circuit board layout. Following points are emphasized.

1. A low ESR/ESL capacitor must be connected close to the IC, and between $V_{DD}$ and $V_{SS}$ pins and between HB and HS pins to support high peak currents being drawn from $V_{DD}$ during turnon of the external MOSFET.
2. To prevent large voltage transients at the drain of the top MOSFET, a low ESR electrolytic capacitor must be connected between MOSFET drain and ground ($V_{SS}$).
3. To avoid large negative transients on the switch node (HS) pin, the parasitic inductances in the source of top MOSFET and in the drain of the bottom MOSFET (synchronous rectifier) must be minimized.
4. Grounding considerations:
   - a) The first priority in designing grounding connections is to confine the high peak currents from charging and discharging the MOSFET gate in a minimal physical area. This will decrease the loop inductance and minimize noise issues on the gate terminal of the MOSFET. The MOSFETs should be placed as close as possible to the gate driver.
   - b) The second high current path includes the bootstrap capacitor, the bootstrap diode, the local ground referenced bypass capacitor and low-side MOSFET body diode. The bootstrap capacitor is recharged on the cycle-by-cycle basis through the bootstrap diode from the ground referenced $V_{DD}$ bypass capacitor. The recharging occurs in a short time interval and involves high peak current. Minimizing this loop length and area on the circuit board is important to ensure reliable operation.
5. The resistor on the RT pin must be placed very close to the IC and seperated from high current paths to avoid noise coupling to the time delay generator which could disrupt timer operation.

### 10.2 Layout Example

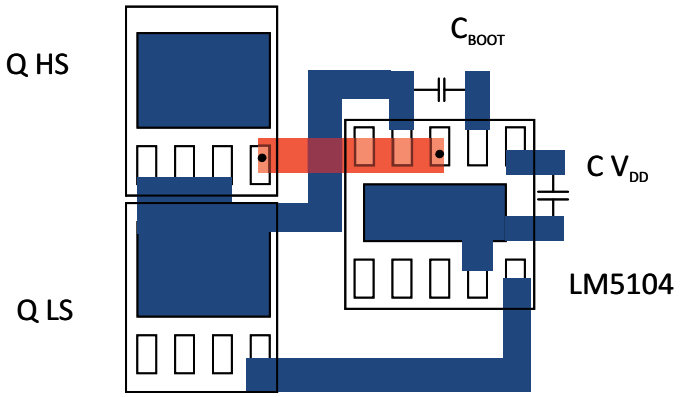



**Figure 21. LM5104 Component Placement**

## 11 Device and Documentation Support

### 11.1 Trademarks

All trademarks are the property of their respective owners.

### 11.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 11.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| LM5104M | NRND | SOIC | D | 8 | 95 | Non-RoHS & Green | Call TI | Level-1-235C-UNLIM | -40 to 125 | 5104 M | |
| LM5104M/NOPB | ACTIVE | SOIC | D | 8 | 95 | RoHS & Green | SN | Level-1-260C-UNLIM | -40 to 125 | 5104 M | Samples |
| LM5104MX/NOPB | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | SN | Level-1-260C-UNLIM | -40 to 125 | 5104 M | Samples |
| LM5104SD/NOPB | ACTIVE | WSON | DPR | 10 | 1000 | RoHS & Green | SN | Level-1-260C-UNLIM | -40 to 125 | 5104SD | Samples |
| LM5104SDX/NOPB | ACTIVE | WSON | DPR | 10 | 4500 | RoHS & Green | SN | Level-1-260C-UNLIM | -40 to 125 | 5104SD | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

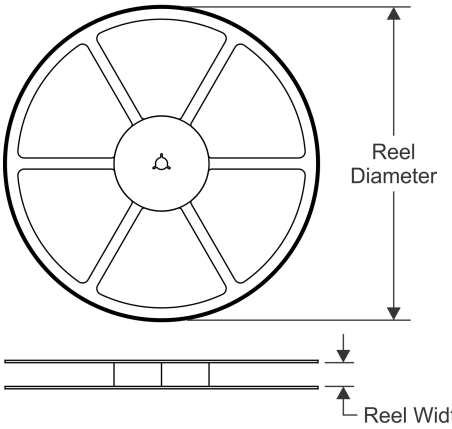
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

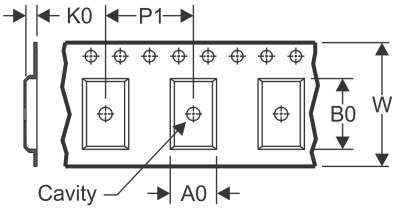
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

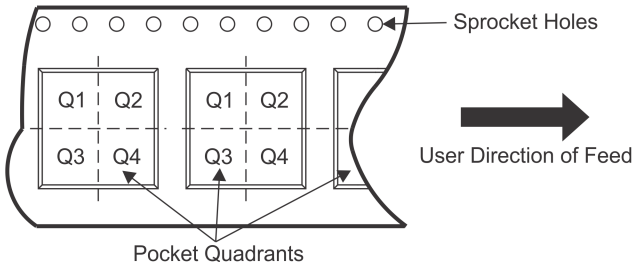



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

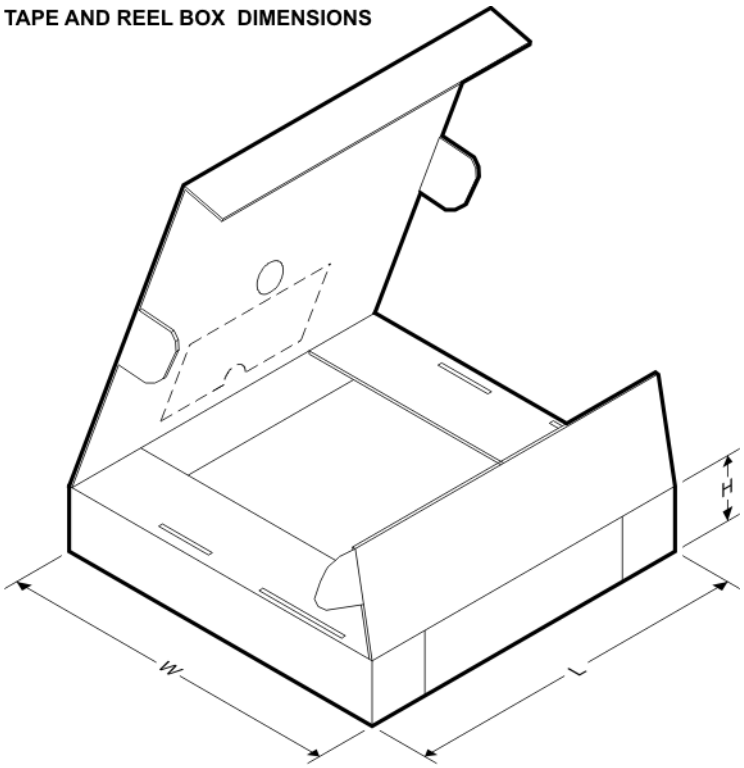
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LM5104MX/NOPB | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.5 | 5.4 | 2.0 | 8.0 | 12.0 | Q1 |
| LM5104SD/NOPB | WSON | DPR | 10 | 1000 | 178.0 | 12.4 | 4.3 | 4.3 | 1.3 | 8.0 | 12.0 | Q1 |
| LM5104SDX/NOPB | WSON | DPR | 10 | 4500 | 330.0 | 12.4 | 4.3 | 4.3 | 1.3 | 8.0 | 12.0 | Q1 |

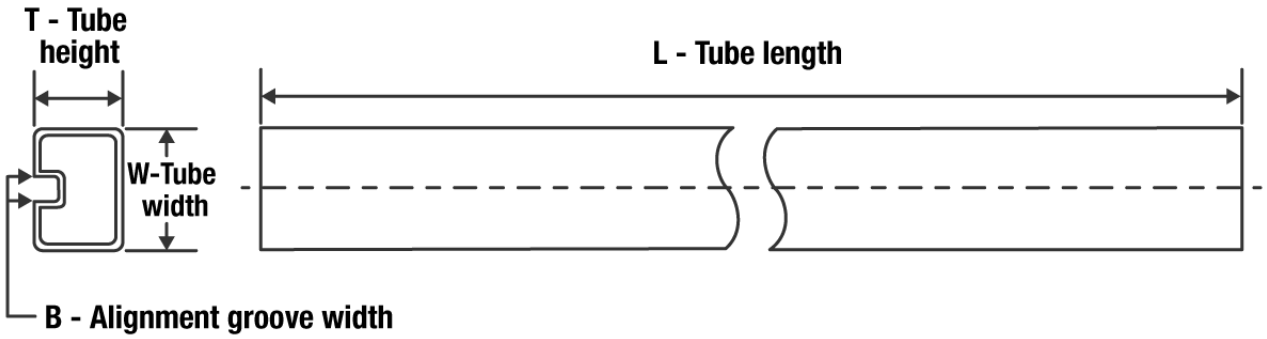
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| LM5104MX/NOPB | SOIC | D | 8 | 2500 | 367.0 | 367.0 | 35.0 |
| LM5104SD/NOPB | WSON | DPR | 10 | 1000 | 208.0 | 191.0 | 35.0 |
| LM5104SDX/NOPB | WSON | DPR | 10 | 4500 | 367.0 | 367.0 | 35.0 |

## TUBE




*All dimensions are nominal

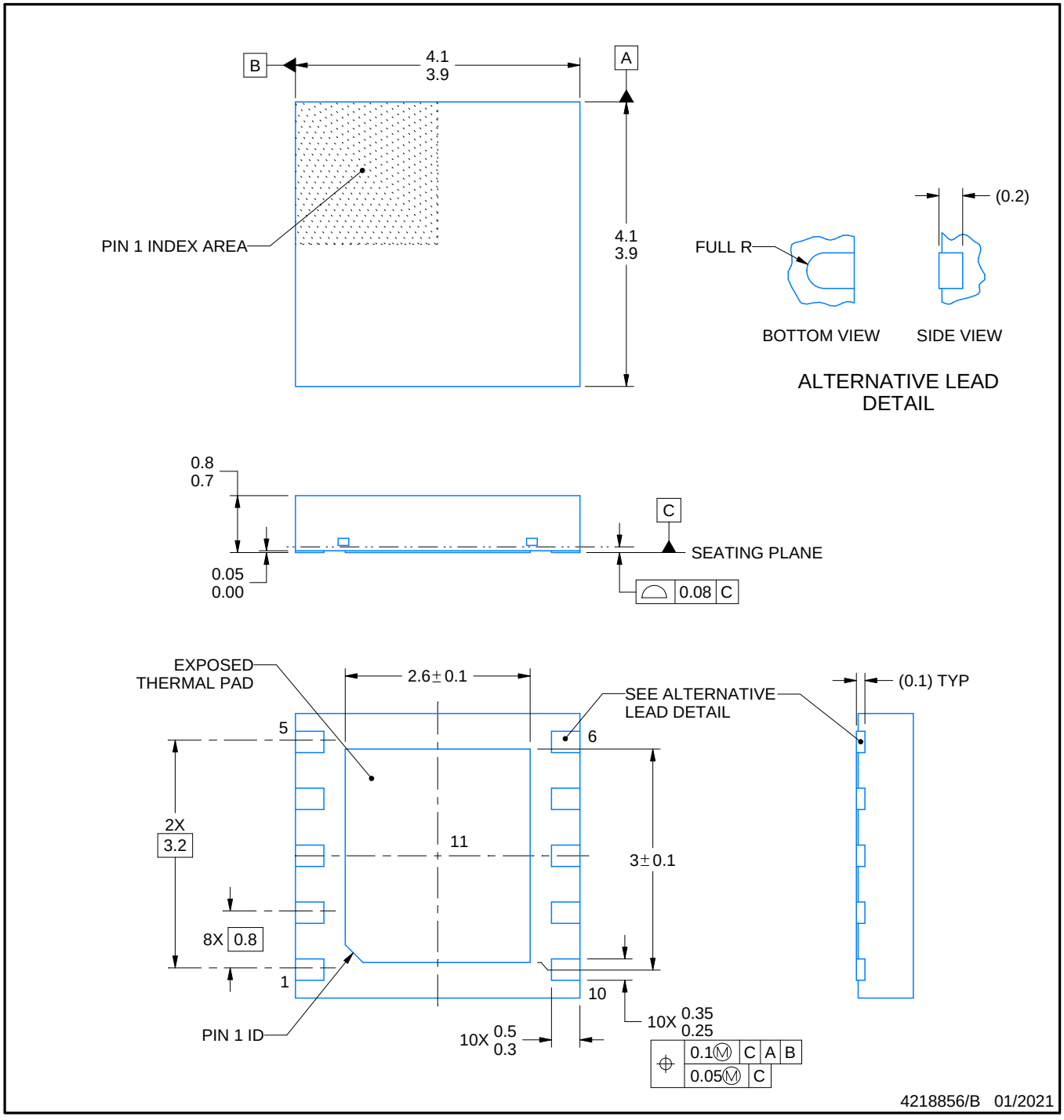
| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| LM5104M | D | SOIC | 8 | 95 | 495 | 8 | 4064 | 3.05 |
| LM5104M | D | SOIC | 8 | 95 | 495 | 8 | 4064 | 3.05 |
| LM5104M/NOPB | D | SOIC | 8 | 95 | 495 | 8 | 4064 | 3.05 |

# PACKAGE OUTLINE

## DPR0010A

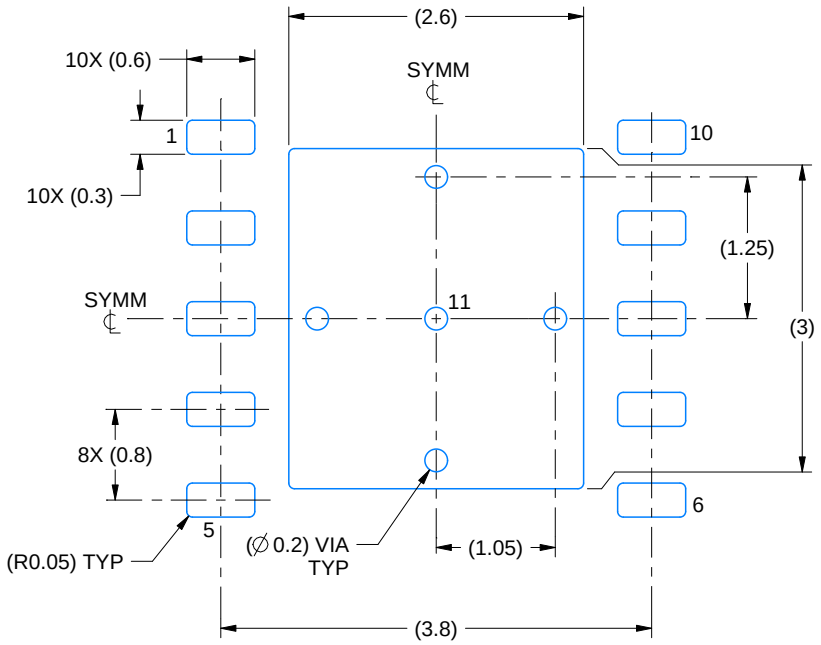
## WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

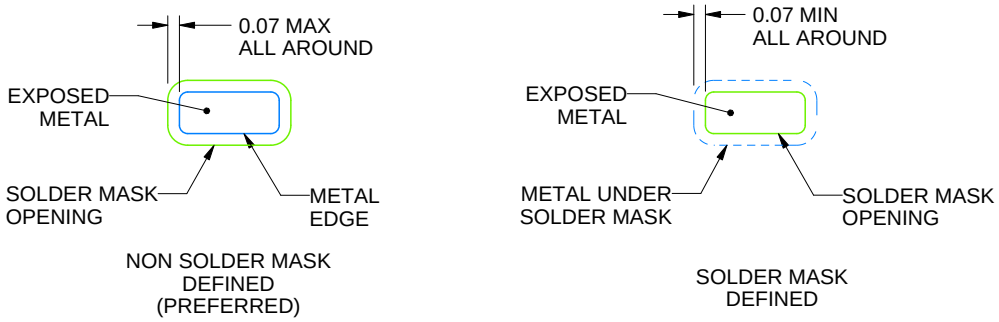



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

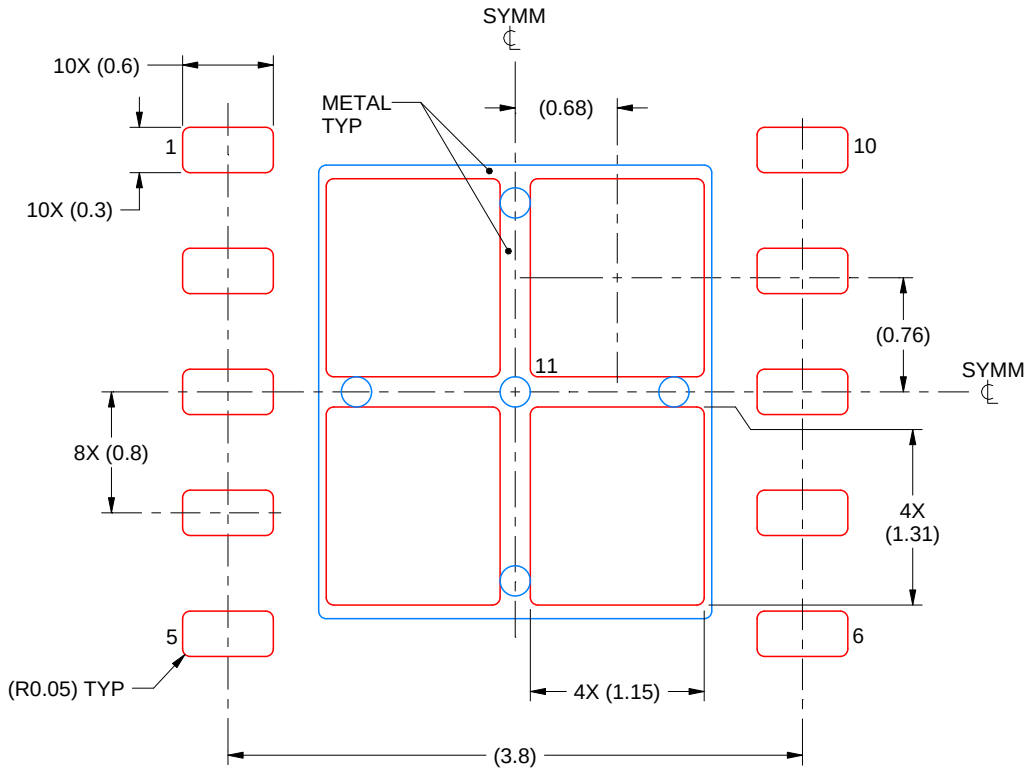



SOLDER MASK DETAILS

4218856/B 01/2021

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



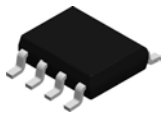

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
77% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

4218856/B 01/2021

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

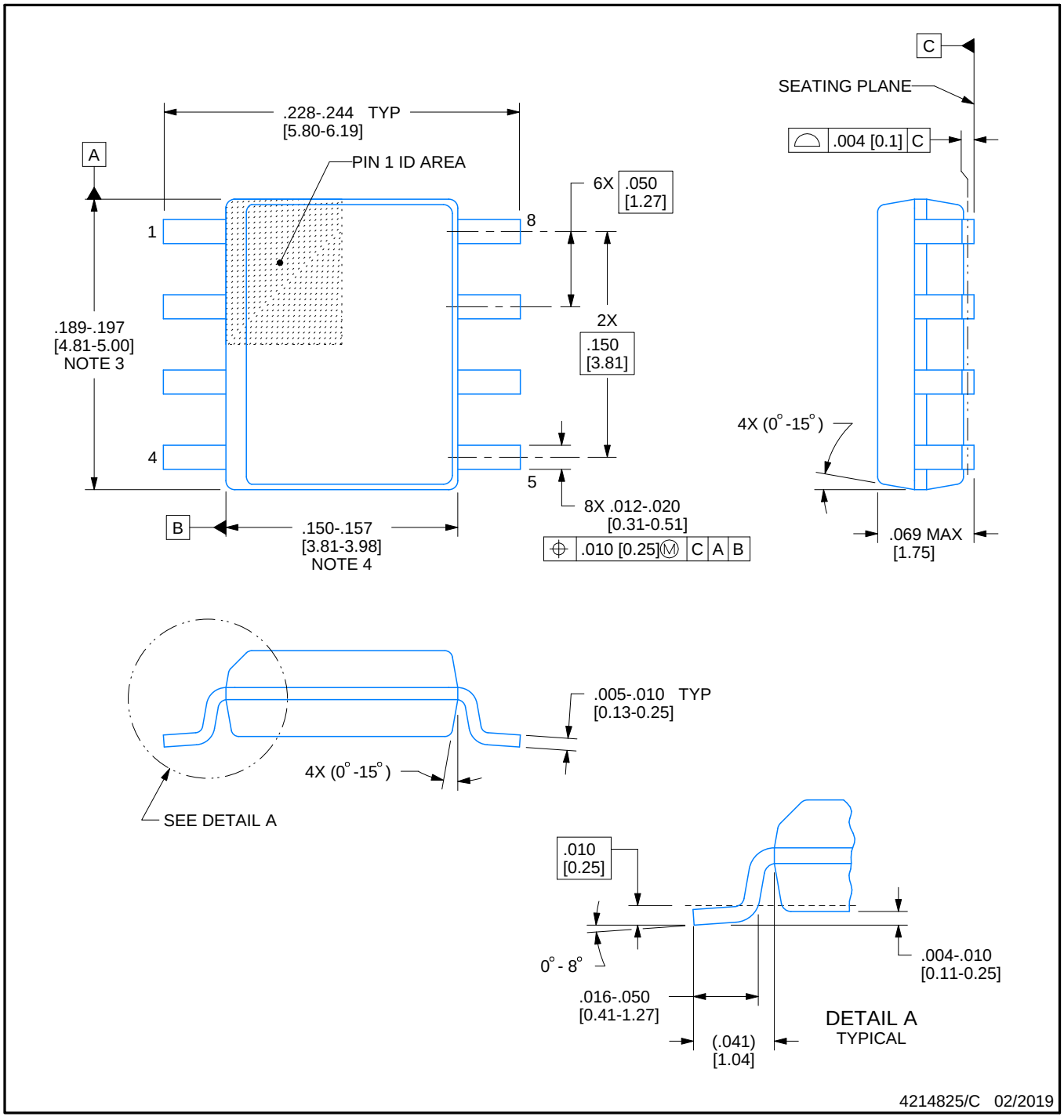


# PACKAGE OUTLINE

## D0008A

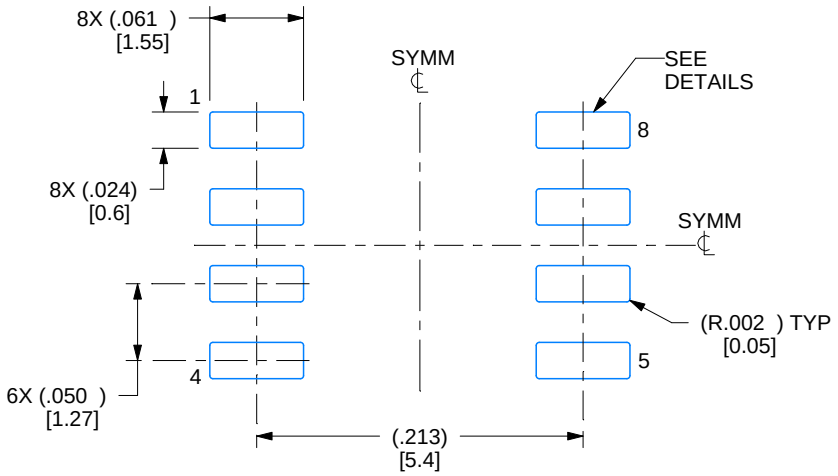
## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

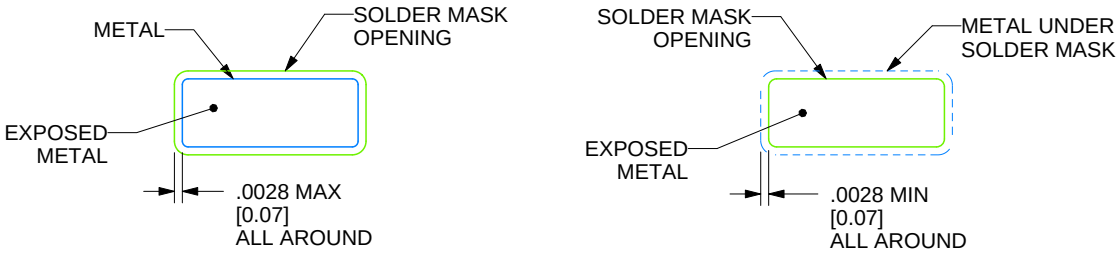



NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X




SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

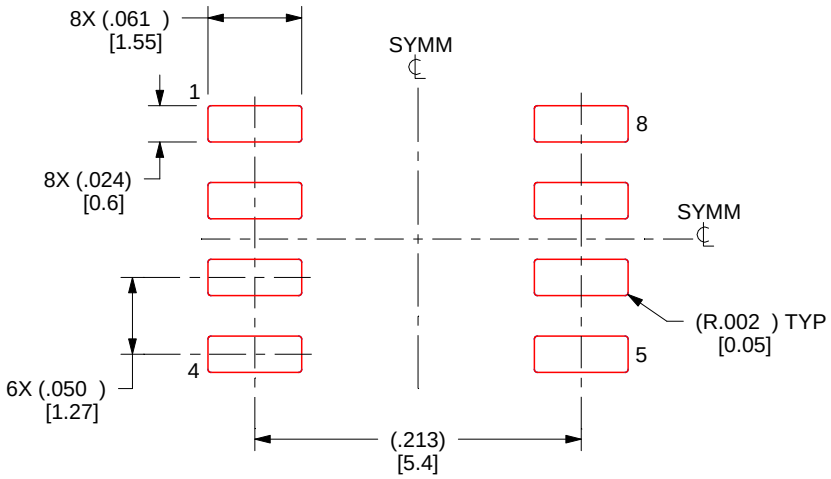
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## D0008A

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT




SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265