*Click **here** to ask an associate for production status of specific part numbers.*

MAX17854

14-Channel, High-Voltage Data-Acquisition System

General Description

The MAX17854 is a flexible data-acquisition system for the management of high-voltage and low-voltage battery modules. The system can measure 14 cell voltages and a combination of six temperatures or system voltage measurements with fully redundant measurement engines in 162µs, or perform all inputs solely with the ADC measurement engine in 99µs. There are 14 internal balancing switches rated for >300mA for cell-balancing current, each supporting extensive built-in diagnostics. Up to 32 devices can be daisy-chained to manage 448 cells and monitor 192 temperatures.

Cell and bus-bar voltages ranging from -2.5V to +5V are measured differentially over a 65V common-mode range, with a typical accuracy of 100µV. If oversampling is enabled, up to 128 measurements per channel can be averaged internally with 14-bit resolution and combined with digital post-processing IIR filtering for increased noise immunity. The system can shut itself down in the event of a thermal overload by measuring its own die temperature.

The system uses Analog Devices' battery-management UART protocol for robust communications and supports an I^2C master interface for external device control, and is optimized to support a reduced feature set of internal diagnostics and rapid-alert communication through both embedded communication and hardware-alert interfaces to support ASIL D and FMEA requirements.

Applications

- High-Voltage Battery Stacks
- Electric Vehicles (EVs)
- Hybrid Electric Vehicles (HEVs)
- Electric Bikes
- Battery-Backup Systems (UPS)
- Super-Cap Systems
- Battery-Powered Tools

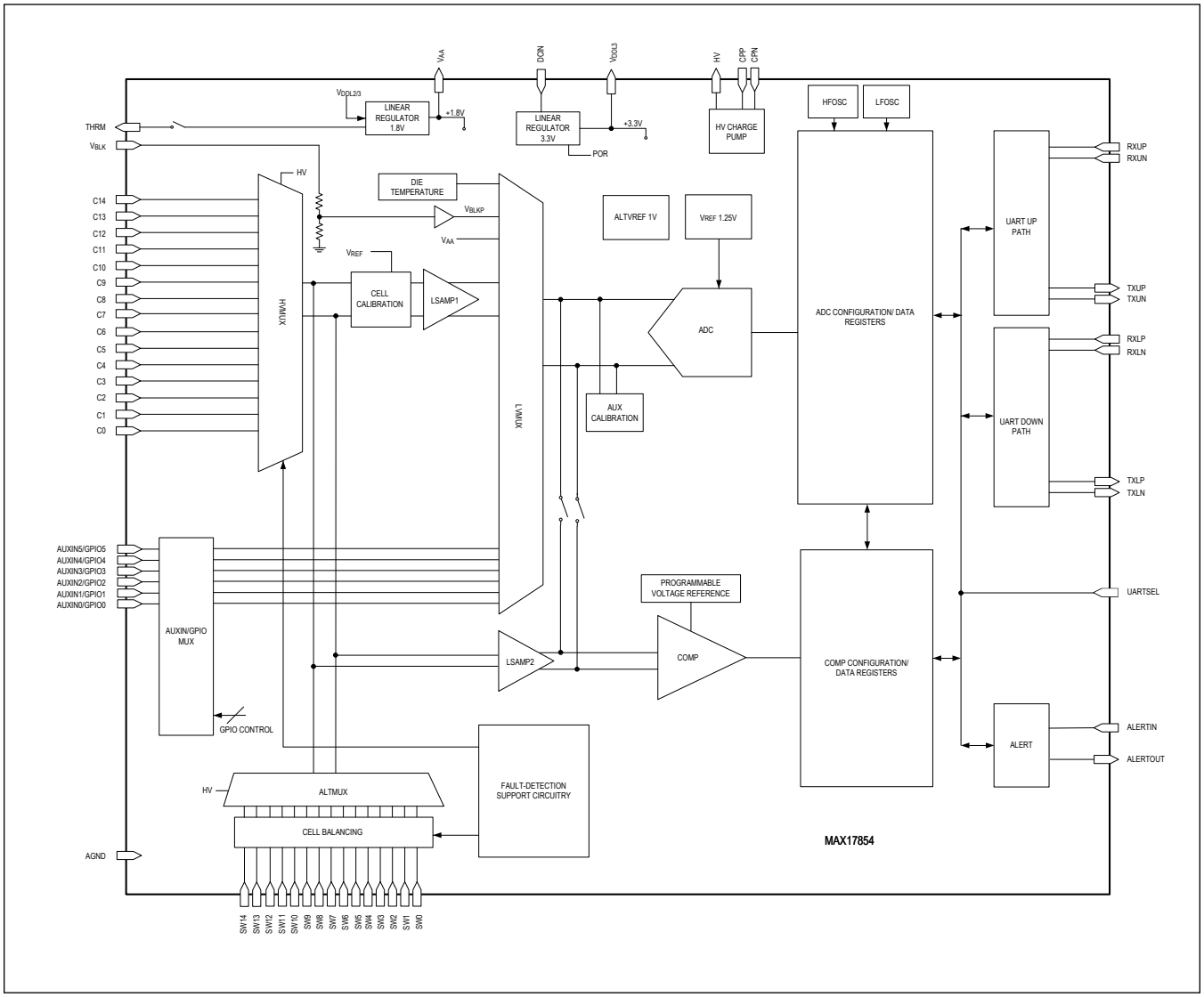
Benefits and Features

- 65V Operating Voltage
- Ultra-Low Power Operation
  - Shutdown Mode: 2µA
- Redundant ADC and Comparator (COMP) Acquisitions
- Simultaneous Cell and Bus-Bar Voltage Acquisitions
- 14 Cell-Voltage Measurement Channels
  - 2.2mV Accuracy (-40°C to +125°C)
  - 1.8mV Accuracy (+5°C to +65°C)
- 14 Cell-Balancing Switches
  - >300mA Software-Programmable Balancing Current
  - Optimized Driving and Parking Balancing Modes
  - Automated Balancing with Individual Cell Timers
  - Automated Balancing by Cell Voltage
  - Emergency Discharge Mode
- Six Configurable Auxiliary Inputs for Temperature, Voltage, or GPIO
- Integrated Die Temperature Measurement
- Automatic Thermal Protection
- Individually Configurable Safety Alerts
  - Overvoltage, Undertemperature Faults
  - Undervoltage, Overtemperature Faults
  - 1-Cell Mismatch Alert
- Support ASIL D Requirements for Cell Voltage, Temperature, Communication
- UART, Dual UART Interface
- Battery-Management UART Protocol
  - Daisy-Chain up to 32 Devices
  - Capacitive Communication-Port Isolation
  - Up to 2Mbps Baud Rate (Auto-Detect)
  - 1.5µs Propagation Delay per Device
  - Packet-Error Checking (PEC)
- I^2C Master
- Configurable Hardware-Alert Interfaces
- 32-Bit Unique Device ID
- AEC-Q100 Grade 1
  - Temperature Range -40°C to +125°C

Ordering Information appears at end of data sheet.

19-101237; Rev 0; 11/21

MAX17854 Functional Block Diagram



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Absolute Maximum Ratings

HV to AGND ..... -0.3V to 80V
DCIN, SWn, V_{BLK}, Cn to AGND -0.3 V to min(V_{HV} + 0.3 or 72)V
Cn to Cn-1 ..... -72V to 72V
SWn to SWn-1 ..... -0.3V to 52V
V_{AA} to AGND ..... -0.3V to 2.2V
V_{DDL1} to GNDL1 ..... -0.3V to 2.2V
V_{AA} to V_{DDL1} ..... -0.3V to 0.3V
V_{DDL2}, V_{DDL3} to GNDL2, GNDL3 ..... -0.3V to 6.0V
AGND to GNDL1, GNDL2, GNDL3 ..... -0.3V to 0.3V
AGND to AUXGND ..... -0.3V
GPIOn/AUXINn ..... -0.3V to V_{DDL2} + 0.3V
THRM to AGND ..... -0.3V to V_{AA} + 0.3V
SHDNL to AGND ..... -0.3V to V_{DCIN} + 0.3V
RXLP, RXLN, RXUP, RXUN, ALERTIN to AGND ..... -30V to 30V
TXLP, TXLN, ALERTOUT to GNDL2 ..... -0.3V to 6V
TXUP, TXUN to GNDL3 ..... -0.3V to 6V
CPP to AGND ..... V_{DCIN} - 1V to V_{HV} + 1V
CPN to AGND ..... -0.3V to V_{DCIN} + 0.3V
Maximum Continuous Current into Any Pin (Note 1) ..... -50mA to 50mA
Maximum Continuous Current into SWn Pin (Note 2) . -650mA to 650mA
Maximum Average Power for ESD Diodes (Note 3) ..... $14.4W\sqrt{t}$
Package Continuous Power (Note 4) ..... mW to 2000mW
Operating Temperature Range ..... -40°C to +125°C
Storage Temperature Range ..... -55°C to +150°C
Junction Temperature (Continuous) ..... +150°C
Soldering Lead Temperature (10s maximum) ..... +300°C

Note 1: Balancing switches disabled.

Note 2: One balancing switch enabled, 60s (max).

Note 3: Average power for time period *t* where *t* is the time constant (in µs) of the transient diode current during hot-plug event. For, example, if *t* is 330µs, the maximum average power is 0.793W. Peak current must never exceed 2A. Actual average power during hot-plug must be calculated from the diode current waveform for the application circuit and compared to the maximum rating.

Note 4: Multilayer board. For T_A > +70°C, derate 25mW/°C.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

LQFP

Package Code	C64+13C
Outline Number	21-0083
Land Pattern Number	90-0141
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	40°C/W
Junction to Case (θ_{JC})	8°C/W

For the latest package outline information and land patterns (footprints), go to ***www.maximintegrated.com/packages***. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to ***www.maximintegrated.com/thermal-tutorial***.

Electrical Characteristics

(V_{DCIN} = +56V, T_A = T_{MIN} to T_{MAX} unless otherwise noted, where T_{MIN} = -40°C and T_{MAX} = +125°C. Typical values are at T_A = +25°C. Operation is with the recommend application circuit. Note 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER REQUIREMENTS						
Supply Voltage, DCIN	V_{DCIN}		9		65	V
Supply Voltage VDDL2, VDDL3	V_{DDL2}, V_{DDL3}, V_{DDIO}	V_{DDL2} = V_{DDL3} External overdrive (>$V_{DDL2/3\_REG}$) allowed. Also used as V_{DDIO} in I^2C applications.	$V_{DDL2/3\_REG}$	3.3	5.5	V

Electrical Characteristics (continued)

(V_{DCIN} = +56V, T_A = T_{MIN} to T_{MAX} unless otherwise noted, where T_{MIN} = -40°C and T_{MAX} = +125°C. Typical values are at T_A = +25°C. Operation is with the recommend application circuit. Note 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DCIN Current, Shutdown Mode	I_{DCSHDN}	V_{SHDNL} = 0V		0.1		µA
DCIN Current, Standby Mode	I_{DCSTBY}	V_{SHDNL} > 1.8V, UART in idle mode; not in acquisition mode; balance switches, test current sources, and alert interface disabled; Note 6	2.2		3.1	mA
DCIN Current, ADC Acquisition Mode	I_{DC_ADC}	All cell and auxiliary measurements enabled, OVSAMPL[2:0] = 000b; Note 6		4.2	5	mA
DCIN Current, COMP Acquisition Mode	I_{DC_COMP}	All cell and auxiliary measurements enabled, OVSAMPL[2:0] = 000b; Note 6		4.6	5.5	mA
DCIN Current, ADC + COMP Acquisition Mode	$I_{DC\_ADCCOMP}$	All cell and auxiliary measurements enabled; Note 6		5.4	6.4	mA
DCIN Incremental Current, UART Communication	I_{DCCOMM_UART}	Baud rate = 2Mbps (0% idle time preambles mode), 200pF load on TXUP and TXUN, TXL not active, not in acquisition mode, BALSWEN, CTSTEN = 0000h; Note 6		160	230	µA
HV Current, ADC Acquisition Mode	I_{HVMEAS}	ADC-only acquisition, all cells and auxiliary channels enabled, V_{HV} = V_{DCIN} + 5.5V	0.7	0.9	1.1	mA
HV Current, Comparator Scan Mode	I_{HVCOMP}	COMP only acquisition, all cells and auxiliary channels enabled, V_{HV} = V_{DCIN} + 5.5V	0.7	0.9	1.1	mA
Incremental HV Current, Cell-Balancing Mode	I_{HVBAL}	V_{HV} = V_{DCIN} + 5.5V, n balancing switches enabled	(n + 1) x 5	(n + 1) x 15.5	(n + 1) x 26	µA
CELL VOLTAGE INPUTS (Cn, V_{BLK})						
Differential Input Range	V_{CELLn}	Unipolar mode, Note 7	0		5	V
		Bipolar mode, Note 7	-2.5		2.5	
Common-Mode Input Range	V_{CnCM}	Not connected to SWn inputs	0		65	V
Input Leakage Current	I_{LKG_Cn}	Not in acquisition mode, V_{Cn} = 65V	-100	±10	100	nA
V_{BLK} Input Resistance	R_{VBLK}	V_{BLK} = V_{DCIN} = 57.6V	4.5	10	20	MΩ
HVMUX Switch Resistance	R_{HVMUX}	CTSTDAC[3:0] = Fh	1.7	3.3	5	kΩ
CELL-BALANCING INPUTS (SWn)						
Leakage Current	I_{LKG_SW}	V_{SW0} = 0V, V_{SWn} = 5V, V_{SWn} - 1 = 0V	-1.0		1.0	µA
Resistance, SWn to SWn-1	R_{SW}	BALSWEN[n-1] = 1, I_{SWn} = 100mA	0.5	1.25	2.25	Ω
		BALSWEN[n-1] = 1, I_{SWn} = 300mA, Note 8		1.3		Ω
Maximum Allowed Balancing Current	I_{BAL_MAX}	T_J = +125°C, CBMEASEN = 0x00, FLXPCKEN1/2 = 0, all even or all odd channels enabled. Note 9		650		mA
AUXILIARY INPUTS (AUXINn)						
Input Voltage Range	V_{AUXIN}	V_{ADCREF} = V_{THRM} or V_{REF} based on AUXREFSEL	0		V_{ADCREF}	V

Electrical Characteristics (continued)

(V_{DCIN} = +56V, T_A = T_{MIN} to T_{MAX} unless otherwise noted, where T_{MIN} = -40°C and T_{MAX} = +125°C. Typical values are at T_A = +25°C. Operation is with the recommend application circuit. Note 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Leakage Current	I_{LKG_AUX}	Not in acquisition mode, V_{AUXINn} = 1.65V	-400	10	400	nA
THRM OUTPUT						
Switch Resistance, V_{AA} to THRM	R_{THRM}			25	70	Ω
Leakage Current	I_{LKG_THRM}	V_{THRM} = V_{AA}	-1		1	µA
MEASUREMENT ACCURACY						
ADC Measurement Error, HVMUX Inputs	$V_{CELLnERR}$	Unipolar mode; V_{CELLn} = 3.6V; SCANMODE = 0x0, 0x1; Note 10		±200		µV
		Unipolar mode; 0.2V ≤ V_{CELLn} ≤ 4.8V; 5°C < temp < +65°C; SCANMODE = 0x0, 0x1; Note 10	-1.8		1.8	mV
		Unipolar mode; 0.2V ≤ V_{CELLn} ≤ 4.8V; -40°C < temp < +125°C; SCANMODE = 0x0, 0x1; Note 10	-2.2		2.2	
		Bipolar mode; V_{CELLn} = 1.1V; SCANMODE = 0x0, 0x1; Note 10		±200		µV
		Bipolar mode; -2.3V ≤ V_{CELLn} ≤ +2.3V; +5°C < temp < +65°C; SCANMODE = 0x0, 0x1; Note 10	-1.8		1.8	mV
		Bipolar mode; -2.3V ≤ V_{CELLn} ≤ +2.3V; -40°C < temp < +125°C; SCANMODE = 0x0, 0x1; Note 10	-2.2		2.2	
ADC Measurement Error, ALTMUX Inputs	V_{SWnERR}	Unipolar mode; V_{CELL} = 3.6V; SCANMODE = 0x0, 0x1; Note 10		±200		µV
		Unipolar mode; 0.2V ≤ V_{CELLn} ≤ 4.8V; SCANMODE = 0x0, 0x1; Note 10	-2.2		2.2	mV
		Bipolar mode; V_{CELLn} = 1.1V; SCANMODE = 0x0, 0x1; Note 10		±200		µV
		Bipolar mode; 0 ≤ V_{CELLn} ≤ 2.3V; SCANMODE = 0x0, 0x1	-2.2		2.2	mV
ADC Measurement Error, V_{BLK} Input	V_{BLKERR}	9V ≤ V_{BLK} ≤ 64.4V; V_{DCIN} = 64.4V; SCANMODE = 0x0, 0x1; Note 11	-160		160	mV
ADC Measurement Error, Ratiometric AUXIN Inputs	$V_{OS\_AUX\_RATIO}$	AUXREF[n] = 0b; SCANMODE = 0x0, 0x1; OVSAMPL != 0x0; Note 11	-3.5		3.5	mV
ADC Measurement Error, Absolute AUXIN Inputs	$V_{OS\_AUX\_ABS}$	AUXREF[n] = 1b; SCANMODE = 0x0, 0x1; Note 11	-4		4	mV
Total Measurement Error, Die Temperature	T_{DIE_ERR}	T_J = -40°C to +125°C; OVSAMPL[2:0] = 000b; Note 8	-5	0	5	°C
Cell Input Referred Noise	$V_{CELLNOISE}$	OVSAMPL[2:0] = 0x3h; Note 8		250		$µV_{RMS}$
Auxiliary Input Referred Noise	$V_{AUXNOISE}$	OVSAMPL[2:0] = 0x3h; Note 8		50		$µV_{RMS}$

Electrical Characteristics (continued)

(V_{DCIN} = +56V, T_A = T_{MIN} to T_{MAX} unless otherwise noted, where T_{MIN} = -40°C and T_{MAX} = +125°C. Typical values are at T_A = +25°C. Operation is with the recommend application circuit. *Note 5*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Differential Nonlinearity (Any Conversion)	DNL			±1.0		LSb
ADC Resolution			12			bits
Level-Shifting Amplifier Offset	V_{OS_LSAMP}	DIAGSEL[2:0] = 011b; *Note 12*	-2	0.1	+2	mV
COMPARATOR						
Input Common-Mode Range	V_{CM_COMP}		0		65	V
Input Differential Mode Range	V_{DM_COMP}		0		5	V
Comparator Accuracy	V_{OS_COMP}	0.2V ≤ V_{CELLn} ≤ 4.8V	-20		20	mV
SHDNL INPUT AND CHARGE PUMP						
Input Low Voltage	V_{IL_SHDNL}				0.6	V
Input High Voltage	V_{IH_SHDNL}		1.8			V
Regulated Voltage	$V_{SHDNLIMIT}$	V_{DCIN} ≥ 12V	7	10.8	14	V
		V_{DCIN} = 9V		8.5		
Pulldown Resistance	$R_{FORCEPOR}$	FORCEPOR = 1	200	500	800	Ω
Input Leakage Current	I_{LKG_SHDNL}	V_{SHDNL} = 3.3V			1	µA
		V_{SHDNL} = 65V		40	75	
Charge Pump Current - UARTL/UARTU	I_{SHDNL}	V_{SHDNL} < $V_{SHDNLIMIT}$; baud rate = 2Mbps; *Note 13*	15	117	350	µA
UARTSEL						
UARTSEL Input High Voltage	$V_{IH\_UARTSEL}$		0.7 x V_{AA}			V
GENERAL-PURPOSE I/O (GPIOn)						
Input Low Voltage	V_{IL_GPIO}				0.3 x V_{DDL2}	V
Input High Voltage	V_{IH_GPIO}		0.7 x V_{DDL2}			V
Pulldown Resistance	R_{GPIO}	AUXINn/GPIOn configured as GPIO input	0.5	2	7.5	MΩ
Output Low Voltage	V_{OL_GPIO}	I_{SINK} = 4mA			0.4	V
Output High Voltage	V_{OH_GPIO}	I_{SOURCE} = 4mA	V_{DDL2} - 0.4			V
ALERTIN						
ALERTIN Comparator Threshold	V_{CL}		$V_{DDL2/3}$/ 2 - 0.4	$V_{DDL2/3}$/ 2	$V_{DDL2/3}$/ 2 + 0.4	V
ALERTIN Comparator Hysteresis	$V_{HYS\_ALERTIN}$			75		mV
ALERTIN Common-Mode Voltage Bias	V_{CM}			$V_{DDL2/3}$/ 2		V
Leakage Current	$I_{LKG\_ALERTIN}$	$V_{ALERTIN}$ = 1.5V		±1.0		µA
Input Capacitance	$C_{ALERTIN}$			2		pF

Electrical Characteristics (continued)

(V_{DCIN} = +56V, T_A = T_{MIN} to T_{MAX} unless otherwise noted, where T_{MIN} = -40°C and T_{MAX} = +125°C. Typical values are at T_A = +25°C. Operation is with the recommend application circuit. *Note 5*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Bit Period	t_{BIT}	*Note 14*		8		1/ f_{OSC_16M}
ALERTIN Fall Time	$t_{ALERTIN\_FALL}$	*Note 8*, *Note 15*			0.5	t_{BIT}
ALERTIN Rise Time	$t_{ALERTIN\_RISE}$	*Note 8*, *Note 15*			0.5	t_{BIT}
ALERTIN Qualification Time	$t_{ALERTIN\_QUAL}$			25		µs
Propagation Delay (ALERTIN Port to ALERTOUT Port)	t_{ALERT_PROP}			2.5	3	t_{BIT}
Start-Up Time from SHNDL High and V_{AA} = 0V to ALERTIN Valid	$t_{ALERTIN\_STARTUP}$			1		ms
ALERTOUT						
Output Low Voltage	$V_{OL\_ALERTOUT}$	I_{SINK} = 20mA			0.4	V
Output High Voltage	$V_{OH\_ALERTOUT}$	I_{SOURCE} = 20mA	V_{DDL2} - 0.4			V
Leakage Current	$I_{LKG\_ALERTOUT}$	$V_{ALERTOUT}$ = 1.5V	-1		1	µA
3.3V REGULATOR (V_{DDL2}, V_{DDL3})						
3.3V Regulator Output Voltage	$V_{DDL2/3\_REG}$	0 ≤ $I_{DDL2/3}$ < 30mA	3.2	3.3	3.4	V
Short-Circuit Current	$I_{DDL2/3\_SC}$	$V_{DDL2/3}$ shorted to AGND	30			mA
1.8V REGULATOR (V_{AA})						
1.8V Regulator Output Voltage	V_{AA}	0 ≤ I_{AA} < 3mA	1.71	1.8	1.89	V
Short-Circuit Current	I_{AA_SC}	V_{AA} shorted to AGND	10			mA
POR Threshold	$V_{1.8REG\_PORRISE}$	V_{AA} rising	1.3	1.5	1.65	V
	$V_{1.8REG\_PORHYS}$			50		mV
THERMAL SHUTDOWN						
Thermal Shutdown Temperature	T_{SHDN}	Temperature rising; *Note 8*		+145		°C
Thermal Shutdown Hysteresis	T_{HYS}	*Note 8*		15		°C
HV CHARGE PUMP						
Output Voltage (VHV - VDCIN)	$V_{HV-DCIN}$	9V ≤ V_{DCIN} ≤ 12V, I_{LOAD} = 1.5mA	6.5	6.9	7.4	V
		12V ≤ V_{DCIN} ≤ 65V, I_{LOAD} = 3mA	6.5	6.9	7.4	
Output Voltage (VHV - VTOPCELL)	$V_{HV-DCIN\_FLEX}$	14V ≤ V_{DCIN} ≤ 65V, I_{LOAD} = 3mA, FLXPCKEN1/2 = 1b	8.0	8.5	9.0	V
Charge Pump Efficiency	Eff_{HVCP}	V_{DCIN} = 57.6V; *Note 16*		38		%

Electrical Characteristics (continued)

(V_{DCIN} = +56V, T_A = T_{MIN} to T_{MAX} unless otherwise noted, where T_{MIN} = -40°C and T_{MAX} = +125°C. Typical values are at T_A = +25°C. Operation is with the recommend application circuit. *Note 5*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OSCILLATORS						
LFOSC Frequency	f_{LFOSC}		32.11	32.768	33.42	kHz
HFOSC Frequency	f_{HFOSC}		15.68	16	16.32	MHz
DIAGNOSTIC TEST SOURCES						
Cell Test Source Current	I_{TSTCn}	CTSTDAC[3:0] = 9h, V_{C0} < $V_{DDL2/3}$ - 1.4V, $V_{DDL2/3}$ = 3.3V	50	62.5	75	µA
		CTSTDAC[3:0] = 6h, V_{C0} < $V_{DDL2/3}$ - 1.4V, $V_{DDL2/3}$ = 3.3V	36	45	54	
		CTSTDAC[3:0] = 6h, V_{C1-C14} > V_{AGND} + 1.4V	-54	-45	-36	
		CTSTDAC[3:0] = 9Fh, V_{C1-C14} > V_{AGND} + 1.4V	-75	-62.5	-50	
HVMUX Test Source Current	$I_{TSTHVMUX}$	CTSTDAC[3:0] = 9h, V_{Cn} < V_{HV} - 1.4V, V_{HV} = 53.5V	25	31.25	37.5	µA
		CTSTDAC[3:0] = 6h, V_{Cn} < V_{HV} - 1.4V, V_{HV} = 53.5V	18	22.5	27	
AUXIN Test Source Current	$I_{TSTAUXIN}$	CTSTDAC[3:0] = 9h, V_{AUXINn} < $V_{DDL2/3}$ - 1.4V, $V_{DDL2/3}$ = 3.3V	50	62.5	75	µA
		CTSTDAC[3:0] = 6h, V_{AUXINn} < $V_{DDL2/3}$ – 1.4V, $V_{DDL2/3}$ = 3.3V	36	45	54	
		CTSTDAC[3:0] = 6h, V_{AUXINn} > V_{AGND} + 1.4V	-54	-45	-36	
		CTSTDAC[3:0] = 9h, V_{AUXINn} > V_{AGND} + 1.4V	-75	-62.5	-50	
DIAGNOSTIC REFERENCES						
ALTREF Voltage	V_{ALTREF}	DIAGSEL[2:0] = 001b; *Note 12*	0.99	1.00	1.01	V
ALTREF Temperature Coefficient ($\Delta V_{ALTREF}/\Delta T$)	A_{ALTREF}	*Note 8*		±25		ppm/°C
PTAT Output Voltage	V_{PTAT}	T_J = +120°C; *Note 8*		1.14		V
PTAT Temperature Coefficient ($\Delta V_{PTAT}/\Delta T$)	A_{V_PTAT}	*Note 8*		2.87		mV/°C
PTAT Temperature Offset	T_{OS_PTAT}	*Note 8*		-4.4		°C
ALERTS						
ALRTVDDL1 Threshold	V_{VDDL1_OC}	V_{AA} = 1.8V	1.62	1.65	1.68	V
ALRTVDDL2/3 Threshold	$V_{VDDL2/3\_OC}$	$V_{DDL2/3}$ = 3.3V	2.9	3.0	3.1	V
ALRTGNDLn Threshold	V_{GNDL_OC}	AGND = 0V	0.05	0.15	0.3	V
ALRTHVUV Threshold	V_{HVUV}	V_{HV} - V_{DCIN} falling, FLXPCKEN1/2 = 0	1.8	2	2.2	V
ALRTHVOV Threshold	V_{HVOV}	V_{HV} - V_{DCIN} rising	9.0	9.5	9.9	V
ALRTHVHDRM Threshold	V_{HVHDRM}	ALRTHVHDRM = 0	3.0			V

Electrical Characteristics (continued)

(V_{DCIN} = +56V, T_A = T_{MIN} to T_{MAX} unless otherwise noted, where T_{MIN} = -40°C and T_{MAX} = +125°C. Typical values are at T_A = +25°C. Operation is with the recommend application circuit. *Note 5*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ALRTTEMP Threshold	$T_{ALRTTEMP}$	*Note 8*	115	120	125	°C
ALRTTEMP Hysteresis	$T_{ALRTTEMPHYS}$	*Note 8*		2		°C
UART OUTPUTS (TXLP, TXLN, TXUP, TXUN)						
Output Low Voltage	V_{OL}	I_{SINK} = 20mA			0.4	V
Output High Voltage (TXLP, TXLN)	V_{OH}	I_{SOURCE} = 20mA	V_{DDL2} - 0.4			V
Output High Voltage (TXUP, TXUN)	V_{OH}	I_{SOURCE} = 20mA	V_{DDL3} - 0.4			V
Leakage Current	I_{LKG_TX}	V_{TX} = 1.5V	-1		1	µA
UART INPUTS (RXLP, RXLN, RXUP, RXUN)						
Input Voltage Range	V_{RX}		-25		25	V
Receiver High Comparator Threshold	V_{CH}	*Note 17*	$V_{AA}/2$ - 0.4	$V_{AA}/2$	$V_{AA}/2$ + 0.4	V
Receiver Zero-Crossing Comparator Threshold	V_{ZC}	*Note 17*	-0.4	0	0.4	V
Receiver Low Comparator Threshold	V_{CL}	*Note 17*	$-V_{AA}/2$ - 0.4	$-V_{AA}/2$	$-V_{AA}/2$ + 0.4	V
Receiver Comparator Hysteresis	V_{HYS_RX}	*Note 17*		75		mV
Receiver Common-Mode Voltage Bias	V_{CM}	*Note 17*		$V_{AA}/2$		V
Leakage Current	I_{LKG_RX}	V_{RX} = 0.9V		±1.0		µA
Input Capacitance (RXLP, RXLN)	C_{RXL}			4		pF
Input Capacitance (RXUP, RXUN)	C_{RXU}			4		pF
UART TIMING						
Bit Period	t_{BIT}	Baud rate = 2Mbps; *Note 14*		8		1/f_{OSC_16M}
		Baud rate = 1Mbps; *Note 14*		16		
		Baud rate = 0.5Mbps; *Note 14*		32		
Rx Idle to START Setup Time	t_{RXSTSU}	*Note 8*	0		1	t_{BIT}
STOP Hold Time to Idle	t_{SPHD}	*Note 8*			0.5	t_{BIT}
Rx Minimum Idle Time (STOP Bit to START Bit)	$t_{RXIDLESPST}$	*Note 8*	1			t_{BIT}
Rx Fall Time	t_{FALL}	*Note 8*, *Note 15*			0.5	t_{BIT}
Rx Rise Time	t_{RISE}	*Note 8*, *Note 15*			0.5	t_{BIT}
Propagation Delay (Rx Port to Tx Port)	t_{PROP}			2.5	3	t_{BIT}

Electrical Characteristics (continued)

(V_{DCIN} = +56V, T_A = T_{MIN} to T_{MAX} unless otherwise noted, where T_{MIN} = -40°C and T_{MAX} = +125°C. Typical values are at T_A = +25°C. Operation is with the recommend application circuit. *Note 5*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Start-Up Time from SHNDL High and V_{AA} = 0V to RXUP/RXUN Valid	$t_{STARTUP}$			1		ms
I²C						
Input Voltage Low	V_{IL}	$V_{DDL2/3} \le V_{DDIO} \le 5.5V$			$0.3V_{DDIO}$	V
Input Voltage High	V_{IH}	$V_{DDL2/3} \le V_{DDIO} \le 5.5V$	$0.7V_{DDIO}$			V
Input Voltage Hysteresis	V_{HYST}			0.15		V
Input Leakage Current	I_{IN}		-1.0	0.1	1.0	µA
Input Capacitance	C_{IN}			10		pF
Output Voltage Low	V_{OL}	I_{SINK} = 3mA			0.4	V
SCL Clock Frequency	f_{SCL}	400kHz mode (I2CFSCL = 1)	0		400	kHz
		100kHz mode (I2CFSCL = 0)	0		100	
Hold Time for a (Repeated) START Condition	$t_{HD;STA}$	400kHz mode (I2CFSCL = 1)	0.6			µs
		100kHz mode (I2CFSCL = 0)	4.0			
SCL Pulse Width Low	t_{LOW}	400kHz mode (I2CFSCL = 1)	1.3			µs
		100kHz mode (I2CFSCL = 0)	4.7			
SCL Pulse Width High	t_{HIGH}	400kHz mode (I2CFSCL = 1)	0.6			µs
		100kHz mode (I2CFSCL = 0)	4.0			
Setup Time for a Repeated START Condition	$t_{SU;STA}$	400kHz mode (I2CFSCL = 1)	0.6			µs
		100kHz mode (I2CFSCL = 0)	4.7			
Data Hold Time	$t_{HD;DAT}$	*Note 18*	0			ns
		Master transmitting data	300			
Data Setup Time	$t_{SU;DAT}$	Master receiving data, and 400kHz mode (I2CFSCL = 1) bus monitor check	100			ns
		Master receiving data, and 100kHz mode (I2CFSCL = 0) bus monitor check	250			
		Master transmitting data	300			
Rise Time of SDA and SCL	t_r				300	ns
Fall Time of SDA and SCL	t_f				300	ns
Setup Time for STOP Condition	$t_{SU;STO}$	400kHz mode (I2CFSCL = 1)	0.6			µs
		100kHz mode (I2CFSCL = 0)	4.0			
Bus Free Time Between a STOP and START Condition	t_{BUF}	400kHz mode (I2CFSCL = 1)	1.3			µs
		100kHz mode (I2CFSCL = 0)	4.7			
Bus Capacitance Allowed	C_b				400	pF

Electrical Characteristics (continued)

(V_{DCIN} = +56V, T_A = T_{MIN} to T_{MAX} unless otherwise noted, where T_{MIN} = -40°C and T_{MAX} = +125°C. Typical values are at T_A = +25°C. Operation is with the recommend application circuit. *Note 5*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Suppressed Spike Pulse Width	t_{sp}	Width of spikes that must be suppressed by the input filter of both SDA and SCL signals		50		ns
Noise Margin at LOW Level	V_{nL}	For each connected device (including hysteresis)	$0.1V_{DDIO}$			V
Noise Margin at HIGH Level	V_{nL}	For each connected device (including hysteresis)	$0.2V_{DDIO}$			V

Note 5: Unless otherwise noted, limits are 100% production-tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.

Note 6: Acquisition mode (ADC conversions) is entered when the SCAN bit is set and ends when SCANDONE is set. With the typical acquisition duty-cycle very low, the average current I_{DCIN} is much less than I_{DCMEAS}. Total supply current during communication I_{DCIN} = I_{DCCOMM} + I_{DCSTBY}.

Note 7: Measurement accuracy range is guaranteed from V_{CELLn_min} + 0.2V and V_{CELLn_max} - 0.2V.

Note 8: Guaranteed by design and not production tested.

Note 9: Not production tested. See the *Cell-Balancing Current* section for details on the maximum allowed balancing current. Duty-cycle is calculated for a 10-year device lifetime.

Note 10: V_{CELLn} = V_{Cn} - V_{Cn-1}, V_{CELLn} = $V_{CELLn-1}$, and V_{DCIN} = 14 x $|V_{CELLn}|$ (V_{DCIN} = 9V, min). Accuracy measurements represent initial total measurement error with the input noise oversampled below 1 LSB.

Note 11: Accuracy measurements represent the initial total measurement error with the input noise oversampled below 1 LSB.

Note 12: As measured during specified diagnostic mode.

Note 13: I_{SHDNL} measured with V_{SHDNL} = 0.3V, STOP characters, zero idle time, V_{RX_PEAK} = 3.3V.

Note 14: In daisy-chain applications, the bit time of the second stop bit may be less than specified to account for clock rate variation and sampling error between devices.

Note 15: Fall time measured 90% to 10%; rise time measured 10% to 90%.

Note 16: Charge pump efficiency = ΔI_{LOAD} / ΔI_{SUPPLY}, where I_{LOAD} is applied from HV to AGND, ΔI_{LOAD} = 5mA, and ΔI_{SUPPLY} = I_{DCIN} (for I_{LOAD} = 5mA) - I_{DCIN} (for I_{LOAD} = 0).

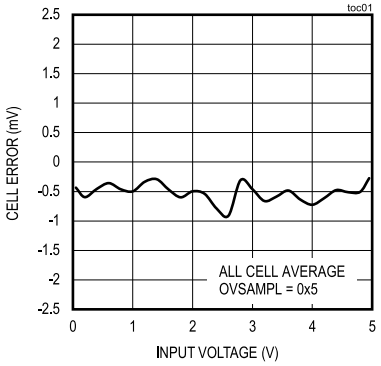
Note 17: Differential signal (V_{UARTP} - V_{UARTN}) where V_{UARTP} and V_{UARTN} do not exceed a common-mode voltage range of ±40V.

Note 18: A device must internally provide a hold time of at least 300ns for the SDA signal (referred to the V_{IH_min} of the SCL signal) to bridge the undefined region of the falling edge of SCL.

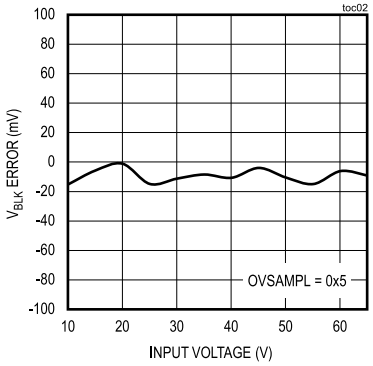
Typical Operating Characteristics

(DCIN = 56V, $V_{DDL2/3}$ = 3.3V, T_A = +25°C, unless otherwise noted)

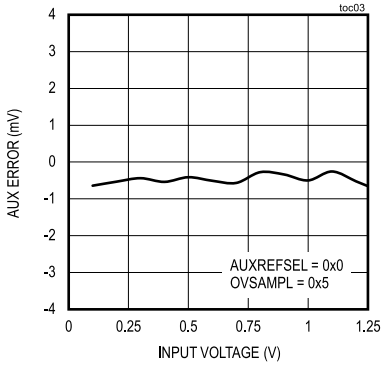
CELL ACCURACY vs. INPUT VOLTAGE



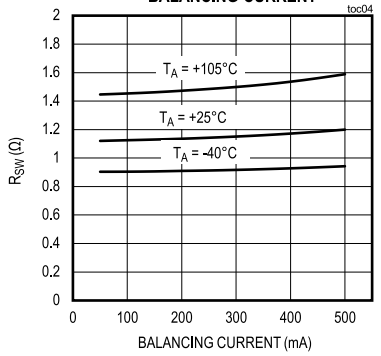
V_{BLK} ACCURACY vs. INPUT VOLTAGE



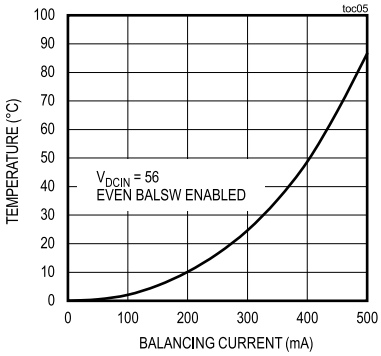
AUX ACCURACY vs. INPUT VOLTAGE



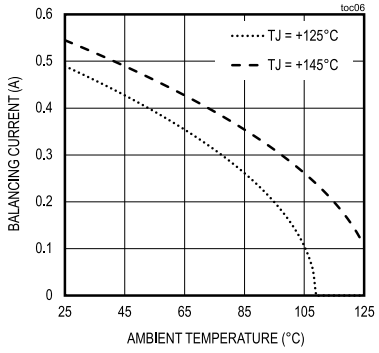
SINGLE-CHANNEL BALANCING SWITCH RESISTANCE vs. BALANCING CURRENT



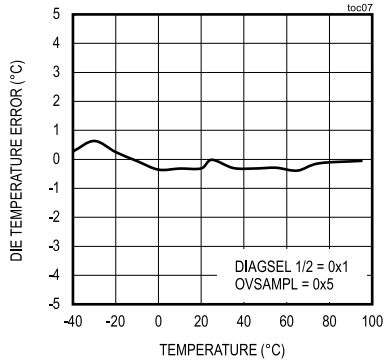
TEMPERATURE RISE vs. BALANCING CURRENT



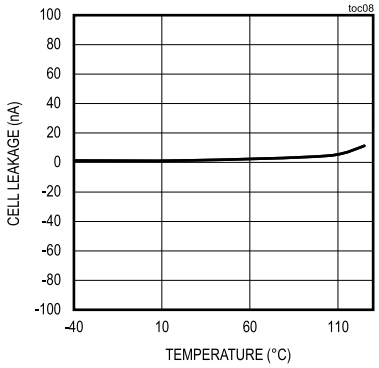
BALANCING CURRENT vs. JUNCTION TEMPERATURE



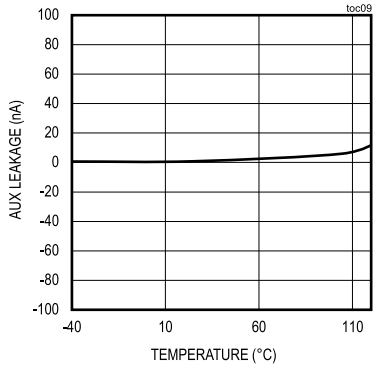
DIE TEMP ERROR vs. AMBIENT TEMP



CELL LEAKAGE vs. TEMPERATURE

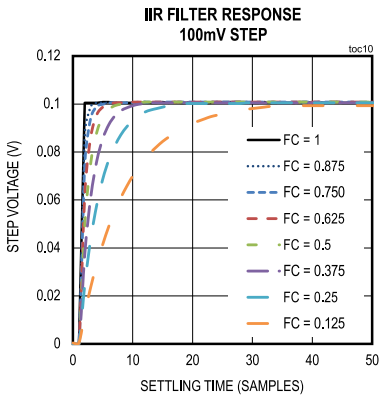


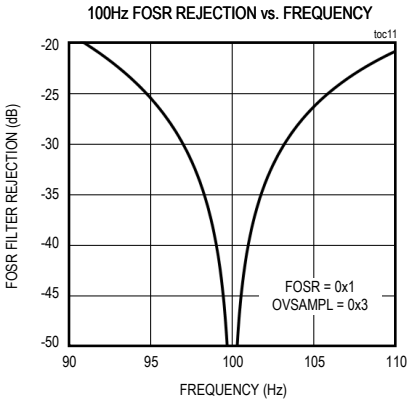
AUX LEAKAGE vs. TEMPERATURE

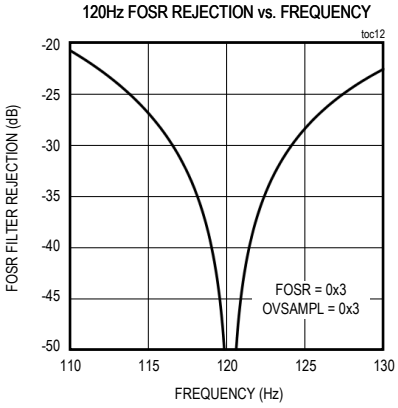


Typical Operating Characteristics (continued)

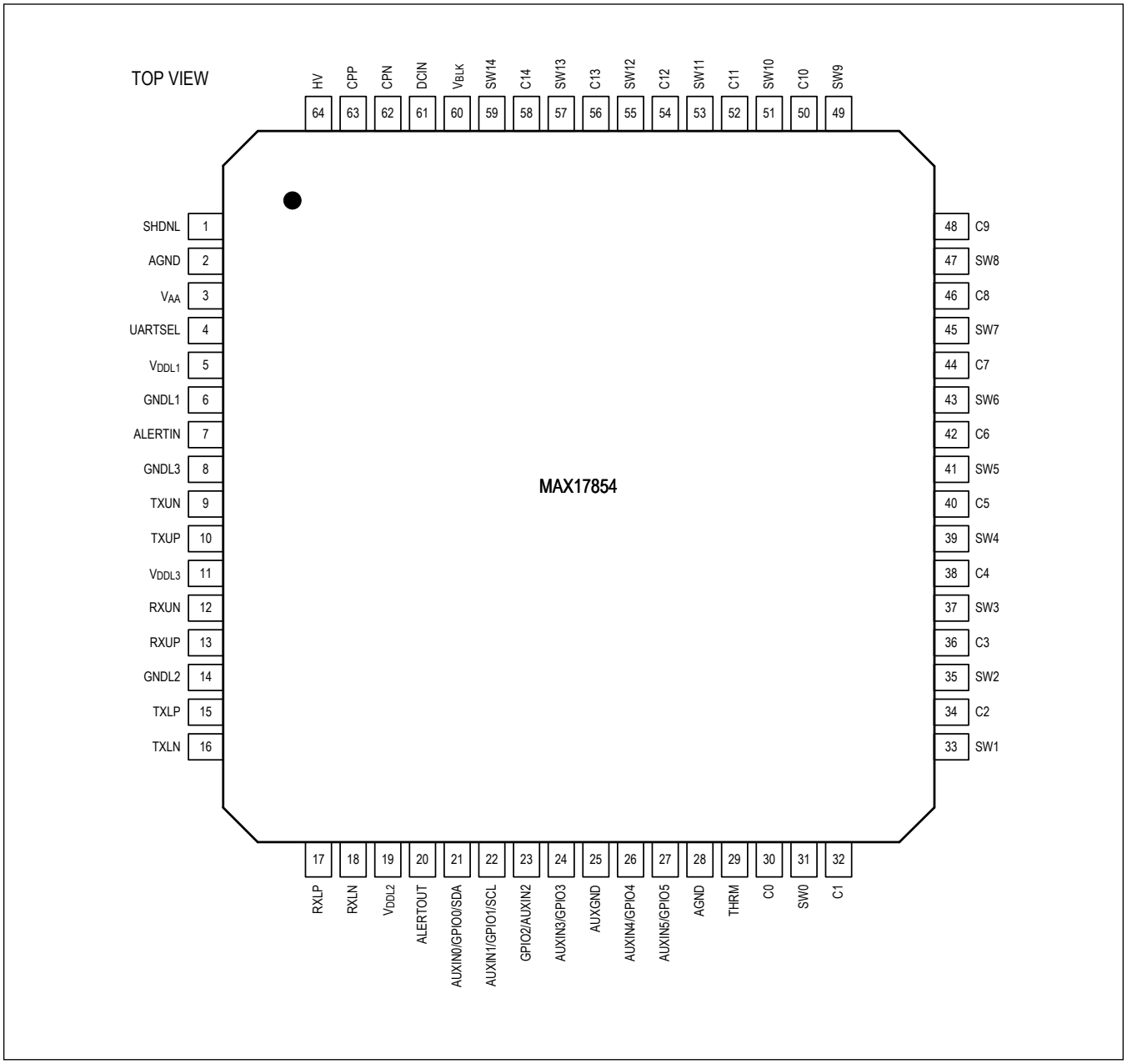
(DCIN = 56V, $V_{DDL2/3}$ = 3.3V, T_A = +25°C, unless otherwise noted)







Pin Configuration



Pin Description

PIN	NAME	FUNCTION	REF SUPPLY	TYPE
1	SHDNL	Shutdown Active-Low Input, +72V Tolerant. This input is controlled solely through UART communication and software control when bypassed with a 1nF capacitor to AGND. Connect only passive components to this pin. For single-ended UART, SHDNL must be driven externally.	AGND	Input
2	AGND	Analog Ground. Connect to the negative terminal of cell 1 and the ground plane.	DCIN	Ground
3	V_{AA}	V_{AA} (1.8V) Regulator Output Used to Supply V_{DDL1}. Bypass with a 1µF capacitor to AGND.	AGND	Power
4	UARTSEL	Connect to V_{AA}	V_{DDL1}	Input
5	V_{DDL1}	1.8V Digital Supply. Connect externally to V_{AA} and bypass with 0.47µF capacitor to GNDL1.	GNDL1	Power
6	GNDL1	Digital Ground. Connect to ground plane.	V_{DDL1}	Ground
7	ALERTIN	Fault Alert Input. Connect to upper daisy-chained device.	V_{AA}	Input
8	GNDL3	Ground for Upper Port Transmitter. Connect to ground plane.	V_{DDL3}	Ground
9	TXUN	Negative Output for Upper UART Transmitter. Driven between V_{DDL3} and GNDL3.	V_{DDL3}	Output/Input
10	TXUP	Positive Output for Upper UART Transmitter. Driven between V_{DDL3} and GNDL3.	V_{DDL3}	Output/Input
11	V_{DDL3}	3.3V Regulator Output. Supply for upper UART transceiver and ALERT pins. Connect externally to V_{DDL2} and bypass with 0.47µF capacitor to GNDL3. External overdrive allowed: V_{DDL3} must be ≥ $V_{DDL2/3\_REG}$.	GNDL3	Power
12	RXUN	Negative Input for Upper UART Port Receiver. If not used, pins can be left unconnected or connected to GNDL3. Tolerates ±30V.	V_{AA}	Input
13	RXUP	Positive Input for Upper UART Port Receiver. If not used, pins can be left unconnected or connected to GNDL3. Tolerates ±30V. If configured for single-ended UART, connect to GNDL3.	V_{AA}	Input
14	GNDL2	Ground for Lower Port Transmitter. Connect to ground plane.	V_{DDL2}	Ground
15	TXLP	Positive Output for Lower UART Transmitter. Driven between V_{DDL2} and GNDL2.	V_{DDL2}	Output
16	TXLN	Negative Output for Lower UART Transmitter. Dependent on UARTSEL selection. Driven between V_{DDL2} and GNDL2.	V_{DDL2}	Output
17	RXLP	Positive Input for Lower UART Port Receiver. If not used, pins can be left unconnected or connected to GNDL3. Tolerates ±30V. If configured for single-ended UART, connect to GNDL3.	V_{AA}	Input
18	RXLN	Negative Input for Lower UART Port Receiver. If not used, pins can be left unconnected or connected to GNDL2. Tolerates ±30V.	V_{AA}	Input
19	V_{DDL2}	3.3V Regulator Output. Supply for Lower UART transceiver and ALERT pins. Connect externally to V_{DDL3} and bypass with 0.47µF capacitor to GNDL3. External overdrive allowed: V_{DDL2} must be ≥ $V_{DDL2/3\_REG}$.	GNDL2	Power
20	ALERTOUT	Alert Output Interface. Configured using SPIDRVINT as daisy-chained CMOS output (connected to ALERTIN), or open-drain output (connected to external 10kΩ pullup to V_{DDL2}, V_{DDL3}).	V_{DDL2}	Output

Pin Description (continued)

PIN	NAME	FUNCTION	REF SUPPLY	TYPE
21	AUXIN0/ GPIO0/SDA	Configurable between Auxiliary Input, GPIO, or SDA. When configured as a ratiometric auxiliary input for temperature measurement, connect to a voltage-divider consisting of a 10kΩ pullup to THRM and a 10kΩ NTC thermistor to AGND. If not used, connect to the pullup only. When configured as a GPIO, it is driven between V_{DDL2} and GNDL2. A 2MΩ internal pulldown is needed when the pin is configured as an input. When configured as an I^2C SDA I/O, an external pullup resistor is required. The pin is driven between V_{DDL2} and GNDL2.	V_{DDL2}	Input/Output
22	AUXIN1/ GPIO1/SCL	Configurable between Auxiliary Input, GPIO, or SCL. When configured as a ratiometric auxiliary input for temperature measurement, connect to a voltage-divider consisting of a 10kΩ pullup to THRM and a 10kΩ NTC thermistor to AGND. If not used, connect to the pullup only. When configured as a GPIO, it is driven between V_{DDL2} and GNDL2. A 2MΩ internal pulldown is needed when the pin is configured as an input. When configured as an I^2C SCL, it becomes the clock output of I^2C.	V_{DDL2}	Input/Output
23	AUXIN2/ GPIO2	Configurable between Auxiliary Input or GPIO. When configured as a ratiometric auxiliary input for temperature measurement, connect to a voltage-divider consisting of a 10kΩ pullup to THRM and a 10kΩ NTC thermistor to AGND. If not used, connect to the pullup only. When configured as a GPIO, it is driven between V_{DDL2} and GNDL2. A 2MΩ internal pulldown is needed when the pin is configured as an input.	V_{DDL2}	Input/Output
24	AUXIN3/ GPIO3	Configurable between Auxiliary Input or GPIO. When configured as a ratiometric auxiliary input for temperature measurement, connect to a voltage-divider consisting of a 10kΩ pullup to THRM and a 10kΩ NTC thermistor to AGND. If not used, connect to the pullup only. When configured as a GPIO, it is driven between V_{DDL2} and GNDL2. A 2MΩ internal pulldown is needed when the pin is configured as an input.	V_{DDL2}	Input/Output
25	AUXGND	Connect to AGND Ground Plane.	V_{AA}	Power

Pin Description (continued)

PIN	NAME	FUNCTION	REF SUPPLY	TYPE
26	AUXIN4/ GPIO4	Configurable between Auxiliary Input or GPIO. When configured as a ratiometric auxiliary input for temperature measurement, connect to a voltage-divider consisting of a 10kΩ pullup to THRM and a 10kΩ NTC thermistor to AGND. If not used, connect to the pullup only. When configured as a GPIO, it is driven between V_{DDL2} and GNDL2. A 2MΩ internal pulldown is needed when the pin is configured as an input.	V_{DDL2}	Input/Output
27	AUXIN5/ GPIO5	Configurable between Auxiliary Input, or General-Purpose I/O. When configured as a ratiometric auxiliary input for temperature measurement, connect to a voltage-divider consisting of a 10kΩ pullup to THRM and a 10kΩ NTC thermistor to AGND. If not used, connect to the pullup only. When configured as a GPIO, it is driven between V_{DDL2} and GNDL2. A 2MΩ internal pulldown is needed when the pin is configured as an input.	V_{DDL2}	Input/Output
28	AGND	Analog Ground. Connect to the negative terminal of cell 1 and the ground plane.	DCIN	Ground
29	THRM	Switched Output Connected Internally to V_{AA}. THRM is used to drive the external NTC voltage-divider for the auxiliary inputs. The output is enabled only during measurements or as configured by THRMMODE[1:0]. This output can source up to 2mA.	AUXGND	Power
30	C0	Voltage Input for Cell 1 Negative. Connect to AGND.		Input
31	SW0	Balance Input for Cell 1 Negative.		Input
32	C1	Voltage Input for Cell 1 Positive (Cell 2 Negative).		Input
33	SW1	Balance Input for Cell 1 Positive (Cell 2 Negative).		Input
34	C2	Voltage Input for Cell 2 Positive (Cell 3 Negative).		Input
35	SW2	Balance Input for Cell 2 Positive (Cell 3 Negative).		Input
36	C3	Voltage Input for Cell 3 Positive (Cell 4 Negative).		Input
37	SW3	Balance Input for Cell 3 Positive (Cell 4 Negative).		Input
38	C4	Voltage Input for Cell 4 Positive (Cell 5 Negative).		Input
39	SW4	Balance Input for Cell 4 Positive (Cell 5 Negative).		Input
40	C5	Voltage Input for Cell 5 Positive (Cell 6 Negative).		Input
41	SW5	Balance Input for Cell 5 Positive (Cell 6 Negative).		Input
42	C6	Voltage Input for Cell 6 Positive (Cell 7 Negative).		Input
43	SW6	Balance Input for Cell 6 Positive (Cell 7 Negative).		Input
44	C7	Voltage Input for Cell 7 Positive (Cell 8 Negative).		Input
45	SW7	Balance Input for Cell 7 Positive (Cell 8 Negative).		Input
46	C8	Voltage Input for Cell 8 Positive (Cell 9 Negative).		Input
47	SW8	Balance Input for Cell 8 Positive (Cell 9 Negative).		Input
48	C9	Voltage Input for Cell 9 Positive (Cell 10 Negative).		Input
49	SW9	Balance Input for Cell 9 Positive (Cell 10 Negative).		Input

Pin Description (continued)

PIN	NAME	FUNCTION	REF SUPPLY	TYPE
50	C10	Voltage Input for Cell 10 Positive (Cell 11 Negative).		Input
51	SW10	Balance Input for Cell 10 Positive (Cell 11 Negative).		Input
52	C11	Voltage Input for Cell 11 Positive (Cell 12 Negative).		Input
53	SW11	Balance Input for Cell 11 Positive (Cell 12 Negative).		Input
54	C12	Voltage Input for Cell 12 Positive (Cell 13 Negative).		Input
55	SW12	Balance Input for Cell 12 Positive (Cell 13 Negative).		Input
56	C13	Voltage Input for Cell 13 Positive (Cell 14 Negative).		Input
57	SW13	Balance Input for Cell 13 Positive (Cell 14 Negative).		Input
58	C14	Voltage Input for Cell 14 Positive.		Input
59	SW14	Balance Input for Cell 14 Positive.		Input
60	V_{BLK}	Block Voltage Positive Input. Internal pulldown resistor of R_{VBLK}.	DCIN	Input
61	DCIN	DC Supply for the Low-Voltage Regulator, HV Charge Pump, and SHDNL Charge Pump. Connect to a voltage source between 9V and 65V through a 100Ω series resistor. Bypass with a 100V, 2.2µF capacitor to ground.		Power
62	CPN	Negative Capacitor Connection for the HV Charge Pump.		Power
63	CPP	Positive Capacitor Connection for the HV Charge Pump. Connect a 100V, 0.1µF capacitor from CPP to CPN.		Power
64	HV	Decoupling Capacitor Connection for the HV Charge Pump. Bypass with a 50V, 4.7µF capacitor to DCIN.		Power

Detailed Description

The data acquisition system consists of the major blocks shown in Figure 1 and described in Table 1.

Table 1. System Blocks

BLOCK	DESCRIPTION
ADC	Analog-to-digital converter. Uses a 12-bit successive-approximation register (SAR) with a reference voltage of 1.25V and supplied by V_{AA}.
HVMUX	14-channel, high-voltage (65V) differential multiplexer for the C0-C14 inputs.
HV CHARGE PUMP	High-voltage charge-pump supply for the HVMUX, ALTMUX, BALSW, and LSAMP circuits that must switch high-voltage signals. Supplied by DCIN.
LSAMP1	Level-shifting amplifier with a gain of 1/4. The result is that a 5V differential signal is attenuated to 1.25V, which is the reference voltage for the ADC.
LVMUX	Multiplexes various low-voltage signals, including the level-shifted signals and temperature signals to the ADC for subsequent analog-to-digital conversion.
ALTMUX	12-channel, high-voltage differential multiplexer for the SW0-SW14 inputs.
BALSW	Cell-balancing switches.
LINREG 1.8V	1.8V (V_{AA}) linear regulator used to power the ADC and digital logic. Supplied by DCIN.
LINREG 3.3V	3.3V ($V_{DDL2/3}$) linear regulator used to power UART transceiver and ALERT.
REF	1.25V precision reference voltage for ADC and LINREG. Temperature compensated.
ALTREF	1V precision reference voltage used for diagnostics.
HFOSC	High-frequency oscillator with 2% accuracy for clocking state machines and UART timing.
LFOSC	Low-frequency oscillator for driving charge pumps and timers.
LOWER PORT	Differential UART for communication with host or down-stack devices. Autodetects baud rates of 0.5Mbps, 1Mbps, or 2Mbps.
UPPER PORT	Differential UART for communication with up-stack devices.
CONTROL AND STATUS	ALUs, control logic, and data registers.
DIE TEMP	A proportional-to-absolute-temperature (PTAT) voltage source used to measure the die temperature.
COMPARATOR	A comparator path to detect OV/UV for cell voltage and AUXIN.
LSAMP2	Level-shifting amplifier with a gain of 1. The result is a 5V differential signal that is compared against programmable OV and UV DAC thresholds.
I2C MASTER	I^2C master interface for communication with a I^2C slave.

MAX17854 Functional Block Diagram

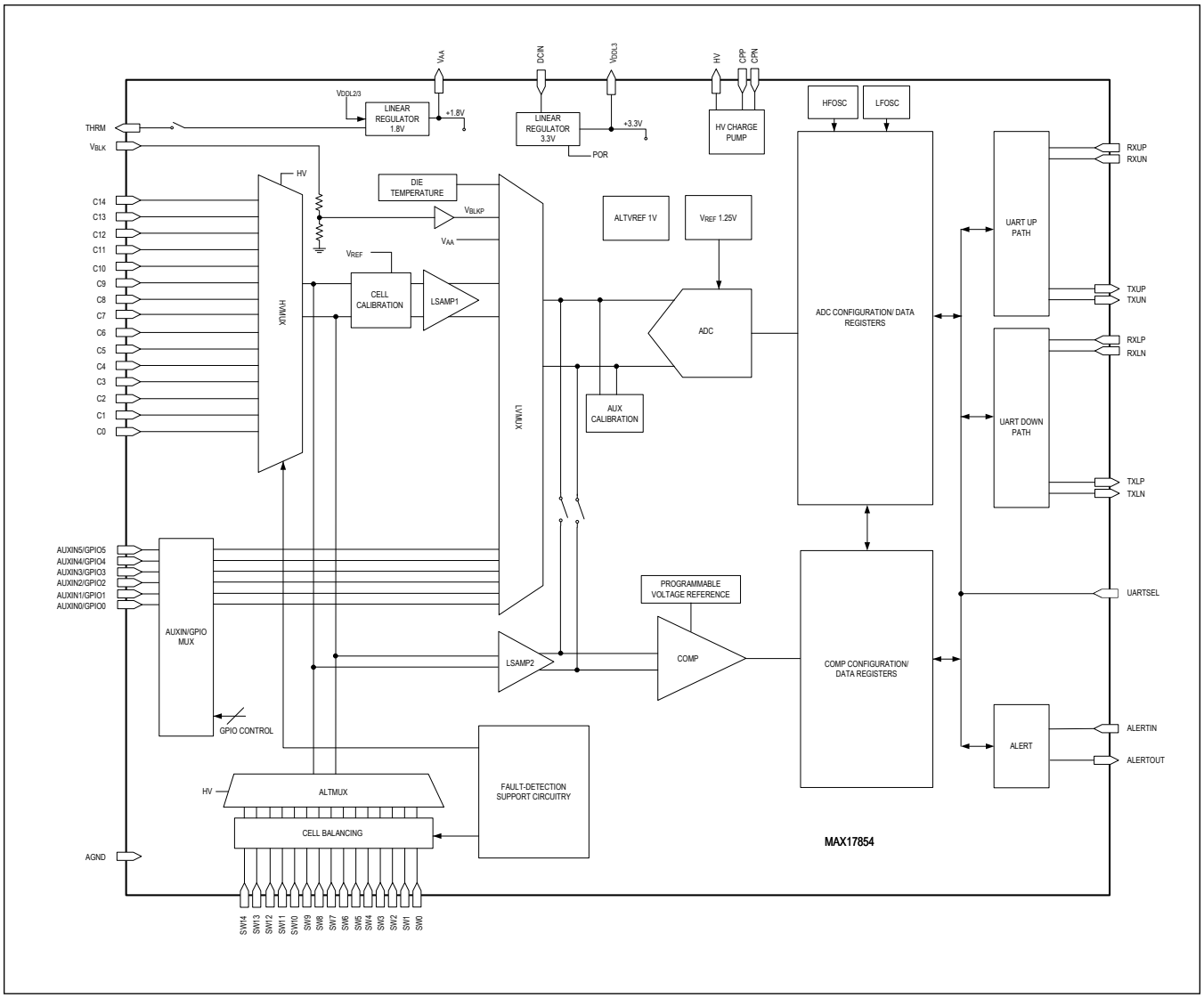


Figure 1. MAX17854 Functional Block Diagram

ESD Diodes Diagram

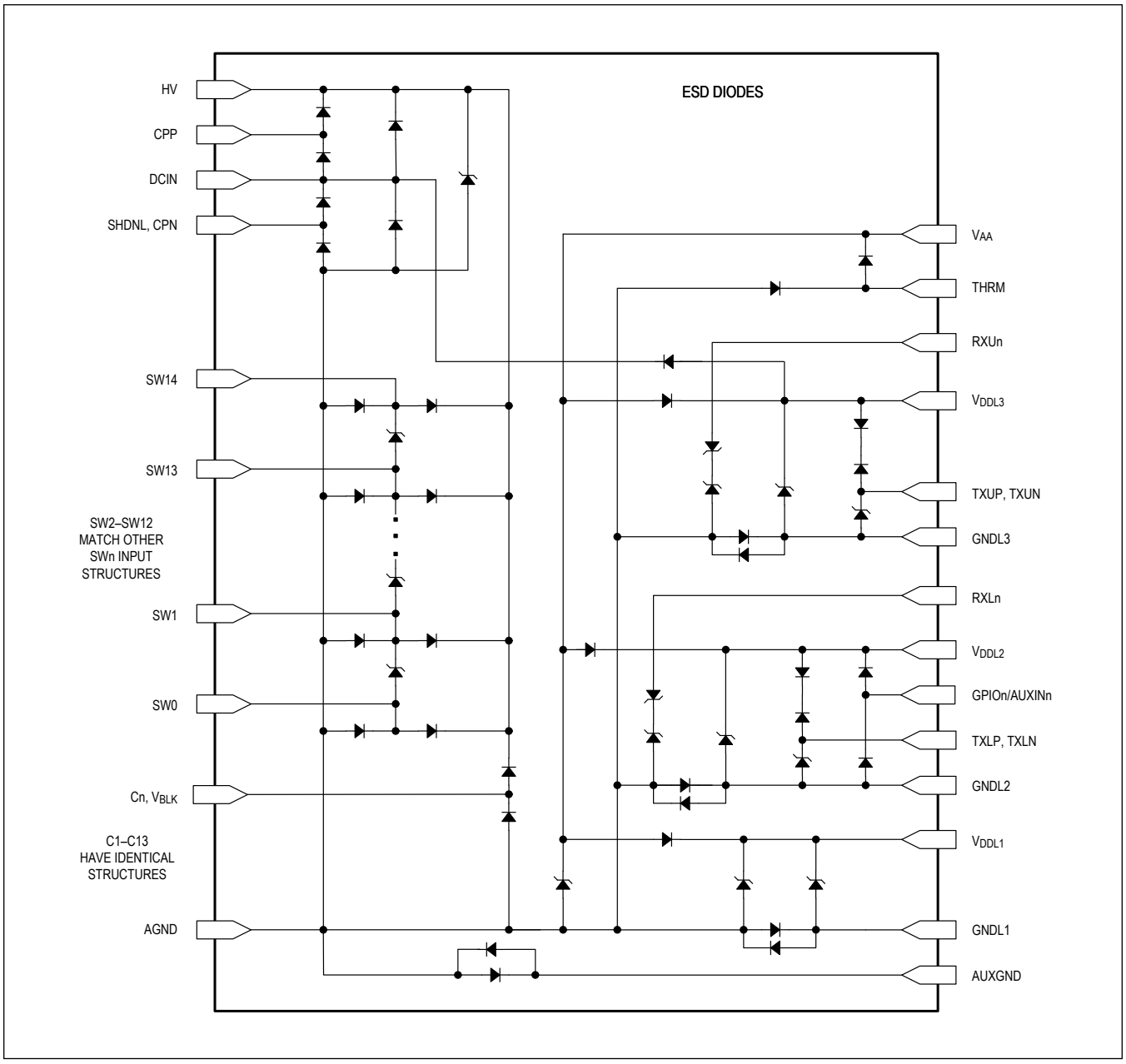


Figure 2. MAX17854 ESD Diagram

Notes:

1. All diodes are rated for ESD clamping conditions. They are not intended to accurately clamp DC voltage.
2. All diodes have a parasitic diode from AGND to their cathode that is omitted for clarity. These parasitic diodes have their anode at AGND.

MAX17854 Analog Front-End

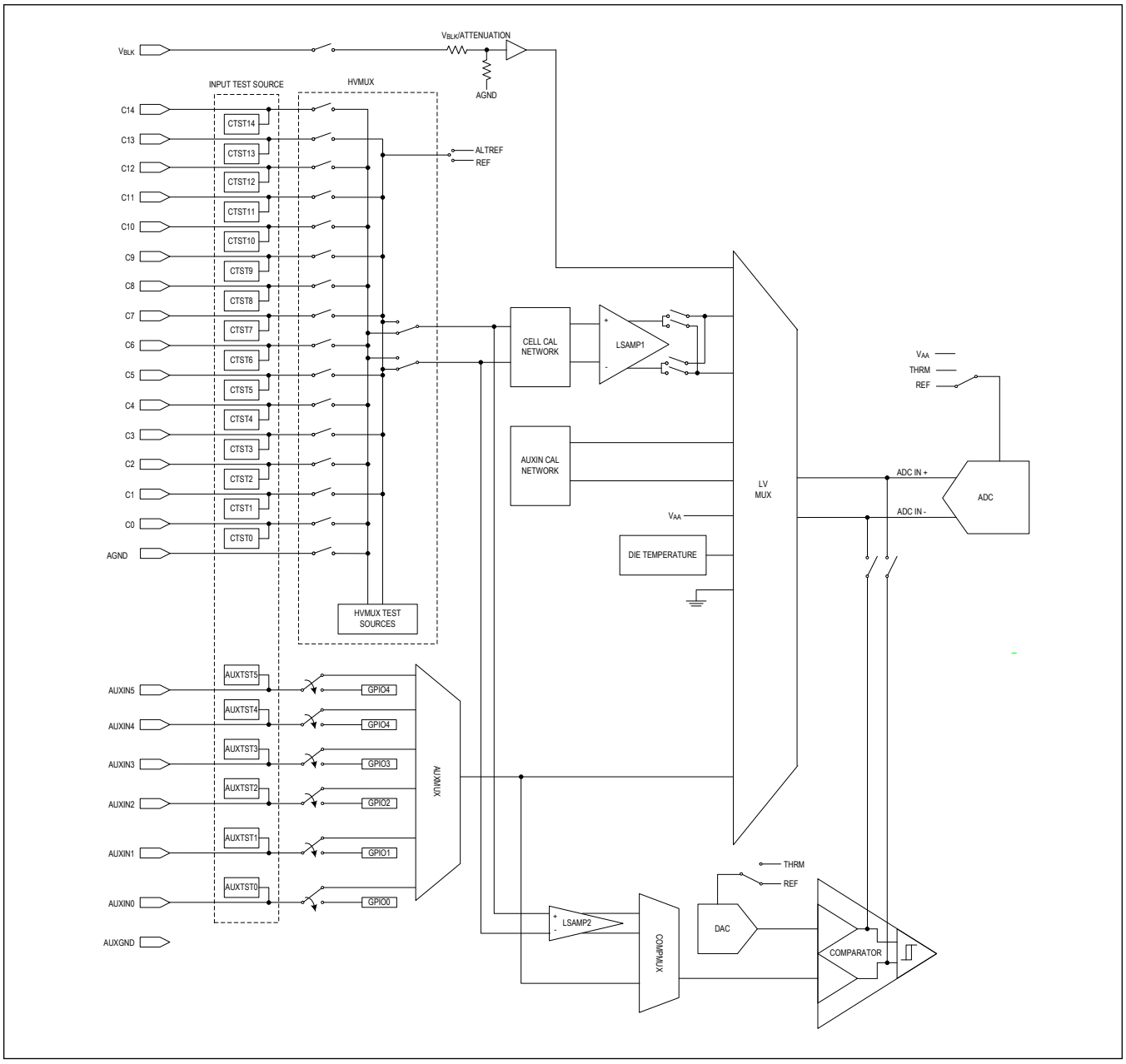


Figure 3. MAX17854 Analog Front-End

Terms, Definitions, and Data Conventions

Data Acquisition

A data acquisition is composed of the distinct processes defined in Table 2 and controlled by various configuration registers described in this section.

Configuration changes should be made prior to the acquisition in which the changes are to be effected.

Table 2. Data Acquisition Process

PROCESS	DESCRIPTION
Conversion	The ADC samples a single input channel, converts it into a binary value, and stores it in an ALU register.
Scan	The ADC sequentially performs conversions on all enabled cell-input channels.
Measurement Cycle or Sample	The ADC performs two scans for the purpose of minimizing cell error. The conversions within the scan (two for each input channel) are chopped and referred as measurement or sample.
Acquisition or Acquisition Mode	If oversampling is enabled, the ADC takes sequential measurements and averages them together to form a single value for each input channel sampled. If there is no oversampling, the acquisition is essentially a single measurement cycle.
Calibration	Factory calibration achieves the accuracy specification within the *Electrical Characteristics* table. No additional device calibration is required.

Data Conventions

Representation of data follows the conventions shown in Table 3. All registers are 16-bit words.

Table 3. Numeric Conventions

DESCRIPTION	CONVENTION	EXAMPLE
Binary number	0b prefix	0b01100001 = 61h
Hexadecimal address	0x prefix	0x61
Hexadecimal data	h suffix	61h
Decimal data	d suffix	61d
Register bitfield	Register name [x]	STATUS[15] = 1
Register field	Field name [x:y]	DA[4:0] = 0b01100 = 0Ch = 12d
Register field and bitfield	Register name:bitfield	ADDRESS:DA
Concatenated numbers	{xxxx, yyyy}	{DA[4:0], 0b001} = 61h

Factory Trimming

The acquisition system is trimmed at the factory. The trim parameters are stored in a ROM consisting of 11 read-only registers (OTP2-OTP12). ROMCRC is an 8-bit CRC value based on the calibration ROM and is stored in OTP12[15:8] at the factory. ROMCRC may be used to check the integrity of the trim as described in the *Diagnostics* section.

The factory trim can be further supplemented with a user on-demand calibration when used in a specific customer application.

An error correction code (ECC) is implemented to the OTP read. This provides additional robustness for the lifetime of product.

Factory-Programmed Device ID

The ID1 register together with ID2 provide a 32-bit manufacturing identification number, DEVID[31:0]. This ID will be unique among all devices with the same model type and version (VERSION:MOD,VER, respectively). Taken together, VERSION, ID1, and ID2 provide a means to uniquely identify all devices shipped by the factory. Although not required, the manufacturing date information provided on the package provides a further means of device tracking. A device ID of zero is invalid.

Introduction

The MAX17854 is a software-configured ASIL D data-acquisition system for both high-voltage and low-voltage 48V-rated applications, supporting a flexible configuration of cell-voltage measurements, pack-voltage measurements, temperature measurements, and auxiliary-voltage measurements. All measurements are synchronously sampled within an acquisition and have minimal delay between acquired samples. Additional programmability is available for balancing currents, and

system-interconnect measurements (bus bars) to provide a complete measurement solution independent of hardware configuration.

The following sections describe the device operation, feature set, and programming of the MAX17854.

Flexible Battery-Pack Configuration

The main supply voltage, DCIN, can be routed internally using the SW8-SW14 inputs of the highest stacked cell. This allows for a single hardware configuration to serve multiple battery modules without requiring external hardware or wiring-harness changes.

The flexible battery-pack configuration is enabled by default using FLXPCKEN1/2 bit, to allow for internal powering conditions. If this configuration is not required, the DCIN can still be driven externally, which will effectively disable the flexible battery-pack configuration. Prior to SDHNL being actively controlled, the DCIN voltage will be driven towards HV and clamped at the highest voltage applied at the SW8-SW14 inputs. When SHDNL is asserted, DCIN will be driven to within 1V below the highest stacked cell, if no external DCIN is provided. In this case, the host must define the TOPCELL1[3:0] and TOPCELL2[3:0] of the stack by writing to the PACKCFG register and by asserting the FLXPCKEN1 and FLXPCKEN2 bits. TOPCELL_[3:0] selection configures the top-cell position if less than 14 channels are used. TOPCELL_[3:0] selections 0x0 to 0x7 and 0xF are not supported and will be mapped to an OFF position (power-on default).

If FLXPCKEN1/2 is unintentionally deasserted while the SHDNL is driven high with no external DCIN connection, it is expected that the voltage seen at the DCIN pin will fall at a rate proportional to the current consumption of the part and the external decoupling capacitance until the POR threshold is reached. This resets the digital logic and returns the FLXPCKEN to the desired power-on reset state.

If FLEXPCKEN1 and FLEXPCKEN2 or TOPCELL1 and TOPCELL2 are not the same, the power-on default values will be applied.

Note: It is important that TOPCELL1 and TOPCELL2 selects the highest applied cell input, as an invalid configuration can create an internal path which would connect the highest battery voltage to the selected TOPCELL1/2 input.

A second mux internally connects V_{BLK} to a selected cell input after host defines the TOPCELL_[3:0] of the stack and asserts the FLXPCKEN_ bit. TOPBLOCK[3:0] selects the Cn pin to be connected to the V_{BLOCK} resistive divider. 0xF (default) selects the V_{BLK} pin. TOPBLOCK_ selections 0x0 through 0x7 are not supported and will be mapped to 0xF (V_{BLK}, default).

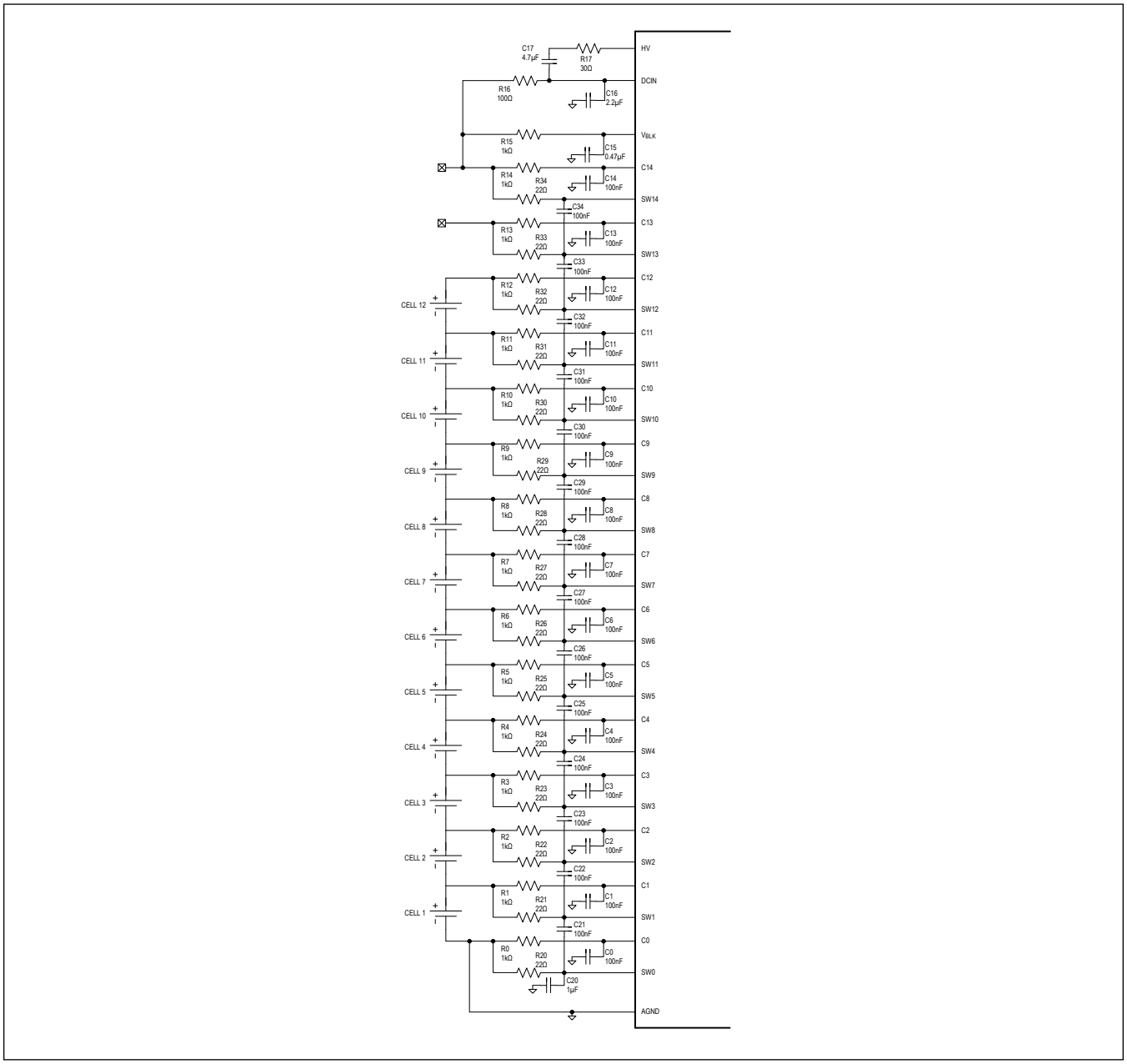


Figure 4. Flexible-Pack Configuration for 12-Cell Pack on 14-Channel CMC

Flexible-Pack Interaction with Acquisitions

If FLXPCKEN1/2 and FLXPCKSCAN are asserted, the switch input denoted in the TOPCELL1 and TOPCELL2 bitfields is disconnected from DCIN and the internal power consumption will be supplied by the external decoupling/hold-up capacitance on the DCIN pin. A 30µs delay will be inserted prior to the TOPCELL conversion, allowing the external switch filter network to settle before converting the input voltage.

Note: FLXPCKSCAN only affects ALTMUX acquisitions. If the ALTMUX accuracy is not required for the application, no

changes are required to the application circuit regardless of the FLXPCKSCAN setting. It is however, recommended to set FLXPCKSCAN = 0 to ensure the quickest sampling rate is achieved.

Power-Multiplexing Operation (Cell Balancing)

The top two balancing switches should not be configured simultaneously while in manual cell balancing mode when the internal power multiplexing is configured. This configuration creates a voltage drop in the DCIN supply equivalent to a cell voltage which can result in large measurement errors of the top-cell reading with both the HVMUX and ALTMUX configured.

TOPCELL_[3:0] and FLXPCKEN_ must refer to the top cell in the pack, and not a bus bar, if the top-used channel in the pack is a bus bar. TOPBLOCK_ can refer to cells above TOPCELL_.

Flexible-Pack Alert

An ALRTDCINMUX is triggered to indicate a fault in the DCINMUX switch. A high condition indicates the enabled DCINMUX is not functioning properly in a flexible-pack application. Performance may be impacted, and/or other related faults may be issued. The ALRTDCINMUX is gated until clear of ALRTRST after power-up has occurred.

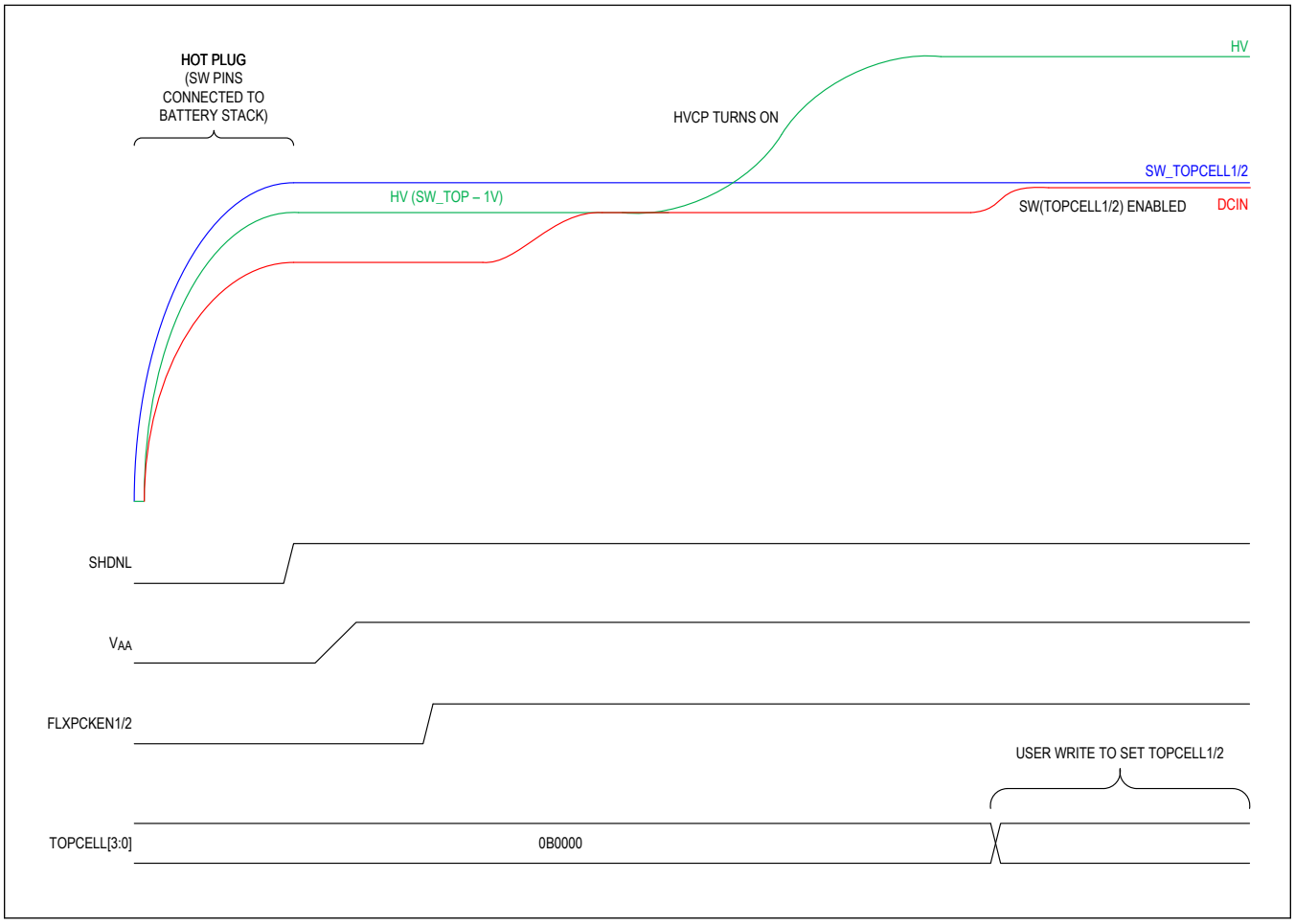


Figure 5. Flexible-Pack Power-On Timing

Cell Inputs

Up to 14 voltage measurements can be sampled differentially from the 15 cell inputs. The differential signal V_{CELLn} is defined as $V_{Cn} – V_{Cn-1}$ for n = 1 to 14.

The cell inputs are selected by the corresponding CELLEN bits in the MEASUREEN1 register. Additionally, the input path for the measurement acquisition is selected using SCANCTRL:ALTMUXSEL. The ALTMUXSEL bit allows for two different measurement configurations: HVMUX and ALTMUX acquisitions. The HVMUX path selection is used for the primary measurement acquisition due to the higher filtering achieved by the external input network. Alternatively, the ALTMUX path selection is primarily used for cell balancing and typically does not have a large RC filter. Due to the parallelism of the external filter network, as well as the internal block structures, the ALTMUX path selection also allows for independent measurement redundancy improving safety performance and device robustness.

During the scan, the selected signal is multiplexed into the level-shifting amplifier (LSAMP1 or LSAMP2) as shown in Figure 6. Since the common-mode range of the input signals is 0 to 65V, the signal must be level-shifted to the common-mode range of the amplifier. Both ADC and comparator signal paths have a gain of 1/4 so that a 5V differential signal is attenuated to the ADC and comparator full scale reference voltage (V_{REF}).

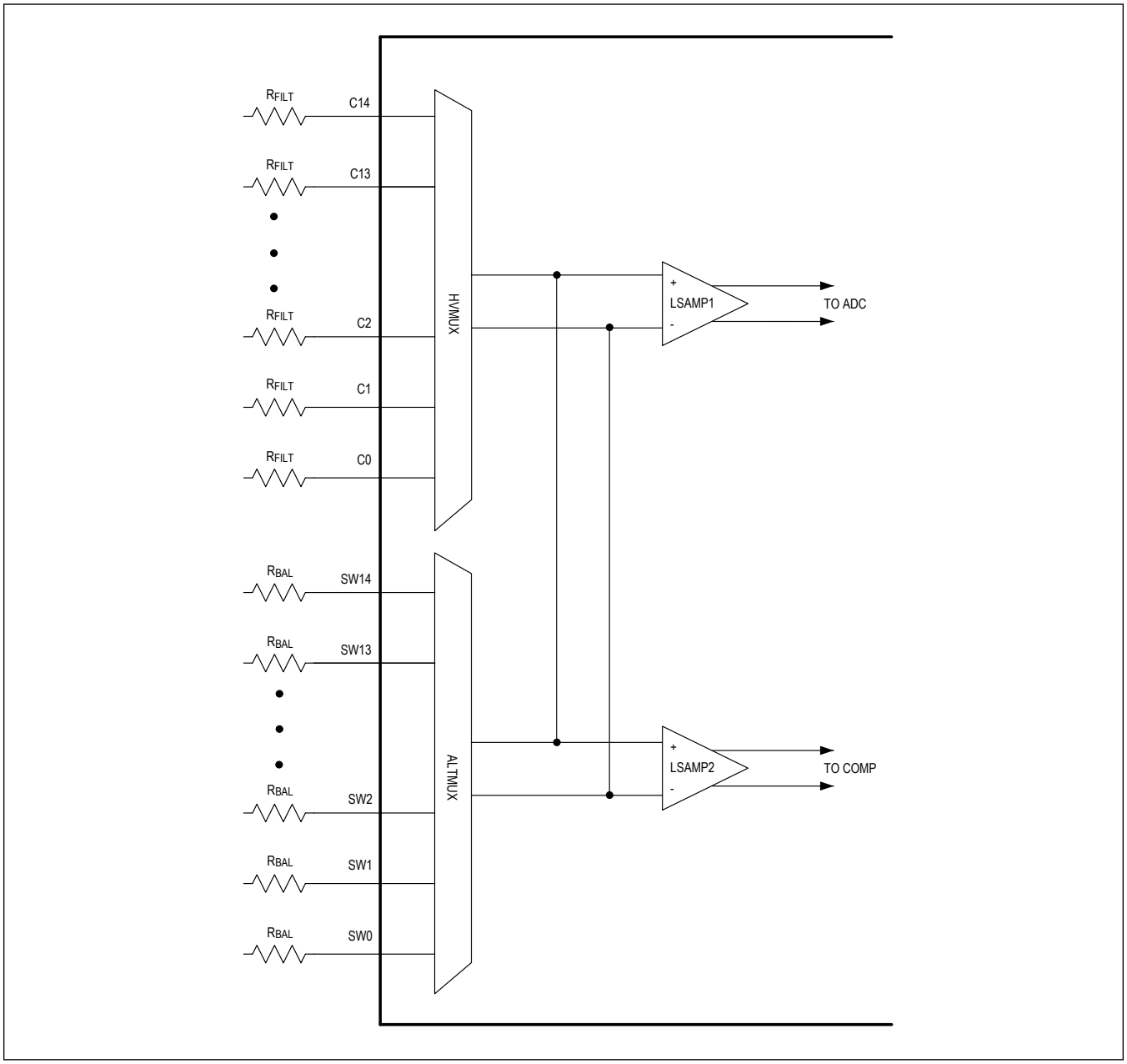


Figure 6. Cell Signal Path

Once the signal is properly conditioned, the ADC starts the conversion. The 12-bit conversion is stored in an ALU register where it can be averaged with subsequent conversions for increased resolution. The ALU output is a 14-bit value, relating to a 305µV voltage resolution, and is ultimately stored in a 16-bit register, CELLnREG, with the two least-significant bits 0. Disabled channels maintain their previous measurement result. Unless stated otherwise, measurement values are assumed to be 14-bit values. The 16-bit register values can be converted to 14-bit values by dividing by 4 (and vice-versa). To convert the measurement value in register CELLnREG to a voltage, convert the 14-bit hexadecimal value to a decimal value and then convert to voltage as follows:

V_{CELLn} = CELLnREG[15:2] x 5V/16384 = CELLnREG[15:2] x 305.176µV

Bus-Bar Inputs

Bus-bar inputs can be applied to any of the 14 cell inputs. Due to the resistive nature of the bus bar, the current applied to the battery pack or discharged from the battery pack will affect the polarity of the voltage measurement. To support this requirement, the POLARITY bits corresponding to the bus-bar location must be configured for bipolar conversion (POLARITY[n] = 1b).

Due to the negative voltage that can be generated across the bus bars SW_n to SW_{n-1} inputs, it is recommended to place an external Schottky diode across the inputs to the reverse voltage seen by the body diode of the internal balancing switch as shown in Figure 7 to shunt current away from the internal conduction path. See the *Bus-Bar Design* section for more details.

Block Voltage Input

The V_{BLK} input pin to the MAX17854 allows for the pack voltage (total cell voltage) to be measured independently of summing the individual cell voltages from an acquisition. This comparison provides an extra layer of measurement redundancy within the system.

The V_{BLK} voltage is attenuated by a voltage-divider of 52 for the acquisition process to translate the 65V full-scale block input voltage into the full-scale ADC input voltage (V_{REF})

Outside of the acquisition, the V_{BLK} input path is opened to avoid power consumption from the internal resistor-divider.

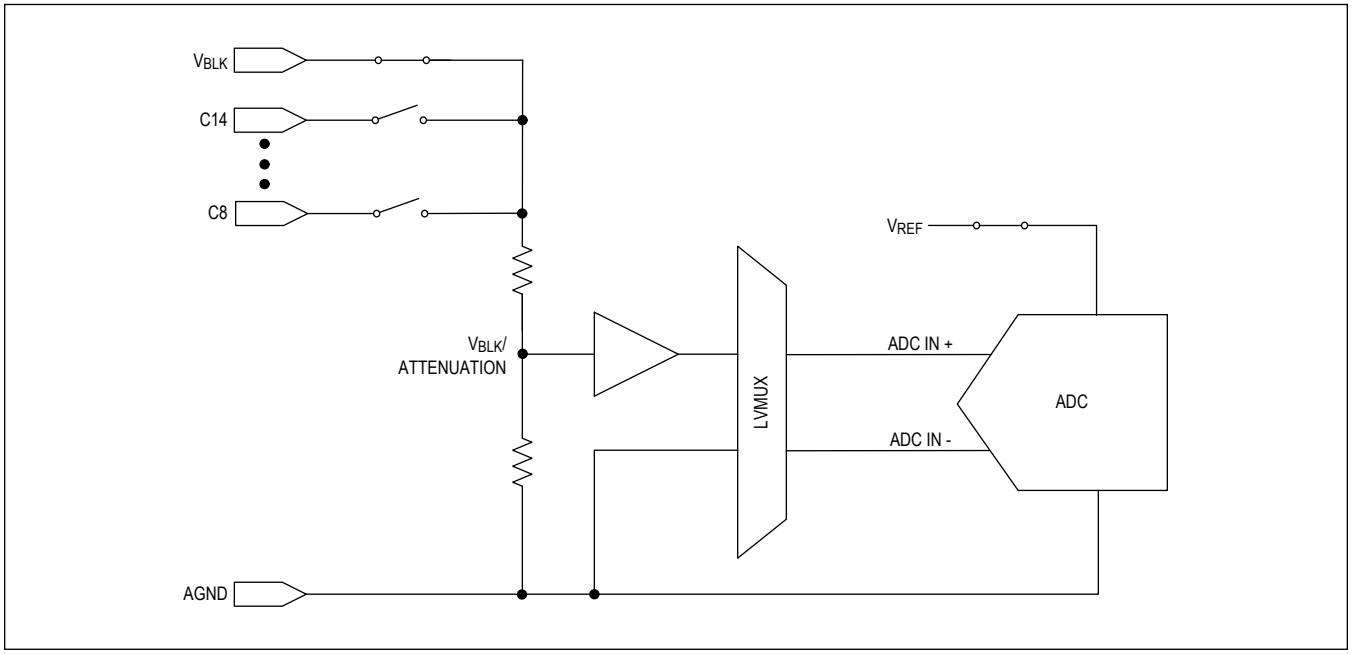


Figure 7. Block Measurement Path

The measurement is enabled in a an acquisition by asserting BLOCKEN in MEASUREEN1 register. The measurement is stored in the VBLOCK[13:0] bits of the BLOCKREG register where each bit has a resolution of 3.967mV.

Auxiliary Inputs

The MAX17854 has 6 auxiliary ports that can be used to measure external temperatures, measure external voltages, or that can be repurposed for digital functions (GPIO or I^2C master).

Auxiliary Inputs: Ratiometric Temperature Measurement

Individual auxiliary ports can be configured to measure external temperatures through enabling auxiliary measurements using the AUXEN bits in the MEASUREEN2 register as well as configuring the conversion voltage as ratiometric using the AUXREFSEL bits in the AUXREFCTRL register.

Note: If the individual auxiliary port is configured as a GPIO using GPIOEN bits in the AUXGPIOCFG register while the corresponding AUXEN bit is high, then the auxiliary setting will be ignored and the port will be configured as a GPIO.

The ratio-metric configuration selects the conversion voltage of both the ADC and comparator to V_{AA}, while also outputting V_{AA} on the THRM pin. An external resistive divider can then be created with a pullup resistor to the THRM pin and a NTC connected to the AUXGND pin, as shown in Figure 8:

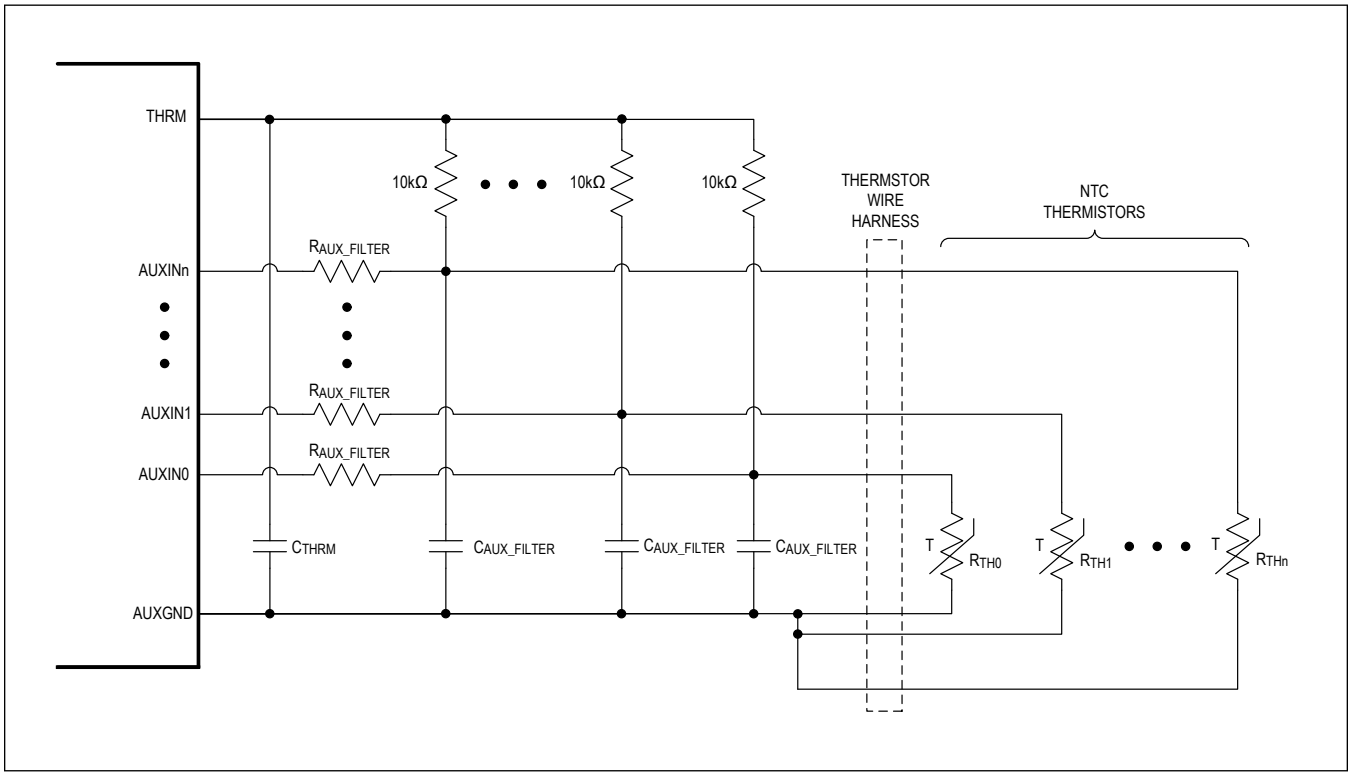


Figure 8. Auxiliary Application Circuit

Explicit control on the THRM pin output is provided using the THRMMODE bits in the ACQCFG register. Setting THRMMODE to 00b or 01b enables automatic mode where the THRM switch will be closed at the beginning of an acquisition. Setting THRMMODE to 11b enables manual mode where the THRM switch is always closed. The ability to configure THRMMODE allows for the application tradeoffs between the external NTC network's power consumption on V_{AA} and the need to settle the external NTC network to achieve the highest accuracy measurements.

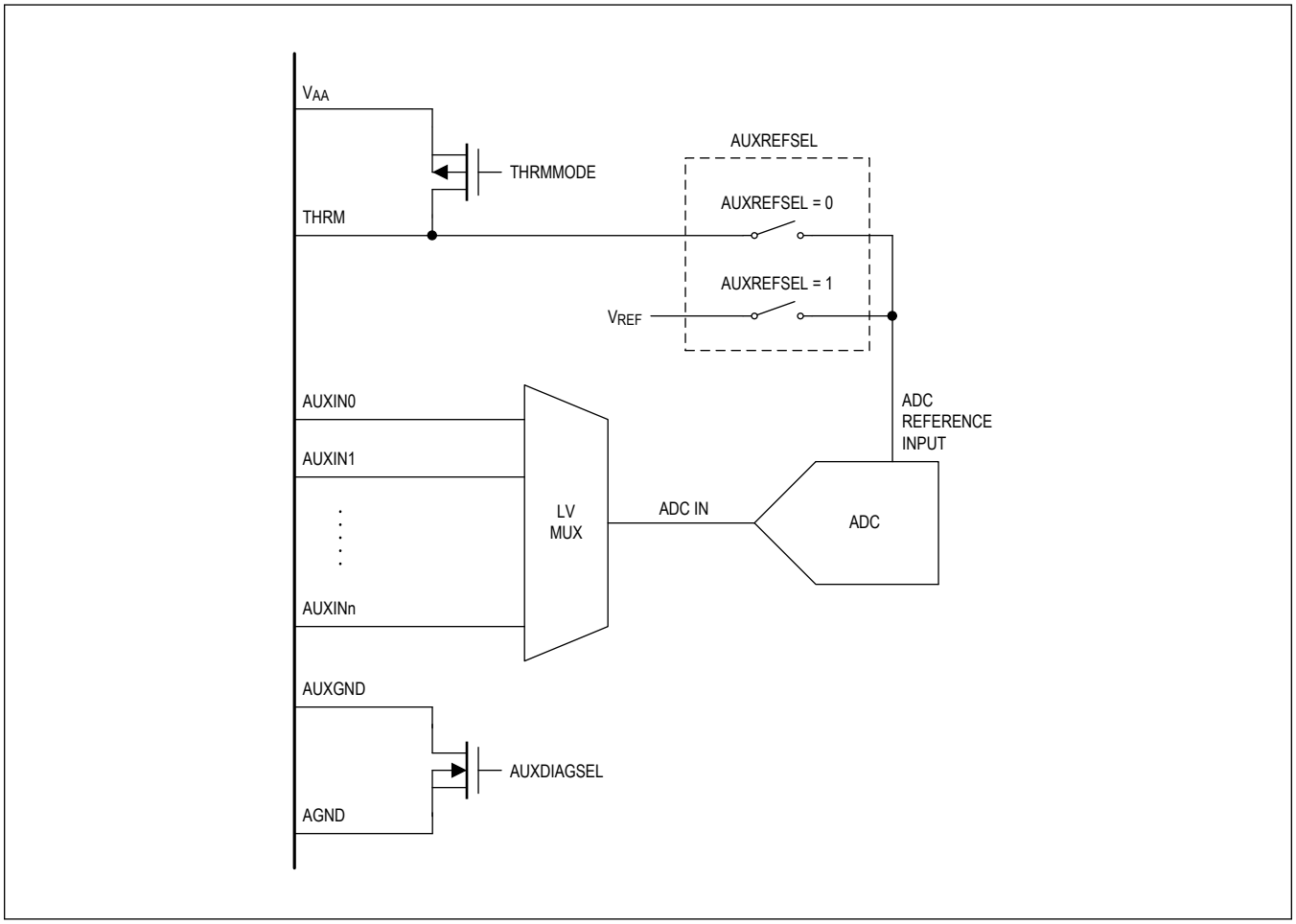


Figure 9. Auxiliary Temperature Measurements

Table 4. THRM Output

MODE	THRMMODE	DESCRIPTION
Automatic	00b	THRM outputs V_{AA} (dynamically enabled at the beginning of the acquisition and disabled at the end of the acquisition)
	01b	
Manual	10b	THRM output disabled (static)
	11b	THRM outputs V_{AA} (static)

Depending on the external temperature network, there may be insufficient settling time to provide accurate measurements. To support the flexibility for different networks, the AUXTIME bits in the AUXTIMEREG register may be configured to impose a fixed delay of 0ms to 6.14ms prior to the first AUXINn measurement. For an acquisition with nondeterministic scan rates, the AUXTIME is allowed to settle through the cell, block, and diagnostic measurement intervals of the first scan. However, for acquisitions requiring deterministic timing, such as 50Hz/100Hz rejection and 60Hz/120Hz rejection, the AUXTIME is applied prior to the beginning of the acquisition. See the *Oversampling* section for further details on FOSR and deterministic acquisitions.

Table 5. AUXTIME

AUXTIME[9:0]	ADDITIONAL SETTLING TIME PER ENABLED AUXILIARY CHANNEL = (AUXTIME x 6µs)
0x000	0µs
0x001	6µs
0x002	12µs
…	…
0x3FF	6138µs

The auxiliary measurements are oversampled to 14-bit values using the OVSAMPL bits in the SCANCTRL register and the output of each auxiliary measurement is stored in the corresponding AUX0-AUX6 registers. See the *Oversampling*, *ADC Acquisition*, *Comparator Acquisition*, and *ADC+COMP Acquisition Time* sections for further details.

Ratiometric Auxiliary Input Range

Temperature measurement are converted ratiometrically to eliminate error due to the biasing of the NTC network. Thus, the conversion range is proportional to the V_{THRM} (V_{AA}) reference as shown in the following tables.

Both ADC and comparator conversions use the same reference during the conversion and thus have the same input range. However, the resolution for both will differ in accordance with the following tables:

Table 6. Auxiliary Temperature Input Range: ADC

AUXILIARY INPUT VOLTAGE	AUXn (14 BITS)		AUXnREG[15:0] (16 BITS)
RATIOMETRIC MODE	HEXADECIMAL	DECIMAL	
0V	0000h	0d	0000h
$V_{AA}/2$	2000h	8192d	8000h
V_{AA}	3FFFh	16383d	FFFCh

Table 7. Auxiliary Temperature Input Range: Comparator

AUXILIARY INPUT VOLTAGE	COMPOVTH, COMPUVTH, COMPAUXROVTH, COMPAUXRUVTH COMPAUXAOTH, COMPAUXAUVTH (10 BITS)		COMPOVTHREG[15:0], COMPUVTHREG[15:0] COMPAUXROVTHREG[15:0], COMPAUXRUVTHREG[15:0] COMPAUXAOTHREG[15:0], OMPAUXAUVTHREG[15:0] (16 BITS)
RATIOMETRIC MODE	HEXDECIMAL	DECIMAL	
0V	000h	0d	0000h
$V_{AA}/2$	800h	2048d	7FF8h
V_{AA}	1000h	4096d	FFF0h

Computing Temperature

As shown in Figure 8:

$$V_{AUXINn} = V_{THRM} \times \frac{R_{TH}}{10k\Omega + R_{TH}}$$

This measurement is stored in the AUXn register. The thermistor resistance can then be solved for as follows:

$$R_{TH} = \frac{V_{AUXINn} \times 10k\Omega}{V_{THRM} - V_{AUXINn}}$$

where V_{THRM} = 1.8V, nom.

Since this is a true ratiometric measurement (ADC reference = V_{THRM}) the following approach can be taken:

$$\frac{V_{AUXINn}}{V_{THRM}} = \frac{AUXn(14BITS)}{16384} = \frac{R_{TH}}{10k\Omega + R_{TH}}$$

By solving it to R_{TH}, we get:

$$R_{TH} = \frac{10k\Omega}{\frac{16384}{AUXn(14BITS)} - 1}$$

The resistance of an NTC thermistor increases as the temperature decreases, and it is typically specified by its resistance R_0 = 10kΩ at T_0 = +25°C = 298.15K and a material constant β (3400K, typ). To the first order, the resistance R_{TH} at a temperature T (in Kelvin) may be computed as follows:

$$R_{TH} = R_0 \times e^{\left(\beta \times \left(\frac{1}{T} - \frac{1}{T_0}\right)\right)}$$

The temperature T of the thermistor (in °C) can then be calculated as follows:

$$T(\text{in}^\circ C) = \frac{\beta}{\ln\left(\frac{R_{TH}}{10k\Omega}\right) + \frac{\beta}{298.15K}} - 273.15K$$

Auxiliary Inputs: Absolute Voltage Measurements

Individual auxiliary ports can be configured to measure absolute voltages through enabling auxiliary measurements using the AUXEN bits in the MEASUREEN2 register, as well as through configuring the conversion voltage as absolute using the AUXREFSEL bits in the AUXREFCTRL register.

The absolute configuration selects the conversion voltage of both the ADC and comparator to V_{REF}. An external voltage may be accurately measured as long as the voltage remains below V_{REF}. If higher voltages are required to be measured, a resistive divider must be used to ensure that the maximum auxiliary input does not exceed V_{REF} otherwise the voltage measurement will saturate to full scale. Additionally the user should take precautions that, in the case of a single point failure on the external network, the maximum auxiliary input does not exceed the absolute maximum rating on the port.

If all AUXREFSEL bits are set to 0b1 (using V_{REF} for the ADC reference), it is recommended that THRMMODE be set to 0b10 (THRM switch always OFF).

Absolute Auxiliary Input Range

Absolute voltage measurement are converted using a fixed precision reference, V_{REF}. All voltages must meet the input range requirements. Otherwise, the digital output will saturate resulting in a loss of resolution. Both ADC and comparator conversions use the the same reference during the conversion but have different resolutions as shown in the following tables:

Table 8. Auxiliary Voltage Input Range: ADC

AUXILIARY INPUT VOLTAGE	AUXn (14 BITS)		AUXnREG[15:0] (16 BITS)
ABSOLUTE MODE	HEXDECIMAL	DECIMAL	
0V	0000h	0d	0000h
V_{REF}/2	2000h	8192d	8000h
V_{REF}	3FFFh	16383d	FFFCh

Table 9. Auxiliary Voltage Input Range: Comparator

AUXILIARY INPUT VOLTAGE	COMPOVTH, COMPUVTH, COMPAUXROVTH, COMPAUXRUVTH COMPAUXAOTH, COMPAUXAUVTH (10 BITS)		COMPOVTHREG[15:0], COMPUVTHREG[15:0] COMPAUXROVTHREG[15:0], COMPAUXRUVTHREG[15:0] COMPAUXAOTHREG[15:0], COMPAUXAUVTHREG[15:0] (16 BITS)
ABSOLUTE MODE	HEXADECIMAL	DECIMAL	

Table 9. Auxiliary Voltage Input Range: Comparator (continued)

0V	000h	0d	0000h
$V_{REF}/2$	200h	512d	8000h
V_{REF}	3FFh	1024d	FFC0h

Auxiliary Inputs: Mixed-Mode Measurements

Ratiometric measurements and absolute voltage measurements can both be performed during the same acquisition. Each measurement type will have individual OV/UV alerts threshold settings as described in the *Measurement Alerts* section.

Note: Auxiliary mixed-mode measurement data for the ADC is output to the AUXn registers. The appropriate conversion as determined by the AUXREFSEL configuration must be applied to obtain correct voltage reading.

Ratiometric Voltage Conversion:

V_{AUXn} = AUXn[14:0] x V_{AA}/16384d = AUXn[14:0] x 109.86µV, or alternatively AUXnREG[15:2] x 109.86µV

where V_{AA} is nominally 1.8V.

Absolute Voltage Conversion:

V_{AUXn} = AUXn[14:0] x V_{REF}/16384d = AUXn[14:0] x 76.29µV, or alternatively AUXnREG[15:2] x 76.29µV

Auxiliary Input Protection

The voltage on the AUXIN0 to AUXIN6 pins should never exceed V_{AA} when configured as an auxiliary input. If this condition does occur, the affected input will self-protect, becoming an open circuit. The associated ALRTAUXPRTCT bit will be set, indicating the overvoltage condition. To retry AUX operation and clear the fault condition, the user must rewrite the desired configuration to the AUXGPIOCFG register.

All 6 ALRTAUXPRTCT bits will be logically OR'd together to form the ALRTAUXPRTCTSUM bit in the FMEA2 register.

GPIO Configuration

Any of the 6 auxiliary ports may be configured as a general-purpose input/output (GPIO) using the GPIOEN bits in the AUXGPIOCFG register. When a GPIOEN bit is high, the corresponding auxiliary port is configured as a GPIO regardless of the AUXEN configuration. When a GPIOEN bit is low, the corresponding GPIO portion is tristated.

Additionally, the AUXIN[1:0] pins can be configured as an I^2C master interface using the I2CEN bit in the AUXGPIOCFG register. When the I2CEN bit is high, AUXIN0 operates as the SDA pin and AUXIN1 operates as the SCL pin. By default, I2CEN is low and the I^2C master is disabled.

Table 10. GPIO/I^2C/Auxiliary Enable Priority

I2CEN	GPIOEN	FUNCTION
0	0	Auxiliary Input
0	1	GPIO
1	x	AUXIN0 = SDA AUXIN1 = SCL

In the GPIO configuration, the I/O status is determined by the GPIODIR bits of the AUXGPIOCFG register. When a GPIODIR bit is programmed to 0b0, the corresponding port is configured as a digital input. The digital input has a 2MΩ pulldown resistance to ensure the input does not float and cause excessive power dissipation. When the GPIODIR bit is programmed to 0b1, the pin is configured as a digital output. Each GPIO port that is configured as a digital output can be configured to drive a logic-high level or logic-low level determined by the assignment in the GPIODRV bits of the GPIOCFG.

If I^2C functionality is enabled, the AUX0 and AUX1 registers will read 0x0000, and the GPIODIR[1:0], GPIOEN[1:0], GPIODRV[1:0] bits will be ignored for functionality but will still read back the user setting.

The GPIORD bits in the GPIOCFG register monitor the pin logic level regardless of whether the port is defined as an input or an output. If a pin is configured as an auxiliary input, the corresponding GPIORD bit will read back 0b0. If the I^2C

functionality is enabled, GPIORD[1:0] reads back 0b00.

Table 11. GPIO Configuration

GPIOEN	GPIODIR	FUNCTION
0	x	Auxiliary input
1	0	Digital input
1	1	Digital output

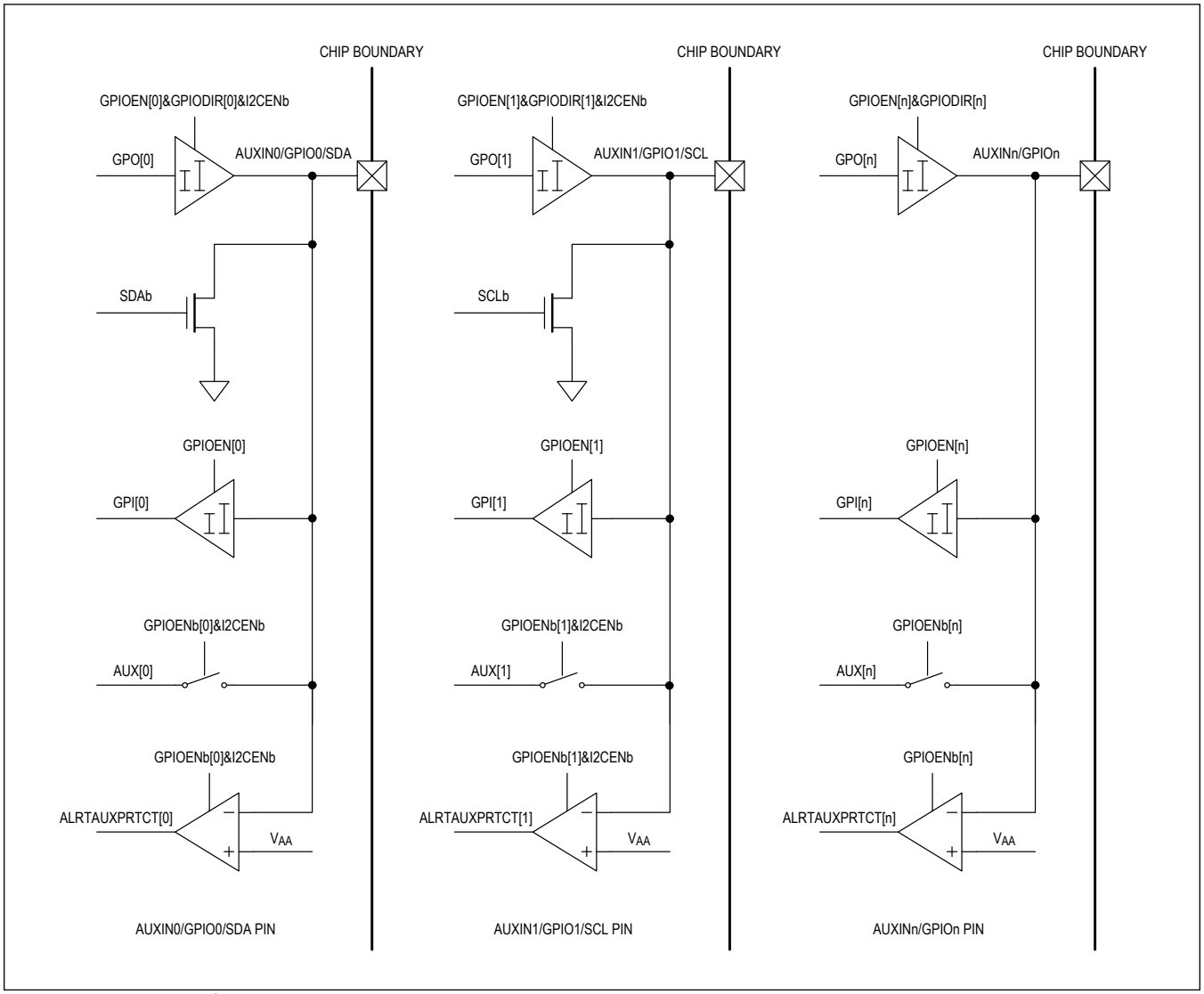


Figure 10. AUX/GPIO/I2C Pin Connections

Operational Modes

There are three different operational modes supported: shutdown mode, standby mode, and acquisition mode. Shutdown mode is controlled by the voltage on the SHDNL pin. When the voltage is below V_{IL_SHDNL}, the device is in an ultra-low-power shutdown mode and the various elements of the internal circuitry are disabled. If the voltage is above V_{IH_SHDNL},

the device is in standby mode and will act upon qualified interface commands. The device will remain in standby mode until the user commands an acquisition, at which point the device transitions into acquisition mode until completed, as signaled by SCANDONE. Alternatively, the transition from sleep mode to acquisition mode is handled independent of user interaction only when long-term autonomous cell balancing with voltage measurements are enabled (see the *Cell Balancing* section for further information).

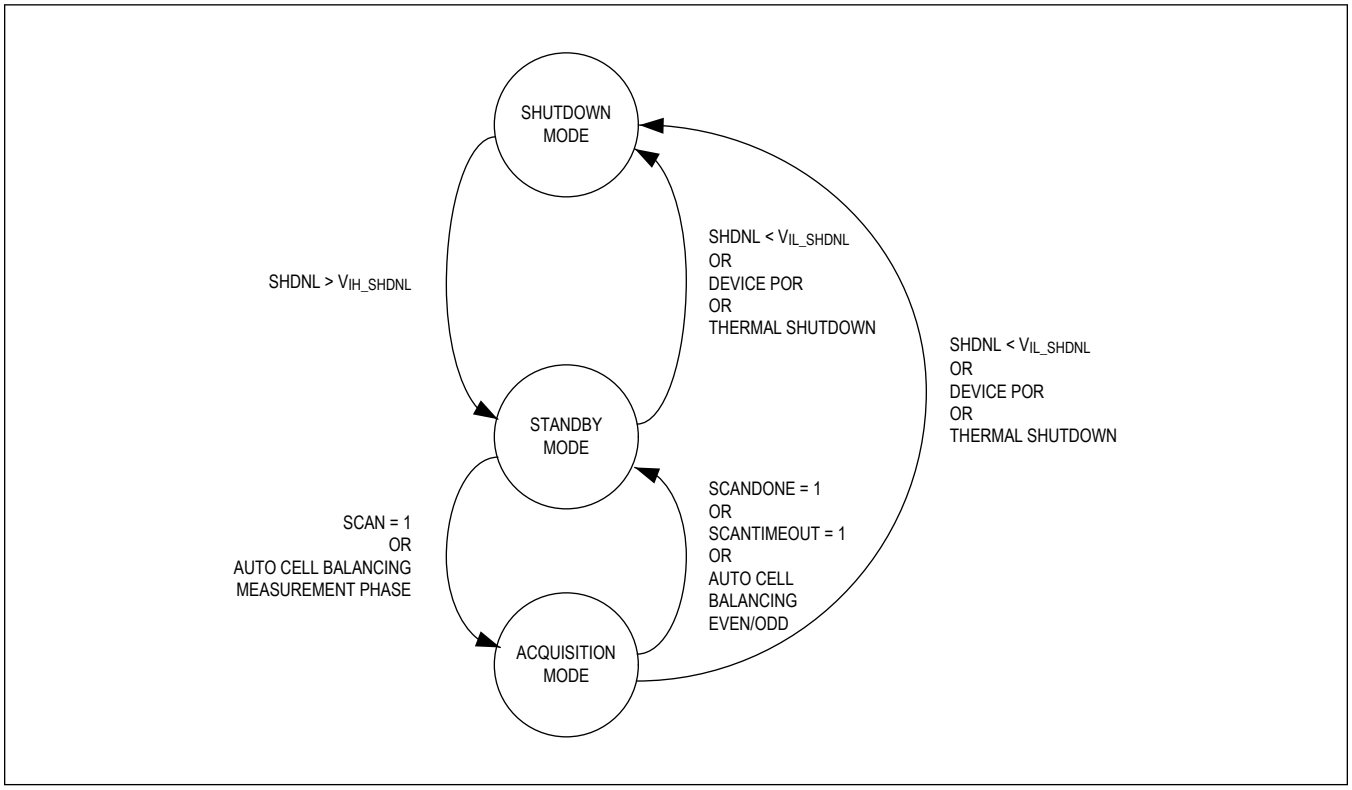


Figure 11. Operational Mode State Diagram

The following sections further detail the operational modes and device interactions.

Power-On (Standby Mode)

The SHNDL pin is driven using internal charge pumps on the UART RXLP/RXLN and RXUP/RXUN inputs. The device relies on the UART interface to drive the external network on the SHDNL pin. The the recommended external network of a single C_{SHDNL} capacitor connected between the SHDNL and AGND pins, the SHDNL voltage will transition above V_{IH_SHDNL} in ~200µs. The charge pump self-regulates to $V_{SHDNLIMIT}$ and can maintain V_{SHDNL} at a logic 1 even with the UART idle 98% of the time. The internal charge pump operation requires a differential signal UART signal.

Note: When configured as a single-ended UART interface, the SHDNL pin must be driven by an external pullup above the V_{IH_SHDNL} threshold.

Once the V_{IH_SHDNL} threshold is reached, the LDO output is enabled and V_{AA} output voltage will begin to rise. At 3V (typ), the $\overline{POR}$ signal is deasserted, the oscillators are enabled, the HV charge pump and digital logic are enabled, and the ALRTRST status bit is set. The device is fully operational (standby mode) within 1ms from the time communication is first received in shutdown mode. Figure 12 details the power-on state transition.

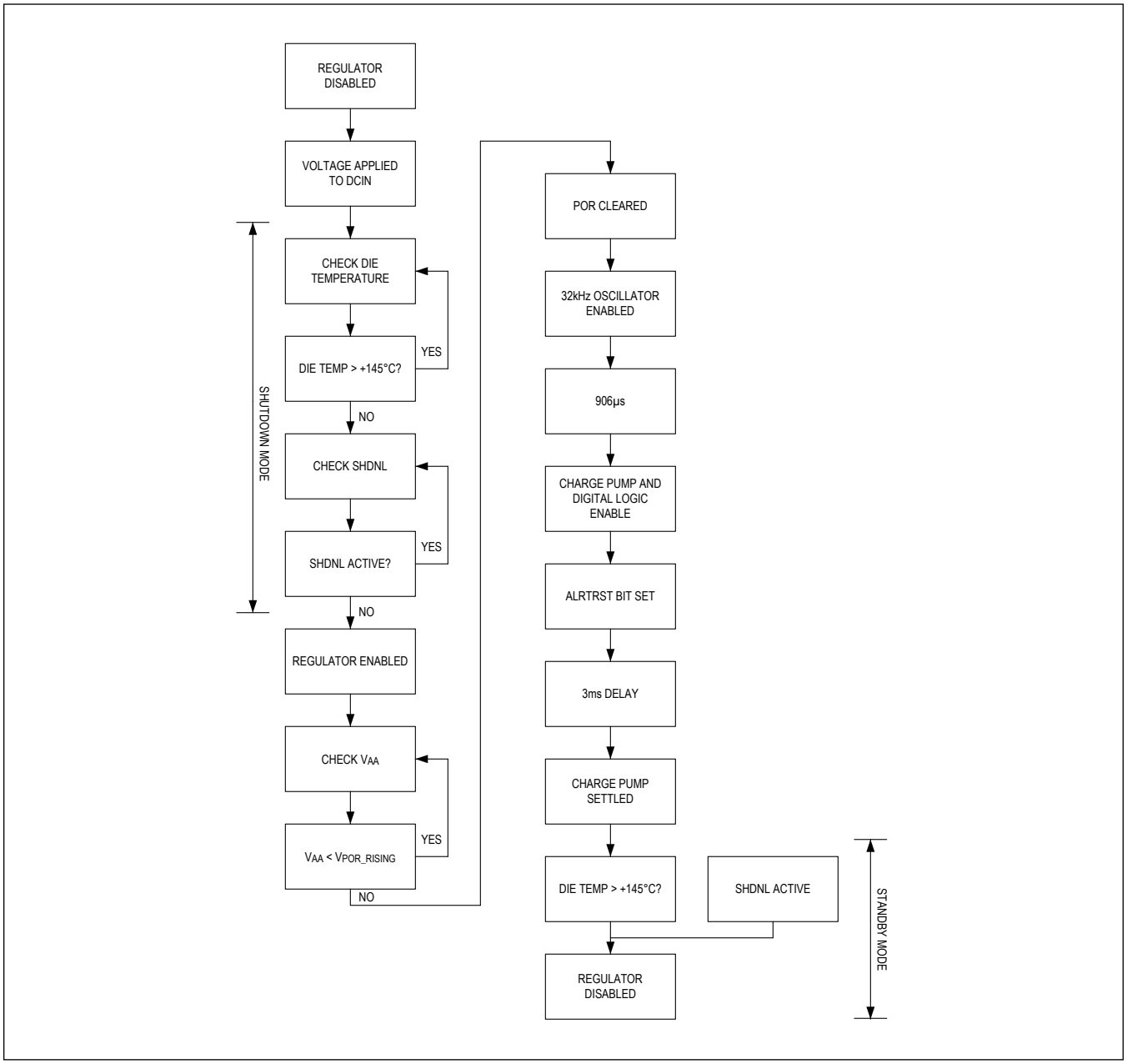


Figure 12. Power-On Sequence

Shutdown Mode

Shutdown mode is entered when SHDNL < V_{IL_SHNDL}. In shutdown, the low-voltage regulator and HV charge pump are disabled as soon as the SHDNL pin goes low. When the V_{AA} voltage discharges below the $V_{1.8REG\_PORRISE}$ threshold, the device's registers are reset and the device remains in an ultra-low-power state until SHDNL is brought high.

The shutdown state is entered by stopping communication (host generated commands, keep-alives, and/or ALERTPACKETs) or writing the FORCEPOR bit. The rate at which shutdown mode is entered is controlled by the

time constant associated with the external C_{SHDNL} and the equivalent pulldown resistance. As an example, stopping communication results in a time constant of ~10ms derived from the internal 10MΩ resistor and C_{SHDNL}. Alternatively, writing the FORCEPOR bit will create a time constant of ~0.47µs from the 400Ω pulldown to create a 4.7µs time constant.

Table 12. Shutdown Timing

SHUTDOWN METHOD	$R_{PULLDOWN}$		C_{SHDNL}	TIME CONSTANT
Register configured FORCEPOR	400Ω	Internal	1nF	0.47µs
Host places UART in idle mode	10MΩ			10,000µs

Note: If a faster transition to the shutdown state is required, an external resistor can be connected between the SHDNL pin and AGND. The resistance value should be greater than 4.7kΩ to avoid any interaction with the internal emergency discharge mode pullup resistance.

If only a register reset is required, the host can issue a soft reset by enabling the SWPOR bitfield. This resets all non-interface-related device bitfields (UARTCFG, TXUIDLEHIZ, TXLIDLEHIZ, ADAPTTXEN, and UARTHOST).

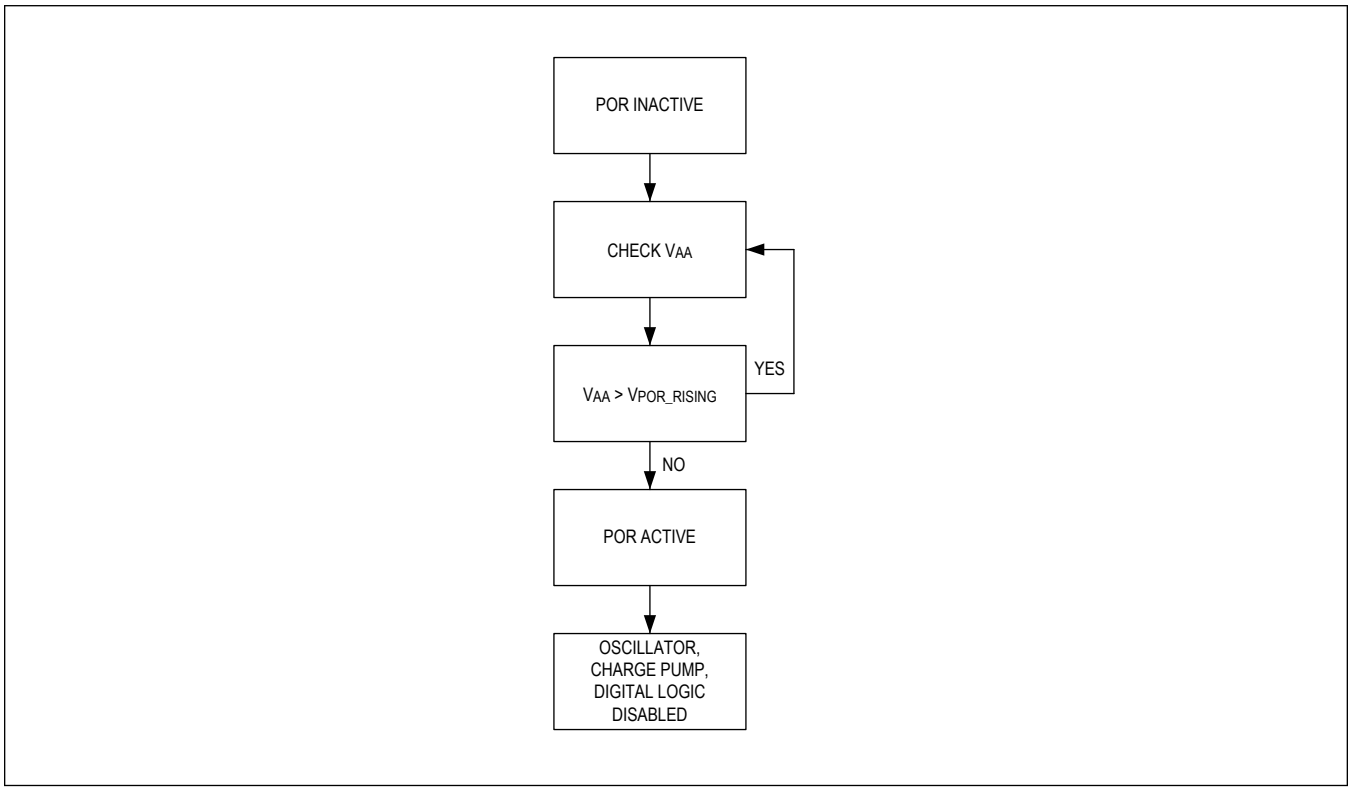


Figure 13. Shutdown Sequence

Power-On and Shutdown Timing

Figure 14 and Table 12 provide details regarding power-on control and shutdown timing, as well as supply sequencing in a high-voltage daisy-chained system controlled by UART communication.

Note: As shown in Table 12, shutdown may also be controlled by writing the specific FORCEPOR bit.

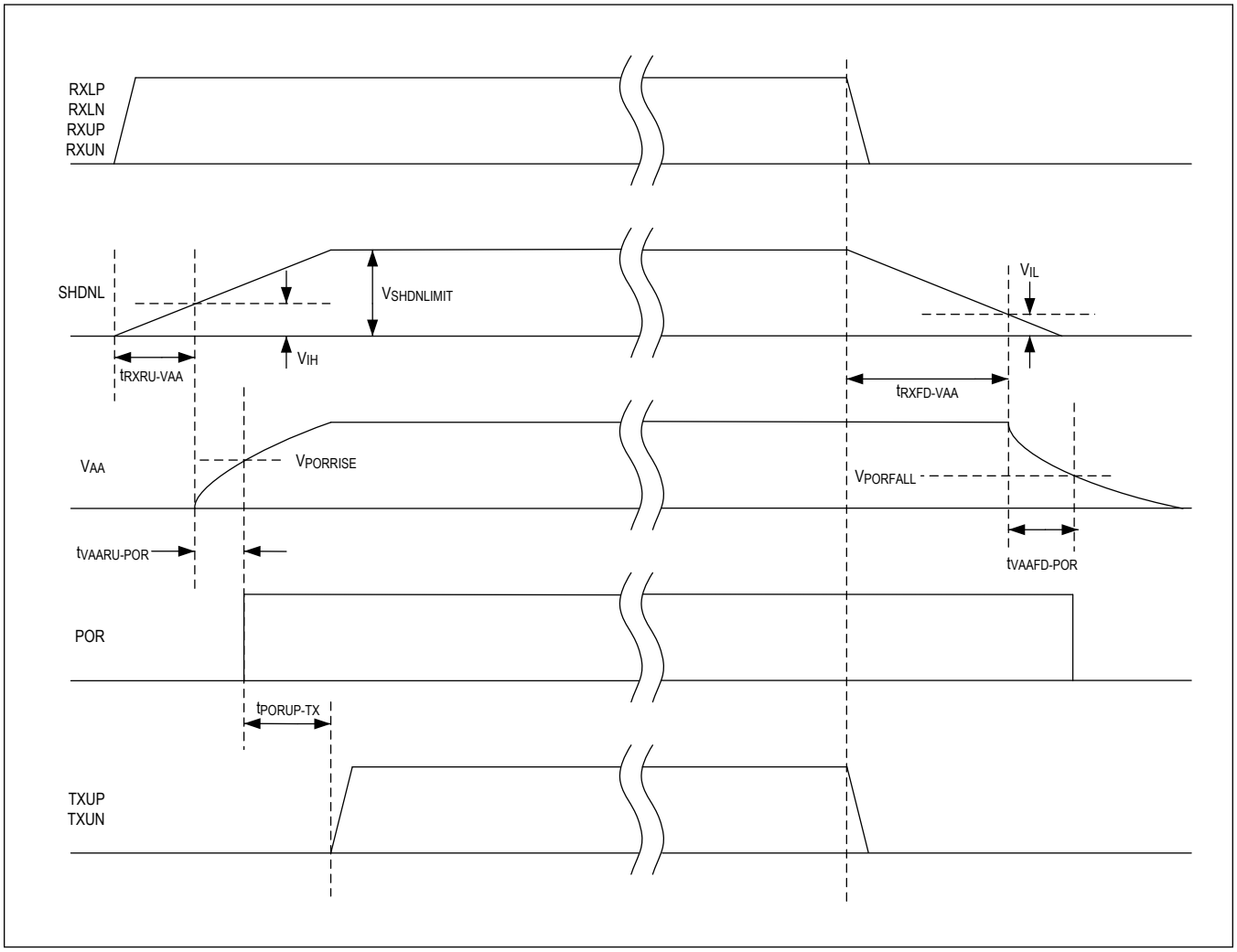


Figure 14. Power-On and Shutdown Timing

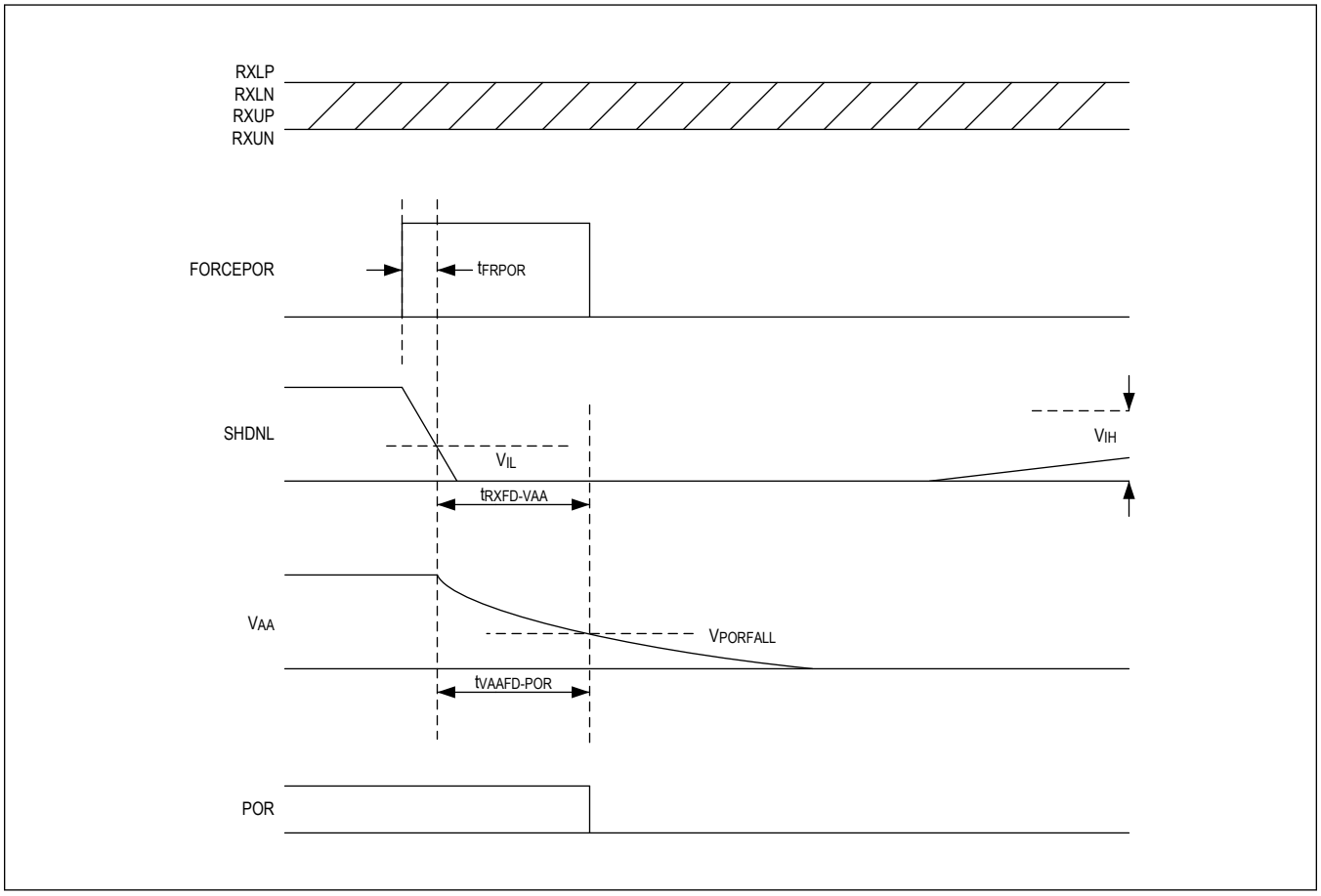


Figure 15. Shutdown Timing

Active Mode

The device will enter acquisition mode upon receiving a SCAN command or during cell-balancing operation with UV threshold detection. The overall time spent in acquisition mode is determined by the settings defined by the SCANCTRL and ACQCFG registers. Once the acquisition is completed (signified by SCANDONE and DATARDY), the device will enter low-power standby mode. If at any point within acquisition mode SHDNL is goes below V_{IL_SHDNL}, T_{SHDNL} is exceeded, or V_{AA} transitions below the POR threshold, the device will exit acquisition and enter shutdown mode.

Precision Internal Voltage References

The measurement system uses two precision, temperature-compensated voltage references. The references are completely internal to the device and do not require any external components. The primary voltage reference, or REF, is used to derive the linear regulator output voltage and to supply the ADC reference. An alternate, independent reference (ALTREF) may be used to verify the primary reference voltage, as described in the *Diagnostics* section.

Scan Methods

The MAX17854 has two parallel measurements engines (ADC and comparator) that are capable of providing three different acquisitions (ADC Acquisition, Comparator Acquisition, and Simultaneous ADC + Comparator Acquisition). The combination of both measurement block provides hardware redundancy to accelerate fault detection and ensure added system reliability.

All modes are able to process the cell and auxiliary temperature/auxiliary voltage measurements and each have their own unique alert threshold settings to accelerate the communication of a system fault. Alert settings are described in further detail in the *Measurement Alerts* section.

ADC Input Range

The ADC supports unipolar and bipolar cell input acquisitions through the configuration settings of the POLARITY[13:0] bits in the POLARITYCTRL register. In the unipolar configuration, the input range is nominally 0 to 5V. In the bipolar configuration, the nominal input range is nominally -2.5V to 2.5V. Through combining the conversion data from the two scan configurations, the input range can effectively be extended from -2.5V to 5V where any bipolar measurements over 2.3V should be supplemented with the unipolar measurements.

The flexibility to support both unipolar and bipolar conversions ensures that both cell measurements, as well as bus-bar measurements, are able to be simultaneously captured within the same acquisition that will help optimize acquisition time and interface throughput.

Note: Conversions for some diagnostic modes automatically preconfigure the device to use either bipolar or unipolar mode regardless of the POLARITY_n bit value in the POLARITYCTRL register.

The ADC also supports both ratiometric and absolute acquisitions for the auxiliary inputs through the configuration setting of the AUXREFSEL[5:0] bits in the AUXREFCTRL register. Ratiometric acquisitions are primarily used for NTC-based temperature measurements and support an input range of 0V to V_{AA}. Absolute acquisitions can be used for any on supplemental voltage measurement required by the application and supports an input range of 0V to V_{REF}. To ensure the highest accuracy for the application, the appropriate mode should be configured. (It is not recommended to perform an ratiometric acquisition for an absolute measurement such as a supply voltage, as the variability in the reference (V_{AA}) can introduce unwanted measurement error.)

The auxiliary configuration supports simultaneous acquisition of both absolute and ratiometric measurements to help optimize acquisition time and interface throughput.

Note: In all ADC configurations, reduced linearity may occur near the zero-scale and full-scale limits. See the *Electrical Characteristics* table for device accuracy specifications.

Table 13. ADC Input Range

CELL INPUT VOLTAGE		AUX RATIO INPUT VOLTAGE	AUX ABSOLUTE INPUT VOLTAGE	CELLn[15:2] AUXn[15:2] (14 BITS)		CELLn[15:0] AUXn[15:0] (16 BITS)
BIPOLAR MODE	UNIPOLAR MODE			HEXADECIMAL	DECIMAL	
-2.5V	0V	0V	0V	0000h	0d	0000h
0V	2.5V	$V_{AA}/2$	$V_{REF}/2$	2000h	8192d	8000h
2.5V	5V	V_{AA}	V_{REF}	3FFFh	16383d	FFFCh

Comparator Input Range

The comparator supports a unipolar cell input range from 0 to 5V input through the configuration of the POLARITY[13:0] bit in the POLARITYCTRL registers. If the individual POLARITY bit is configured for a bipolar acquisition, the comparator cell measurement will be omitted from the scan.

The comparator also supports ratiometric and absolute acquisition for the auxiliary input that follows the same configuration as described in the *ADC Input Range* section. Ratiometric acquisitions support an input range of 0V to V_{AA} and absolute acquisitions supports an input range of 0V to V_{REF}.

Table 14. Comparator Input Range

CELL INPUT VOLTAGE	AUX RATIO INPUT VOLTAGE	AUX ABSOLUTE INPUT VOLTAGE	COMPOVTH, COMPUVTH, COMPAUXROVTH, COMPAUXRUVTH COMPAUXAOTH,COMPAUXAUVTH (12 BITS)		COMPOVTH[15:0], COMPUVTH[15:0], COMPAUXROVTH[15:0], OMPAUXRUVTH[15:0], COMPAUXAOTH[15:0], COMPAUXAUVTH[15:0] (16 BITS)
			HEXADECIMAL	DECIMAL	
0V	0V	0V	000h	0d	0000h
2.5V	$V_{AA}/2$	$V_{REF}/2$	7FFh	2047d	7FF0h
5V	V_{AA}	V_{REF}	FFFh	4095d	FFF0h

Scan Configuration

The SCANCFG bits in the SCANCTRL register selects the acquisition that is to be performed. All available configurations are listed below.

1. ADC
2. ADC and Comparator (ADC+COMP)
3. Comparator
4. Calibration
5. Balancing Switch Short
6. Balancing Switch Open
7. Cell Sense Open Odds
8. Cell Sense Open Evens

ADC, comparator, and ADC+COMP acquisitions have programmable sample intervals through the configuration of the FOSR bit. This setting, when coupled with the OVSAMPL, allows for specific frequency rejection at either 50Hz/100Hz or 60Hz/120Hz. If not configured, the user may specifically control the sample interval through the timing of the interface to support any desired post processing on the host controller.

Note: The balance switch and cell sense acquisitions will immediately configure the internal balance switches once the SCANCFG bitfield is written. See the *BALSW Diagnostics* section for details on the operation of this acquisition mode.

ADC Configurations and Properties

ADC Polarity Configuration

Unipolar and bipolar measurements are supported within a single acquisition to capture all cell and bus bar data without the need to reconfigure multiple scan configuration registers or perform multiple acquisitions. Cell polarity is configured using the POLARITYCTRL register where all cells are defaulted to unipolar measurements (POLARITY [13:0] = 0000h).

Bipolar cells are fault-masked during BALSWDIAG ADC measurement scans. MINMAXPOL determines whether bipolar cells are included in MIN/MAXCELL and ALRTMSMTCH calculations.

Bipolar cell measurements are checked against BIPOVTH and BIPUVTH thresholds rather than OVTH and UVTH thresholds.

Bipolar cells are not included in comparator measurement scans, and ALRTCOMPOV/ALRTCOMPUV alerts are not evaluated.

ADC Scan Properties

ADC acquisitions can be applied to the cell, auxiliary, block, and diagnostics measurements.

The cell measurements can be programmed through the SCANMODE bit in the SCANCTRL register to use two-conversion phases (pyramid mode) or a single-conversion phase (ramp mode).

For the cell inputs, pyramid mode (SCANMODE = 0) performs the first conversion phase in ascending cell order (bottom-enabled cell to top-enabled cell) and the second conversion phase is in descending order (top-enabled cell to bottom-enabled cell). The two-conversion scan allows for chopping of the inputs to effectively remove any offsets or reference

induced errors, as well as create a virtual sampling time that is the same for all cell measurements.

The ramp mode (SCANMODE = 0b1) performs a single-conversion phase (bottom-enabled cell to top-enabled cell), which will improve conversion speed.

The auxiliary measurements do not require a pyramid (dual-phase) sampling approach, and are sampled in a single conversion regardless of SCANMODE configuration.

ADC Acquisition

ADC acquisitions can be configured for the cell, auxiliary, block, and diagnostics. The acquisition is initiated by writing a logic one to the SCAN bit in the SCANCTRL register. This write acts as a strobe, and the SCAN bit content is automatically cleared, reading back a logic 0 if polled. In daisy-chained devices, acquisitions in either UART path (depending on the master configuration) are delayed by the propagation delay, t_{PROP}, of the command packet through each device. The acquisition for the device is signaled complete when the SCANDONE bit is a logic 1.

Note: If any additional write to the SCANCFG is issued prior to the SCANDONE bit being cleared, this command will be ignored.

Pyramid Mode Acqusition Sequence

The ADC acquisition process for Pyramid mode (SCANMODE = 0) is outlined as follows:

1. Disable the HV charge pump.
2. The following conversions initiate, if enabled:
   a. V_{BLK} conversion (first phase)
   b. All enabled cell conversions (first phase) in ascending order (1 through 14)
   c. All enabled cell conversions (second phase) in descending order (14 through 1)
   d. V_{BLK} conversion (second phase)
   e. <End of Pyramid>
   f. DIAG1 conversion (first phase)
   g. DIAG1 conversion (second phase)
   h. DIAG2 conversion (first phase)
   i. DIAG2 conversion (second phase)
   j. Auxiliary conversions
3. Enable the HV charge pump for the recovery period unless:
   a. OVSAMPL = 000b (no oversampling), or
   b. All oversample measurements are complete
4. Repeat steps 1 and 2 until all oversamples are done.
5. Set the SCANDONE bit.

ADC Pyramid Mode Figures

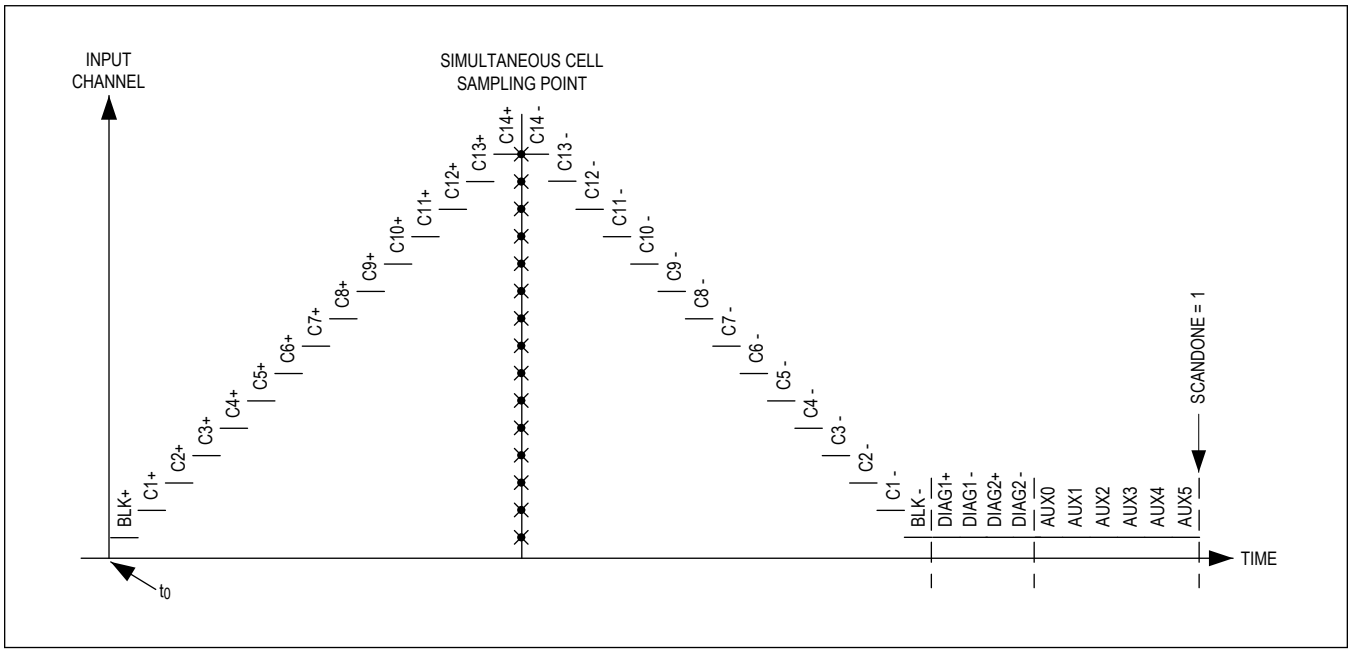


Figure 16. Acquisition - SCANCFG = 0h, SCANMODE = 0, OVSAMPL = 0h, ALTMUXSEL = 0, BLOCKEN = 1, DIAGSEL1 > 0h, DIAGSEL2 > 0h, AUXEN = 3Fh

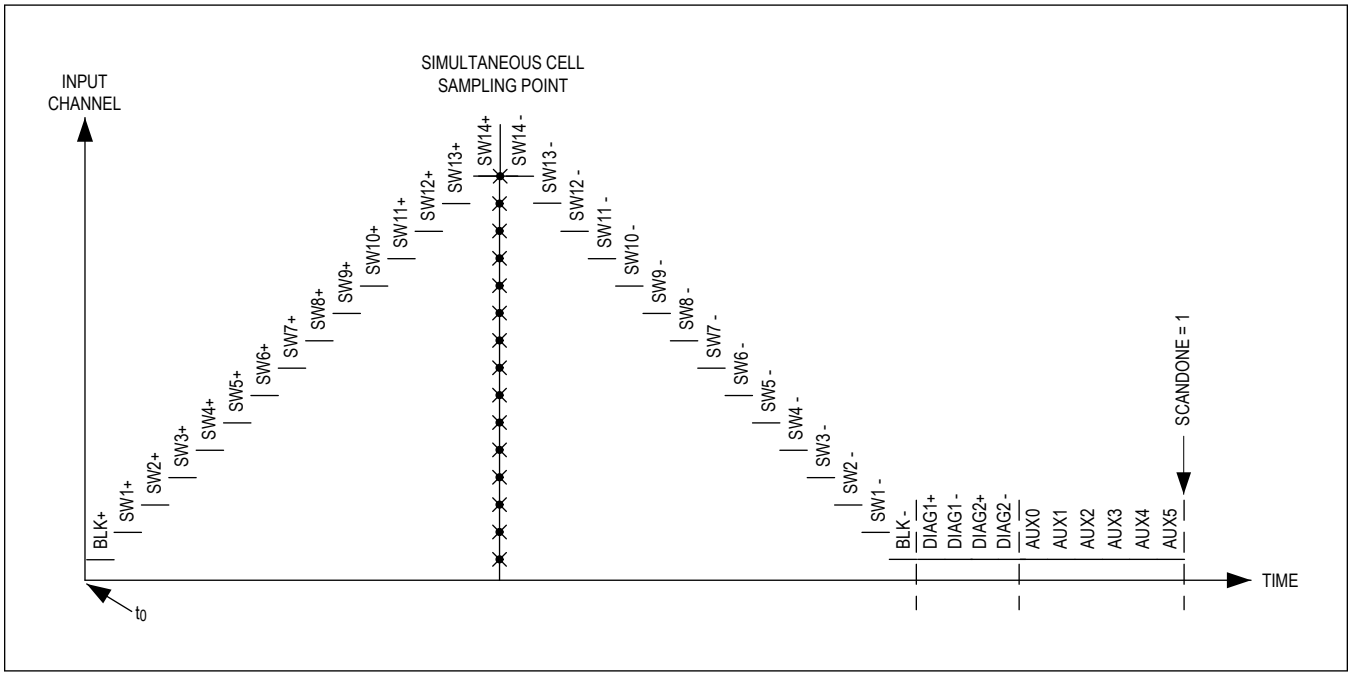


Figure 17. Acquisition - SCANCFG = 0h, SCANMODE = 0, OVSAMPL = 0h, TOPCELL1/2 = 14, ALTMUXSEL = 1, BLOCKEN = 1, DIAGSEL1 > 0h, DIAGSEL2 > 0h, AUXEN = 3F

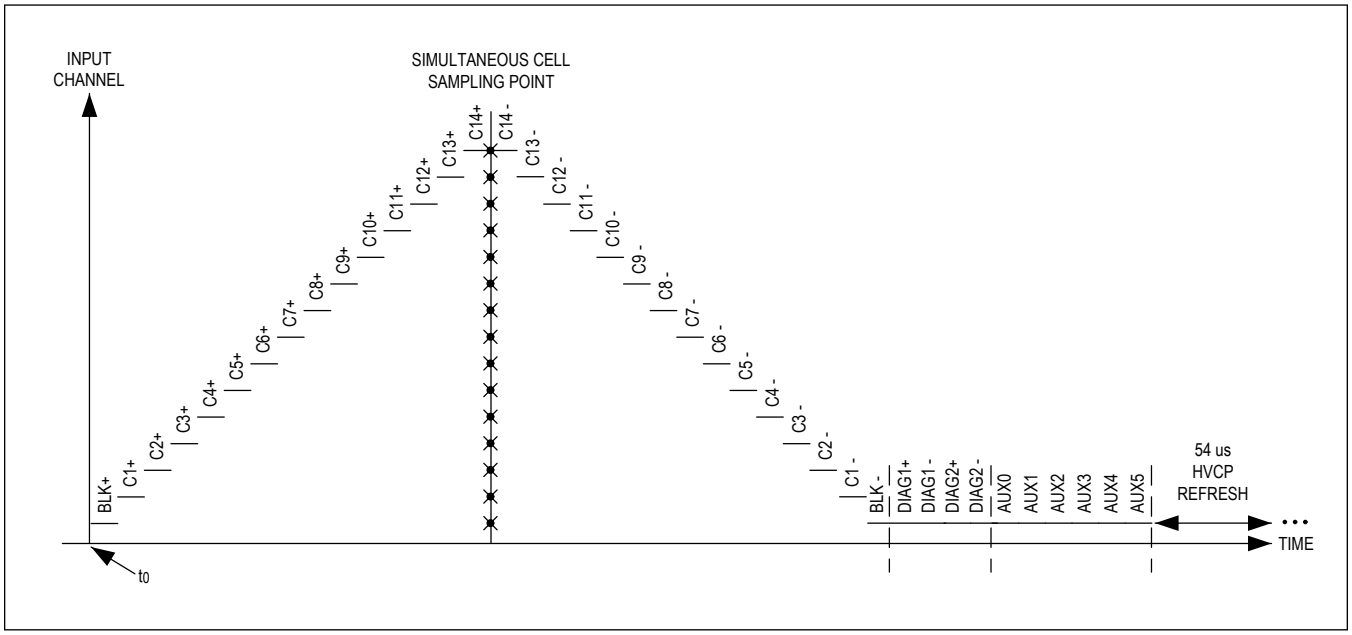


Figure 18. Acquisition - SCANCFG = 0h, SCANMODE = 0, OVSAMPL > 0h, ALTMUXSEL = 0, BLOCKEN = 1, DIAGSEL1 > 0h, DIAGSEL2 > 0h, AUXEN = 3Fh

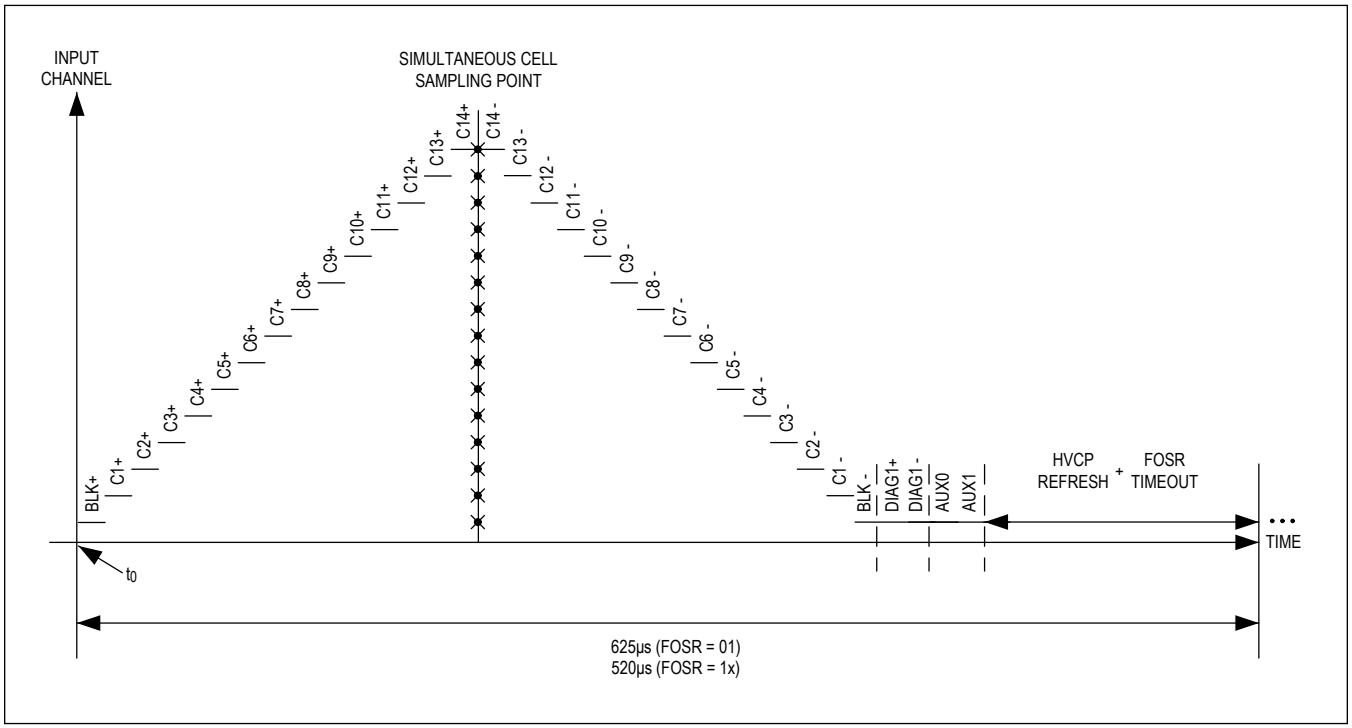


Figure 19. Acquisition - SCANCFG = 0h, SCANMODE = 0, OVSAMPL > 0h, ALTMUXSEL = 0, BLOCKEN = 1, DIAGSEL1 > 0h, AUXEN = 03h, FOSR > 0h

Pyramid Mode Acquisition Time

The total time for ADC Pyramid mode acquisitions can be calculated by summing all the conditional process times as shown in following tables. There is one measurement cycle per oversample acquisition.

ADC Acquisition Timing - Pyramid Mode

Table 15. ADC Pyramid Mode (SCANMODE = 0) Acquisition Time

PROCESS	TIME (µs)	CONDITION	FREQUENCY
Initialization	15	Oversample > 1	Once per acquisition
	35	Oversample = 1	
AUXIN Settling (if enabled)	6 * AUXTIME[9:0]	THRMMODE = Automatic mode and FOSR = 1.6kHz, 1.92kHz mode	Once per acquisition
	6 * AUXTIME[9:0] - $t_{Initialization}$ - t_{VBLK} - $t_{Cell\_Scan\_Setup}$ - t_{Cell_Scan} - t_{Diag_Total}	THRMMODE = Automatic mode and FOSR = Free Run mode	
V_{BLK} Measurement (if enabled)	31.5	BLOCKEN =1	Every measurement cycle
Cell Measurement	9 x y	For y = # of enabled cell inputs	
DIAG1 Measurement and/or DIAG2 Measurement (if enabled)	33.5	Die Temperature diagnostic	
	24.75	V_{AA} diagnostic	
	29.25	Comp Signal Path diagnostic	
	24.75	Cell Gain Calibration diagnostic	
	87.75	V_{ALTREF} diagnostic	
	20.25	DAC 3/4, DAC 1/4	
	5.44	All other diagnostics	
AUXIN Measurement (if enabled)	6.75 * x	For x = # of enabled AUXIN inputs	
HV Recovery (if oversampling enabled)	57 * (z-1)	For z = # of oversamples	Every measurement cycle except last
ADCZSFS Diagnostic (if enabled)	11.2	ADCZSFSEN = 1	End of acquisition
COMPACC Diagnostic (if enabled)	13.5	COMPACCEN = 1	End of acquisition

Ramp Mode Acquisition Sequence

The ADC acquisition process for Ramp mode (SCANMODE = 0) is outlined below:

1. Disable the HV charge pump.
2. The following conversions initiate, if enabled:
   a. V_{BLK} conversion (first phase)
   b. All enabled cell conversions (1 through 14)
   c. V_{BLK} conversion (second phase)
   d. <End of Ramp>
   e. DIAG1 conversion
   f. DIAG2 conversion
   g. Auxiliary conversions
3. Enable the HV charge pump for recovery period unless:
   a. OVSAMPL = 000b (no oversampling), or

b. All oversample measurements are complete

4. Repeat steps 1 and 2 until all oversamples are done.
5. Set the SCANDONE bit.

ADC Ramp Mode Figures

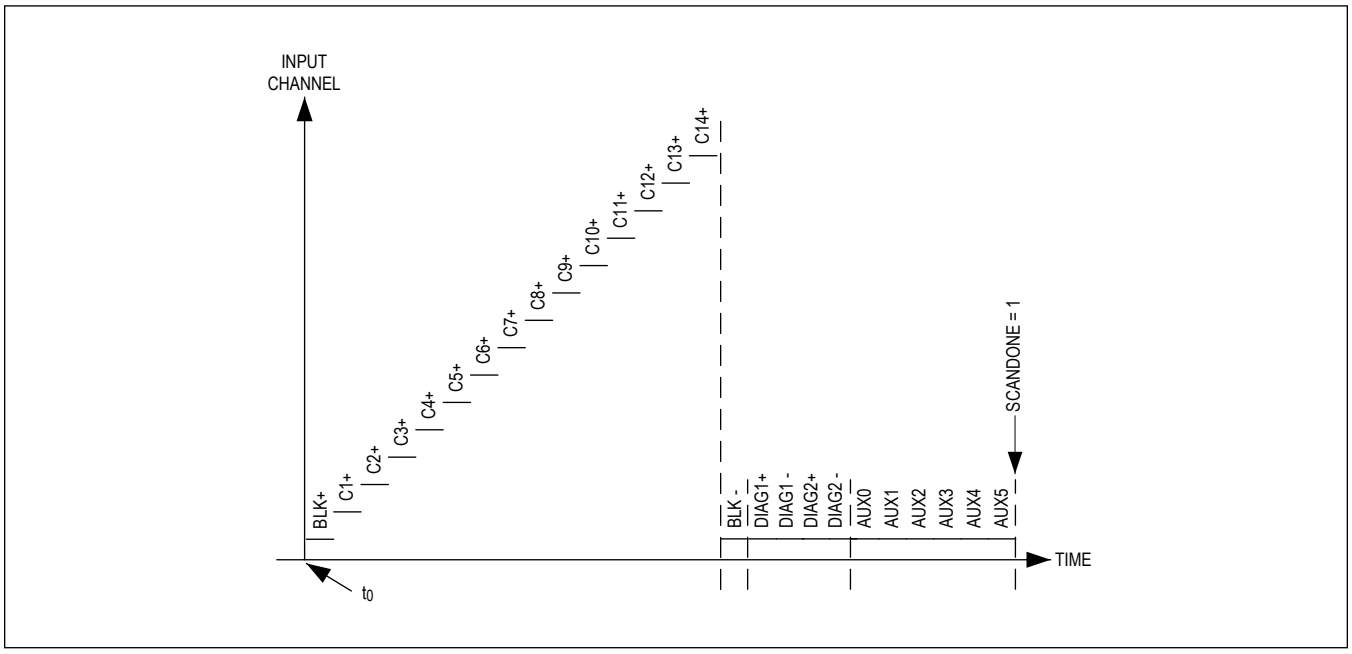


Figure 20. Acquisition - SCANCFG = 0h, SCANMODE = 1, OVSAMPL = 0h, ALTMUXSEL = 0, BLOCKEN = 1, DIAGSEL1 > 0h, DIAGSEL2 > 0h, AUXEN = 3Fh

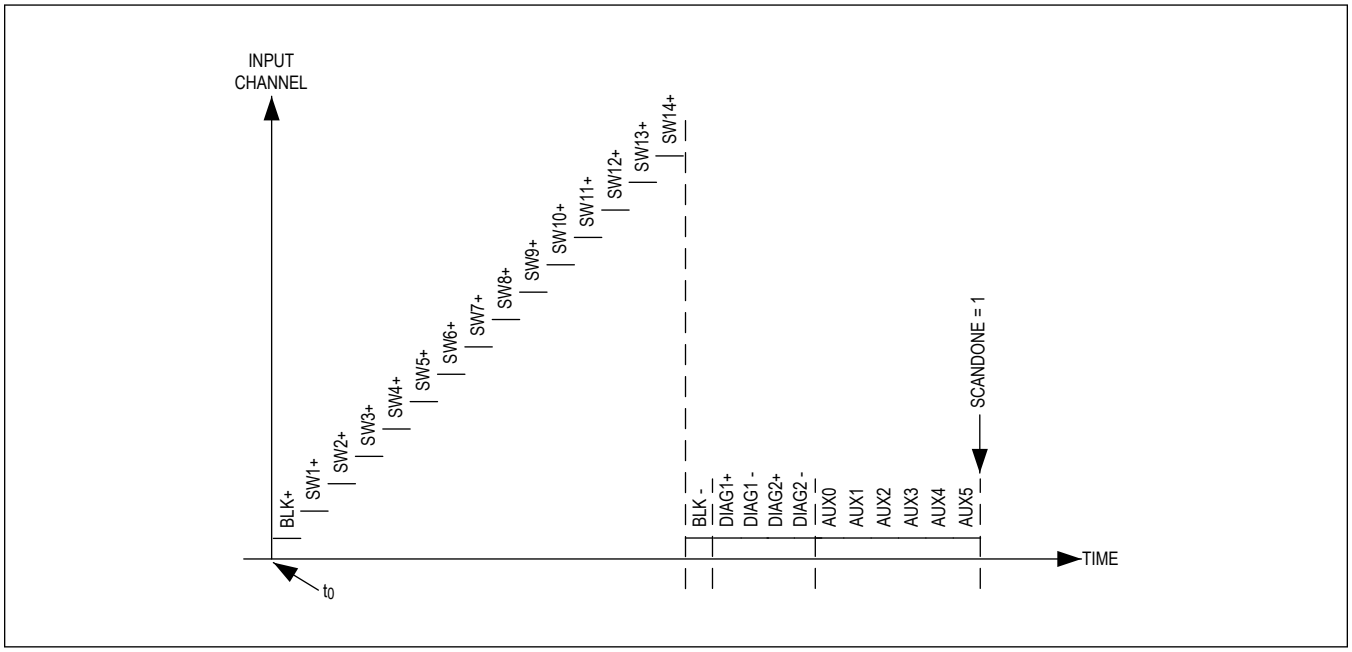


Figure 21. Acquisition - SCANCFG = 0h, SCANMODE = 1, OVSAMPL = 0h, TOPCELL1/2 = 14, ALTMUXSEL = 1, BLOCKEN = 1, DIAGSEL1 > 0h, DIAGSEL2 > 0h, AUXEN = 3Fh

Ramp Mode Acquisition Time

The total time for ADC Ramp mode acquisitions can be calculated by summing all the conditional process times as shown in Table 16. There is one measurement cycle per oversample acquisition.

ADC Acquisition Timing - Ramp Mode

Table 16. ADC Ramp Mode (SCANMODE = 1) Acquisition Time

PROCESS	TIME (µs)	CONDITION	FREQUENCY
Initialization	15	Oversample > 1	Once per acquisition
	35	Oversample = 1	
AUXIN Settling (if enabled)	6 * AUXTIME[9:0]	THRMMODE = Automatic mode and FOSR = 1.6kHz, 1.92kHz mode	Once per acquisition
	6 * AUXTIME[9:0] • $t_{Initialization}$ • t_{VBLK} • $t_{Cell\_Scan\_Setup}$ • t_{Cell_Scan} • t_{Diag_Total}	THRMMODE = Automatic mode and FOSR = Free Run mode	
V_{BLK} Measurement (if enabled)	31.5	BLOCKEN = 1	Every measurement cycle
Cell Measurement	4.5 * y	For y = # of enabled cell inputs	
DIAG1 Measurement and/or DIAG2 Measurement (if enabled)	33.5	Die Temperature diagnostic	
	24.75	V_{AA} diagnostic	
	29.25	Comp Signal Path diagnostic	
	24.75	Cell Gain Calibration diagnostic	

Table 16. ADC Ramp Mode (SCANMODE = 1) Acquisition Time (continued)

	87.75	V_{ALTREF} diagnostic	
	20.25	DAC 3/4, DAC 1/4	
	5.44	All other diagnostics	
AUXIN Measurement (if enabled)	6.75 * x	For x = # of enabled AUXIN inputs	
HV Recovery (if oversampling enabled)	57 * (z-1)	For z = # of oversamples	Every measurement cycle except last
ADCZSFS Diagnostic (if enabled)	11.2	ADCZSFSEN = 1	End of acquisition
COMPACC Diagnostic (if enabled)	13.5	COMPACCEN = 1	End of acquisition

ADC Acquisition Time Example

Table 17 provides an example of common configuration and the associated acquisition time that can be achieved.

Table 17. ADC Acquisition Time Examples (with AUXTIME[9:0] = 000h)

ENABLED MEASUREMENTS	NO OVERSAMPLING (OVSAMPL[2:0] = 0h)		8x OVERSAMPLING (OVSAMPL[2:0] = 2h)		16x OVERSAMPLING (OVSAMPL[2:0] = 3h)	
	PYRAMID SCAN	RAMP SCAN	PYRAMID SCAN	RAMP SCAN	PYRAMID SCAN	RAMP SCAN
14 cells	161.2µs	98.25µs	1424µs	920µs	2890µs	1882µs
14 cells, V_{BLK}	192.6µs	129.6µs	1675µs	1171µs	3392µs	2384µs
14 cells, 6 aux	201.7µs	138.7µs	1748µs	1244µs	3538µs	2530µs
14 cells, V_{BLK}, 6 aux	233.1µs	170.1µs	1999µs	1495µs	4040µs	3032µs
14 cells, V_{BLK}, die temp DIAG, 6 aux	266.6µs	203.5µs	2266.5µs	1762.5µs	4475µs	3567µs

Comparator Configuration and Properties

Comparator Scan Properities

The comparator acquisition can be configured for unipolar cell measurements and auxiliary measurements. If a cell input is configured for bipolar operation in the POLARITYCTRL register, the comparator measurement is idle for this acquisition period and the associated alert reporting in the ALRTCOMPOVREG and ALRTCOMPUVREG registers will not be updated. If acquisition time is of critical importance for a comparator scan, it is recommended to disable bipolar inputs in the MEASUREEN1 register to prior to issuing a SCAN as this will omit these measurements from the acquisition.

The SCANMODE bit configuration also does not apply to the comparator acquisition and the comparator will operate only on the inputs indicated by the MEASUREEN1 and ALRTOVEN, ALRTUVEN registers. This is illustrated in the following comparator acquisition process.

Comparator Acquisition

The acquisition is initiated by writing a logic 1 to the SCAN bit in the SCANCTRL register. This write acts as a strobe, and the SCAN bit content is automatically cleared, reading back a logic 0 if polled. In daisy-chained devices, acquisitions in either UART path (depending on the master configuration) will be delayed by the propagation delay, t_{PROP}, of the command packet through each device. The acquisition for device is signaled complete when SCANDONE bit is a logic 1.

Note: If any additional write to the SCANCFG is issued prior to the SCANDONE bit being cleared, this command will be ignored.

Comparator Acquisition Process

1. Disable the HV charge pump.

2. Perform overvoltage conversion on all enabled cell inputs (MEASUREEN1) against the COMPOVTH threshold in ascending order (1 through 14).
3. Update the ALRTCOMPOV register (MEASUREEN1 and ALRTOVEN).
4. Perform undervoltage conversion on all enabled cell inputs (MEASUREEN1) against the COMPUVTH threshold in descending order (14 through 1).
5. Update the ALRTCOMPUV register (MEASUREEN1 and ALRTUVEN).
6. Perform overvoltage conversion on all enabled auxiliary inputs (MEASUREEN2) against COMPAUXOVTH in ascending order (0 through 5).
7. Update the ALRTCOMPAUXOV register (MEASUREEN2 and ALRTAUXOVEN).
8. Perform undervoltage conversion on all enabled auxiliary inputs (MEASUREEN2) against COMPAUXUVTH in ascending order (0 through 5).
9. Update the ALRTCOMPAUXUV register (MEASUREEN2 and ALRTAUXUVEN)
10. Enable the HV charge pump refresh.
11. Repeat steps 2 through 6 until all oversamples are complete.
12. Compare the results against the comparator thresholds and update alert status.
13. Enable the HV charge pump.

Note: Comparator results are only available when the corresponding OV/UV alerts are enabled.

Comparator Thresholds

The comparator cell measurements and auxiliary measurements can be programmed with OV/UV thresholds that are independent of the ADC OV/UV thresholds. However, all cell measurements share the same threshold settings as defined by the COMPOVTH and COMPUVTH registers. Additionally, all ratiometric auxiliary measurement share the same thresholds settings as defined by the COMPAUXROVTH and COMPAUXRUVTH registers, and all absolute auxiliary measurements share the same threshold settings as defined by the COMPAUXAOVTH and COMPAUXAUVTH registers.

As defined in the *Comparator Input Range* section, each threshold register is programmable up to 12 bits allowing for 1.22mV, 0.439mV, and 0.076mV of adjustable resolution on the cell, ratiometric auxiliary, and absolute auxiliary measurements respectively.

Note: For the auxiliary inputs since the full scale is dependent on V_{AA} this may have an impact on the resolution of the comparator over loading and temperature conditions.

If the pin configuration for the auxiliary input is set to GPIO or I^2C mode, both ALRTAUXOVEN and ALRTAUXUVEN are disabled (logic 0).

Comparator Acquisition Time

The total time for comparator acquisitions can be calculated by summing all the conditional process times as shown in Table 18. There is one measurement cycle per oversample acquisition.

Table 18. Comparator Acquisition Time

PROCESS	TIME (µs)	CONDITION	FREQUENCY
Initialization	15	Oversample > 1	Once per acquisition
	35	Oversample = 1	
AUXIN Settling (if enabled)	6 * AUXTIME[9:0]	THRMMODE = Automatic mode and FOSR = 1.6kHz, 1.92kHz mode	Once per acquisition
	6 * AUXTIME[9:0] - $t_{Initialization}$ - t_{VBLK} - $t_{Cell\_Scan\_Setup}$ - t_{Cell_Scan} - t_{Diag_Total}	THRMMODE = Automatic mode and FOSR = Free Run mode	
Cell Measurement	9 * y	For y = # of enabled cell inputs	Every measurement cycle
AUXIN Measurement (if enabled)	13.5 x	For x = # of enabled AUXIN inputs	

Table 18. Comparator Acquisition Time (continued)

HV Recovery (if oversampling enabled)	57 * (z-1)	For z = # of oversamples	Every measurement cycle except last
COMPACC Diagnostic (if enabled)	13.5	COMPACCEN = 1	End of acquisition

Comparator Acquisition Timing Example

Table 19 provides an example of common configuration and the associated acquisition time that can be achieved.

Table 19. Comparator Acquisition Time Examples (with AUXTIME[9:0] = 000h)

ENABLED MEASUREMENTS	NO OVERSAMPLING (OVSAMPL[2:0] = 0h)	8x OVERSAMPLING (OVSAMPL[2:0] = 2h)	16x OVERSAMPLING (OVSAMPL[2:0] = 3h)
14 cells	161.2µs	1424µs	2890µs
14 cells, 6 aux	242.2µs	2072µs	4186µs

Comparator Scan Figures

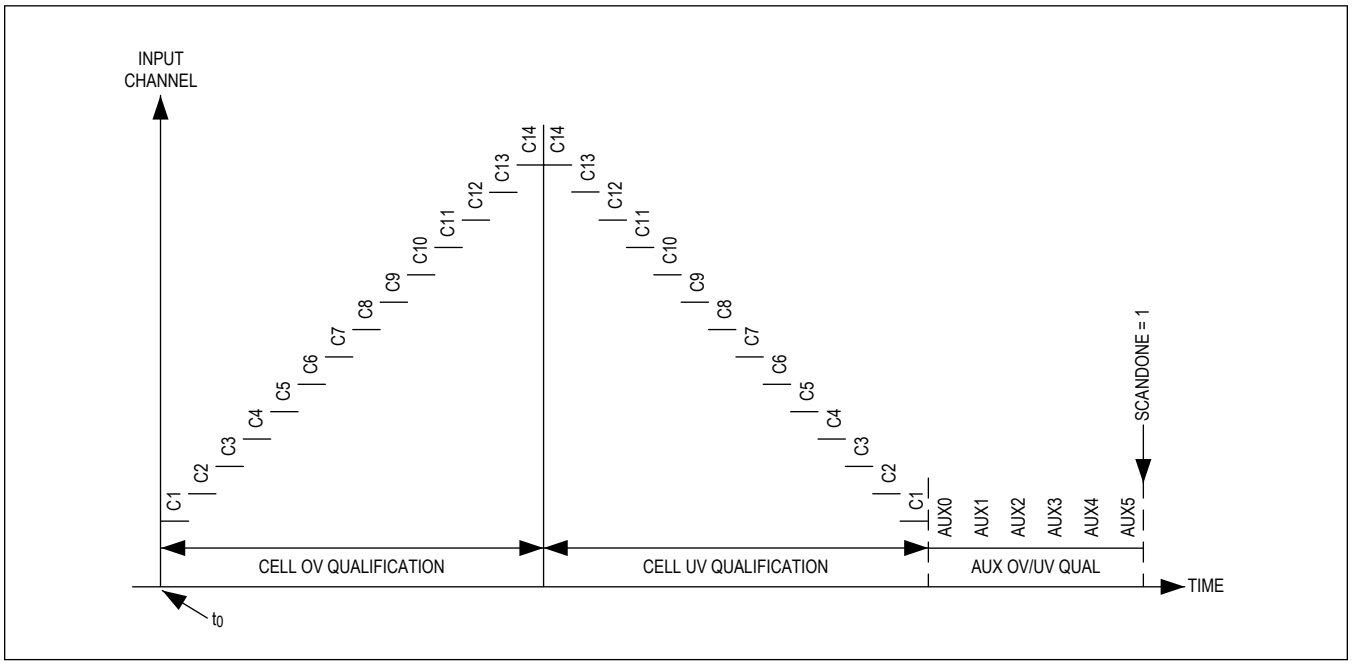


Figure 22. Comparator Single Scan Mode

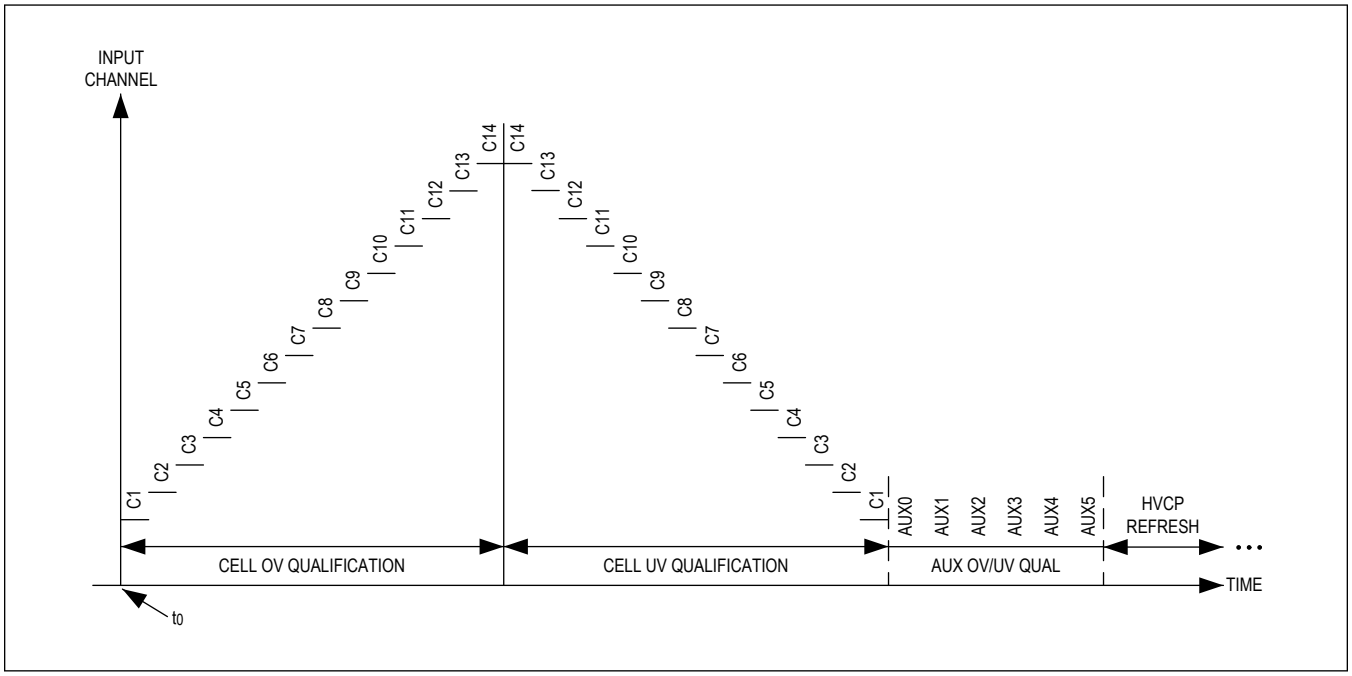


Figure 23. Comparator Single Scan with Oversampling

ADC+COMP Configuration and Properties

ADC+COMP Scan Mode

ADC+COMP acquisitions can be applied to the cell, auxiliary, block, and diagnostics measurements. Each measurement engine (ADC or comparator) retains the functionality discussed previously with additional clarification detailed below.

The comparator acquisition is applied to the unipolar cell and auxiliary inputs and is idle during bipolar cell, block, and diagnostics measurements. OV/UV alerts for the the cell path (OVALRTEN and UVALERTEN) and auxiliary path (AUXOVALRTEN and AUXUVALRTEN) are applied to both the ADC and comparator with each capable of setting it unique threshold. If any OV/UV alert is disabled the ADC measurement still occurs; however, the comparator is idle during this portion of the acquisition.

In ADC+COMP scan mode, the ADC acquisition only operates in Pyramid mode and the SCANMODE bit is ignored.

ADC+COMP Acquisition Time

The total time for ADC+COMP acquisitions can be calculated by summing all the conditional process times as shown in following tables. There is one measurement cycle per oversample acquisition.

Table 20. ADC+COMP Acquisition Time

PROCESS	TIME (µs)	CONDITION	FREQUENCY
Initialization	15	Oversample > 1	Once per acquisition
	35	Oversample = 1	
AUXIN Settling (if enabled)	6 * AUXTIME[9:0]	THRMMODE = Automatic mode and FOSR = 1.6kHz, 1.92kHz mode	Once per acquisition

Table 20. ADC+COMP Acquisition Time (continued)

	6 * AUXTIME[9:0] - $t_{Initialization}$ - t_{VBLK} - $t_{Cell\_Scan\_Setup}$ - t_{Cell_Scan} - t_{Diag_Total}	THRMMODE = Automatic mode and FOSR = Free Run mode	
V_{BLK} Measurement (if enabled)	31.5	BLOCKEN = 1	Every measurement cycle
Cell Measurement	9 * y	For y = # of enabled cell inputs	
DIAG1 Measurement AND/OR DIAG2 Measurement (if enabled)	33.5	Die temperature diagnostic	
	24.75	V_{AA} diagnostic	
	29.25	Comp signal path diagnostic	
	24.75	Cell gain calibration diagnostic	
	87.75	V_{ALTREF} diagnostic	
	20.25	DAC 3/4, DAC 1/4	
	5.44	All other diagnostics	
AUXIN Measurement (if enabled)	13.5 * x	For x = # of enabled AUXIN inputs	
HV Recovery (if oversampling enabled)	57 * (z-1)	For z = # of oversamples	Every measurement cycle except last
ADCZSFS Diagnostic (if enabled)	13.5	ADCZSFSEN = 1	End of acquisition
COMPACC Diagnostic (if enabled)	13.5	COMPACCEN = 1	End of acquisition

ADC+COMP Acquisition Time Example

Table 21 provides examples of common configuration and the associated acquisition time that can be achieved.

Table 21. ADC+COMP Acquisition Time Examples (with AUXTIME[9:0] = 000h)

ENABLED MEASUREMENTS	NO OVERSAMPLING (OVSAMPL[2:0] = 0h)	8x OVERSAMPLING (OVSAMPL[2:0] = 2h)	16x OVERSAMPLING (OVSAMPL[2:0] = 3h)
14 cells	161.2µs	1424µs	2890µs
14 cells, V_{BLK}	192.6µs	1675µs	3392µs
14 cells, 6 aux	242.2µs	2072µs	4186µs
14 cells, V_{BLK}, 6 aux	273.6µs	2323µs	4688µs
14 cells, V_{BLK}, die temp DIAG, 6 aux	307µs	2590.5µs	5223µs

ADC+COMP Scan Figures

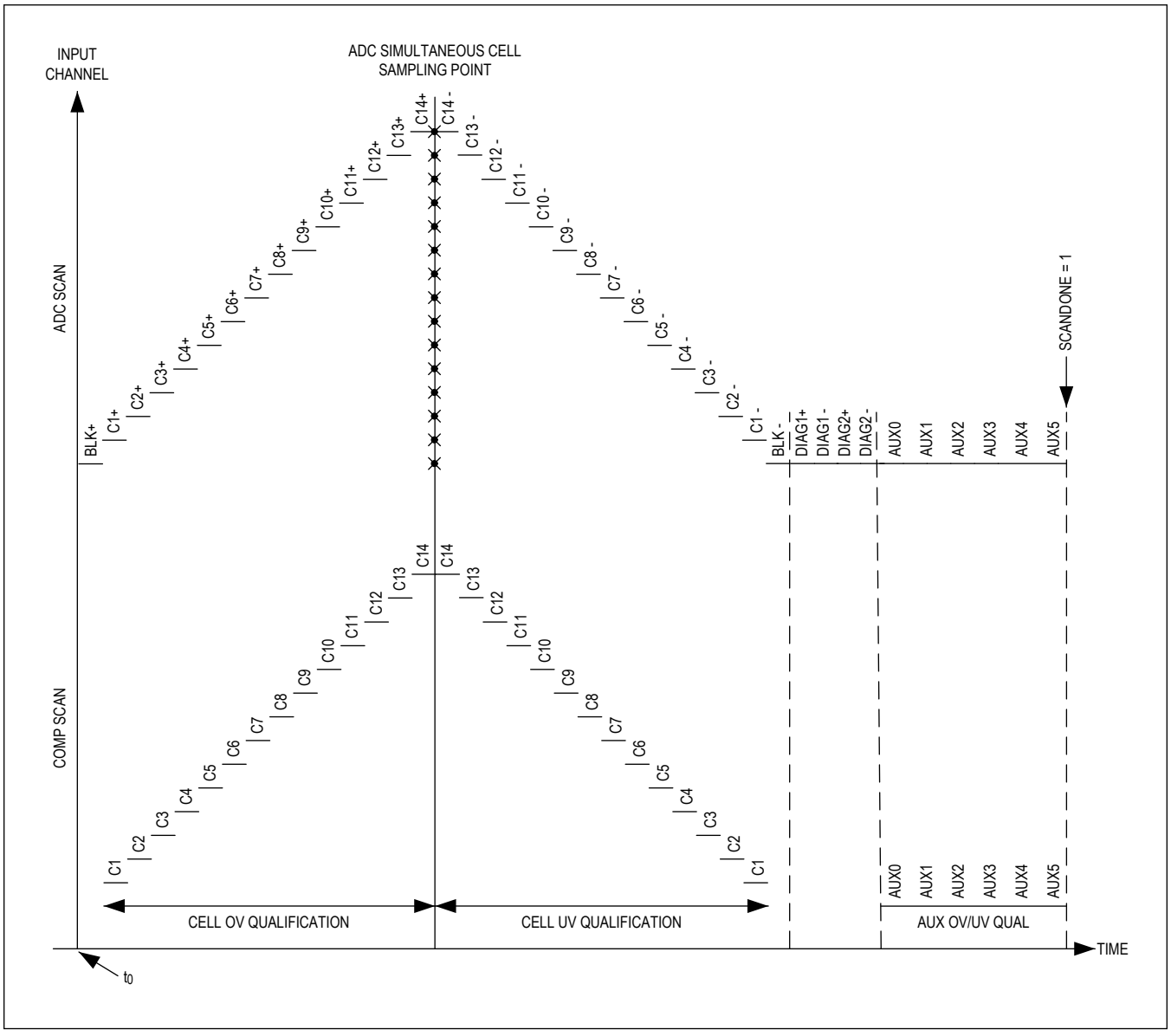


Figure 24. Simultaneous ADC+COMP Scan Mode

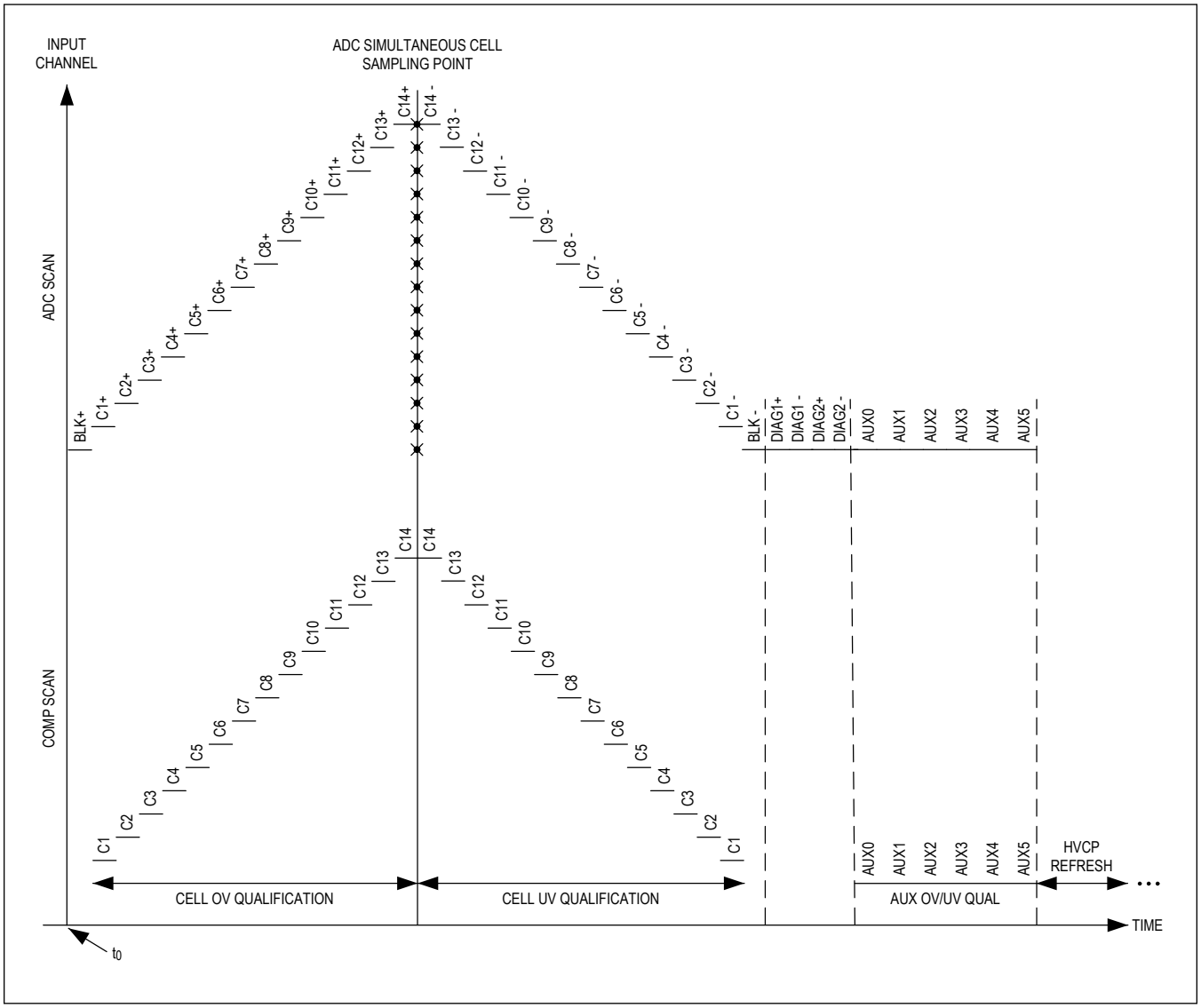


Figure 25. Simultaneous ADC+COMP Scan with Oversampling

On-Demand Calibration

The MAX17854 supports an integrated on-demand calibration procedure which can be commanded by the user to improve the internal measurement accuracy from inaccuracies of the internal signal chain. It should, however, be noted that the calibration process does not correct for inaccuracies within the external application components. The calibrated accuracy is described within the Measurement Accuracy section of the *Electrical Characteristics* table.

For a valid on-demand calibration, a calibration acquisition must be commanded using the SCANCFG bits of the SCANCTRL register. The calibration acquisition automatically configures the internal calibration sources and performs ADC acquisitions to calculate and store calibration coefficients for the cell inputs, auxiliary inputs, and block input. The completion of the calibration acquisition is signaled by the issuance of the SCANDONE bit like any other acquisition. Any commands that are sent before the calibration acquisition is completed are ignored, but will still propagate through the daisy-chain.

The calibration time is 3.75ms.

Note: The calibration acquisition is independent of the Scan Control registers and Scan Setting registers (POLARITYCTRL, SCANCTRL, ACQCFG).

The ADCCALEN bit must be set for the calibration coefficients to be applied to the measurement results. If ADCCALEN is disabled, even with the successful completion of a calibration acquisition, the measurement results will not have the calibration coefficients applied.

Note: The on-demand calibration is independent of the factory calibration. In the event that the on-demand calibration is applied, the device will retain its factory calibration setting. The factory calibration setting can never be overwritten and can be verified using the ROM CRC diagnostic in the *Diagnostics* section. See the *ADC Scan Properties* section for details on using calibration to maintain Ramp mode accuracy over DCIN voltage range; factory calibration defaults are programmed using a 50V DCIN voltage.

Table 22 indicates which calibration alerts are associated to the various measurement path.

Table 22. Measurement Path Calibration Alerts

MEASUREMENT PATH	CALIBRATION ALERTS
Cell Input - Pyramid (SCANMODE = 0b)	ALRTCALGAINP, ALRTCALOSADC
Cell Input - Ramp (SCANMODE = 1b)	ALRTCALGAINR, ALRTCALOSR
Auxiliary Input - Absolute (REFSEL = 1b)	ALRTCALOSADC
Auxiliary Input - Ratiometric (REFSEL = 0b)	ALRTCALOSTHRM
Block Input	ALRTCALOSADC
CSA Input	ALRTCALOSADC

The on-demand calibration adjustments can be verified by using the Cell Calibration and Offset Calibration commands in the DIAGSEL1 and DIAGSEL2 bits. See the *Diagnostics* section for further details.

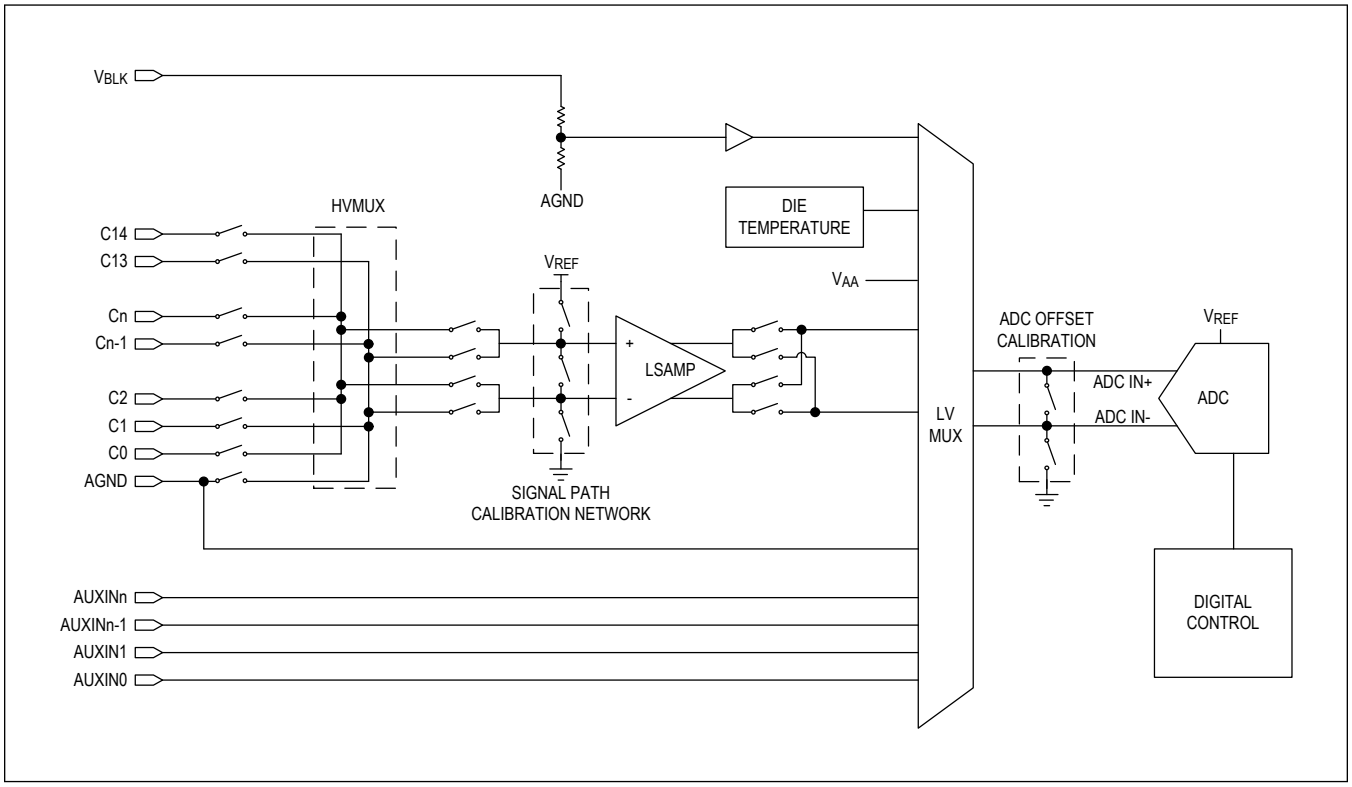


Figure 26. On-Demand Calibration Block Diagram

Calibration Alerts

Internal safety mechanisms are implemented to ensure that the applied calibration coefficients are within predetermined bounds. If a calibration coefficient were to fall outside of these bounds, this would immediately raise a fault in the ALRTSUM register for the affected calibration process (ALRTCALOSADC, ALRTCALOSR, ALRTCALOSTHRM, ALRTCALGAINP, ALRTCALGAINR). This fault condition then propagates to the STATUS1 alert register, which is capable of flagging an issue within the Data Check byte or within the hardware alert interface.

If the integrity of the calibration coefficients is questionable, it is recommended to issue a new calibration to verify and/or correct the fault, or to deassert ADCCALEN and use the factory default calibration.

Oversampling

ADC Oversampling

Oversampling performs multiple measurement cycles in a single acquisition and averages the samples to reduce the measurement noise and effectively increase the resolution of each acquisition. The net increase of the measurement resolution depends on the number of oversamples. To add n bits of measurement resolution, at least 2^{2n} oversamples are required. Since the ADC resolution is 12 bits, 13-bit resolution requires at least 4 oversamples. In order to achieve the maximum 14-bit resolution, at least 16 oversamples are required. Therefore with no oversampling, only the higher 12-bits of the measurement are statistically significant. With 4 or 8 oversamples, only the highest 13-bits are statistically significant. Taking more than 16 oversamples further reduces the measurement variation. With no oversampling, measurements can be averaged externally to achieve increased resolution, but at a higher computational cost for the host.

Comparator Oversampling

To effectively mitigate high-frequency noise from affecting the comparator measurement, the output can be oversampled using the OVSAMPL bits in the SCANCTRL register. The accumulated oversamples are digitally averaged from the comparator output to gauge if a valid OV/UV condition is present. An OV/UV condition requires the comparator readings to meet or exceed the threshold listed in Table 23 for an alert to be generated as shown the table. Thus, an OVSAMPL setting of 8 will afford one sample outside of the OV/UV condition before setting an alert. It is recommended for higher noise immunity that the OVSAMPL setting should be configured to 8 or higher for comparator acquisition with oversampling. When the ADC and comparator are simultaneously sampled, the oversampling is typically set by the noise reduction required for ADC measurements.

Table 23. Comparator Faults for Alerts vs. Oversampling

OVSAMPL	COMPARATOR FAULTS FOR ALERT
1	1
4	1
8	2
16	3
32	5
64	10
128	20

Note: The comparator acquisition can be performed using the cell input path (C_n) or the switch input path (SW_n) as configured by the ALTMUXSEL bit. In the event that the comparator acquisition is performed on the switch input path, it is recommended to increase the oversampling to account for the lessened noise attenuation from the inputs due to the higher lowpass cutoff frequency.

Oversampling Watchdog Timeout

Table 24. Watchdog-Timeout Duration

OVSAMPL	SAMPLES	ACQUISITION WATCHDOG TIMEOUT
0b000	1	750µs
0b001	4	3ms
0b010	8	6ms
0b011	16	12ms
0b100	32	24ms
0b101	64	48ms
0b110	128	96ms

Note 1: *When AUTOBALSWDIS = 1, the watchdog timeout duration is extended by SWDLY or CELLDLY (depending on ALTMUXSEL).*

Note 2:*When AUXTIME is > 0, the timeout duration is extended by AUXTIME.*

100Hz and 120Hz Filtering

There are two types of scan configurations in which oversampling frequency can be utilized, each providing a different benefit to the system performance.

The first configuration is entered through the FOSR = 0b00 mode, which performs the acquisition with minimal time delay between measurement cycles to recharge the HV charge pump. The FOSR = 0b00 mode yields the highest number of measurements per sample period, allowing for higher oversampling rates and further noise reduction. The total acquisition time is proportional to the number of oversamples configured by OVSAMPL and the type and number of enabled channels.

The FOSR settings of 0b01, 0b10, or 0b11 enables a notch filter at a frequency of 50Hz, 60Hz, 100Hz, or 120Hz. This mode may be particularly useful for accurate voltage detection during vehicle charging where noise from the power mains

will effect the voltage seen by the battery pack. To enable proper filtering for 50Hz or 100Hz, the FOSR must be set to 0b01. For 60Hz or 120Hz filtering, the FOSR must be set to either 0b10 or 0b11.

Note: When configuring the FOSR, the acquisition period is automatically preconfigured to 625µs for 50Hz/100Hz and 520µs for 60Hz/120Hz.

Table 25. FOSR Notch-Filter Setting

REJECTION FREQUENCY (Hz)	FOSR	OVSAMPL
50	0x1	0x4
60	0x2 or 0x3	0x4
100	0x1	0x4 or 0x3
120	0x2 or 0x3	0x4 or 0x3
None	0x0	Don't Care

The typical notch filter responses are shown in the *Typical Operating Characteristics* section for both 100Hz and 120Hz, respectively.

Acquisition Watchdog Timeout

If the acquisition does not finish within a predetermined time interval, the SCANTIMEOUT bit is set, the ADC logic is reset, the ALU registers are cleared, and the measurement data registers are also cleared. The acquisition watchdog timeout interval depends on the oversampling configuration as shown in Table 24.

If double-buffer mode is enabled (DBLBUFEN = 1), the ALU registers are cleared, but the data registers remain unchanged as these are known good values previously stored. Once a move operation is evoked (SCAN = 1), the previously cleared ALU data is moved from the ALU registers to the data registers and the data registers now show as cleared. See the *Double Buffer Mode* section for detailed information on the data control in the mode.

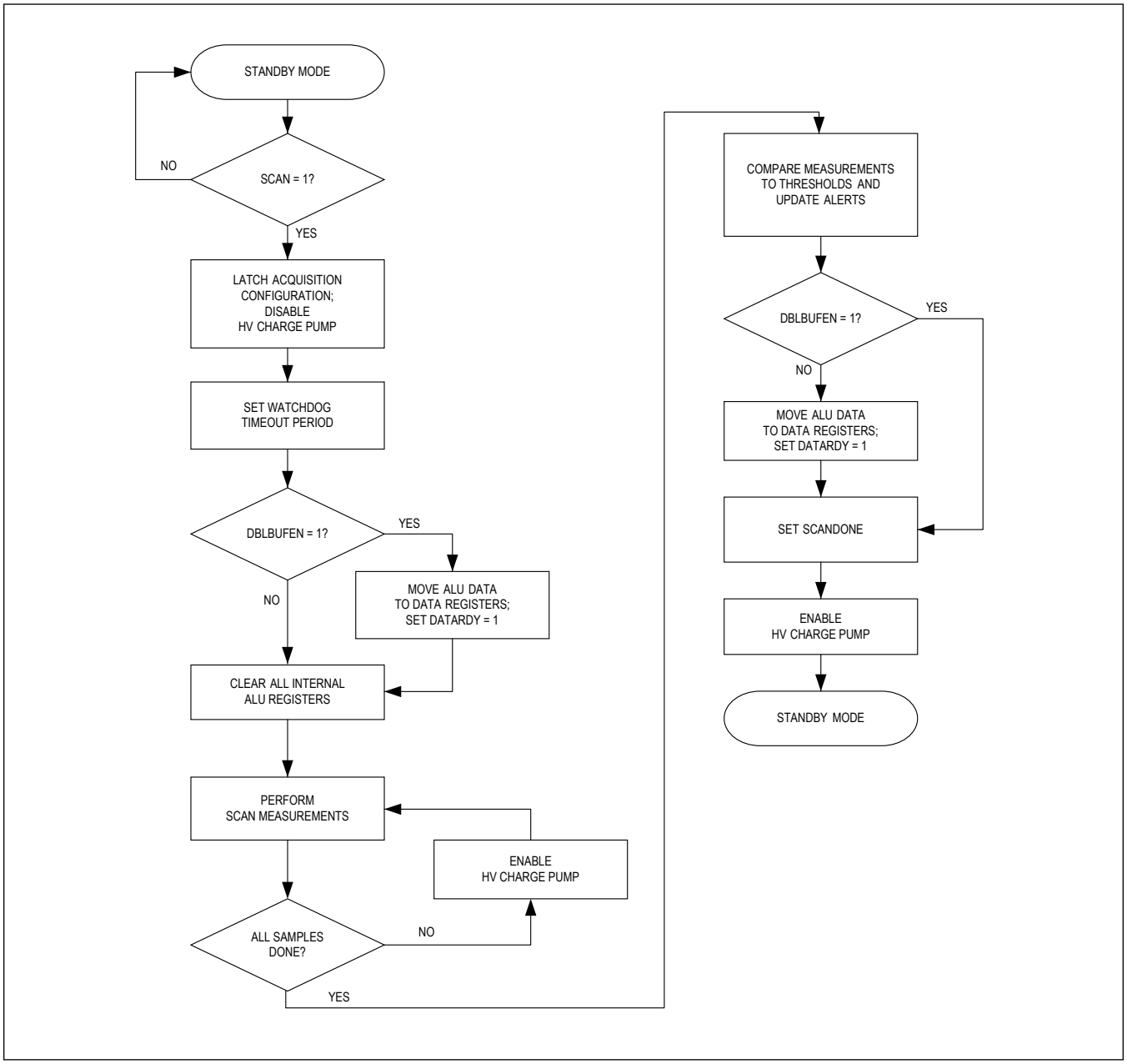


Figure 27. Acquisition-Mode Flowchart

Data Control

Acquisition Data Transfer and Control

The ADC data flow (Figure 28) can be directed through multiple data processing paths until it reaches the register space (CELLnREG, AUXnREG, BLOCKREG, DIAG1REG, DIAG2REG, TOTALREG, and MINMAXCELL) depending on the enabled configuration. The following sections detail the data flow through:

- Calibration
- IIR filter
- Single buffer data transfer
- Double buffer data transfer
- Cell balancing with embedded measurements

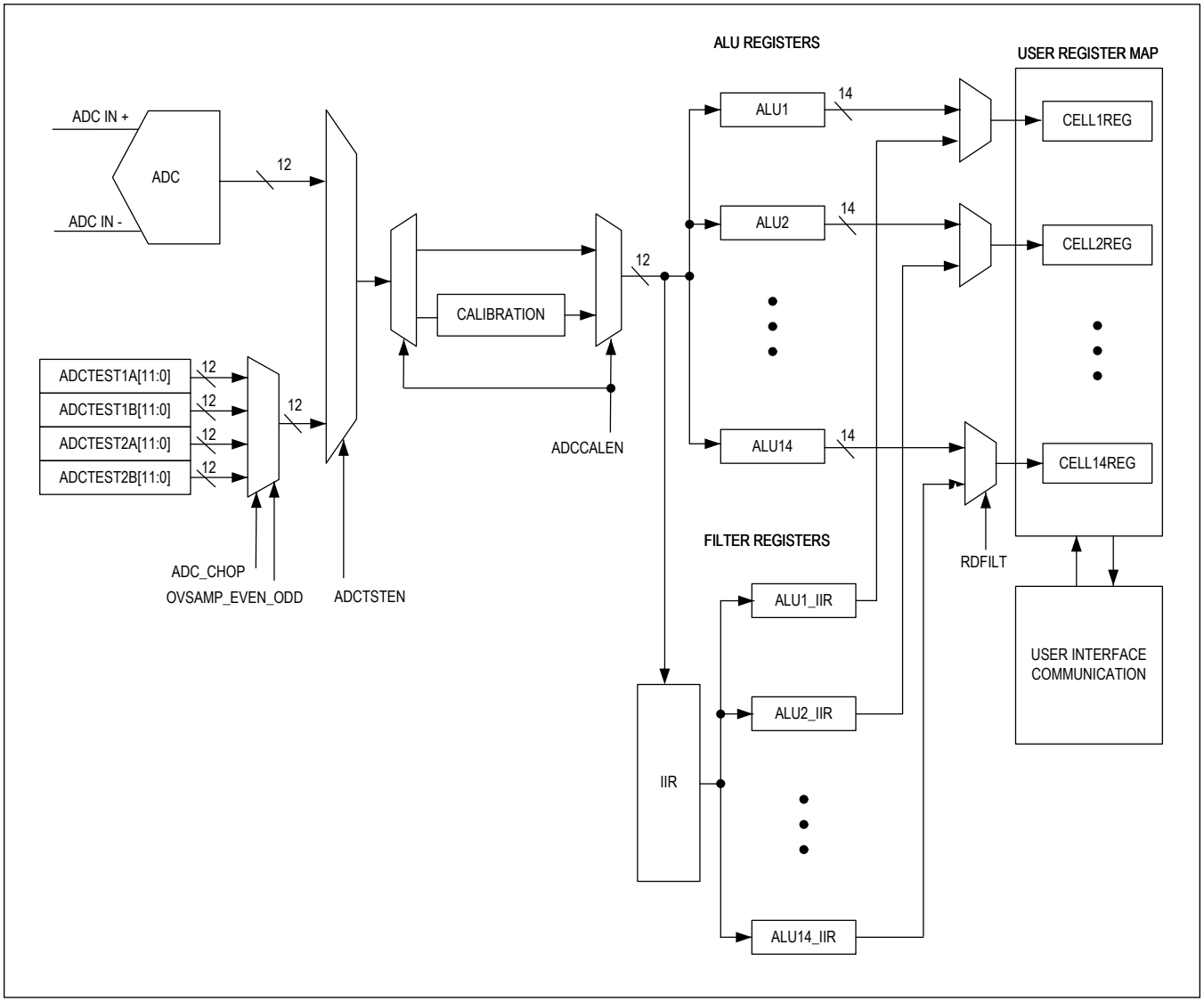


Figure 28. Data-Flow Diagram

Calibration Data Control

The ADC data is either directly output to the ALU or acted upon by the calibration block, depending on the state of the ADCCALEN bit. See the *On-Demand Calibration* section for details on the configuration and application of calibration.

IIR Filter

To augment the accuracy performance over multiple measurement cycles, the user can enable the embedded IIR filter.

The filter acts upon all enabled Cn and V_{BLK} inputs according to the user-defined settings in the MEASUREEN1 register. The TOTAL register does not have a unique IIR filter, but is instead directly computed from the sum of the IIR data registers as selected through RDFILT.

Additionally, when oversampling is enabled, the system response of the measurement data is the combination of the IIR filter and oversampling noise reduction.

Although the IIR filter can be updated dynamically on any individual acquisition through AMENDFILT, it is recommended to always allow nondiagnostic acquisitions into the IIR filter. Using the IIR filter leads to the greatest benefit in noise reduction with the external hardware filter combined with the digital filtering.

Diagnostics (including BALSWDIAG results) or higher noise data from ALTMUXSEL = 1 should not be processed within the IIR as this will corrupt the desired measurement result. This involves (but is not limited to) configuration with the diagnostic current sources (CTSTCFG, MUXDIAGEN).

Note: IIR filtering is always applied to measurement cycle during automatic cell balancing. In the event the IIRFC = 111b (off) in automatic cell-balancing modes, the IIR filter is internally forced to 000b (1/8). All other selection of IIRFC are valid.

Filter Description

The IIR filter is implemented per the following transfer function, as illustrated in Figure 29:

Y(n) = FC*X(n) + (1-FC)*Y(n-1)

FC is a 3-bit user-programmable filter coefficient. The default value of 0b010 has a weight of 3/8.

The detailed filter coefficient settings are defined in the IIRFC register. The smaller the coefficient is, the more the history is represented by Y(n-1) outputs in the equation. It is a tradeoff between response times to change in input value versus the noise attenuation.

The filter can be turned off by setting the filter coefficient to 1 (IIRFC = 0b111). The filter can be temporarily bypassed by setting AMENDFILT = 0; this is useful when performing periodic safety and diagnostic checks, as the filtered main measurement results will be preserved within the filter memory registers. Both filtered and raw result data can be read back using the RDFILT option.

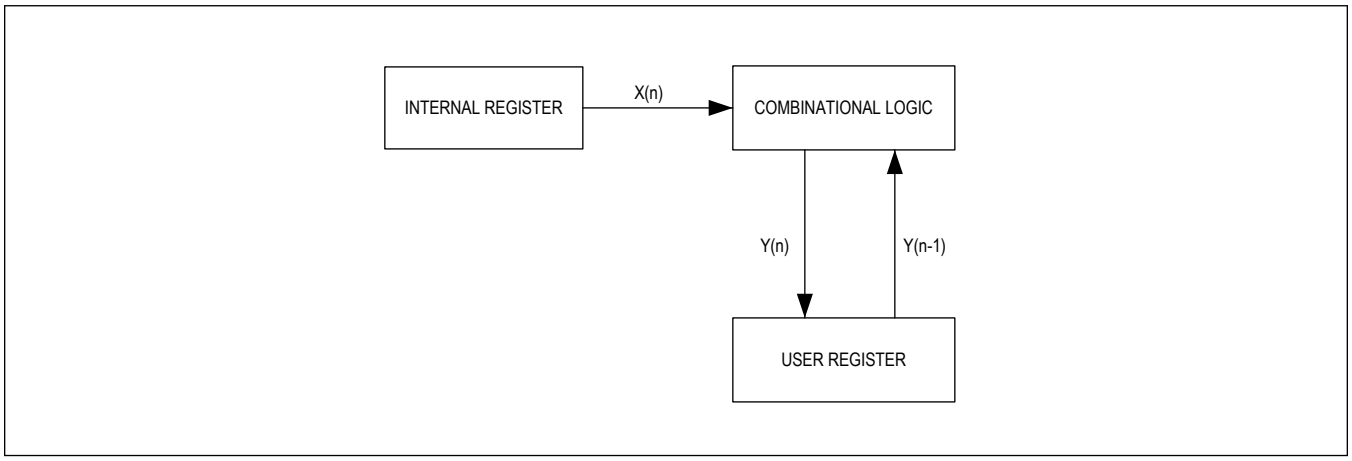


Figure 29. IIR Filter Algorithm

Filter Response

The IIR filter provides a means to improve measurement noise rejection at a cost of increased settling time. This tradeoff can be managed by selecting the proper IIR filter coefficient for the application. Table 26 shows the number of samples taken by the IIR filter to settle a full-scale step (ex. 0V to 100mV unipolar cell transition) to 12-bit and 14-bit accuracy. Note this settling time can be significantly shortened after power-up, or when operating mode changes require large step responses by using the MEASUREEN2:SCANIIRINIT or BALCTRL:CBIIRINIT initialization options, which accelerate

settling by loading the next acquired sample into the filter's accumulated result memory. See the *Typical Operating Characteristics* section for a typical operating behavior of that filter.

Table 26. IIR 100mV Step Response Settling

IIRFC SETTING:	0b000	0b001	0b010	0b011	0b100	0b101	0b110	0b111
IIR FILTER COEFFICIENT (FC):	**1/8**	**1/4**	**3/8**	**1/2**	**5/8**	**3/4**	**7/8**	**1**
12-Bit Settling (# Samples):	33	16	10	7	5	4	3	1
14-Bit Settling (# Samples):	44	21	13	9	6	5	3	1

IIR Data Control

The control of ADC data into and around the IIR filter is performed using dedicated register bits (AMDENDFILT, RDFILT, ALRTFILT) in the SCANCTRL register. The following sections detail this operation.

AMENDFILT and RDFILT

The AMENDFILT bit directs the ALU data into the IIR for filtering operations or around the IIR filter to the output data registers (BLOCKREG 0x55).

When the AMENDFILT bit is deasserted, the ADC acquisition in the ALU is not transferred into the IIR accumulator at the end of the scan sequence. This setting should be used for diagnostic operations which disrupt the input data or for operations which utilize a different measurement path, as both operations would corrupt the normal data. Examples of measurement modes that disrupt the input data are when the cell test current sources or HVMUX test current sources are enabled using the CTSTEN bit and MUXDIAGEN bits respectively. Alternatively, when AMENDFILT is asserted, the ADC acquisition in the ALU is automatically scaled and transferred into the IIR accumulator at the end of the scan sequence.

The RDFILT bit determines if IIR filtered data or normal acquisition data is read from the output data registers is issued (BLOCKREG 0x55). See the *Single-Buffer Mode* and *Double-Buffer Mode* sections for details on how the RDFILT affects data transfer.

Note:

If DBLBUFEN = 0 and SCAN = 1, the ALU results are loaded into the IIR automatically at the end of the requested measurement sequence.

If DBLBUFEN = 1 and SCAN = 1, the ALU results are loaded into the IIR automatically at the beginning of the following sequence.

If DBLBUFEN = x and SCAN = 0, the ALU results are loaded into the IIR during the requested data move sequence if DATARDY = 0.

Table 27 shows the interactions that can occur between the IIR data control settings:

Table 27. IIR Data-Control Settings

AMENDFILT	RDFILT	USAGE
0	0	IIR Filter Disabled
0	1	Potential Stale Data Fetch IIR is not updated, but the IIR results are read. **Note:** This operation is not recommended.
1	0	Reads Current Unfiltered Acquisition Data: IIR is updated, but the current acquisition is read. See the *Out-of-Scan Data Transfer* section for information on reading both filtered and unfiltered results.
1	1	IIR Filter Updated and IIR Filter Read

ALRTFILTSEL

When IIR filter operation is enabled, there are two possible data sources for user access: the raw sequencer outputs (oversampling still applies) or the IIR filtered outputs. The Alert Filtering Selection bit, ALRTFILTSEL, is used to select one of these outputs to generate the relevant alerts.

When ALRTFILTSEL = 0, the raw sequencer outputs are used. This data source is used to assert all related alert bit assertions, calculate MINMAXCELL and TOTAL registers, and perform cell mismatch MSMTCH checks.

When ALRTFILTSEL = 1, the IIR filtered data is used. This IIR data is used to assert all related alert bit assertions, calculate MINMAXCELL and TOTAL registers, and perform cell mismatch MSMTCH checks.

Regardless of the ALRTFILTSEL settling, the DIAG1 and DIAG2 registers always come from the unfiltered sequencer outputs.

IIR Initialization

When IIR operation is engaged, the data to be operated upon initially is controlled by the Sequencer IIR Initialization Request bit, SCANIIRINIT.

By default, SCANIIRINIT = 0, and the IIR filter is in Continuation mode. In Continuation mode, the current value in the IIR accumulators is kept (presumably from previous cell measurements) and sequencer measurements are amended normally.

When SCANIIRINIT = 1, the IIR filter is in Initialization mode. In Initialization mode, the IIR accumulators are reinitialized to the first measurement taken, and further cell-balancing measurements are amended normally.

Single-Buffer Mode

The Single-Buffer mode (Figure 30) is activated when DBLBUFEN = 0. In this mode, data is moved to the CELLnREG, AUXnREG, BLOCKREG, DIAG1REG, DIAG2REG, TOTALREG, and MINMAXCELL registers at the end of the scan, indicated by SCANDONE = 1 and DATARDY = 1.

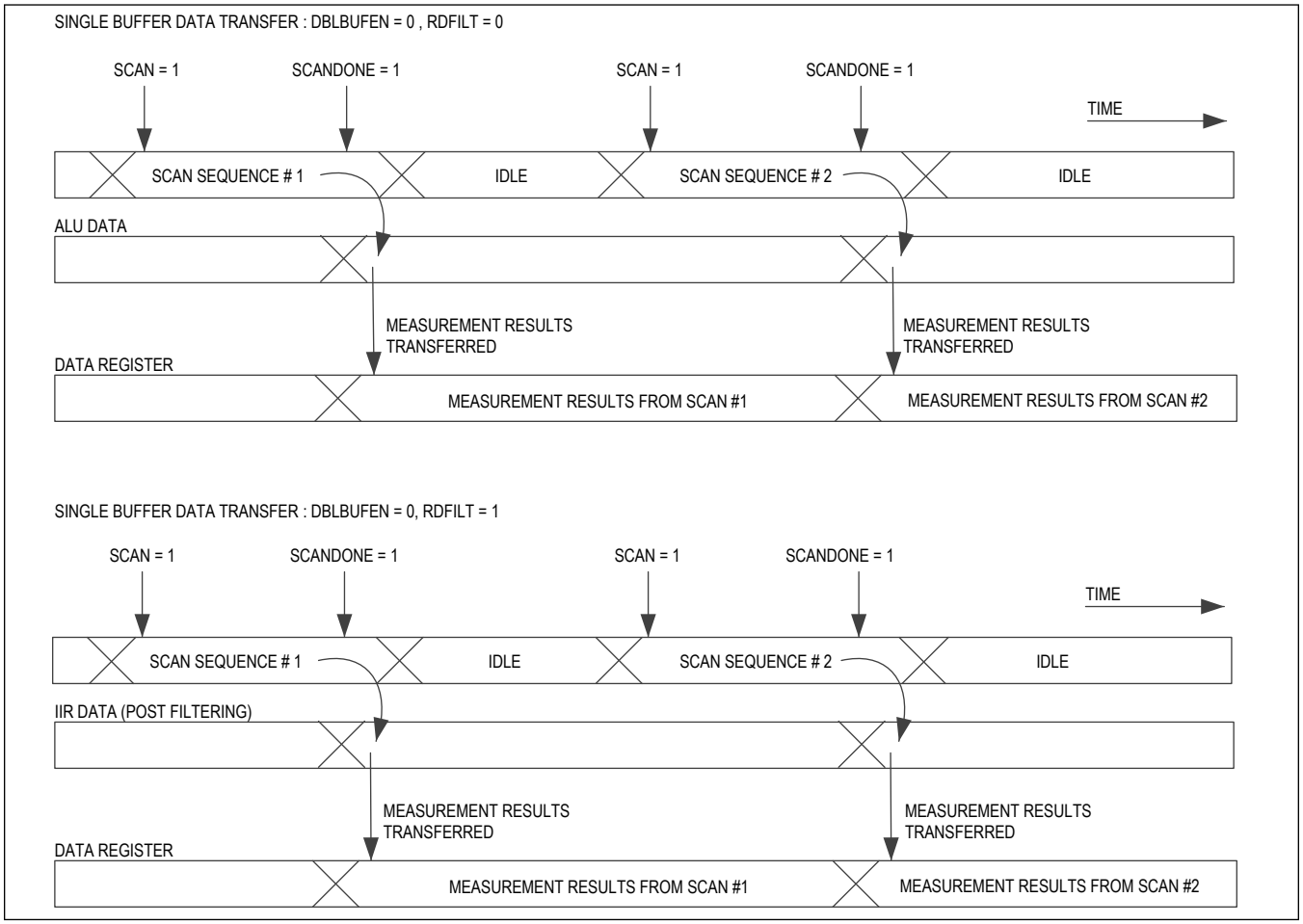


Figure 30. Single-Buffer Data Transfer

Double-Buffer Mode

With DBLBUFEN = 1, the Double Buffer mode (Figure 31) is activated. In this mode, data is moved to the CELLnREG, AUXnREG, BLOCKREG, DIAG1REG, DIAG2REG, TOTALREG, and MINMAXCELL registers at the start of the next scan when SCAN = 1 and is indicated by DATARDY = 1. This allows the host to read data from the last scan while the current scan is in progress. In the event that a final measurement is requested prior to a sleep or shutdown event, the host would need to issue another SCAN request to force the data transfer from the last acquisition or move the data through the out-of-scan data transfer method.

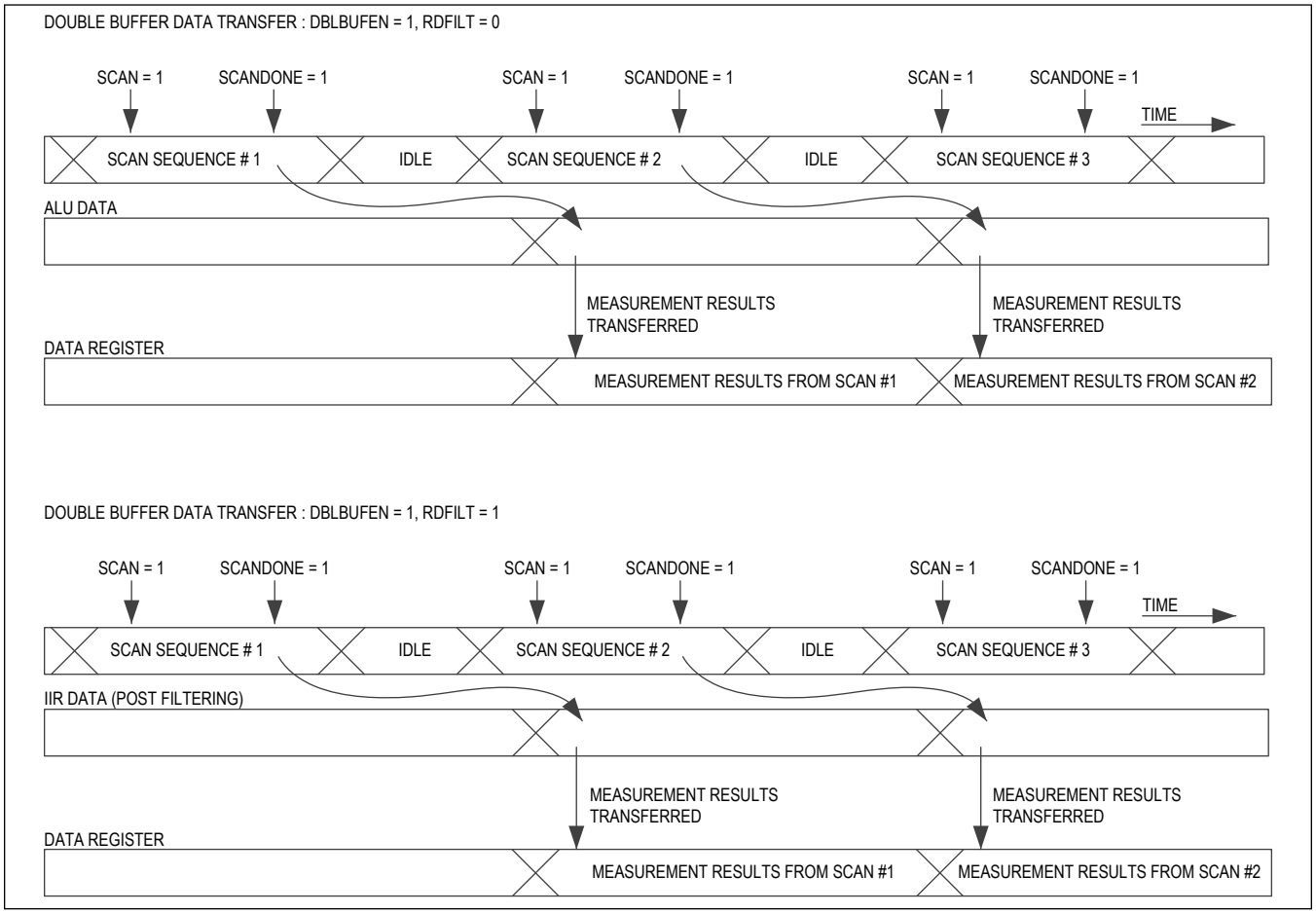


Figure 31. Double-Buffer Data Transfer

Out-of-Scan Data Transfer

Out-of-scan data transfer occurs in the period after a scan is complete, indicated by SCANDONE = 1, and before a new scan request (SCAN = 1) is issued by the host. Because the data exists in both the ALU and IIR accumulator, but only one set is transferred to the data registers depending on the RDFILT setting, this procedure allows access to the other set of data that was not transferred to the data registers. By setting DATARDY = 0, RDFILT = 0 and SCAN = 0, data from the ALU is transferred to the data registers. By setting DATARDY = 0, RDFILT = 1 and SCAN = 0, data from the IIR accumulator is transferred to the data registers.

If an out-of-scan data transfer is issued, the MINMAXCELL, TOTAL, and MSMTCH registers are not updated when changing RDFILT and SCAN = 0. Additionally, out-of-scan alert processing is not updated when changing ALRTFILTSEL and SCAN = 0. If updated data processing is required, a new acquisition (SCAN = 1) must be requested.

Cell Balancing with Embedded Measurement Data Control

The data control for cell balancing with embedded measurements is controlled by the CBSCAN bit in the BALDATA register. This bit acts as a strobe, and the CBSCAN bit content is automatically cleared, reading back a logic 0 when polled.

Upon writing CBSCAN (and after any auto cell-balancing measurement operation in complete), all enabled conversion parameters are updated in the CELLnREG, AUXnREG, BLOCKREG, DIAG1REG, DIAG2REG, TOTALREG, and MINMAXCELL output registers. See the *Cell Balancing* section for further detail.

Measurement Alerts

After the acquisition, the ALU compares the enabled measurement data to the enabled OV/UV thresholds for both measurement paths (ADC and comparator) as shown in Table 28. If outside of the configured threshold, the associated alert bit is set during data transfer into the ALU or IIR ALU blocks. In the event that calibration is enabled using the ADCCALEN bit, the digital correction is performed prior to the alert generation. This ensures that the alert is generated from the correct accuracy results.

Note: The ALRTFILTSEL bit for the IIR data control determines if the alerts will be generated upon filtered or unfiltered data.

The data control settings impact the management of alert signaling. The aforementioned alert handling details the Single-Buffer mode data control. Since the Double-Buffer mode allows for simultaneous data offload and acquisition, it is recommended to read the alert status after SCANDONE for the current acquisition and prior to initiating the next acquisition.

Table 28. Measurement Alerts

DESCRIPTION	SIGNAL PATH	CONDITION OR RESULT	ALERT BIT	LOCATION
Cell overvoltage (OV)	ADC	$V_{Cn} - V_{Cn-1} > V_{OVTHSET}$ for POLARITYn = 0	ALRTCELLOVST, ALRTADCOVST, ALRTOVn	STATUS1, ALRTSUM, ALRTOVCELL
	COMP	$V_{Cn} - V_{Cn-1} > V_{COMPOVTH}$	ALRTCELLOVST, ALRTADCOVST, ALRTCOMPOVn	STATUS1, ALRTSUM, ALRTCOMPOVREG
Cell undervoltage (UV)	ADC	$V_{Cn} - V_{Cn-1} < V_{UVTHSET}$ for POLARITYn = 0	ALRTCELLUVST, ALRTADCUVST, ALRTUVn	STATUS1, ALRTSUM, ALRTUVCELL
	COMP	$V_{Cn} - V_{Cn-1} < V_{COMPUVTH}$	ALRTCELLUVST, ALRTADCUVST, ALRTCOMPUVn	STATUS1, ALRTSUM, ALRTCOMPUVREG
Bipolar cell/bus-bar overvoltage (OV)	ADC ONLY	$V_{Cn} - V_{Cn-1} > V_{BIPOVTHSET}$ for POLARITYn = 1	ALRTCELLOVST, ALRTADCOVST, ALRTOVn	STATUS1, ALRTSUM, ALRTOVCELL
Bipolar cell/bus-bar undervoltage (UV)	ADC ONLY	$V_{Cn} - V_{Cn-1} < V_{BIPUVTHSET}$ for POLARITYn = 1	ALRTCELLUVST, ALRTADCUVST, ALRTUVn	STATUS1, ALRTSUM, ALRTUVCELL
Block overvoltage (OV)	ADC ONLY	$V_{BLK} > V_{BLKOVTHSET}$	ALRTBLKOV	STATUS1
Block undervoltage (UV)	ADC ONLY	$V_{BLK} < V_{BLKUVTHSET}$	ALRTBLKUV	STATUS1
Cell mismatch	ADC ONLY	$V_{MAX} - V_{MIN} > V_{MSMTCH}$	ALRTMSMTCH	STATUS1
Cell with minimum voltage	ADC ONLY	n where $V_{CELLn} = V_{MIN}$ Unipolar if MINMAXPOL= 0, else bipolar	None	MINMAXCELL
Cell with maximum voltage	ADC ONLY	n where $V_{CELLn} = V_{MAX}$ Unipolar if MINMAXPOL= 0, else bipolar	None	MINMAXCELL
Total of all cell voltages	ADC ONLY	ΣV_{CELLn} for n = 1 to TOPCELL1/2	None	TOTAL
AUXINn overvoltage (undertemperature)	ADC	$V_{AUXINn} > (V_{AUXROVTHSET}$ or $V_{AUXAOVTHSET})$	ALRTAUXOVST, ALRTADCAUXOVST, ALRTAUXOVn	STATUS1, ALRTSUM, ALRTAUXOV

Table 28. Measurement Alerts (continued)

	COMP	V_{AUXINn} > ($V_{COMPAUXROVTH}$ or $V_{COMPAUXAOVTH}$)	ALRTAUXOVST, ALRTCOMPAUXOVST, ALRTCOMPAUCOVn	STATUS1, ALRTSUM, ALRTCOMPAUXOV
AUXINn undervoltage (overtemperature)	ADC	V_{AUXINn} < ($V_{AUXRUVTHSET}$ or $V_{AUXAUVTHSET}$)	ALRTAUXUVST, ALRTADCAUXUVST, ALRTAUXUVn	STATUS1, ALRTSUM, ALRTAUXUV
	COMP	V_{AUXINn} < ($V_{COMPAUXRUVTH}$ or $V_{COMPAUXAUVTH}$)	ALRTAUXUVST, ALRTCOMPAUXUVST, ALRTCOMPAUCUVn	STATUS1, ALRTSUM, ALRTCOMPAUXUV

Voltage Alerts

The ALRTOVEN and ALRTUVEN registers are configured to enable voltage alerts for the cell and block inputs. These alerts have programmable OV/UV set thresholds, as well as programmable OV/UV clear thresholds, allowing for programmable hysteresis in both OV or UV measurements as mentioned in Table 29. This is beneficial for the programming of alert detection in lithium-ion (Li+) cells where there are different characteristics at fully charged and discharged states.

Overvoltage alerts in the ALRTOVCELL or ALRTCOMPOVREG registers are set when the CELLn voltage exceeds the programmed threshold voltages $V_{OVTHSET}$ and $V_{COMPOVTH}$, respectively. Alternatively, undervoltage alerts in the ALRTUVCELL and ALRTCOMPUVREG registers are set when the CELLn voltage exceeds the programmed threshold voltage $V_{UVTHSET}$ and $V_{COMPUVTH}$, respectively. It is important to note that, due to the different resolutions of the ADC and comparator (described in the *ADC Input Range* and *Comparator Input Range* sections), the user may experience a condition where the alert for the ADC may be set while the alert for the comparator my be cleared and vice versa.

Note: ADC alerts provide the most accurate indications of the acquisition.

Alerts are cleared when the cell voltage moves in the opposite direction and crosses the OVTHCLR, COMPOVTH and UVTHCLR, COMPUVTH thresholds. The voltage must cross the threshold; if it is equal to a threshold, the alert flag does not change. Therefore, setting the overvoltage set threshold to full-scale, or setting the undervoltage set threshold to zero-scale, effectively disables voltage alerts independent of the ALRTOVEN and ALRTUVEN.

Table 29. Set- and Clear-Threshold Selection

DESCRIPTION	SIGNAL PATH	OVERVOLTAGE THRESHOLD	UNDERVOLTAGE THRESHOLD	OV HYSTERESIS	UV HYSTERESIS
Cell	ADC	OVTHSET	UVTHSET	OVTHCLR	UVTHCLR
Cell	COMP	COMPOVTH	COMPUVTH	Not applicable	Not applicable
Bus bar	ADC	BIPOVTHSET	BIPUVTHSET	BIPOVTHCLR	BIPUVTHCLR
Block	ADC	BLKOVTHSET	BLKUVTHSET	BLKOVTHCLR	BLKUVTHCLR

Alert conditions for the individual ADC cell inputs are summarized using the ALRTADCOVST and ALRTADCUVST bits in the ALRTSUM register and occur when any alert bit is set in the ALRTOVCELL or ALRTUVCELL registers, respectively. Similarly, alert conditions for the individual comparator cell inputs are set using the ALRTCOMPOVST and ALRTCOMPUVST bits in the ALRTSUM register when any alert bit is set in the ALRTCOMPOVREG or ALRTCOMPUVREG registers, respectively. To ease identification of any OV/UV alerts, both ADC summary alerts and comparator summary alerts are further logically OR'ed and summarized in the ALRTCELLOVST and ALRTCELLUVST bits in the STATUS1. This enables the alert information to get propagated using the hardware alert interface or the data check byte.

Alert conditions for the block input are directly summarized using the ALRTBLKOVST and ALRTBLKUVST bits in the STATUS1 register when the acquired BLOCK voltage is over $V_{BLKOVTHSET}$ or under $V_{BLKUVTHSET}$, respectively.

If an alert does not need to be propagated using the alert interface or data check byte, these can be individually masked. See the *Alert Interface* section for further details on the masking.

The cell and block voltage hysteresis diagram is as shown in Figure 32.

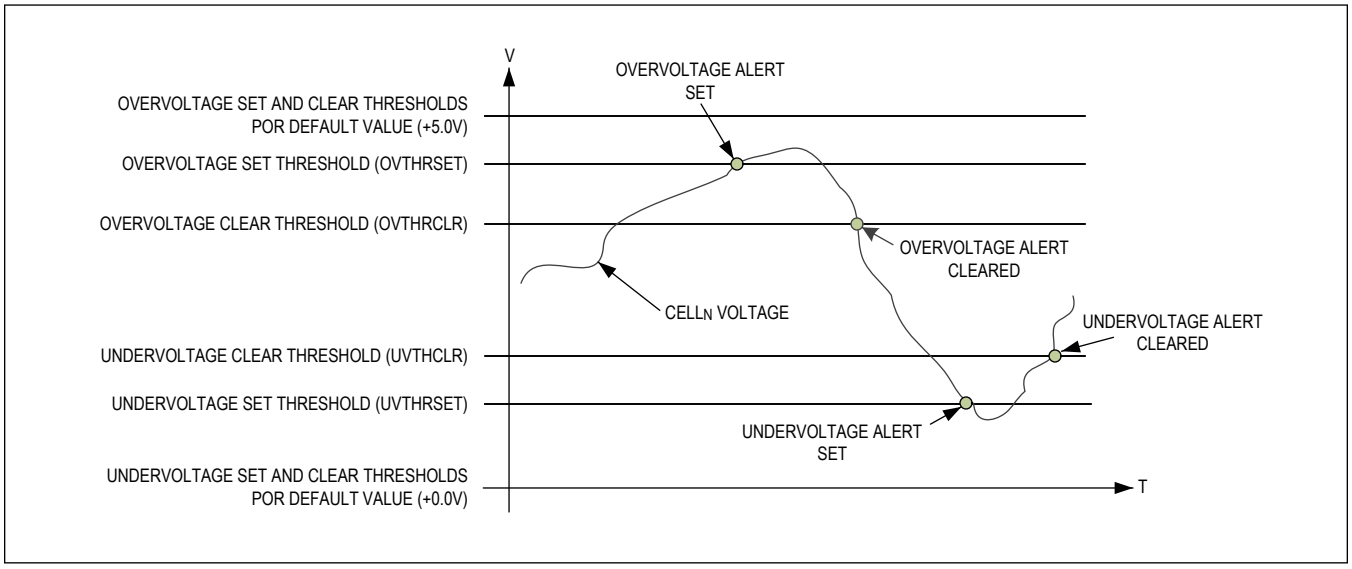


Figure 32. Cell Voltage-Alert Thresholds

Cell Mismatch

Enable the mismatch alert to signal when the minimum and maximum cell voltages differ by more than a specified voltage. The MSMTCHREG register sets the 14-bit threshold ($V_{MSMTCHREG}$) for the mismatch alert, ALRTMSMTCH. Whenever $V_{MAX} - V_{MIN} > V_{MSMTCHREG}$, then ALRTMSMTCH = 1. The alert bit is cleared when a new acquisition does not exceed the threshold condition. To disable the alert, write 3FFFh to the MSMTCHREG register bitfield (default value).

Cell Statistics

The cell numbers corresponding to the lowest and highest enabled voltage measurements are stored in the MINCELL, MAXCELL bitfields. When multiple cells have the same minimum or same maximum voltage, only the lowest cell position having that voltage is reported. For acquisitions with no enabled cell inputs, the MINCELL, MAXCELL, and TOTAL bitfields are not updated.

The RDFILT bit determines the source data (filtered/unfiltered) used for the MINCELL, MAXCELL bitfields and TOTALREG (x56) register.

The MINMAXPOL bit ensures that only like measurements are used for the statistical processing of MINCELL, MAXCELL, and ALRTMSMTCH. This ensures that bus bars do not affect the cell statistics in mixed-mode acquisitions. When MINMAXPOL = 0 only unipolar measurements are used. When MINMAXPOL = 0b1, only bipolar measurements are used.

Note: For Li+ applications, MINMAXPOL should be configured for unipolar statistics, while fuel-cell application should be configured for bipolar statistics.

The sum of all enabled cell voltages, regardless of the POLARITY configuration, is stored in the TOTAL register as a 16-bit value.

Example:

Assume four cell inputs are enabled—CELL1, CELL2, CELL3, and CELL4—where CELL1, CELL2 are configured as unipolar, CELL3 as bipolar, and CELL4 as unipolar. The measured values after the acquisition read 2V, 2V, -1V, and 2.5V, respectively.

The TOTALREG register reads:

TOTAL = 2 + 2 - 1 + 2.5 = 5.5V

The MINCELL bitfield reads CELL1 and the MAXCELL bitfield reads CELL4.

Temperature Alerts

The ALRTAUXOVEN and ALRTAUXUVEN registers are configured to enable the temperature alerts for the enabled AUXn inputs. Like the cell-voltage alerts, the temperature alerts have programmable OV/UV set thresholds as well as programmable OV/UV clear thresholds to provide user-programmable hysteresis to avoid unwanted alerts in the presence of measurement noise, as shown in Table 30.

Table 30. Temperature Alert Threshold

DESCRIPTION	SIGNAL PATH	TYPE	OVERVOLTAGE THRESHOLD/ UNDERTEMPERATURE	UNDERVOLTAGE THRESHOLD/ OVERTEMPERATURE	HYSTERESIS OV	HYSTERESIS UV
AUXINn	ADC	Ratiometric	AUXROVTHSET	AUXRUVTHSET	AUXROVTHCLR	AUXRUVTHCLR
AUXINn	ADC	Absolute	AUXAOVTHSET	AUXAUVTHSET	AUXAOVTHCLR	AUXAUVTHCLR
AUXINn	COMP	Ratiometric	COMPAUXROVTH	COMPAUXRUVTH	Not applicable	Not applicable
AUXINn	COMP	Absolute	COMPAUXAOVTH	COMPAUXAUVTH	Not applicable	Not applicable

Overvoltage alerts in the ALRTAUXOV or ALRTCOMPAUXOV registers are set when the AUXn voltage exceeds the programmed threshold voltages of $V_{AUXAOVTHSET}$ OR $V_{AUXROVTHSET}$ and $V_{COMPAUXAOVTH}$ OR $V_{COMPAUXROVTH}$, respectively. The appropriate threshold used is determined by the AUXREFSEL bits, which can be different per channel. Alternatively, undervoltage alerts in the ALRTAUXUVREG and ALRTCOMPAUXUVREG registers are set when the AUXn voltage exceeds the programmed threshold voltage $V_{AUXUVTHSET}$ OR $V_{AUXRUVTHSET}$ and $V_{COMPAUXRUVTH}$ OR $V_{COMPAUXAUVTH}$, respectively. It is important to note that, due to the different resolutions of the ADC and comparator (described in the *ADC Input Range* and *Comparator Input Range* sections), the user may experience a condition where the alert for the ADC may be set while the alert for the comparator may be cleared and vice versa.

Note: An OV alert for the ratiometric acquisition signals an undertemperature (UT) event for the NTC measurement, and an UV alert signals an overtemperature (OT) event for the NTC measurement.

Alerts are cleared when the cell voltage moves in the opposite direction and crosses the AUXROVTHCLR,AUXAOVTHCLR and AUXRUVTHCLR,AUXAUVTHCLR thresholds. The voltage must cross the threshold; if it is equal to a threshold, the alert flag does not change. Therefore, setting the overvoltage set threshold to full-scale, or setting the undervoltage set threshold to zero-scale, effectively disables voltage alerts independent of ALRTAUXOVEN and ALRTAUXUVEN.

Alert conditions for the individual ADC auxiliary inputs are summarized using the ALRTADCAUXOVST and ALRTADCAUXUVST bits in the ALRTSUM register and occur when any alert bit is set in the ALRTAUXOV or ALRTAUXUV bitfields, respectively.

Note: The ALRTSUM alert status does not specify the auxiliary input measurement mode in AUXREFSEL. However, this can be determined from polling the alert channel within ALRTAUXOV or ALRTAUXUV.

Similarly, alert conditions for the individual comparator auxiliary inputs are set using the ALRTCOMPAUXOV and ALRTCOMPAUXUV bits in the ALRTSUM register when any alert bit is set in the ALRTCOMPAUXOVSTREG or ALRTCOMPAUXUVREG registers, respectively.

To ease identification of any OV/UV alerts, both ADC summary alerts and comparator summary alerts are further logically OR'ed and summarized in the ALRTAUXOVST and ALRTAUXUVST bits in the STATUS1. This enables the alert information to get propagated using the hardware alert interface or the data check byte.

Cell Balancing

Cell balancing may be performed using any combination of the 14 internal cell-balancing switches according to the programming of the enabled BALSWCTRL:BALSWEN configuration and POLARITYCTRL configuration. Each configured channel performs cell balancing according to the configured operational mode, which includes manual or automatic balancing, discharge control using a timer and/or undervoltage threshold, and duty cycle configuration.

Cell-Balancing Mode Configurations

Cell balancing is initiated using the CBMODE bits in the BALCTRL register. This selection defines automatic versus manual balancing control, channel timer configuration, and timer resolution. Once a CBMODE mode is selected and started, the device remains in this mode until a new value is written to CBMODE, or until a successful exit criteria is

achieved from all enabled conditions (UV threshold, timer, and thermal).

To determine the current state of cell balancing, the CBACTIVE bits can be polled using the BALCTRL, BALSTAT or BALUVSTAT registers. The current timer value can be read through CBTIMER, a 1Hz alive counter can be read through CBCNTR. The timer units (i.e., second, minute, hour) can be read through CBUINT. These status registers are only cleared when CBMODE is written to a new mode or disabled. The combination of these bitfields allow for user verification that the cell-balancing machine is responsive; meanwhile, an internal health check is performed prior to verify a hardware integrity prior to balancing. ALRTCBTIMEOUT notifies the user of a health check failure (if one is found).

Once a CBMODE mode is selected and started, the device remains in this mode until a new value is written to CBMODE. Note that all CBMODE active operations automatically end due to either timer expiration(s), thermal faults, and/or cell UV thresholds being met. In these cases, the CBMODE is still engaged, although the balancing operation is ended. The status of the operation can be checked by reading the BALSTAT and BALUVSTAT registers.

After cell balancing is initiated, write access to specific cell-balancing registers is blocked; if a write to a blocked register is attempted, it will be ignored and the ALRTRJCT flag will be set in the STATUS2 register. See Table 31 for specific register behavior. Note that blockage operations are implemented at the register level.

Table 31. Cell-Balancing Register Write Behavior when Cell Balancing Is Selected

REGISTER	BITFIELD	AUTO (INDIVIDUAL OR GROUP) MODE (1xx)			MANUAL MODE (01x)			EMERGENCY DISCHARGE MODE (001)		
		Data applicable in this mode?	Write accepted in this mode?	ALRT-RJCT Status	Data applicable in this mode?	Write accepted in this mode?	ALRT-RJCT Status	Data applicable in this mode?	Write accepted in this mode?	ALRT-RJCT Status
BALSWCTRL	CBRESTART	No	No	1	Yes	Yes	-	No	Yes	-
	BALSWEN	Yes	No		Yes	Yes		No	Yes	
BALEXP1	BALEXP1	Yes	No	1	Yes	No	1	Yes	No	1
BALEXP2-14	BALEXP2-14	Yes	No	1	No	Yes	-	No	Yes	-
BALAUTOUVTHR	CBUVTHR	Yes	No	1	No	Yes	-	No	Yes	-
	CBUVMINCELL	Yes	No		No	Yes		No	Yes	
BALDLYCTRL	CBNTFYCFG	Yes	No	1	No	Yes	-	Yes	No	1
	CBCALDLY	Yes	No		No	Yes		Yes	No	

Note: The CBRESTART is a strobe bit to manually restart/refresh the watchdog timer during manual mode cell-balancing operation. Although this can be written in other balancing modes, no internal action is taken.

Note: Writes to the BALSWEN bitfields during manual cell-balancing mode are expected and supported.

Note: Writes to BALAUTOUVTHR with CBUVMINCELL = 1 are rejected if a measurement scan is in progress (since data from the last completed scan is used to populate CBUVTHR).

Any value (re)written to CBMODE other than 000 (disable) will restart the CBTIMER at zero and (re)launch the requested mode of operation.

Manual Mode

In Manual mode, balance switches (BALSWn) are controlled directly by BALSWEN[14:1] with a watchdog timeout set by CBEXP1 as follows:

BALSWn = BALSWEN[n] & (CBTIMER ≤ CBEXP1) & ~(AUTOBALSWDIS and measurement in progress)

CBTIMER is incremented on a real-time basis, regardless of BALSWEN settings or suspensions for ADC or CAL events. This means the watchdog will time out as set in CBEXP1 once manual cell balancing is initiated.

Manual cell-balancing operations can be temporarily suspended during measurements using the AUTOBALSWDIS feature.

In certain instances, as defined by the AUTOBALSWDIS operation or other manual diagnostic operation, the user may wish to have explicit control of the BALSWEN without the desire to refresh the CBTIMER watchdog. In this case, the user can configure CBEXP1 = 3FFh to disable the timer. Thus, balancing is controlled only using the BALSWEN; this is also equivalent to the cell-balancing behavior supported in Maxim legacy battery-management devices.

CBRESTART is provided as a means to refresh the active balancing switches or the watchdog timer during normal BALSWn cycling operations. CBUVTHR exit settings are ignored; measurements and calibrations operations are requested through normal scan control registers allowing for simultaneous measurements and balancing.

Notes: Writing 1 to CBRESTART after cell-balancing timer expiration has no effect. To perform another manual mode cell-balancing event, the user must issue a separate write to the BALCTRL register.

Manual balancing allows for adjacent balancing switches to turn on simultaneously according to the application requirement. Enabling adjacent balancing switches simultaneously under manual cell-balancing modes increases the balancing current significantly, so care must be taken to not exceed the device's maximum operating conditions.

AUTOBALSWDIS Feature

Configuring AUTOBALSWDIS = 1 automatically disables the balancing switches (in manual cell-balancing modes only) during measurements to eliminate the additional voltage drop caused due to cell-balancing application circuits. This ultimately allows the system to achieve higher accuracy cell measurements to help calculate higher accuracy of state of charge (SoC).

Measurement settling time control for cell measurement (CELLDLY) and BALSW diagnostic/ALTMUX (SWDLY) is configured in the BALSWDLY register. These delay registers provide programmable settling (wait) times from 0µs up to 24.57ms, in steps of 96µs, between the time when the acquisition is enabled and the start of actual measurement to allow for the external application circuit to settle to accurate voltages. In the BALSWDLY register, CELLDLY is the upper 8-bit delay setting for cell recovery time, while SWDLY is the lower delay setting for certain diagnostics such as sense wire open. When AUTOBALSWDIS = 1 and ALTMUXSEL = 0, CELLDLY is selected. When AUTOBALSWDIS = 1 and ALTMUXSEL sets to 1, SWDLY is selected. Hence, this feature can be used during normal cell measurements as well as during diagnostic measurements with two separate delay timers which can be independently set. Any write to the BALSWDLY register will be ignored, signaled by ALRTRJCT, while a measurement sequence or an auto cell-balancing mode is active.

Note: The appropriate delay time is dependent on the application circuit and the level of accuracy required. For the typical application circuit on the cell input, utilizing a input filter network of 1kΩ and 0.1µF, it is recommended to choose a settling time of 960µs to achieve calibrated accuracy specified in the *Electrical Characteristics* table.

Note: AUTOBALSWDIS effects cell-balancing switch behavior in manual cell-balancing modes only.

Note: Cell-balancing timer incrementing/expiration behavior is not effected by the AUTOBALSWDIS setting.

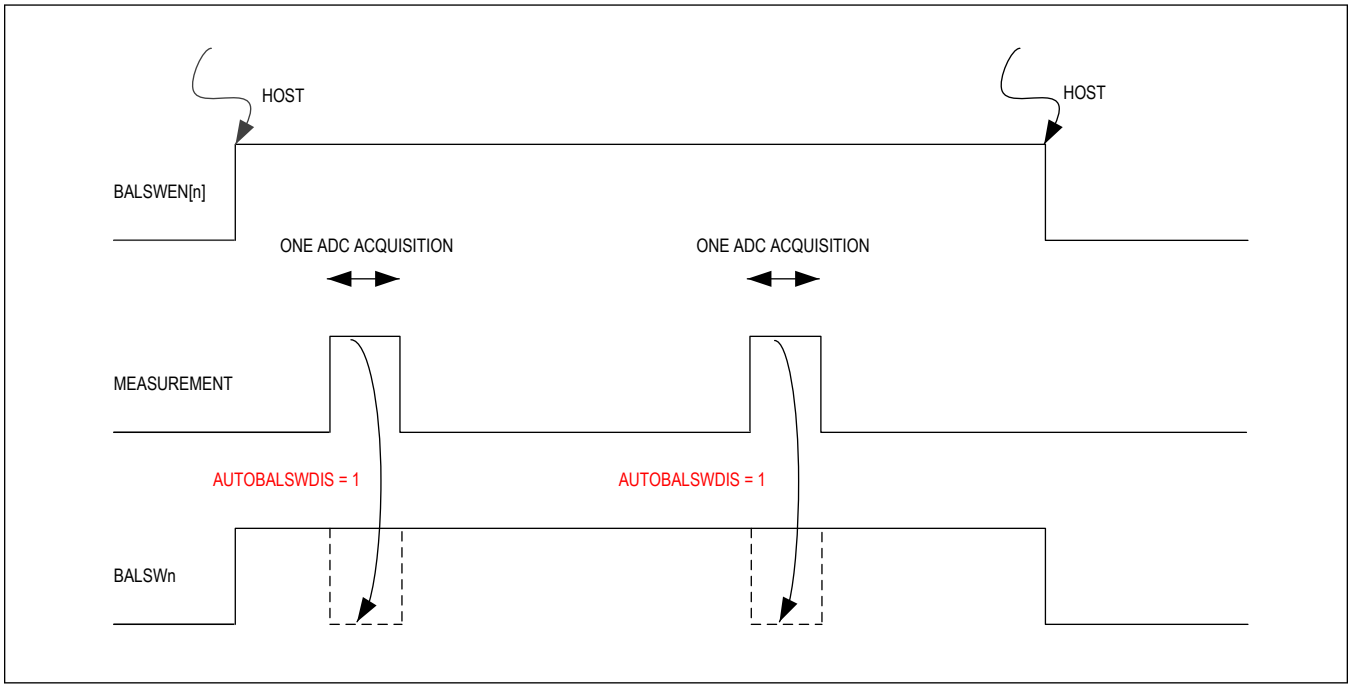


Figure 33. Logic Diagram when Balancing Switches Will Be Disabled

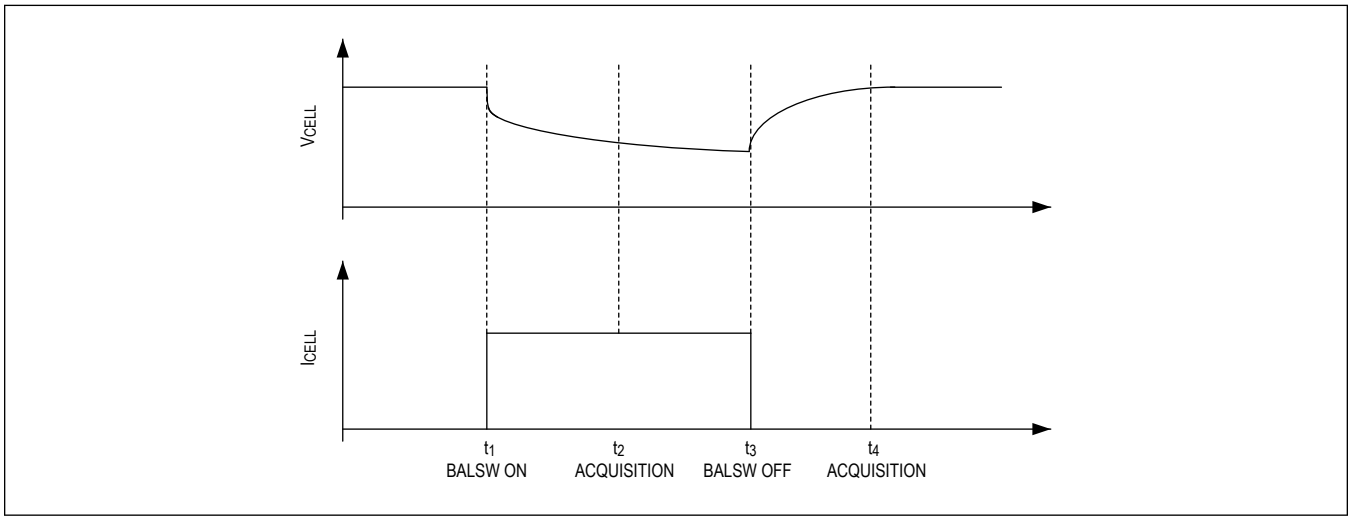


Figure 34. AUTOBALSWDIS Measurement Settling

Manual Cell-Balancing Mode with Flexible-Pack Configuration

During manual cell balancing, the top two consecutive cells should not be enabled for manual cell balancing. This creates a situation where $SW_{TOPCELL1/2}$, $SW_{TOPCELL1/2-1}$, and $SW_{TOPCELL1/2-2}$ could potentially all be 5V below the TOPCELL1/2 cell input voltage. Although, the MAX17854 digital logic will not prevent user from using such a configuration, ALRTHVUV is expected to trip and the TOPCELL1/2 cell input measurements will not be valid.

Auto Individual Mode

The Auto Individual mode performs cell balancing in a controlled manner so that the cells can be individually discharged for a duration and/or to a specific voltage level, as required in the end application. The host initiates an Auto Individual mode by setting CBMODE to 0b100 (duration is seconds) or 0b101 (duration in minutes), configuring CBEXPn to the desired value (where the LSB = 1 second or minute, respectively), and setting individual BALSWENn bits; a group voltage target can also be set using CBUVTHR.

In Auto Individual mode, the balancing switches defined by BALSWEN[n] are automatically controlled through nonoverlapping even/odd cycling in accordance with the programmable timer duration (CBEXPn) and/or the undervoltage threshold (CBUVTHR). The balancing switch duty cycle can further be controlled using CBDUTY to programmatically set the average balancing current. This is indicated as follows:

Even Cells (2, 4, ... 14):

BALSWn = BALSWEN[n] & (CBTIMER ≤ CBEXPn) & CBEVEN & (((CBMEASEN ==0b11) & (CELLn ≥ CBUVTHR)) | (CBMEASEN != 0b11))

Odd Cells (1, 3, ... 13):

BALSWn = BALSWEN[n] & (CBTIMER ≤ CBEXPn) & CBODD & (((CBMEASEN ==0b11) & (CELLn ≥ CBUVTHR)) | (CBMEASEN != 0b11))

CBUVTHR exit settings apply, and ADC measurement and calibration operations can be performed, if enabled, to support host controller read back.

CBTIMER is incremented on a duty-cycled basis, indicating the time each channel is subject to discharge (i.e., one T_{CBEO} cycle out of each E/O/M discharge cycle). This means, in real time, the discharge operation will always run at least 2x the maximum value set in CBEXPn. As an example, if both an even and odd cells must be balanced for 1 hour and the CBDUTY = 100%, the associated timers would be set accordingly and the operation would last for ~2 hours (accounting for nonoverlap timing). If the CBDUTY is now set to 50% with the same timer settings, the total operation time would extend to ~4 hours.

The read-only counter CBCNTR increments at a 1Hz rate with periodic roll-over at 0b11. The host can read this counter periodically to confirm the auto individual mode is active.

SHDNL operation can be controlled by HOLDSHDNL, preventing device shutdown during auto individual mode in case of an extended lapse in host communication.

Once initiated, Auto Individual mode normally continues to run until CBTIMER reaches max(CBEXPn) or all cells reach the voltage CBUVTHR (whichever comes first, depending on configuration settings). At this point, balancing switch operations cease and CBACTIVE is set to 0b10, indicating a normal exit condition. Cell-balancing checks for thermal, calibration, and watchdog faults apply, if enabled; if any of these conditions occur, switching activity will be halted immediately and CBACTIVE will be set to 0b11, notifying the µC of the result. The cell-balancing timer (CBTIMER) continues to run until expiration (CBEXPn), and HOLDSHDNL extensions are supported, if enabled. This allows the µC to confirm the exit condition.

Auto Group Mode

The Auto Group mode performs cell balancing in a controlled manner so that the cells can be discharged as a group for a duration and/or to a specific voltage level, as required in the end application. The host initiates an Auto Group mode by setting CBMODE to 0b110 (duration is seconds) or 0b111 (duration in minutes), configuring CBEXP1 to the desired value (where the LSB = 1 second or minute, respectively), and setting individual BALSWENn bits; a group voltage target can also be set using CBUVTHR.

In Auto Group mode, the balancing switches defined by BALSWEN[n] are automatic controlled through nonoverlapping even/odd cycling in accordance with the programmable timer duration (CBEXP1) and/or the undervoltage threshold (CBUVTHR). The balancing switch duty cycle can further be controlled using CBDUTY to programmatically set the average balancing current. This is indicated as follows:

Even Cells (2, 4, ... 14):

BALSWn = BALSWEN[n] & (CBTIMER ≤ CBEXP1) & CBEVEN & (((CBMEASEN ==0b11) & (CELLn ≥ CBUVTHR)) | (CBMEASEN != 0b11))

Odd Cells (1, 3, ... 13):

BALSWn = BALSWEN[n] & (CBTIMER ≤ CBEXP1) & CBODD & (((CBMEASEN ==0b11) & (CELLn ≥ CBUVTHR)) | (CBMEASEN != 0b11))

Auto Group modes are identical to Auto Individual modes, except that all timer durations are checked against CBEXP1 (a single expiration event).

Emergency Discharge Mode

The Emergency-Discharge mode performs cell balancing in a controlled manner so that the cells can be discharged in the event of an emergency or battery end-of-life.

The host initiates the Emergency-Discharge mode by setting CBMODE to 0b001 and configures CBEXP1 to the desired value (where the LSB = 1 hour). After Emergency-Discharge mode is activated, battery cells are discharged until CBTIMER expires or CBMODE is set to 0b000 (disabled).

In Emergency-Discharge mode, all balance switches (BALSWn) are enabled regardless of BALSWEN[n] settings, with a CBTIMER duration set by CBEXP1, and they are governed by nonoverlapping even/odd cycling, as follows:

Even Cells (2, 4, ... 14):

BALSWn = (CBTIMER ≤ CBEXP1) & CBEVEN

Odd Cells (1, 3, ... 13):

BALSWn = (CBTIMER ≤ CBEXP1) & CBODD

CBUVTHR exit settings do not apply, but ADC measurement and calibration operations can still performed, if enabled, to support host controller readback.

CBTIMER is incremented on a duty-cycle basis indicating the time each channel is subject to discharge (i.e., one T_{CBEO} cycle out of each E/O/M discharge cycle). This means, in real time, the discharge operation always runs at least 2x the maximum value set in CBEXP1. As an example, if both an even and odd cell must be balanced for 1 hour and the CBDUTY = 100%, the associated timers would be set to 0x3C and the operation would last for ~2 hours (accounting for nonoverlap timing). If the CBDUTY is now set to 50% with the same timer setting, the total operation time would extend to ~4 hours.

The read-only counter CBCNTR increments at a 1Hz rate with periodic rollover at 0b11. The host can read this counter periodically to confirm the Emergency-Discharge mode is active.

SHDNL operation can be controlled by HOLDSHDNL, preventing device shutdown during Emergency-Discharge mode due to the extended lapse in host communication.

Once initiated, Emergency-Discharge mode typically continues to run until CBTIMER reaches CBEXP1. At this point, balancing switch operations cease and CBACTIVE is set to 0b10, indicating a normal exit condition. Cell-balancing checks for thermal, calibration, and watchdog faults apply, if enabled. If any of these conditions occur, switching activity will be halted immediately and CBACTIVE will be set to 0b11, notifying the µC of the result. The cell-balancing timer (CBTIMER) continues to run until expiration (CBEXPn), and HOLDSHDNL extensions are supported, if enabled. This allows the µC to confirm the abnormal exit condition.

Cell-Balancing Modes Summary

Table 32 summarizes the cell-balancing modes supported by the MAX17854.

Table 32. Cell-Balancing Modes

CBMODE[2:0]	DESCRIPTION	CBEXPn[9:0]	TIMER RESOLUTION	TCBEO	RRANGE OF CBEXPn[9:0]	
					MIN	MAX
000b	Cell Balancing Disabled	000h	-	-	-	

Table 32. Cell-Balancing Modes (continued)

001b	Emergency/EOL Discharge by Hour	001h - 3FFh	1hr	0.5min	1hr	1022hr
010b	Manual Cell Balancing by Second	001h - 3FFh	1s	-	1s	1022s
011b	Manual Cell Balancing by Minute	001h - 3FFh	1min	-	1min	1022min
100b	Auto Individual Cell Balancing by Second	001h - 3FFh	1s	0.5s	1s	1022s
101b	Auto Individual Cell Balancing by Minute	001h - 3FFh	1min	0.5min	1min	1022min
110b	Auto Group Cell Balancing by Second	001h - 3FFh	1s	0.5s	1s	1022s
111b	Auto Group Cell Balancing by Minute	001h - 3FFh	1min	0.5min	1min	1022min

Note: T_{CBEO} is the effective time that the even or odd switches are balanced within the timer resolutions

Auto Even-Odd Cell Balancing

Auto even-odd cell-balancing control the enabling of adjacent balancing switches automatically with timing resolution from 1 second to 1 hour, depending on the CBMODE configuration. This ensures that only even or odd switches are not enabled simultaneously, while balancing equally within the balancing period. This allows the host to program the BALSWEN bit once without having adjust the balance switches or timer period, which can be beneficial during system low-power operational modes where the host controller is asleep.

In order to prevent simultaneous channel conduction, a nonoverlap period ($t_{NONOVERLAP}$ = 1µs) is inserted between disabling one switch and enabling the adjacent switch. When the UV threshold is disabled, the total cell-balancing period is (t_{CBEO} + $t_{NONOVERLAP}$) x 2. When the UV threshold is enabled, the cell-balancing period is increased by the ADC measurement time ($t_{MEASUREMENT}$). In this case, the total cell-balancing period is (t_{CBEO} + $t_{NONOVERLAP}$) x 2 + $t_{MEASUREMENT}$.

Note: T_{CBEO} = 1/2 x timer resolution

The measurement time ($t_{MEASUREMENT}$) includes the cell-balancing path recovery delay selection (CELLDLY), a user-programmable delay determined by the external application circuit which is imposed after each pair of even and odd discharge cycles. The other component to the measurement time will include the physical time for ADC acquisition as defined in the SCANCTRL register (OVSAMPL in cell-balancing mode is nonprogrammable and fixed at 16 to ensure the highest accuracy measurements).

Note: CELLDLY is used in manual cell-balancing mode when using AUTOBALSWDIS = 0b1 and ALTMUXSEL = 0b0. Also used in automatic cell-balancing and discharge modes after each pair of even and odd discharge cycles.

CBMODE = 0x4, CBUVTHR = 0x3FF

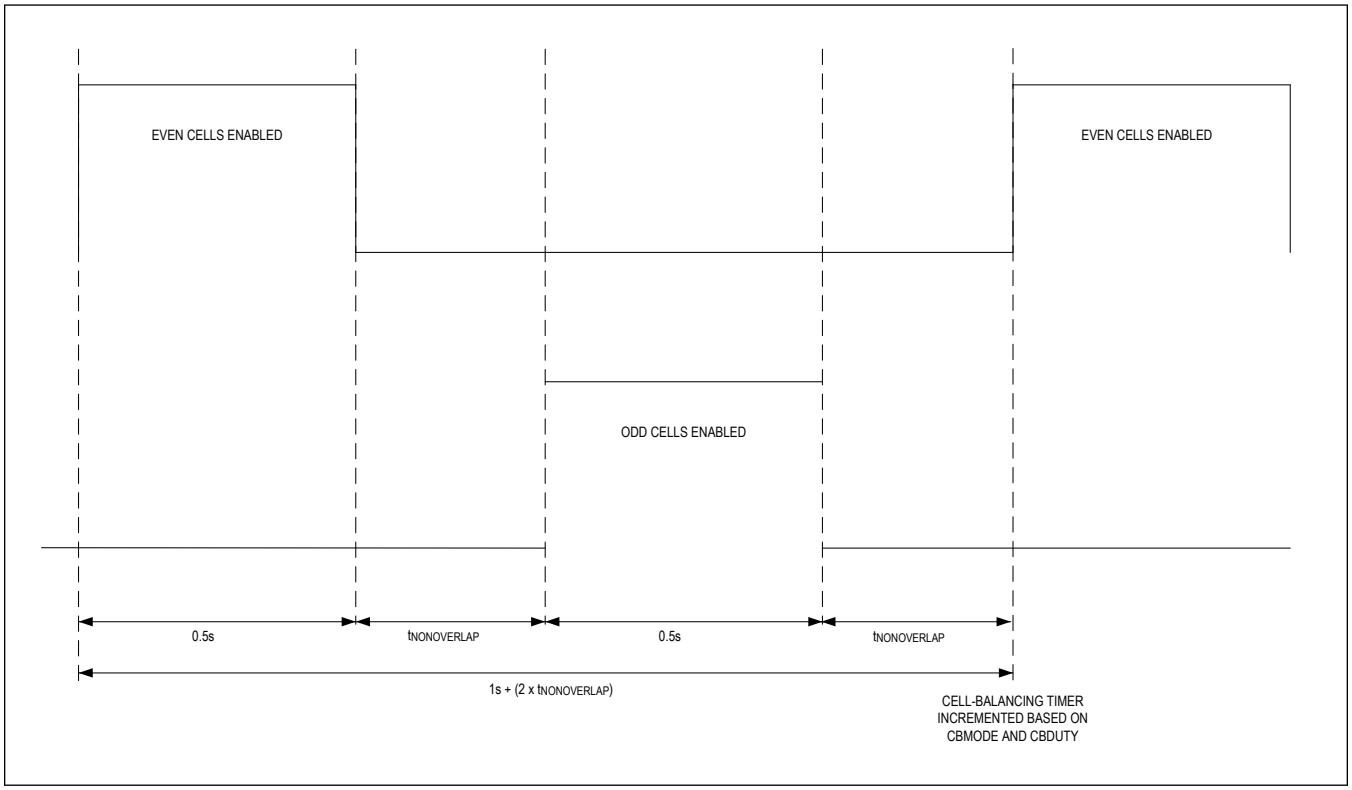


Figure 35. Auto Even and Odd Cell Balancing without UV Detection

CMODE = 5h, FLXPCKEN1/2 = 1, TOPCELL1/2 = ODD

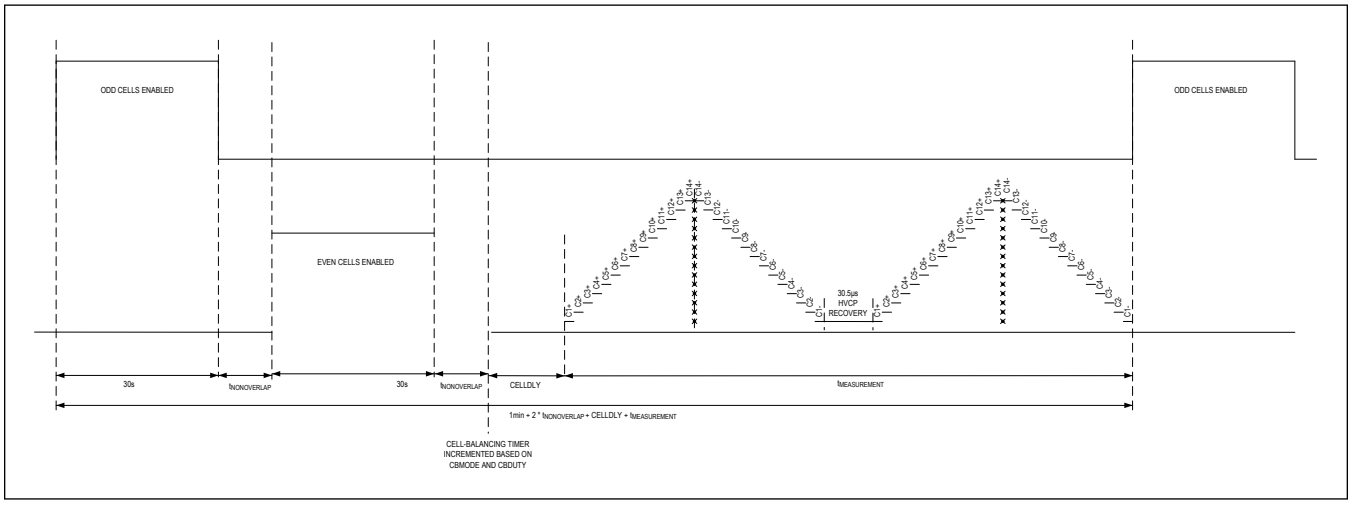


Figure 36. Auto Even Odd Cell Balancing with UV Detection, ADC with OVSAMPL

Note: Figure 35 and Figure 36 are not drawn to exact timescale. Some sections have been exaggerated for visibility. See the *Cell-Balancing UV Detection* section for further details and recommendation for embedded measurements during

cell balancing.

Cell-Balancing Timer - CBTIMER

Manual, Emergency Discharge, and Auto Group Mode Timing: In Manual, Emergency Discharge, and Auto Group modes, the CBEXP1 bitfield within the BALEXP1 register is used as the cell-balancing timer duration setting. The duration can be configured from 1-1023 seconds, from 1-1023 minutes, or from 1-1023 hours depending on the CBMODE setting (LSB = hour, minute, or second). A value of 0x3FF allows the switches to be enabled indefinitely for CELLn if BALSWENn is also enabled (CBTIMER is active, and rolls over at 3FFh, but is not checked against CBEXP1). In Manual, Emergency Discharge, and Auto Group modes, the 10-bit timer (CBTIMER) counts up until it reaches the duration set by BALEXP1. When the cell-balancing timer expires, all cell balancing switches are disabled.

When CBEXP1 is non-zero, the cell balancing timer (CBTIMER) will run and any requested measurement and calibration operations will be performed until expiration, even if BALSWEN[14:1] = 000h (i.e., no balancing switches are actually activated). This ensures that the µC can still access the device to confirm balancing operation progress and exit status.

A value of CBEXP1 = 000h ensures that no cell balancing will occur.

For safety concerns, having all BALEXPn defaulted to 0x000 ensures that no cell balancing will occur without prior configuration.

Auto Individual Mode Timing: In Auto Individual mode, the CBEXPn bits within the BALEXPn registers are used as individual cell-balancing duration times for each corresponding CELLn. Individual durations can be configured from 1–1023 seconds, or from 1–1023 minutes depending on the CBMODE setting (LSB = minute, or second). A value of 0x3FF allows the switches to be enabled indefinitely for CELLn if BALSWENn is also enabled. (CBTIMER will be active and will rollover at 3FFh, but it is not checked against CBEXPn.) The 10-bit expiration timer (CBTIMER) counts up until it reaches the maximum CBEXPn timeout value in the register block (regardless of BALSWENn settings), governing the balancing operations of all balancing switches. When an individual cell expiration time is reached (determined by CBEXPn), the CELLn switch is disabled going forward.

When any CBEXPn is non-zero, the cell-balancing timer runs and any requested measurement and calibration operations are performed until expiration, even if BALSWEN[14:1] = 000h (i.e., no balancing switches are actually activated). This ensures that the µC can still access the device to confirm balancing operation progress and exit status.

If all 14 CBEXPn settings are 000h, no cell balancing will occur for the switches.

General Timing and Safety Features (All Modes): For safety concerns, all BALEXPn are defaulted to 0x000, which ensures that no cell balancing will occur without prior configuration.

The CBTIMER runs to expiration, even if active cell balancing is halted due to UV or thermal exit conditions. This ensures that the µC can still access the part to confirm balancing operation progress and exit status. If an extended SHDNL hold time is requested (HOLDSHDNL = 1x), CBTIMER will read back the governing CBEXP time for the duration of the extended hold interval, allowing the µC to confirm that the requested balancing operation has run to completion.

CBRESTART Usage in Manual Mode

The CBRESTART bit within the BALSWCTRL register must periodically be written to a 1 to restart the watchdog timer and prevent the cell-balancing switches from being automatically disabled due to exiting manual mode when CBTIMER reaches CBEXP1. In the event that a host fails to write the CBRESTART bit or forgets to disable the cell-balancing switches, the cell-balancing watchdog can automatically disable all cell-balancing switches, regardless of the BALSWEN configuration. The cell-balancing watchdog does not modify the contents of the BALSWEN bits within the BALSWCTRL register.

The CBRESTART bit is used in manual cell-balancing mode only. It provides a means to select new BALSW settings and refresh the watchdog timer with a single command.

This bit is ignored and has no effect outside of an active manual cell-balancing operation. If a manual operation was selected and the timer is allowed to expire, the operation must be relaunched with a write to BALCTRL (i.e., CBRESTART will not reinitiate a manual operation that has allowed the CBTIMER to expire).

Emergency-Discharge Mode and CBDUTY Behavior

In Emergency-Discharge mode, CBTIMER is incremented on a duty-cycled basis, indicating the effective time that each channel is subject to discharge. Because the active duty-cycle within each 30s t_{CBEO} period is specified by CBDUTY

register, the CBTIMER is incremented at specified fractions of 30s (see Table 33).

For example, when CBDUTY is set to 1h, CBTIMER is incremented in steps of 3.750s at the end of the E/O/M cycle.

Table 33. Emergency-Discharge Mode

FUNCTION	REGISTER FIELD	CONFIGURATION	BEHAVIOR
Emergency Discharge Duty-Cycle	CBDUTY[3:0]	0x0	Switches on for 6.25% for 30s (1.875s per 30s)
		0x1	Switches on for 12.5% for 30s (3.750s per 30s)
		…	…
		0xF	Switches on for 100% for 30s (less $t_{NONOVERLAP}$)

Note: It is recommended to design the external balancing current at 100% duty cycle operation to avoid potential thermal issues

Notification Alerts Using CBNTFYCFG

In Automatic and Discharge modes, the Cell-Balancing Notification alert (ALRTCBNTFY) can be issued to confirm normal progression of automated operations. The frequency of issuance is 1 hour, 2 hours, or 4 hours in real time (i.e., not CBDUTY-adjusted). Notification alerts will continue to be issued during HOLDSHDNL extension periods.

Cell-Balancing Expiration Timer Summary

In summary, the implementation of the CBTIMER is shown in Figure 37.

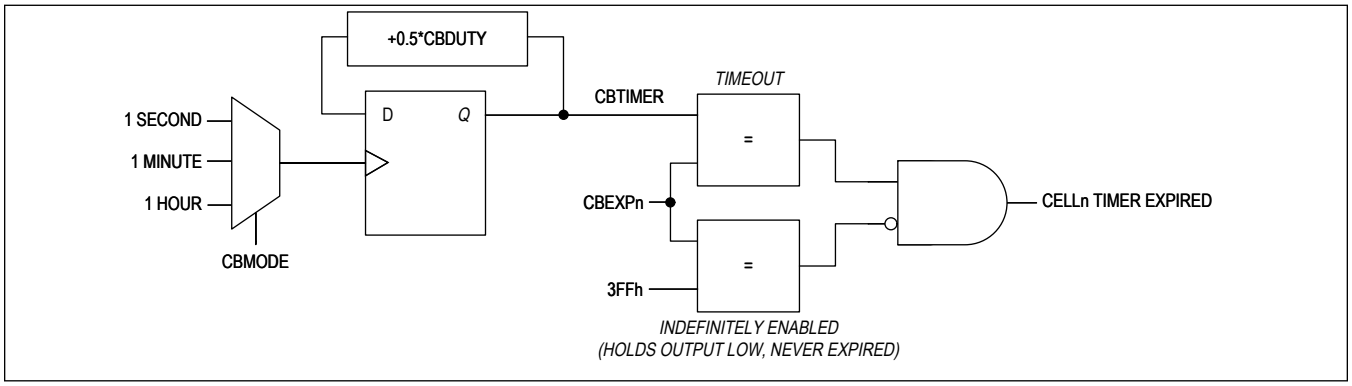


Figure 37. Cell-Balancing Expiration Timer

Note: The CELLn time-expired output feeds into the cell-balancing stop control logic.

Cell-Balancing UV Detection

Cell balancing to a UV threshold allows for all enabled cells configured by BALSWEN to be individually balanced to a specified and uniform voltage level as shown in Figure 38. When a cell reaches the UV threshold, the corresponding balance switch will be disabled and remain in an idle state until reinitialized by the host.

Automatic cell balancing with CBUVTHR checking is only supported for unipolar cell measurements in locations with BALSWEN[n] = 0b1. The user must also ensure CELLEN[n] = 0b1 and POLARITY[n] = 0b0 to allow the required measurement updates. If the measurement is not supported, balancing of the cell automatically ends with a CBUVSTAT[n] = 0b1 exit condition.

CBUVSTAT[n] in the BALUVSTAT register indicates the corresponding CELLn+1 result falls below the threshold specified by CBUVTHR and that cell-balancing operations on that cell have ended. CBUVSTAT[n] is only cleared when CBMODE is written to 0b000 (disabled) or when a new CBMODE operation is initiated through BALCTRL.

Automatic cell balancing to a UV threshold is configured by setting the CBMEASEN bits within the BALCTRL register to 0b11. The UV threshold can be used independently or along side the cell-balancing timer(s) (CBEXP1 or CBEXPn). In the case that a timer is programmed, it will serve as a redundant mechanism to ensure that a cell is not overdischarged.

When all cells have reached the UV threshold, all cell-balancing switches will be disabled, but the cell-balancing timer will run until completion. This ensures that the µC can still access the device to confirm balancing operation progress and exit status. To use a defined UV threshold, the threshold level must be written to the CBUVTHR in the BALAUTOUVTHR register. This register allows for 14 bit values relating to a 305µV LSB.

Optionally, the MINCELL value from the prior ADC acquisition can be used as the the desired threshold value. When CBUVMINCELL is disabled, the value written to CBUVTHR during a valid write to BALAUTOUVTHR will be loaded to CBUVTHR. When CBUVMINCELL is enabled, the current value in the CELL[n] register corresponding to the MINCELL address will be automatically loaded to CBUVTHR during a valid write to BALAUTOUVTHR (and the content in CBUVTHR during the write will be ignored). When the BALAUTOUVTHR register is read back, the current value of CBUVTHR will be provided, with CBUVMINCELL indicating the means by which it was selected.

The HVMUX and ADC signal chain is used for the balancing measurement and threshold comparison. The acquisition is determined by the channels enabled in the BALSWEN bitfield as well as the parameters set in the SCANCTRL register. The achievable accuracy of the UV measurement is determined by ADC accuracy specifications in the *Electrical Characteristics*. For the highest accuracy, calibration should be asserted prior to initiating balancing.

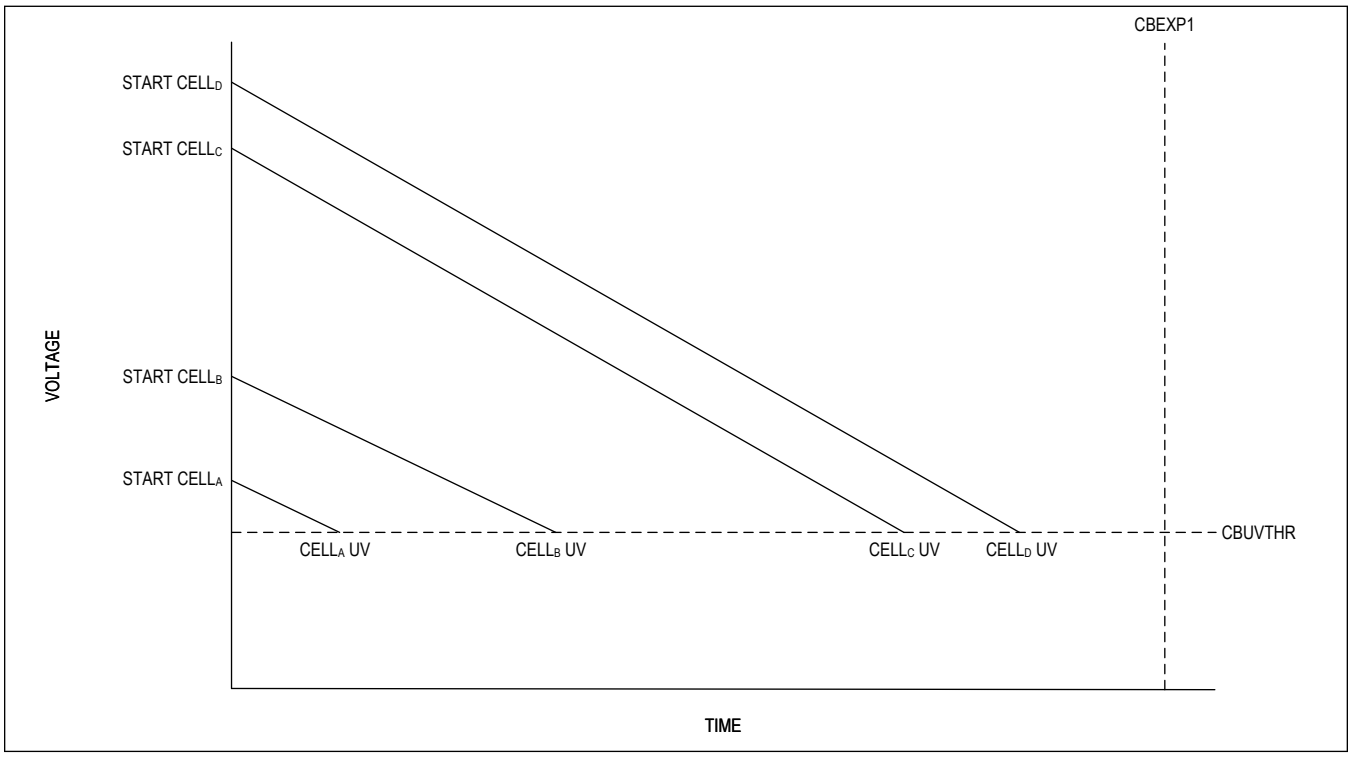


Figure 38. Cell-Balancing UV Threshold Crossing

Note: $CELL_A$, $CELL_B$, $CELL_C$, and $CELL_D$ are nonspecific cells. $CELL_A$ represents the cell with the lowest starting voltage. $CELL_D$ represents the cell with the highest starting voltage. In this example, CBUVTHR is the UV threshold for all cells and CBEXP1 is the cell-balancing expiration timer for auto group cell-balancing mode (CBMODE = 0b11x). The $CELL_N$ UV-threshold crossings are inputs to the cell-balancing stop control logic.

Cell-Balancing Measurement

Embedded cell-balancing measurements only occur when requested by CBMEASEN, as indicated in Table 34:

Table 34. Cell-Balancing Measurement Enable

CBMEASEN[1:0]	DESCRIPTION
0b0x	Provides the highest duty cycling by skipping all measurement operations. Only cell-balancing timer(s) are used to terminate cell balancing normally.
0b1x	Enables embedded measurements for manual UV monitoring or supervision by the host processor.
0b11	Enables embedded measurements and internal CBUVTHR checks in automated modes. (Checking is not supported in Emergency Discharge mode.)

CBMEASEN selections are only functional in discharge and automated cell-balancing modes; this setting is ignored in all other modes.

Measurements are taken using the ADC with a fixed OVSAMPL = 16x, SCANMODE = 'pyramid' to provide the highest accuracy measurements. All other scan parameters are set according the current SCANCTRL, ACQCFG, DIAGCFG, POLARITYCTRL registers. Any attempt to overwrite the scan parameters during balancing are ignored and an ALRTRJCT condition is issued..

Cell-Balancing IIR Filtering

In automatic and discharge cell-balancing modes, the automated ADC measurements are processed through each of the individual cells' IIR filter. This filter allows for more accurate measurements and provides noise immunity to maintain robust balancing performance.

In these modes, the IIR filter will maintain the setting configured by the user, if enabled (IIRFC != 0b111). In the event that the IIR is not used in the normal application (IIRFC = 0b111 = 8/8), the IIR filter will be enabled with an equivalent IIRFC = 0b000 = 1/8 for use in debouncing measurements.

In addition, if the IIR filter is not used in normal applications or has not been routinely updated using AMENDFILT, the CBIIRINIT bit should be used to initialize the IIR with the first acquisition's measurements to avoid falsely exiting the UV threshold due to the long settling response. How the filter behaves upon entry into an automatic or Emergency Discharge cell-balancing mode thus depends on the CBIIRINIT setting:

- In Continuation mode (CBIIRINIT = 0) , the current value in the IIR accumulators is kept (presumably from previous cell measurements) and cell-balancing measurements are amended normally.
- In Initialization mode (CBIIRINIT = 1), the IIR accumulators will be reinitialized to the first measurement taken, and further cell-balancing measurements are amended normally. CBUVTHR checking is not enabled after the 16th measurement is taken (checking begins on the 17th measurement), giving the IIR time to settle.

Cell-Balancing Calibration

In automated and discharge modes, after each pair of even/odd cell-balancing periods, a supervisory ADC measurement can be taken (and checked against CBUVTHR, if enabled/applicable; see CBMEASEN). Due to the expected temperature rise during cell balancing, it is recommend to allow automated calibration sequences to be interleaved with the measurement acquisitions. This is done by programming the CBCALDLY to a non-zero value, which signifies how many measurement cycles are taken prior to a calibration being taken. See Table 35.

Table 35. Cell-Balancing Calibration Selection

ADCCALEN (APPLY CALIBRATION)	CBCALDLY (PERFORM CALIBRATION	RESULTING OPERATION
1 (ON)	Non-zero (ON)	ADC results are post-processed based on calibration coefficients obtained periodically during the cell-balancing operation.
1 (ON)	000 (OFF)	ADC results are post-processed based on calibration coefficients obtained prior to the cell-balancing operation.
0 (OFF)	Non-zero (ON)	Calibration is performed during the cell-balancing operation, but ADC results are based on factory defaults (not recommended).
0 (OFF)	000 (OFF)	ADC results are based on factory defaults.

CBCALDLY settings are only functional if CBMEASEN = 0b1x (cell-balancing measurements are requested); otherwise,

they are ignored.

A value of 0x00 (default) in the CBCALDLY bits within the BALDLYCTRL register disables CAL operations (only ADC measurement operations are performed).

If a non-zero value is selected, the first ADC measurement (ADC) operation will be replaced with an On-Demand Calibration (CAL) operation. From that point on, this selection determines how often the ADC operation is automatically replaced with an CAL operation (to address thermal drift due to power dissipation during cell balancing). 0b001 means ADC and CAL alternate every other cycle. 0b010 means a CAL occurs once every 4 cycles; 0b111 (maximum setting) means a CAL occurs once every 32 cycles. A list of all possible settings are shown in Table 36:

Table 36. Calibration Frequency

CBCALDLY	CALIBRATION FREQUENCY
0b000	Periodic Calibration Disabled
0b001	2 cycles
0b010	4 cycles
0b011	8 cycles
0b100	12 cycles
0b101	16 cycles
0b110	24 cycles
0b111	32 cycles

Calibration Out-of-Range During Cell Balancing

After a measurement or calibration is completed, the cell balancer will check the status of ALRTCAL register bit if calibration is enabled (ADCCALEN = 1). If ALRTCAL is set, it indicates that calibration is out of range, and that calibrated ADC results could be corrupted as a result.

If ALRTCAL is set and calibration is enabled (ADCCALEN = 1), the ALRTCBCAL bit will be set and active cell-balancing operations will be immediately halted to prevent balancing errors due to inaccurate measurements. All subsequent measurement, calibration, and switching cycles will be skipped until the cell balancing duration expires, or is otherwise aborted/restarted. The cell-balancing timer (CBTIMER) continues to run until the governing CBEXP time is reached, and HOLDSHDNL extensions still apply (if enabled), allowing the µC to confirm exit status. Note that once ALRTCBCAL is issued, data in the CBUVSTAT bitfield and data fetched by CBSCAN requests should be treated as compromised.

If an ALRTCAL/ALRTCBCAL condition is issued, the user can exit the cell-balancing operation, and attempt to resolve the condition. If the condition can not be resolved, cell-balancing operations can be requested using factory calibration defaults by setting ADCCALEN = 0.

Cell Balancing with No Calibration

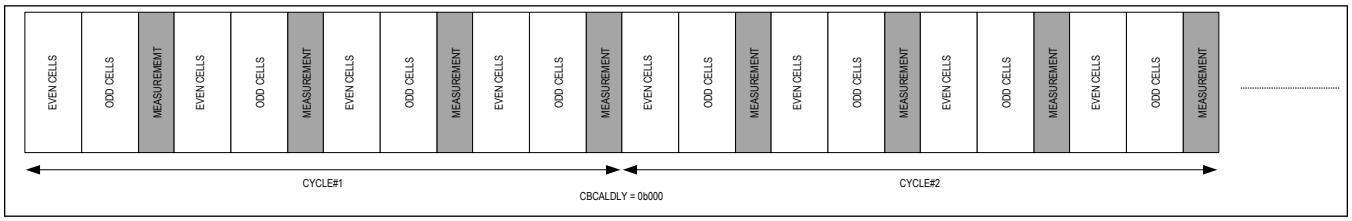


Figure 39. Cell Balancing with No Calibration

Cell Balancing with Calibration

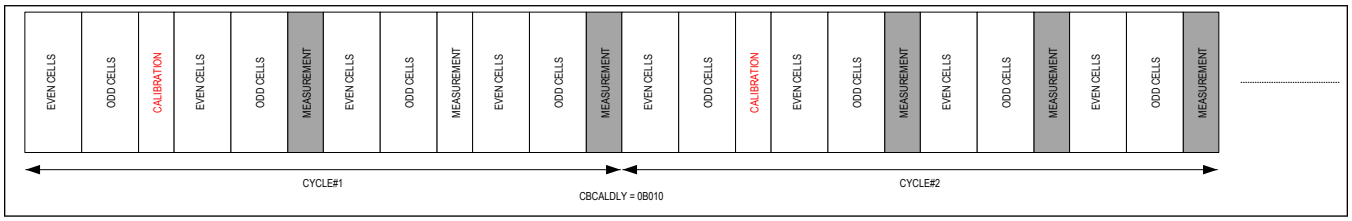


Figure 40. Cell Balancing with Calibration

Transfer-Measurement Results using CBSCAN

The CBSCAN bit in the BALDATA register can initiate a manual transfer of results from the IIR to the CELL data registers (RDFILT is ignored, and IIR data is always transferred, since the IIR governs cell-balancing operations). CBSCAN is provided to support readback of measurement results taken during Automated and Emergency Discharge cell-balancing modes. If CBSCAN is issued during these cell balance measurements, the move will be executed once the sequence is complete.

CBSCAN acts as a strobe bit and therefore does not need to be cleared (self-clearing); it always reads logic 0.

CBSCAN is not valid outside of automated cell-balancing operation. If automated cell balancing is stopped or when manual balancing is operational, the measurement scan bitfields in the SCANCTRL register must be used for data control into the cell registers.

Cell-Balancing Completion

In summary, after the host initializes the cell-balancing operation, the operation will be stopped by any of the following:

- Watchdog timer expiration (CBTIMER = CBEXPn)
- Reaching the UV threshold (per cell in Automated modes only, if CBMEASEN = 0b11)
- Thermal fault condition (Automated and Discharge modes only, if CBTEMPEN = 0b1)
- Calibration fault condition (Automated and Discharge modes only, if ADCCALEN = 0b1)
- Aborting the operation by changing CBMODE to 0b000 (disabled)
- Reinitiating an operation by changing CBMODE to a value other than 0b000

Manual cell-balancing mode switch activity can be temporarily suspended for calibration or ADC measurements if AUTOBALSWDIS = 0b1.

In Discharge, Manual, and Auto Group modes, the CBTIMER will be stopped when it reaches CBEXP1, regardless of BALSWEN settings.

In Auto Individual modes, the CBTIMER will be stopped when it reaches MAX(CBEXPn), regardless of BALSWENn settings.

Automated and Discharge modes are halted if temperature exit is enabled (CBTEMPEN = 0b1) and an overtemperature fault occurs.

Automated and Discharge modes are halted if CBMEASEN = 0b1x and a calibration fault occurs.

All timed modes run CBTIMER for the full duration specified, even if actual cell-balancing operations are stopped due to UV or thermal exit conditions, allowing the µC to confirm the exit status. Additional time for the µC to check the exit status can be afforded using HOLDSHDNL options.

CBACTIVE allows confirmation of cell-balancing operation status. A cell-balancing operation is considered completed normally if the CBTIMER expires (all CB modes), or when all enabled cells reach the programmed CBUVTHR limit (Automatic modes only, if CBMEASEN = 1b1). A cell-balancing operation is considered completed abnormally in the event of an ALRTCBCAL or ALRTCBTEMP condition.

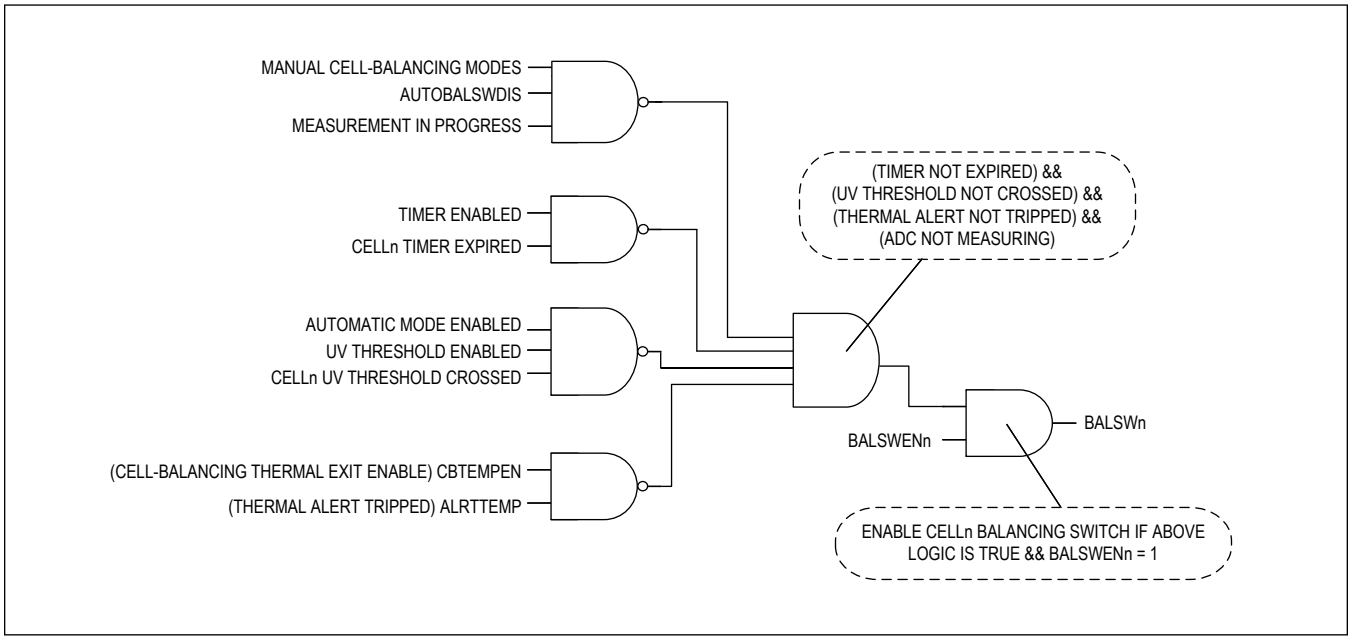


Figure 41. Cell-Balancing Stop Control

Note: The thermal fault will limit the temperature rise to a safe level below the maximum junction temperature of the device as defined by the ALRTTEMP specification in the *Electrical Characteristics* table. For applications requiring maximum cell-balancing current, this can be disabled, but the system should take caution to ensure that the device is not damaged by exceeding the absolute maximum rated junction temperature.

Cell-Balancing and Low Power Auto-Polling Exit Criteria

Cell-balancing and auto-polling exit criteria are summarized in Table 37. The stop criteria does not exit the current state, but stops either the cell balancing (disables the cell-balancing switches) or stops the auto-polling (discontinues measurements). The exit result reflects the first exit criteria encountered.

Table 37. Cell-Balancing and Auto-Polling Stop Criteria

	AUTO-POLLING STOP	CELL-BALANCING STOP	REGISTER CONFIGURATION
CBTIMER (by second, by minute, by hour)	Exit Criteria: CBTIMER = CBEXP1 for Group CBTIMER = Max(CBEXPn) for Individual Exit Result (Normal): CBACTIVE = 0b10 ALRTCBDONE = 0b1 All timers and measurements stop.	Exit Criteria: CBTIMER = CBEXP1 for Manual, Discharge, and Auto-Group, CBTIMER = Max(CBEXPn) for Auto-Individual Exit Result (Normal): CBACTIVE = 0b10 ALRTCBDONE = 0b1 All timers, cell balancing, and measurements stop.	CBMODE = 0b1XX (Auto) for Auto-Polling CBMODE != 0b000 for Cell Balancing

Table 37. Cell-Balancing and Auto-Polling Stop Criteria (continued)

CBUV Threshold Enabled, Measurement Enabled	*Exit Criteria:* *Auto-polling will only exit based on timer or timeout criteria.* *CBACTIVE = 0b10 at auto-polling entry, but timer and measurements continue to run.*	Exit Criteria: All enabled CELLn (internal) < CBUVTHR Exit Result (Normal): CBACTIVE = 0b10 ALRTCBDONE = 0b0 All timers and measurements continue (ALRTCBDONE will be issued on timer expiration - see above). Cell-balancing switch activity stops.	CBMODE = 0b1XX (Auto) CBMEAS = 0b11 (Embedded Measurement, CBUVTHR Checking Enabled)
CBUV Threshold Disabled, Measurement Enabled	*Exit Criteria:* *Auto-polling will only exit based on timer or timeout criteria.*	*Exit Criteria:* *N/A - Cell measurements will not induce an exit.* *Exit Result:* *N/A - Cell balancing will only exit on other criteria*	CBMODE = 0b1XX (Auto) CBMEAS = 0b10 (Embedded Measurement, CBUVTHR Checking Enabled)
Timeout Fault	Exit Criteria: Timer integrity fault found. Exit Result (Fault): CBACTIVE = 0b11 ALRTCBTIMEOUT = 0b1 All timers and measurements stop (state machine compromised).	Exit Criteria: Timer integrity or oscillator fault found. Exit Result (Fault): CBACTIVE = 0b11 ALRTCBTIMEOUT = 0b1 All timers, measurements, and cell balancing switch activity stops (timer compromised).	CBMODE = 0b1XX (Auto) for auto-polling CBMODE != 0b000 or 0b001 for cell balancing
Thermal Fault	*Exit Criteria:* *Auto-polling will only exit based on Timer or Timeout criteria* *Die Temperature faults will be reported through the Alert Packet (FMEA2.ALRTTEMP = 0b1)*	Exit Criteria: A die temperature fault is detected (FMEA2.ALRTTEMP = 0b1). Exit Result (Fault): CBACTIVE = 0b11 ALRTCBTEMP = 0b1 All timers continue. Measurement, calibration, and cell-balancing switch activity stops.	CBMODE = 0b1XX (Auto), 0b001 (Emergency Discharge) CBTEMPEN = 0b1
Calibration Fault	*Exit Criteria:* *Auto-polling will only exit based on timer or timeout criteria.* *Calibration faults will be reported through the Alert Packet (STATUS1.ALRTCAL = 0b1).*	Exit Criteria: A calibration fault is detected (STATUS1.ALRTCAL = 0b1). Exit Result (fault): CBACTIVE = 0b11 ALRTCBCAL = 0b1 Timers continue. Measurement and cell-balancing switch activity stops (measurements compromised).	CBCALDLY != 0b000 ADCCALEN = 0b1 (Enabled)

Note: Auto-polling will not assert the ALRTCBTEMP, ALRTCBCAL, and ALRTCBAUX status bits since it does not exit the mode based on the insertion. Any underlying alert conditions will be reflected in ALRTTEMP, ALRTCAL, ALRTAUXOV, ALRTAUXOV, and ALRTAUXPRTCTSUM.

Note: Auto-polling and auto cell-balancing operation only updates the CELLn, AUXn, and DIAGn registers upon issuance of a CBSCAN during operation with CBMODE != 0b000, 0b001.

Note: All timed modes run CBTIMER for the full duration specified, even if actual cell-balancing operations are stopped due to a UV condition or thermal fault.

In addition to the above criteria, both auto-polling and cell balancing may be stopped by aborting the operation (CBMODE = 0b000) or reinitializing the operation by changing CBMODE to a value other than 0b000.

CBACTIVE allows confirmation of cell-balancing operation status. A cell-balancing operation is considered completed normally if the CBTIMER expires (all CB modes), or when all enabled cells reach the programmed CBUVTHR limit (Automatic modes only, if CBMEASEN = 1b11). A cell-balancing operation is considered completed abnormally in the event of an ALRTCBTIMEOUT, ALRTCBCAL, ALRTCBTEMP, or ALRTCBAUX condition.

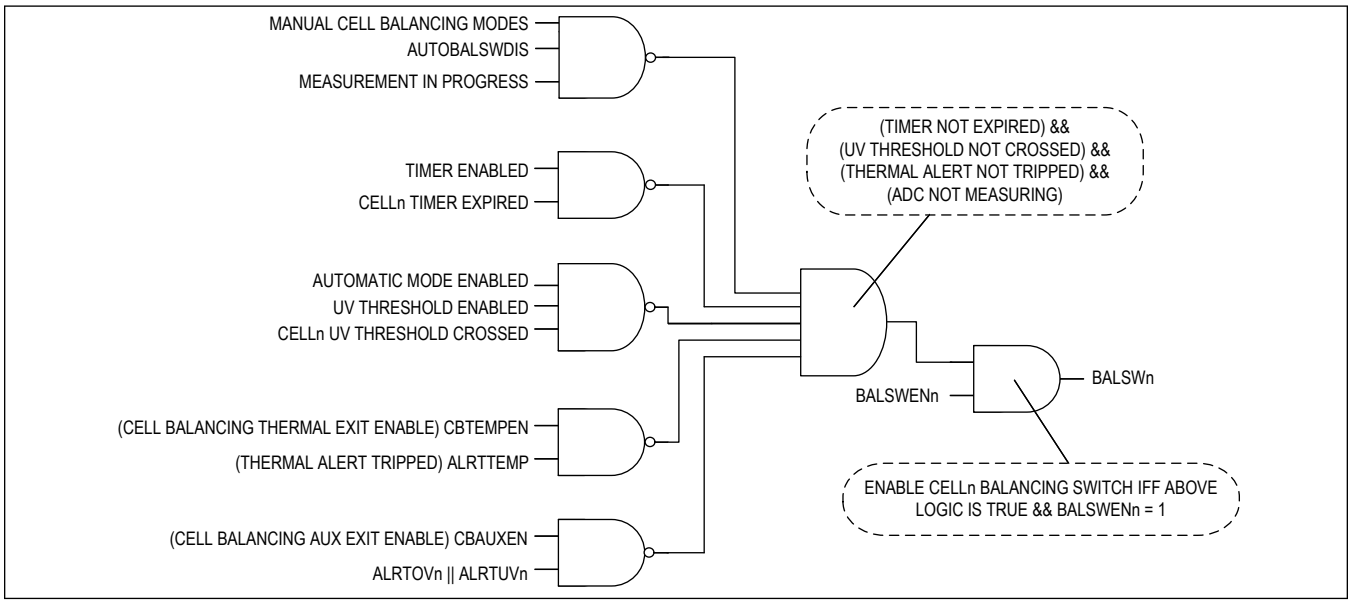


Figure 42. Cell-Balancing Stop Control

Note: The thermal fault limits the temperature rise to a safe level below the maximum junction temperature of the device as defined by the ALRTTEMP specification in the *Electrical Characteristics* table. For applications requiring maximum cell-balancing current, this can be disabled, but the system should take caution to ensure that the device is not damaged by exceeding the absolute maximum rated junction temperature.

Automatic SHDNL Control using HOLDSHDNL

In order to allow for timed balancing with no host interaction, the SHDNL pin can be pulled up to V_{AA} to keep SHDNL high while the timers or UV detection are running by appropriately configuring the HOLDSHDNL bitfield within the BALCTRL register. When enabled and engaged, this mode activates an internal diode pullup from the V_{AA} pin to SHDNL. This keeps the device operational, even if UART operation is suspended for long periods of time.

The HOLDSHDNL options have no effect in Disabled or Manual modes.

In mode 0b01, the pullup is engaged for the selected CBEXP1 interval for group operations, or the longest CBEXPn time selected for individual operations, even if switch activity is halted due to thermal protection (ALRTCBTEMP), calibration issues (ALRTCBCAL), or reaching the specified voltage target (CBUVTHR).

In mode 0b10, the pullup is engaged for the selected CBEXP1 interval for group operations, or the longest CBEXPn time selected for individual operations even if switch activity is halted due to thermal protection (ALRTCBTEMP), calibration issues (ALRTCBCAL), or reaching the specified voltage target (CBUVTHR). After CBTIMER expires, HOLDSHDNL continues to be held for the larger of 5 minutes or 6.25% of the relevant CBEXPn interval. If CBEXPn timing is disabled/ infinite (3FFh), SHDNL will be held until removed by a write to BALCTRL.

In mode 0b11, the pullup is engaged until removed by a write to BALCTRL.

If HOLDSHDNL = 0b1x, CBTIMER will read back the governing CBEXP time for the duration of the extended hold interval, allowing the µC to confirm the requested balancing operation has run to completion. In modes HOLSDSHDNL

= 0b1x, the hold behavior can be removed after operations are completed and the exit status has been confirmed by writing CBMODE to disabled, allowing the device to power down.

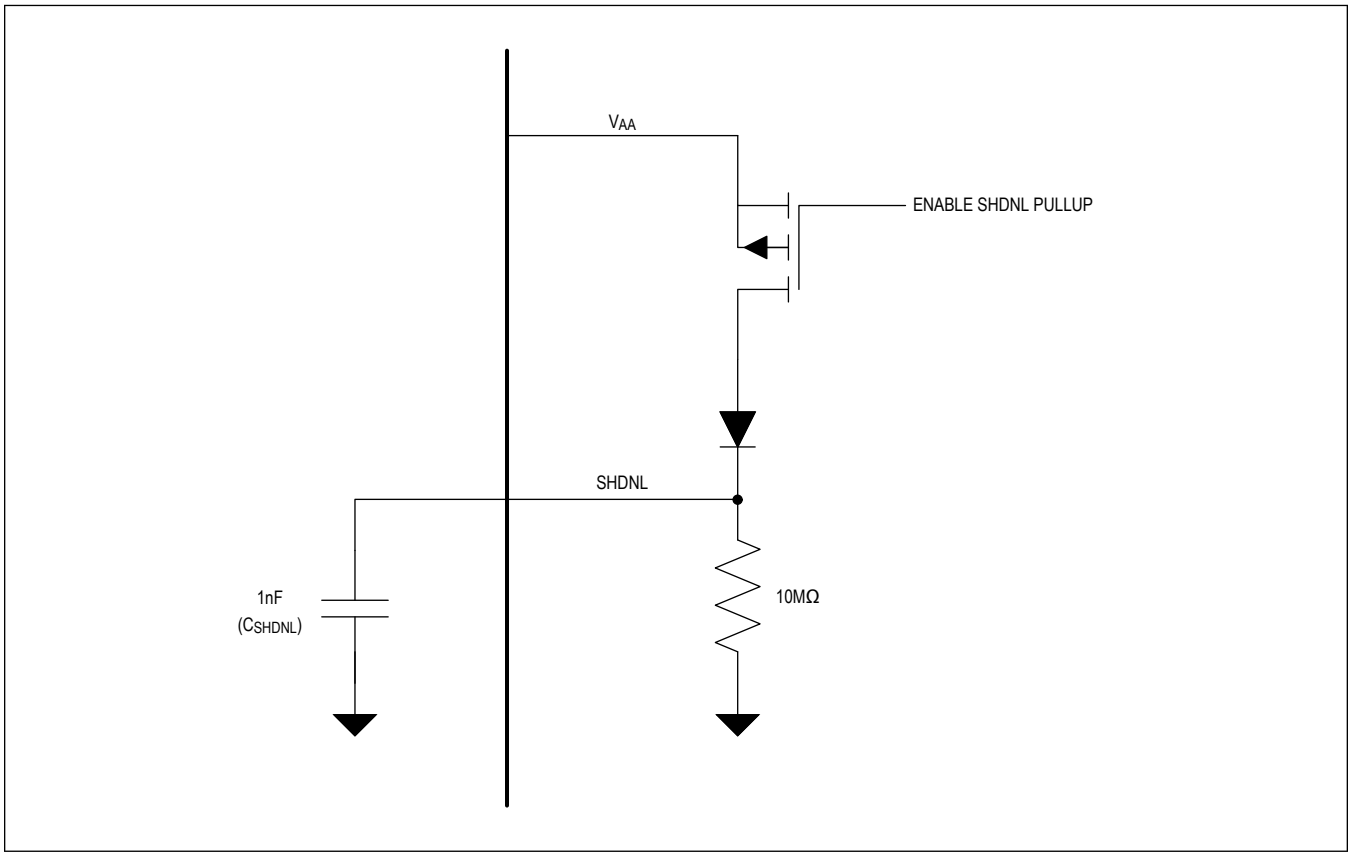


Figure 43. SHDNL Pullup Control

Cell Balancing Switches

The cell-balancing current is limited by the external balancing resistance ($R_{BALANCE}$) and the internal balancing switch resistance (R_{SW}), as shown in Figure 44. Cell-balancing switches are internally controlled with even and odd switching sequences in auto/manual modes or independently in Emergency Discharge mode. Fault detection is described in the *Diagnostics* section.

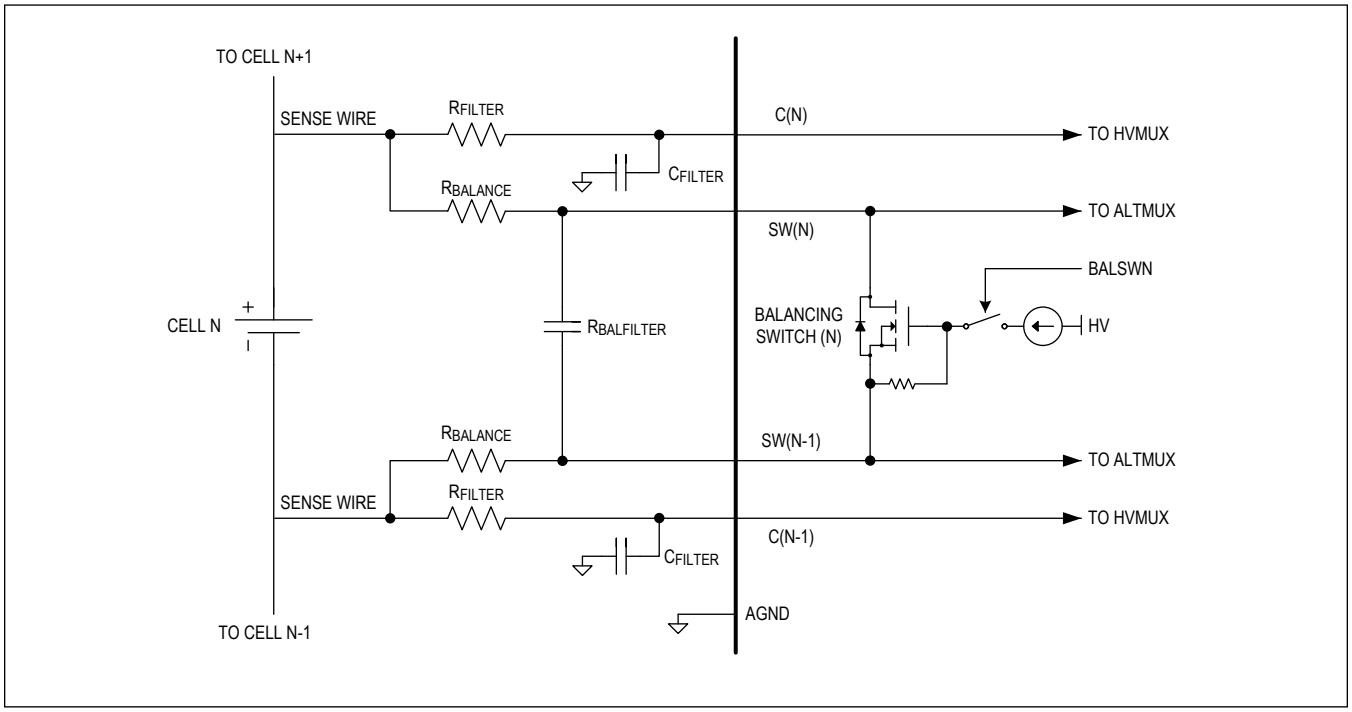


Figure 44. Internal Cell-Balancing Switches

Cell Balancing Current

The cell-balancing current is limited by package power dissipation, average die temperature, average duty cycle, and the number of switches conducting current at any one time. The system designer must carefully control the device power dissipation by selecting a balancing current resistance ($R_{BALANCE}$) to ensure the die and package temperature are below the absolute maximum package rating and neither the device thermal shutdown threshold nor the ADC measurement accuracy is impacted. The typical thermal performance with a per-switch balancing current of 300mA for 7 switches concurrently enabled at elevated ambient temperature as shown in Figure 45. The typical thermal performance during balancing is also detailed in the *Typical Operating Characteristics* section.

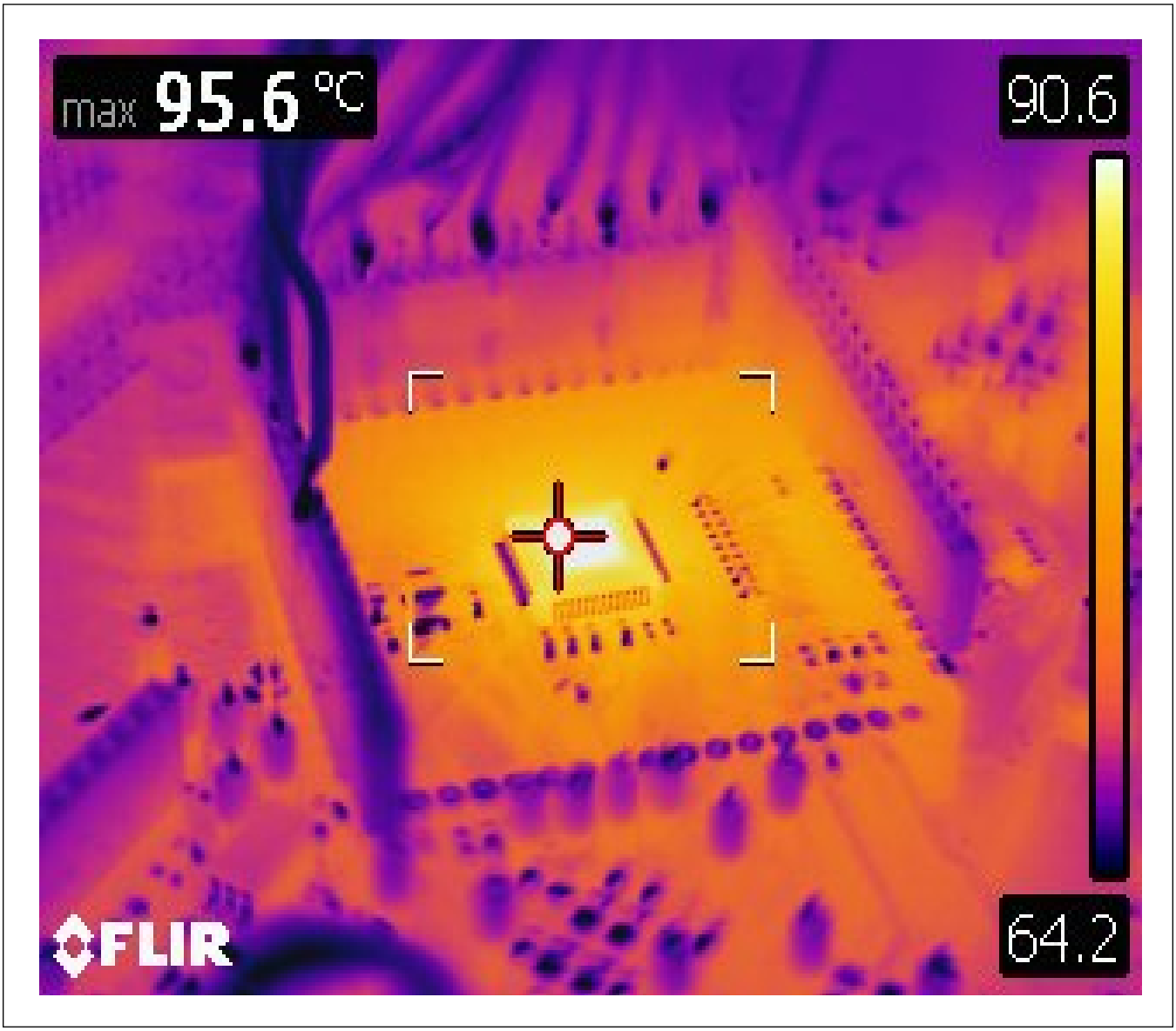


Figure 45. Thermal Image During Balancing of 7 Cells, 300mA, +60°C Ambient

Example: Autonomous Cell Balancing by Time

Autonomous cell balancing can be commanded within the MAX17854, which enables balancing while the host microcontroller enters a sleep state. The following procedure illustrates how autonomous cell balancing invoked with the primary stop mechanism as a timer:

1. Host calculates SOC for each of the individual cells.
2. Host determines which cells to balance and associated balancing time.
3. Host programs balancing channels using BALSWEN[13:0].
4. Host programs effective balancing current.

Effective balancing current = V_{CELLn}/(2 x RBALANCE) x CBDUTY[7:4]

5. Host programs CBEXP1-CBEXP14 based on effective balancing current and SOC.
6. Host programs HOLDSHDNL to determine shutdown behavior at completion of cell balancing.
7. Host initiates balancing using CBMODE "auto-individual cell balancing by second" or "auto-Individual cell balancing by minute."

Example: Autonomous Cell Balancing with Programmable UV Threshold

Autonomous cell balancing controlled through a programmable UV thresholds can be commanded within the MAX17854 to enables balancing while the host microcontroller enters a sleep state. The following procedure illustrates how balancing is invoked with the primary stop mechanism configured to be a voltage measurement and a secondary stop mechanism being a programmable timer.

1. Host calculates SOC for each of the individual cells.
2. Host determines which cells to balance and associated balancing time.

   Timer is a secondary stop mechanism and should have additional margin applied as not to interact with primary UV measurement stop threshold.

3. Host programs balancing channels using BALSWEN[13:0].
4. Host programs effective balancing current.

   Effective balancing current = $V_{CELLn}/(2 \times R_{BALANCE}) \times$ CBDUTY[7:4]

5. Host programs CBEXP1-CBEXP14 based on effective balancing current and balancing time calculation.
6. Host programs CBUVTHR or CBUVMINCELL to program UV measurement stop threshold.
7. Host programs CBMEASEN as "Embedded ADC/CAL Measurements enabled, CBUVTHR checking enabled."
8. Host programs CBCALDLY to force measurement calibration to account for temperature rise from balancing.

   Calibration choice should be chosen based on the thermal time constant of the board

9. Host programs HOLDSHDNL shutdown behavior at completion of cell balancing.
10. Host initiates balancing using CBMODE as "auto-individual cell balancing by second" or "auto-individual cell balancing by minute."

Interface

UART Interface

UART Interface

The battery-management UART protocol allows up to 32 devices to be independently addressed in a daisy-chain fashion as shown in Figure 46. The host initiates all communication with the daisy-chain devices through a UART interface such as the MAX17841 or MAX17851. The UART can be configured to support a variety of flexible implementations depending on the application requirement. The configurations as defined using UARTCFG are shown in Table 38.

Table 38. UART Configurations

UARTCFG	UART CONFIGURATION	UART UP PATH	UART DOWN PATH
0b00	Single UART Interface with External Loopback	Active	Inactive (Buffered/Pass Through)
0b01	Single UART Interface with Internal Loopback	Active	Inactive (Buffered/Pass Through)
0b10	Single UART Interface with Differential Alert Interface	Active	Differential Alert
0b11	Dual UART Interface	Active	Active

Single UART Interface with External Loopback

When UARTCFG is configured for Single UART with External Loopback, the data flow is always unidirectional from the host—it flows up the daisy-chain (Up Path) and then loops back down the daisy-chain (Down Path) to the host as shown in Figure 46.

In the Up Path, each device first receives data at its lower Rx port and immediately retransmits data from its upper Tx port to the lower Rx port of the next device. The last device uses an external loopback differential cable to transfer data from its upper TX port directly into its upper Rx port, and then it immediately retransmits the data from its lower Tx port to the

upper Rx port of the next down-stack device. The Down Path then acts as a pass-through, buffering and retransmitting the data. It does not act on any commands in this configuration.

The external loopback has two advantages:

1. It is quicker to determine device count for applications where the host does not assume what the device count is
2. It helps to match the supply current of the last device to that of the other daisy-chained devices (because the hardware configuration is identical).

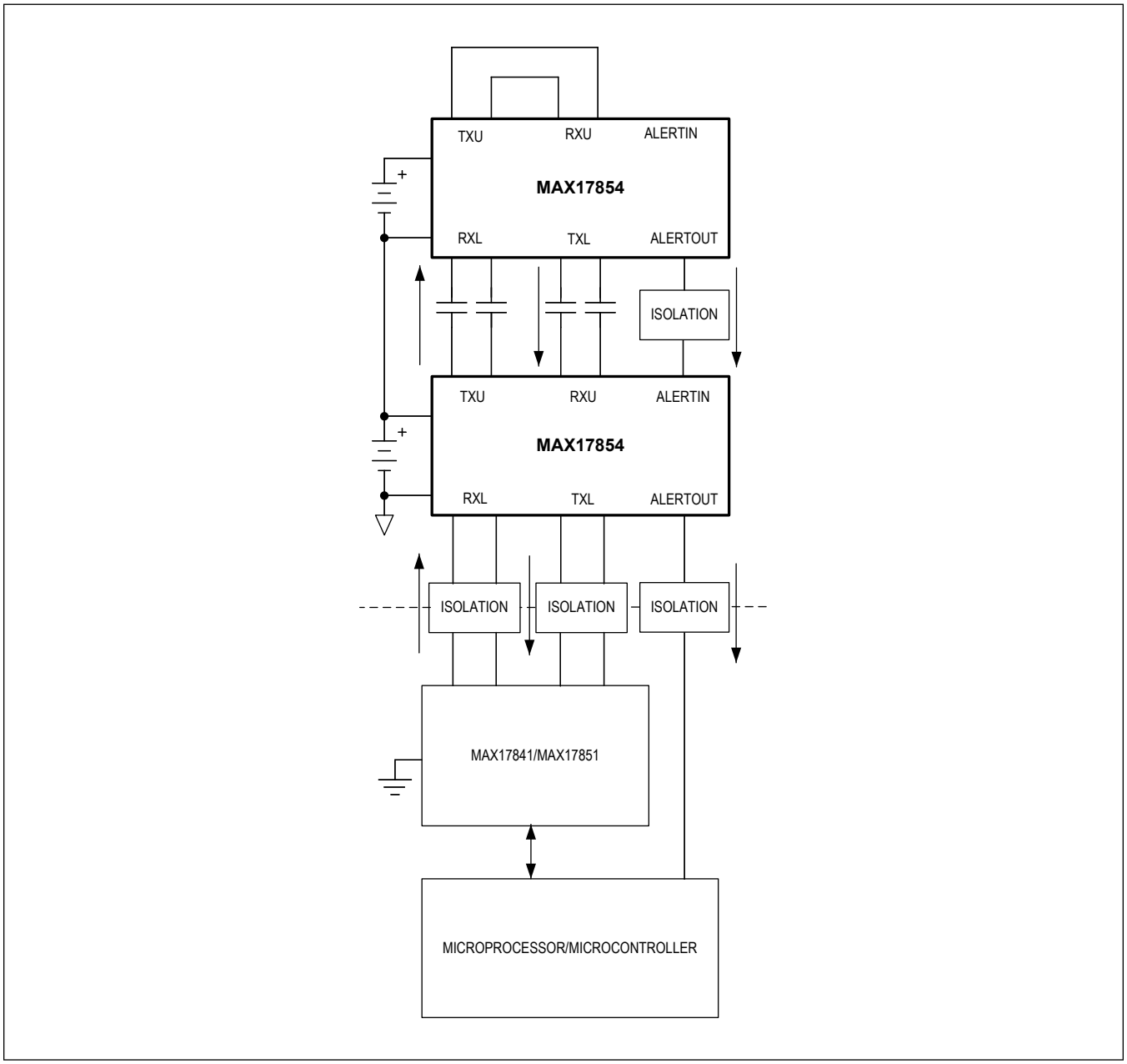


Figure 46. Single UART with External Loopback

Single UART with Internal Loopback

The Single UART with Internal Loopback (UARTCFG = 0b01) configuration routes the upper port transmit data internally to the upper port receiver. This can be used to configure the top device in the daisy chain to prevent the need for external components and wire connections. Additionally, this mode is useful to diagnose the location of daisy-chain signal breaks. This is done by enabling the internal loopback mode on the first device, checking communication, then moving the loopback mode to the next device, and continuing up the stack until communication is lost.

Changing the UART configuration to Single UART with Internal Loopback immediately changes that device's Upper Port configuration such that the signal is routed internally from the upper transmitter to the upper receiver while external signals present on the upper port receivers' input pins are ignored. Therefore when UARTCFG is written to 0b01, the write command that is forwarded in the Up Path is interrupted in the down-stack direction, thus interrupting its return to the host. To verify if the operation is successful, it is recommended to issue this command twice. If the MAX17841 or MAX17851 interface is used, its receive buffer should be cleared before changing UARTCFG, and cleared again after changing the loopback configuration because the communication was interrupted.

Single UART with Differential Alert Interface

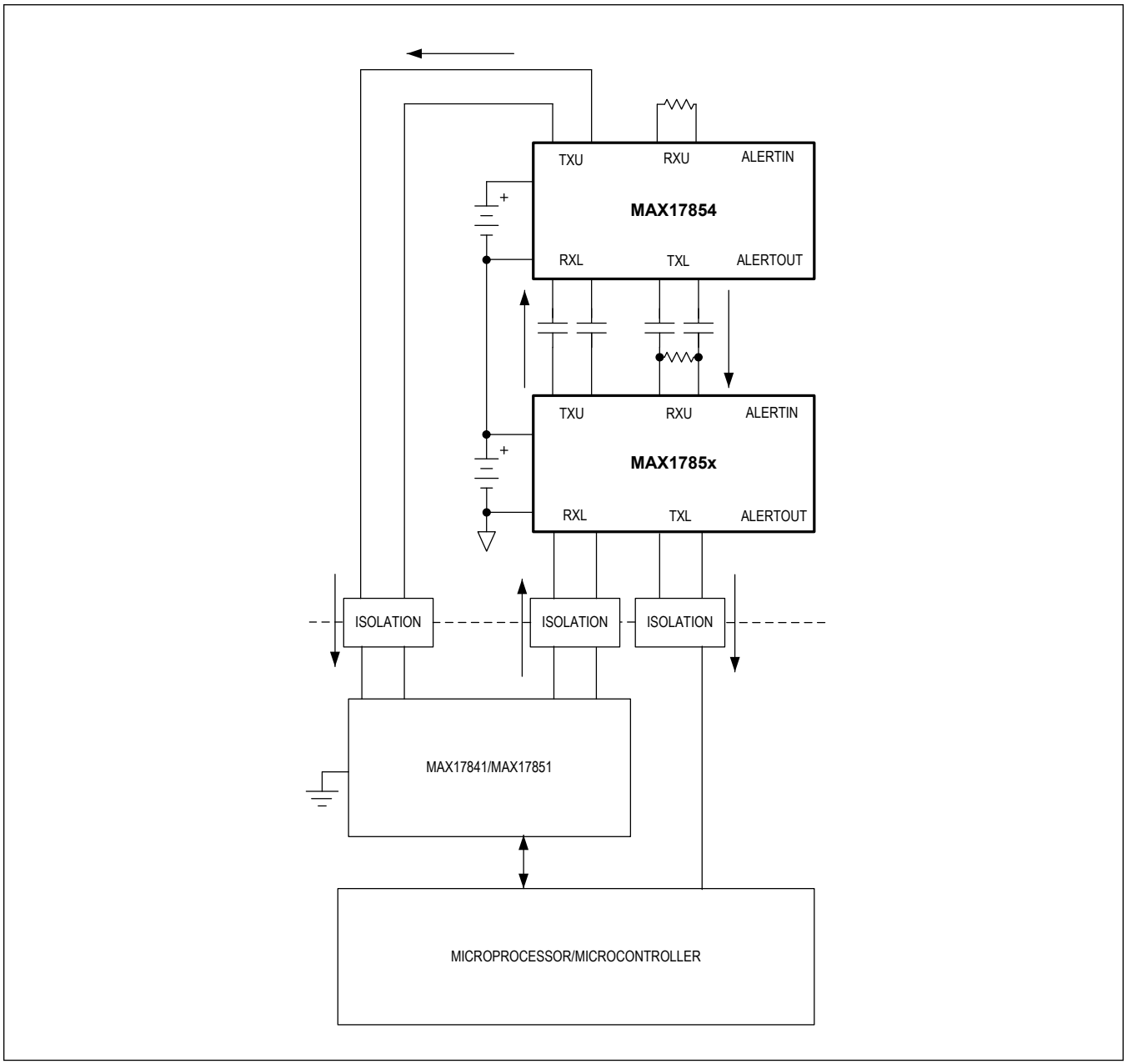


Figure 47. Single UART with Differential Alert Interface

Dual UART Interface

In the event that the end application requires higher data throughput or redundant communication path for safety, the Dual UART Interface configuration may be utilized by writing UARTCFG to 0b11. When configured, the Down Path acts as an independent UART path, which enables simultaneous Read processing from both UART paths. This will essentially double the effective interface rate to ~4Mbps. Additionally, the independent UART paths allow for uninterrupted access to all devices in the daisy chain in the event of a broken interface wire by dynamically changing the master interface with

no loss of functionality.

Note: For this configuration to be utilized, both the hardware and software configurations should match.

By default, the Down Path UART operates as a slave, meaning it will have no response to a Write or WriteAll command. The slave interface only responds to the Read, Readall, and ReadBlock commands. In the event that a Write command is issued on the slave UART, the write will be ignored and passed through to the next device in the daisy chain eventually returning to the MAX17841. Each device in the daisy chain asserts its ALRTDUALUART bit in the STATUS2 register to indicate that a valid write command was received but not acted upon. This bit remains set until cleared by the master interface.

Configuration of the master is performed using the UPHOST or DOWNHOST commands, and identification of the master is performed by reading the UARTHOST bit. See the *Battery-Management UART Protocol Commands* section.

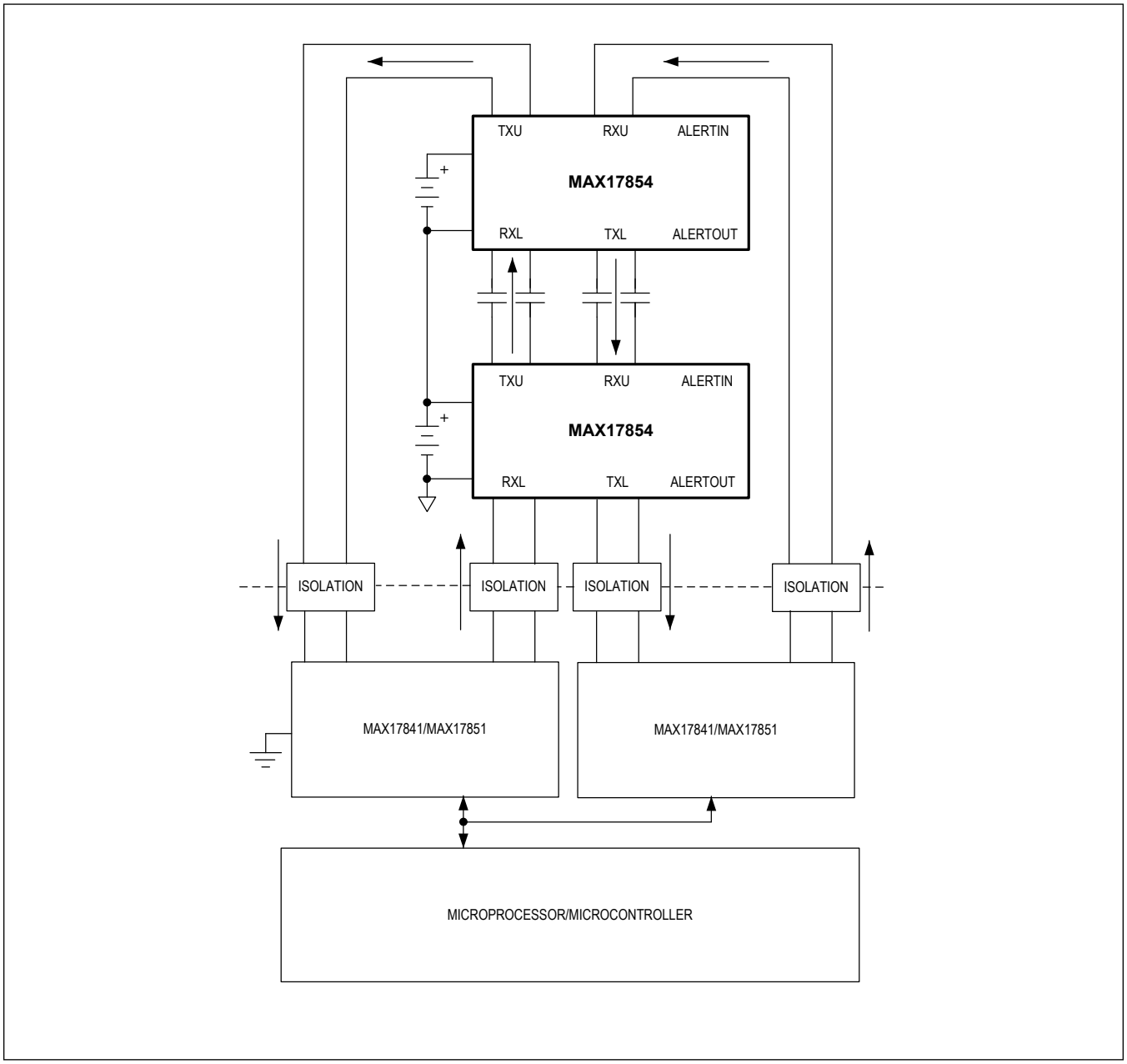


Figure 48. Dual-UART Interface

Dual-UART Master Configuration

In the event that the upstream UART path cannot communicate due to a failure condition, the downstream UART path can reinitialize itself as the master through a DOWNHOST UART command packet issued by the host. This allows the downstream path to have full read and write capability. The upstream path will then hand over master functionality and configure itself as a slave. If the upstream path regains functionality, it will then only be able to issue read commands unless it reinitializes itself as the master using the UPHOST command.

If an interface is reinitialized, the host should poll the UARTHOST bit to ensure that all device within the daisy chain are configured to the same master interface.

Note: The UPHOST command is only valid on the upstream UART, and the DOWNHOST command is only valid on the downstream UART. If an UPHOST command is issued on the downstream UART, no action will be taken and the ALRTDUALUART bit will be set.

Dual UART Master Slave Interaction

The upstream and downstream UART timing should be synchronized by the host controller to avoid the reading potentially data from the prior acquisition. This may occur when the master issues a write command and the slave attempts to read the data before the entire data packet propagates through the last device on the daisy chain. See Figure 49 and Figure 50 as examples of the timing considerations. The master UART path will not prevent this interaction and should be handled by the host.

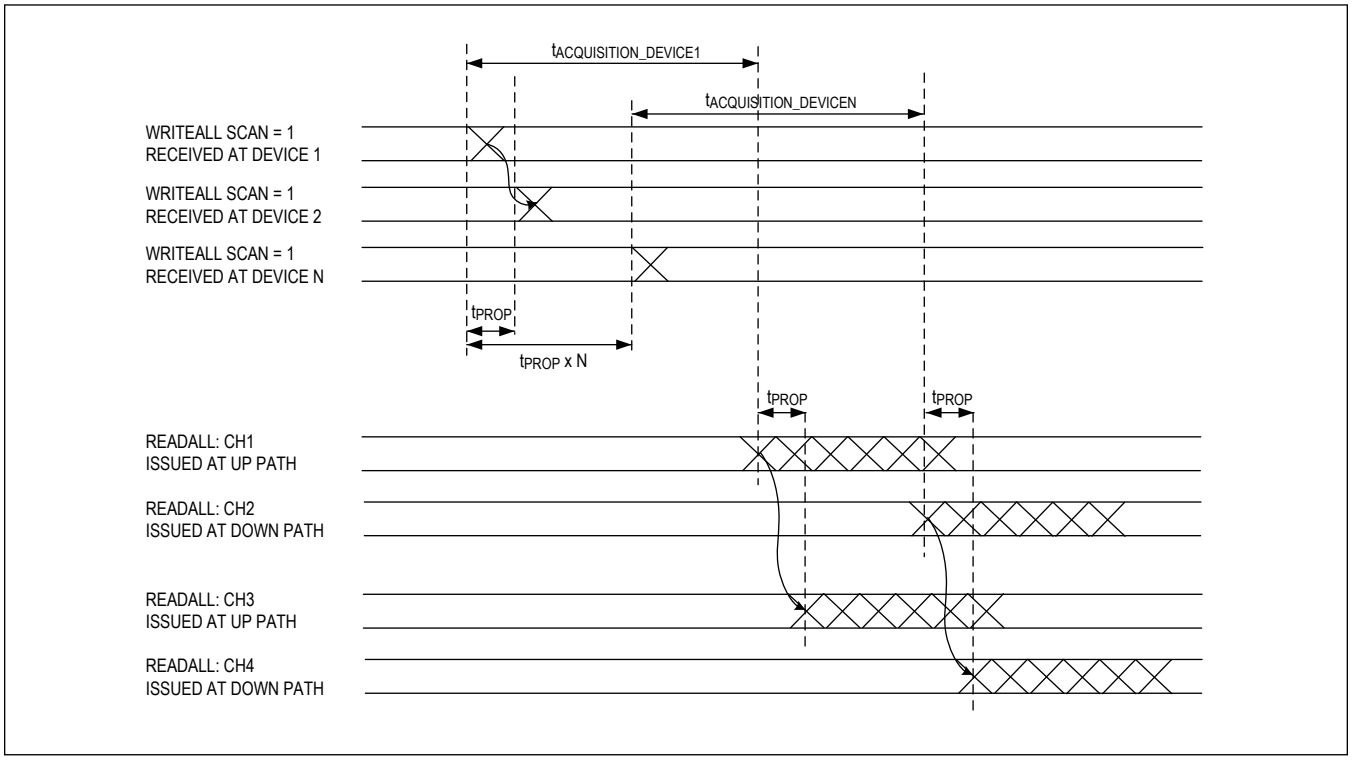


Figure 49. Dual-UART Master Slave Interaction (Timing Considerations)

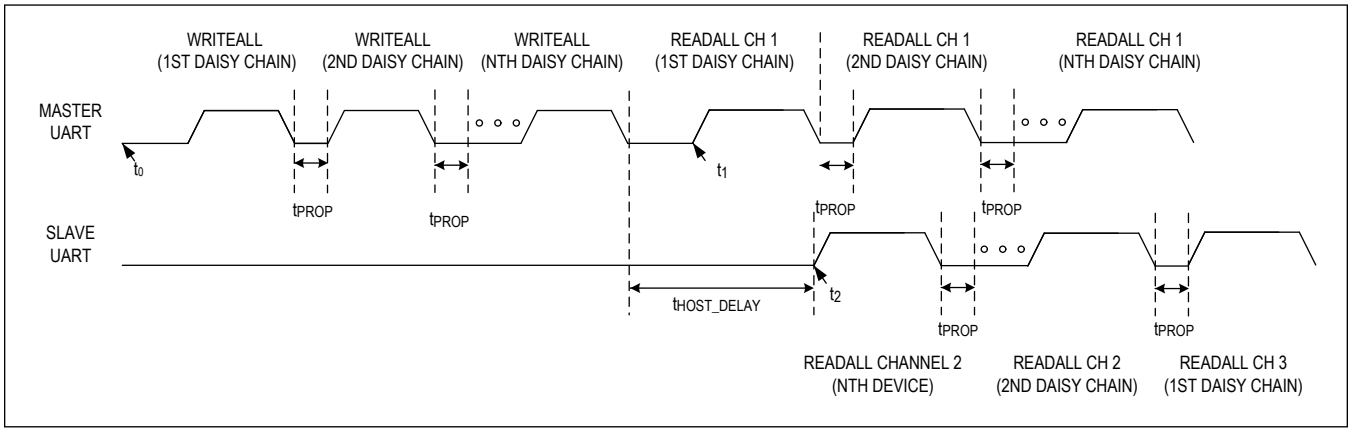


Figure 50. Dual-UART Command Timing

Similarly, the UPHOST and DOWNHOST commands should not be sent simultaneously to avoid an unknown state to the host controller. The host controller will be able to diagnose the incorrect state by reading the UARTHOST bit or by invalid commands signified by the ALRTDUALUART.

UART Ports

Two UART ports are utilized: a lower port (RXL/TXL) and an upper port (RXU/TXU). Each port consists of a differential line driver and differential line receiver. DC-blocking capacitors or transformers may be used to isolate daisy-chained devices that are operating at different common-mode voltages. During communication, the character encoding provides a balanced signal (50% duty-cycle) that ensures charge neutrality on the isolation capacitors.

UART Transmitter

When no data is being transmitted by the UART, the differential outputs must be driven to a common level to maintain a neutral charge difference between the AC-coupling capacitors or to avoid saturation of the isolation transformers. In the default idle mode (low-Z), the transmitter drives both outputs to a logic-low level to balance the charge on the capacitors; this also works well with transformer coupling. The high-Z idle mode (TXLIDLEHIZ, TXUIDLEHIZ = 0b1) places the Tx pins in a high-Z state during time periods where the UART is inactive, which may be desirable to minimize the effects of charging and discharging the isolation capacitors. The idle mode for the upper and lower ports may be controlled independently through the TXUIDLEHIZ and TXLIDLEHIZ configuration bits.

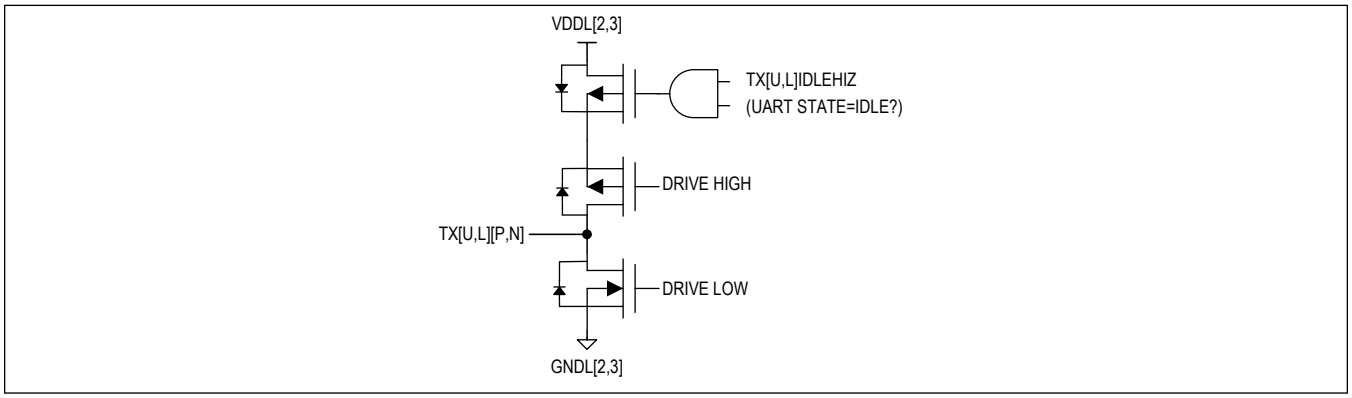


Figure 51. UART Transmitter

UART Receiver

The UART receiver has a wide common-mode input range to tolerate harsh EMC conditions. It can be operated in differential mode or single-ended mode per Table 38. By default, the UART receivers are configured for differential mode. In single-ended mode, the RXP input is grounded and the RXN input receives inverse data as described in the *Applications* section (Figure 105). In single-ended mode, the receiver input threshold is negative so that a zero differential voltage (V_{RXP}, V_{RXN} = 0V) is considered to be a logic 1 and a negative differential voltage (V_{RXN} high) is a logic 0.

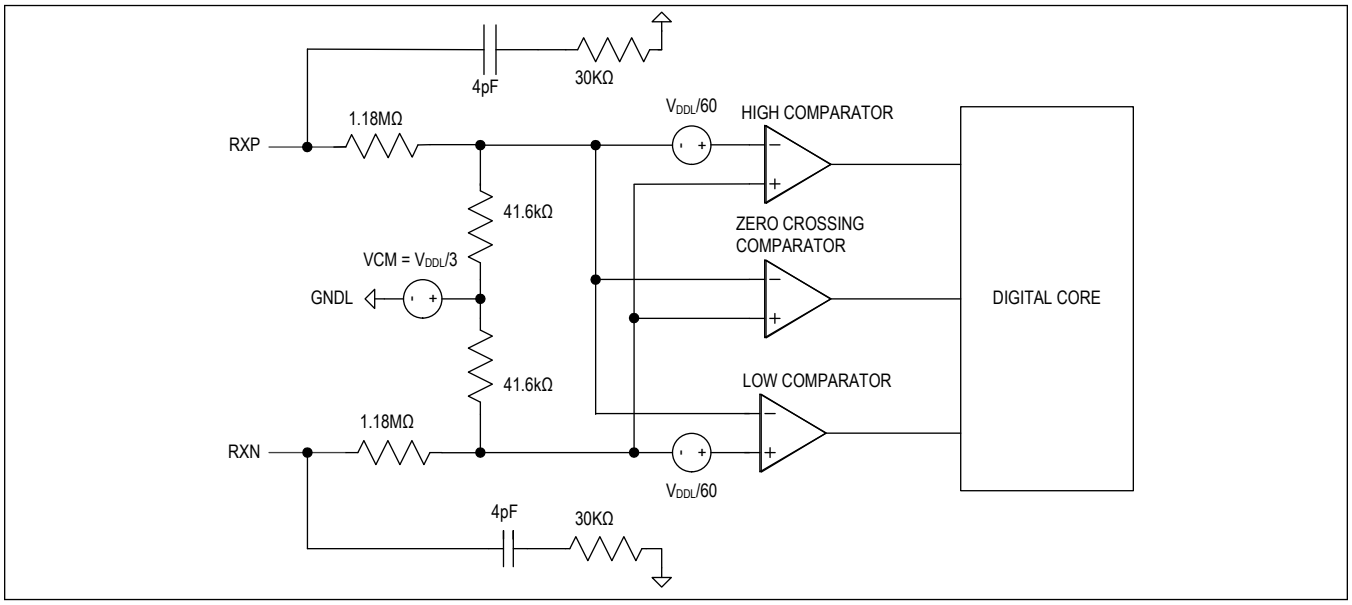


Figure 52. UART Receiver

SHDNL Charge Pump

The SHNDL pin is controlled using UART communication. Using a differential UART, the signaling on the lower port receiver drives an internal charge pump that charges up the external 1nF capacitor connected to the SHDNL input, as shown in Figure 53. V_{SHDNL} reaches 1.8V in 200µs (typ). The charge pump then self-regulates to the $V_{SHDNLIMIT}$ and can maintain V_{SHDNL} even with the UART idle for long durations. In the event that communication is halted, the SHDNL pin voltage will fall with a 10ms time constant (assuming a 1nF capacitor).

Note: Do not connect active components to SHDNL.

Note: Both upper and lower UART Rx ports are enabled with charge pumps, allowing for communication on either the Up Path or Down Path to initialize the device.

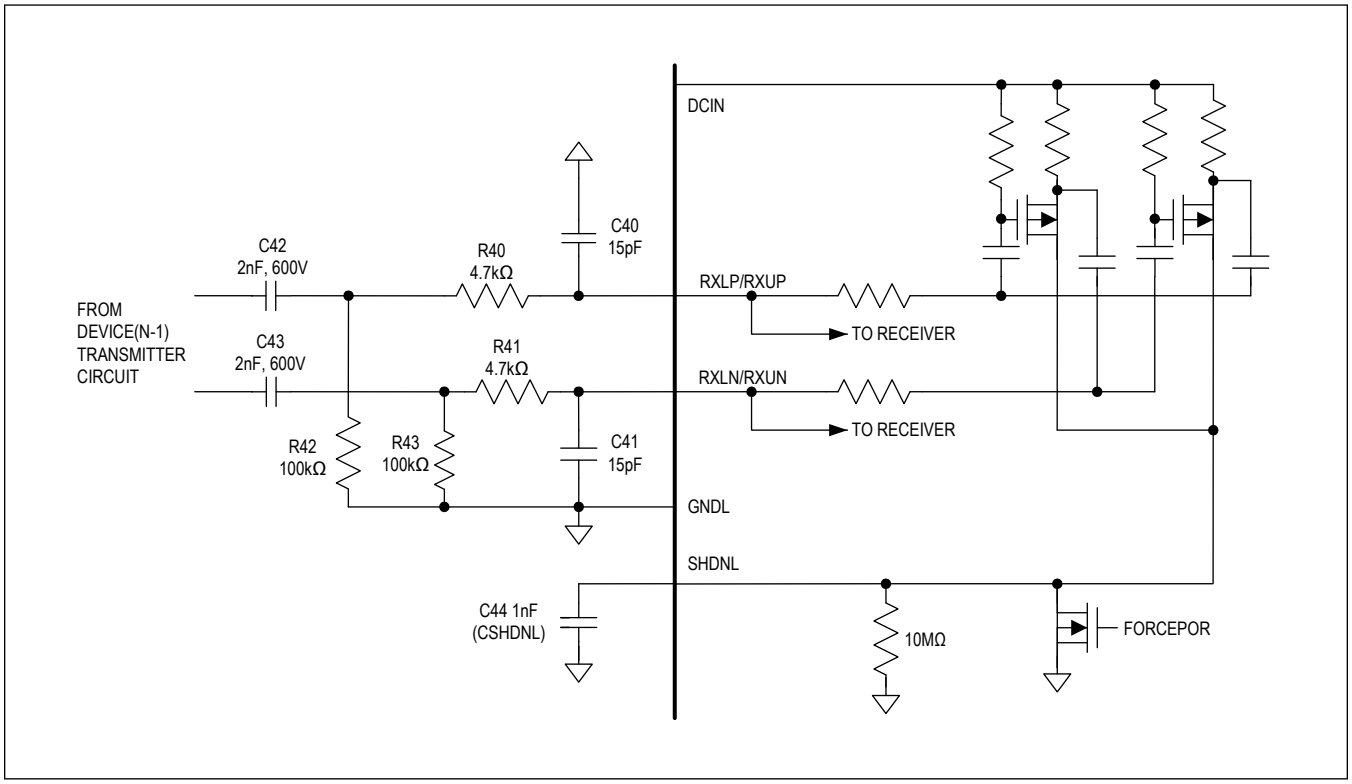


Figure 53. SHDNL Charge Pump

Baud-Rate Detection

The UART may operate at a baud rate of 2Mbps, 1Mbps, or 0.5Mbps. The baud rate is controlled by the host and is automatically detected by the device when the first preamble character is received after reset. If the host changes the baud rate, it must issue a reset and resend a minimum of 2 x n preambles (where n is number of devices) at the new baud rate. The 2 x n preambles are necessary since the transmitter for the upper port will not transmit data until the lower port receiver has detected the baud rate and, likewise, the transmitter on the lower port will not transmit data until the upper port receiver has detected the baud rate. A simple way to do this is for the host to start transmitting preambles and stop when a preamble has been received back at the host Rx port.

Sending 2 x n preambles will complete baud detection on all the n devices in the chain. To be able to receive a preamble back at the host Rx port, (2 x n) + 1 preambles must be sent.

Note: Baud rate for the dual-UART configuration is determined upon the initialization sequence of either the Up Path or Down Path. Both paths operate at the same communication rate.

Battery-Management UART Protocol

The battery-management UART protocol uses the following features to maximize the integrity of the communications:

- All transmitted data bytes are Manchester-encoded where each data bit is transmitted twice with the second bit inverted (G.E. Thomas convention).
- Every transmitted character contains 12 bits which include a start bit, a parity bit, and two stop bits.
- Read/write packets contain a CRC-8 packet error checking (PEC) byte.
- Each packet is framed by a preamble character and stop character.
- Read packets contains a data-check byte for verifying the integrity of the transmission.

The protocol is designed to minimize power consumption by allowing slave devices to shut down if the UART is idle for a

specified period of time. (See the *SHDNL Charge Pump* section for additional detail.)

Command Packet

A command packet is defined as a sequence of UART characters originating at the host. Each packet starts with a preamble character, followed by data characters, and ending with a stop character as shown in Figure 54. After sending a packet, the host either goes into idle mode or sends another packet.

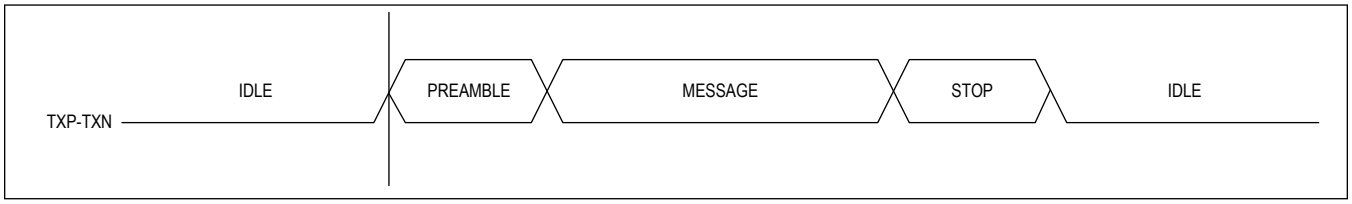


Figure 54. Command Packet

Preamble Character

The preamble is a framing character that signals the beginning of a command packet. It is transmitted as an unencoded 15h with a logic 1 parity bit and a balanced duty cycle. If any bit(s) other than the stop bits deviate from the unique preamble sequence, then the character is not interpreted as a valid preamble, but rather as a data character.

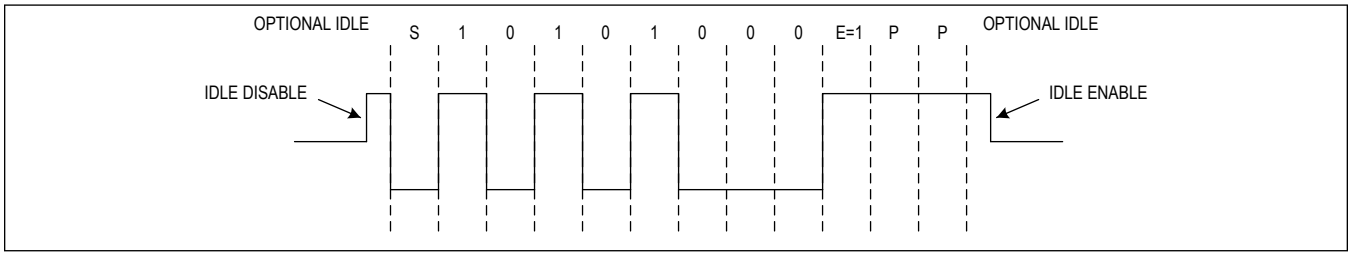


Figure 55. Preamble Character

Data Characters

Each data character contains a single-nibble (four-bit) payload, and so two characters must be transmitted for each byte of data. All data is transmitted least-significant bit, least-significant nibble, and least significant byte first. The data itself is Manchester encoded, meaning that each data bit is followed by its complement. If the UART detects a Manchester-encoding error in any received data character, it will set the ALRTMANUP, or ALRTMANDN bit in the STATUS2 register. All single-UART configurations set the ALRTMANUP bit. In a dual-UART configuration, a Manchester error in the UP path sets ALRTMANUP, and a Manchester error in the DOWN path sets ALRTMANDN.

The parity is even meaning that the parity bit's value should always result in an even number of logic 1 bits in the character. Given that the data is Manchester-encoded and that there are two stop bits, the parity bit for data characters is always transmitted as a logic 0. If the UART detects a parity error in any received data character, it will set the ALRTPARUP or ALRTPARDN bit in the STATUS register. All single UART configurations set the ALRTPARUP bit. In a DUAL UART configuration, a parity error in the UP path sets ALRTPARUP, and a parity error in the DOWN path sets the ALRTPARDN.

Table 39. Data Character Description

BIT	NAME	SYMBOL	DESCRIPTION
1	Start	S	First bit in character, always logic 0
2	Data0		Least significant bit of data nibble (true)
3	Data0/		Least significant bit of data nibble (inverted)

Table 39. Data Character Description (continued)

4	Data1		Data bit 1 (true)
5	Data1/		Data bit 1 (inverted)
6	Data2		Data bit 2 (true)
7	Data2/		Data bit 2 (inverted)
8	Data3		Most significant bit of data nibble (true)
9	Data3/		Most significant bit of data nibble (inverted)
10	Parity	E	Always logic 0 (even parity)
11	Stop	P	Always logic 1
12	Stop	P	Last bit in character, always logic 1

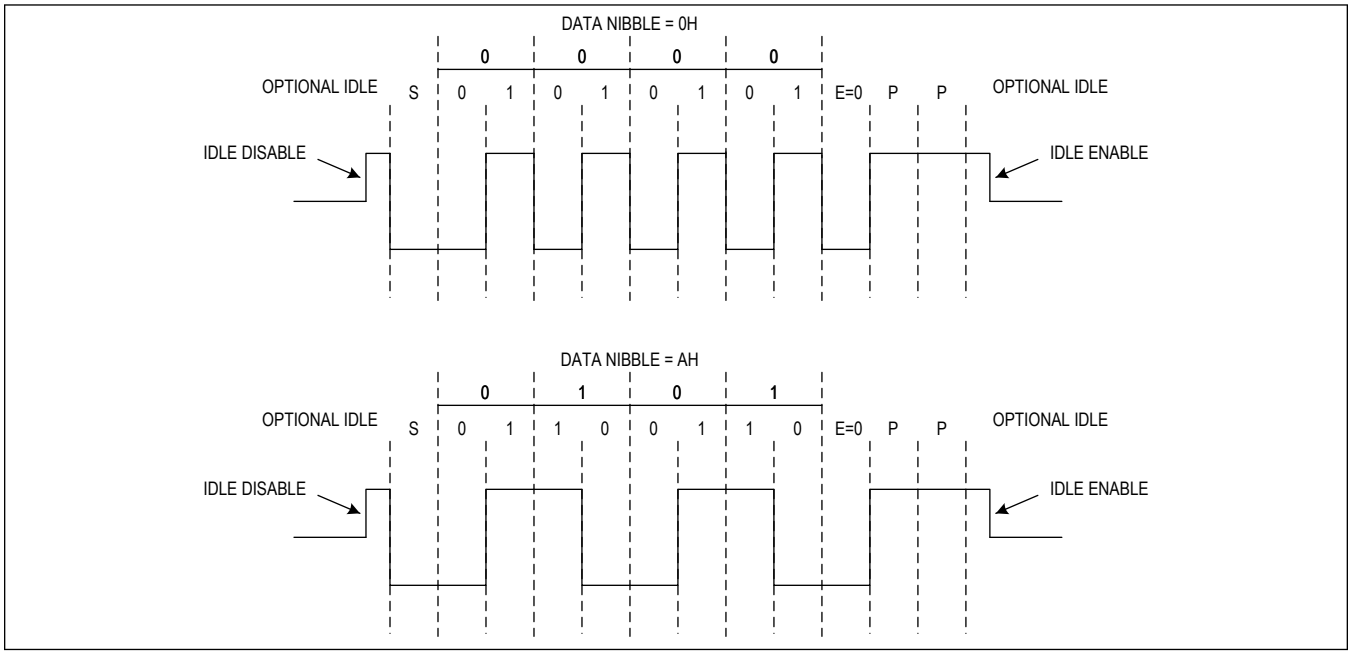


Figure 56. Data Characters

Stop Character

The stop character is a framing character that signals the end of a command packet. It is transmitted as an unencoded 54h with a logic 1 parity bit and a balanced duty cycle.

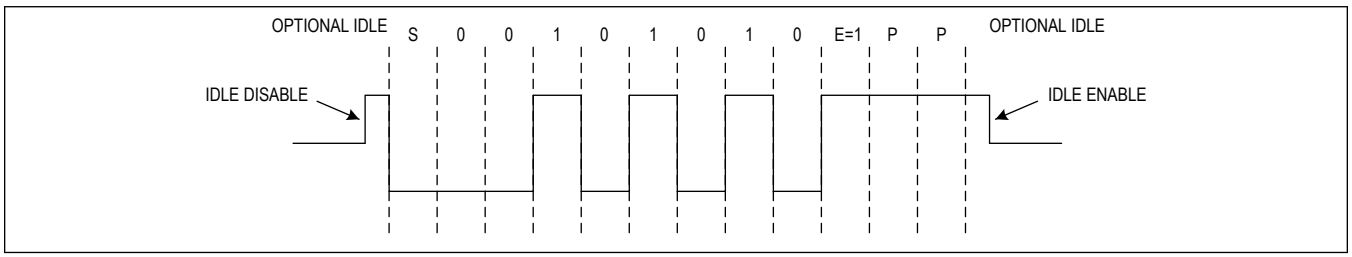


Figure 57. Stop Character

UART Idle Mode

In the low-Z (default) idle mode, the transmitter outputs are both driven to 0V as shown in Figure 58. In the high-Z idle mode, the transmitter outputs are not driven by the UART. The MAX17841 or MAX17851 interface automatically places its transmitter in idle mode immediately after each command packet and remains in idle mode until either the next command packet is sent or it goes into keep-alive mode, sending periodic stop characters to prevent the daisy-chained device(s) from going into shutdown.

UART Communication Mode

When transitioning from idle mode to communication mode, the TXP pin must be pulled high (logic 1) prior to signaling the start bit (logic 0) as shown in Figure 58. The duration of the logic 1 is minimized to maintain a balanced duty cycle while still meeting the timing specification. When transitioning from the stop bit back to idle mode, the delay (if any) is also minimized.

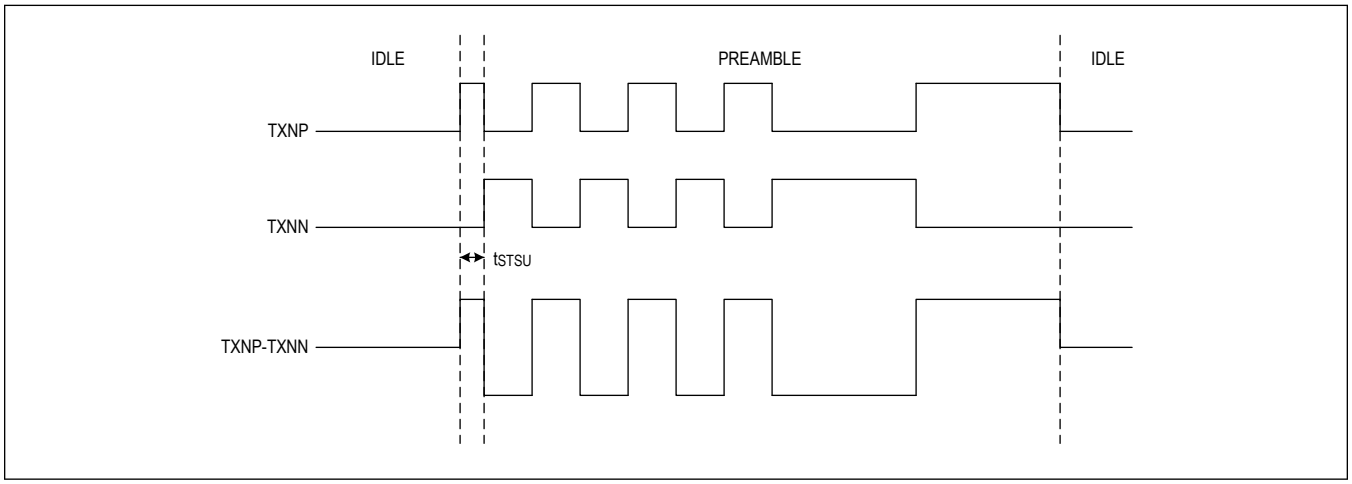


Figure 58. Communication Mode

Data Types

The battery-management UART protocol employs several different data types as described in Table 40.

Table 40. Data Types

DATA TYPE	DESCRIPTION
Command byte	A byte defining the command packet type, generally either a read or a write
Register address	A byte defining the register address to be read or written
Register data	Register data bytes being read or written
Data-Check byte	An error and alert status byte sent and returned with all reads
Packet-Error Checking byte	A packet-error checking byte (PEC) sent and returned with every packet except HELLOALL
Alive counter	A byte functioning as a device counter on all reads and writes, if ALIVECNTEN = 1
Fill byte	Bytes transmitted in READALL and READBLOCK command packets (clocking purposes only)

Command Bytes

The battery-management UART protocol supports eight command types summarized in Table 41.

Table 41. Command Packet Types

COMMAND	DESCRIPTION	DATA CHECK	PEC	ALIVE COUNTER	PACKET SIZE (CHARACTERS)

Table 41. Command Packet Types (continued)

HELLOALL	Writes a unique device address to each device in the daisy-chain. Required for system initialization.	No	No	No	8
WRITEALL	Writes a specified register in all devices.	No	Yes	Yes	14
WRITEDEVICE	Writes a specified register in a single device.	No	Yes	Yes	14
READALL	Reads a specific register from all devices.	Yes	Yes	Yes	12 + (4z)
READDEVICE	Reads a specified register from a single device.	Yes	Yes	Yes	16
READBLOCK	Reads a set of registers from a single device.	Yes	Yes	Yes	14 + (4* BS)
UPHOST	Makes the Up Path the master in a DUAL UART configuration. Sets bit field UARTHOST to 0b1.	No	Yes	No	10
DOWNHOST	Makes the Down Path the master in a DUAL UART configuration. Sets bit field UARTHOST to 0b0.	No	Yes	No	10

Note: z = total number of devices, ALIVECNTEN = 1, packet size includes framing characters

* Block size[4:0] = 1-32 which is the number of registers read.

Command Byte Encoding

Command bytes encoding is described in Table 42. For READDEVICE and WRITEDEVICE commands, the device address is encoded in the Command byte. The device ignores those commands containing a device address other than its own.

Table 42. Battery-Management Protocol Command Byte Encoding

COMMAND	BYTE*	7	6	5	4	3	2	1	0
HELLOALL	57h	0	1	0	1	0	1	1	1
ALERTPACKET	21h	0	0	1	0	0	0	0	1
WRITEDEVICE	04h	DA[4]	DA[3]	DA[2]	DA[1]	DA[0]	1	0	0
WRITEALL	02h	0	0	0	0	0	0	1	0
READDEVICE	05h	DA[4]	DA[3]	DA[2]	DA[1]	DA[0]	1	0	1
READALL	03h	0	0	0	0	0	0	1	1
READBLOCK	06h	BS[4]	BS[3]	BS[2]	BS[1]	BS[0]	1	1	0
DOWNHOST	09h	0	0	0	0	1	0	0	1
UPHOST	08h	0	0	0	0	1	0	0	0

*Assumes DA[4:0] = 0x00 where DA[4:0] is the device address in the ADDRESS register.

BS[4:0] = Block size (1-32)

Register Addresses

All register addresses are single-byte quantities and are defined in the Register Map. In general, if the register or device address in a received command is not a valid address for the device, the device will ignore the read or write and simply pass through the packet to the next device.

Register Data

All registers are 16-bit words (two data bytes) and are defined in the Register Map.

Data-Check Byte

The host uses the returned Data-Check byte to promptly determine if any communication errors occurred during the packet transmission and to check if alert flags are set in any devices, as shown in Table 43. Individual alert conditions can be masked out of the Data-Check byte using settings in ALRTIRQEN; however, the underlying alert information is always available for readback in the STATUS1 register. The Data-Check byte is returned by the READALL, READDEVICE, and

READBLOCK commands. For READDEVICE, the data-check byte is updated only by the addressed device.

The Data-Check byte sent by the host is a seed value normally set to 00h, although non-zero values may be used as a diagnostic. Each device logically ORs the received Data-Check byte with its own status and transmits it to the next device. A PEC error detected by any device sets the appropriate ALRTPECUP or ALRTPECDN bit in the STATUS2 register, and thus the ALRTPEC roll-up bit in the STATUS1 register. Also the device sets the PEC Error bit in the Data-Check byte within the associated path's command packet, as described in Table 43.

Table 43. Data-Check Byte

BIT	NAME	DESCRIPTION
7	PEC ERROR	PEC error detected during the current transaction on the Up/Down Path issuing this bit
6	ALRTFMEA	(ALRTFMEA1 & FMEA1ALRTEN) or (ALRTFMEA2 & FMEA2ALRTEN)
5	ALRTSTATUS	ALRTRST or (ALRTMSMTCH & MSMTCHALRTEN) or (ALRTBLKOVST & BLKOVALRTEN) or (ALRTBLKUVST & BLKUVALRTEN) or (ALRTINTRFC & INTRFCALRTEN) or (ALRTCAL & CALALRTEN) or (ALRTCBAL & CBALALRTEN)
4	AUXOV (UT)	(ALRTAUXOVST & AUXOVSTALRTEN)
3	AUXUV (OT)	(ALRTAUXUVST & AUXUVSTALRTEN)
2	CELLOV	(ALRTCELLOVST & CELLOVSTALRTEN)
1	CELLUV	(ALRTCELLUVST & CELLUVSTALRTEN)
0	RESERVED	0

Note: STATUS1[15]:ALRTSCAN is a procedural notification bit and is intentionally not included in the DCByte; it is available for inclusion in the ALERT Interface to support interrupt-driven applications. STATUS1[14]:ALRTRST indicates a POR condition, and thus cannot be masked. STATUS1[5]:ALRTPEC is intentionally not included in the DCByte.

PEC Byte

The PEC byte is a CRC-8 packet error check sent by the host with all read and write commands. If any device receives an invalid PEC byte, it sets the ALRTPECUP, or ALRTPECDN bit in the STATUS2 register, and also the ALRTPEC bit in the STATUS1 register. All single UART configurations set the ALRTPECUP bit. In a DUAL UART configuration, a PEC error in the UP path sets ALRTPECUP, and a PEC error in the DOWN path sets the ALRTPECDN. During any write transaction, a device does not execute the write command internally unless the received PEC matches the expected calculated value. For read commands, the device must return its own calculated PEC byte based on the returned data. The host should verify that the received PEC byte matches the calculated value and, if an error is indicated, the data should be discarded. See the *Applications Information* section for details on the PEC calculation.

Alive-Counter Byte

The Alive-Counter byte is the last data byte of the command packets (except HELLOALL, UPHOST, and DOWNHOST) if the ALIVECNTEN bit is set in the DEVCFG1 register. The host typically transmits the alive-counter seed value as 00h, but any value is permitted. For WRITEALL or READALL commands, each device retransmits the alive counter incremented by 1. For WRITEDEVICE or READDEVICE commands, only the addressed device will increment it. The alive-counter is not used in the HELLOALL, UPHOST, and DOWNHOST commands. If the alive-counter reaches FFh, the next device increments it to 00h.

Since the alive-counter comes after the PEC byte, an incorrect PEC value does not affect the incrementing of the Alive-Counter byte. Also, the PEC calculation does not include the Alive-Counter byte. The host should verify that the alive-counter equals the original seed value + the number of devices and, considering that if the alive counter reaches FFh, the next device increments it to 00h.

Fill Bytes

In the READALL command, the host sends two fill bytes for each device in the daisy-chain. The fill bytes are the locations within the packet and used by the device to place the read data. The fill byte values transmitted by the MAX17841 or MAX17851 interface alternate between C2h and D3h. As the command packet propagates through the device, the device overwrites the appropriate fill bytes with the register data. The device uses the ADDRESS register to determine which specific fill bytes in the packet are to be overwritten.

For a READBLOCK command, the number of fill bytes sent is equal to the read data block size.

For a READDEVICE command, only two fill bytes are required, since only one device responds (returning two data bytes). Also, fill bytes are not required for write commands because the data received is exactly the same as the data retransmitted.

Battery-Management UART Protocol Commands

HELLOALL Command

The HELLOALL command initializes the daisy-chained device addresses after a POR. The device addresses are stored in the DA[4:0] bits of the ADDRESS register with the highest address being 0x1F. Thus, a maximum of 32 devices may be addressed.

The device address bits (DA[4:0]) in the HELLOALL command packet are seeded by host µC. The command proceeds to the first device of the daisy-chain and is stored in that device's DA bits of the ADDRESS register. The first device is then incremented or decremented the HELLOALL command packet DA[4:0] bitfield according the UARTHOST configuration settling (see the *HELLOALL Operation in Dual-UART Configuration* section). Thus, the initial seeded value corresponds to the first device's address of the daisy-chain. The command continues to propagate to the next device until it returns to the host, at which point the host will be able to determine the total number of devices in the daisy-chain for subsequent READALL, READ DEVICE, READ BLOCK commands.

Table 44. HELLOALL Command Packet

HELLOALL
Preamble
57h
00h
{0b000,DA[4:0]}
Stop

HELLOALL Operation in Dual-UART Configuration

By default, dual-UART operation is configured with the primary communication path being the Up Path (see the UARTCFG and UARTHOST bits in the DEVCFG1 register for details about default and possible configurations), where the Up Path is defined as transmission from the TXU port to the RXL port. The DA[4:0] bits in the HELLOALL command packet are incremented as they progress up the daisy-chain. Thus, when the HELLOALL is received by the host microcontroller, the DA[4:0] value returned is one greater than address assigned to the top device.

It is recommended that the host seeds the initial address of the Up Path at a value of 0x00. This configuration applies the first address of the daisy-chain at the same value of the default condition of the bottom address (BA bits in the ADDRESS register). Thus it is not necessary to write the bottom address BA[4:0] to all of the devices. The host microcontroller should never set the bottom address at a value which would result in the device address exceeding 0x1F.

Note: The device address will only be stored and incremented in the Up Path and will pass through the Down Path, leaving the device address unaffected. As such, if the hardware is configured as a single daisy-chain and the UART is looped back using the Down Path, the UARTHOST configuration will prevent the Down Path from changing the device address that has already been determined.

Table 45. HELLOALL Up Path Sequencing

HELLOALL UP PATH SEQUENCING (z = TOTAL NUMBER OF DEVICES)			
HOST Tx	**DEVICE (n) RXL**	**DEVICE (n) TXU**	**HOST Rx**
Preamble	Preamble	Preamble	Preamble
57h	57h	57h	57h
00h	00h	00h	00h
{0b000,DA[4:0]}	{0b000,DA[4:0]+n-1}	{0b000,DA[4:0]+n}	{0b000,DA[4:0]+z}
Stop	Stop	Stop	Stop

The HELLOALL command packet can also be applied through the Down Path, where the Down Path is defined as transmission from the TXL port to the RXU port. For proper operation, the host µC must first send the DOWNHOST command through the Down Path prior to sending the HELLOALL.

The device address in the HELLOALL command packet is decremented as it progresses down the daisy-chain. Thus, the address of the top daisy-chain (first device in the Down Path) will be the value that is seeded in the DA[4:0] bits of the HELLOALL command packet. This top daisy-chained device proceeds to decrement the DA[4:0] and propagate the value down the daisy-chain. When the HELLOALL is received by the host µC, the DA[4:0] value returned is one less than address assigned to the bottom device. The host µC should never set the top address at a value that would result in a DA[4:0] decremented below 0x0.

After the HELLOALL is processed, the Top Address bits (TA bits) in the ADDRESS register must be set to the initial DA[4:0] seeded value.

It is recommended that the host seeds the initial address of the Down Path at a value equal to the number of devices in the daisy chain such that the bottom address is 0x00. This configuration ensures that whether the HELLOALL is sent through the Up Path or Down Path, the device address will remain the same, which will be ideal for consistency with the addressing of the READ DEVICE and READ ALL commands.

Note: The device address is only stored and decremented in the Down Path and passes through the Up Path, leaving the device address unaffected (i.e., HELLOALL sent in the Up Path with UARTHOST set to 1'b0).

Table 46. HELLOALL Down Path Sequencing

HELLOALL SEQUENCING (z = TOTAL NUMBER OF DEVICES)			
HOST Tx	**DEVICE (n) RXU**	**DEVICE (n) TXL**	**HOST Rx**
Preamble	Preamble	Preamble	Preamble
57h	57h	57h	57h
00h	00h	00h	00h
{0b000,ADDR[4:0]}	{0b000,ADDR[4:0]-(n-1)}	{0b000,ADDR[4:0]-n}	{0b000,ADDR[4:0]-z}
Stop	Stop	Stop	Stop

HELLOALL Operation in Single-UART Configuration

In single-UART configuration, the HELLOALL will be processed the same as in the dual-UART Up Path.

Special considerations exist if the host desires to use internal loopback instead of external loopback. The first HELLOALL command does not return to the host because the internal loopback (UARTCFG) for the top device has not yet been written. If the number of devices is known to the host, the host can use a WRITEDEVICE to set the internal loopback bit on the last device and then verify with a READALL. If the number of devices is unknown, the internal loopback bit must be set on the first device, verified, and then cleared. It can then be set on the second device and verified, and so on incrementally until there is no response (end of stack). With the number of devices known, the loopback bit can be reset on the top device and all ADDRESS registers verified.

HELLOALL Address Lock

When a device receives a valid HELLOALL command, it clears the ADDRUNLOCK bit of the ADDRESS register. When this bit is 0, HELLOALL commands are ignored to prevent inadvertently changing any device address. In order to reconfigure the device address, the ADDRUNLOCK bit must first be set to 1, or a POR event must occur. After configuring the device addresses, they should be verified using the READALL command.

WRITEALL Command

The WRITEALL command writes a 16-bit value to a specified register in all daisy-chained devices. Since most configuration information is common to all the devices, this command allows faster setup than writing to each device individually. If the register address is not valid for the device, the command is ignored. The command sequence is shown in Table 47.

The register value is written immediately after the valid PEC byte is received or, if NOPEC is set, after the last byte is received. If the received PEC byte does not match the internal calculation, the command is not executed, but is still

forwarded to the next device. The PEC is calculated from the first four bytes of the command starting after the preamble. If any device receives an invalid PEC byte, it sets the ALRTPECUP, or ALRTPECDN bit in the STATUS2 register, and also ALRTPEC bit in the STATUS1 register. All single-UART configurations set ALRTPECUP bit. In a dual-UART configuration, a PEC error in the UP path sets ALRTPECUP, and a PEC error in the DOWN path sets ALRTPECDN.

Table 47. WRITEALL Sequencing (Unchanged by Daisy-Chain)

HOST Tx	DEVICE(n) RXL (UP PATH) OR RXU (DOWN PATH)	DEVICE(n) TXU (UP PATH) OR TXL (DOWN PATH)	HOST Rx
Preamble	Preamble	Preamble	Preamble
02h	02h	02h	02h
[REG ADDR]	[REG ADDR]	[REG ADDR]	[REG ADDR]
[DATA LSB]	[DATA LSB]	[DATA LSB]	[DATA LSB]
[DATA MSB]	[DATA MSB]	[DATA MSB]	[DATA MSB]
[PEC]	[PEC]	[PEC]	[PEC]
[ALIVE]*	[ALIVE]*	[ALIVE]*	[ALIVE]*
Stop	Stop	Stop	Stop

* If Alive-Counter mode is enabled.

WRITEDEVICE Command

The WRITEDEVICE command writes a 16-bit value to the specified register in the addressed device only. If the register address is not valid for the device, the command is ignored. The command sequence is shown in Table 48.

The register value is written immediately after the valid PEC byte is received or, if NOPEC is set, after the last byte is received. If the received PEC byte does not match the internal calculation, the command is not executed, but is still forwarded to the next device. The PEC is calculated from the first 4 bytes of the command starting after the preamble. If the addressed device receives an invalid PEC byte, it sets the ALRTPECUP, or ALRTPECDN bit in the STATUS2 register, and also ALRTPEC bit in the STATUS1 register. All single-UART configurations set ALRTPECUP bit. In a dual-UART configuration, a PEC error in the Up Path sets ALRTPECUP, and a PEC error in the Down Path sets ALRTPECDN. A PEC error can only occur in the addressed device.

Table 48. WRITEDEVICE Sequencing (Unchanged by Daisy-Chain)

HOST Tx	DEVICE RXL (UP PATH) OR RXU (DOWN PATH)	DEVICE TXU(UP PATH) OR TXL (DOWN PATH)	HOST Rx
Preamble	Preamble	Preamble	Preamble
{(DA[4:0]),0b100}	{(DA[4:0]),0b100}	{(DA[4:0]),0b100}	{(DA[4:0]),0b100}
[REG ADDR]	[REG ADDR]	[REG ADDR]	[REG ADDR]
[DATA LSB]	[DATA LSB]	[DATA LSB]	[DATA LSB]
[DATA MSB]	[DATA MSB]	[DATA MSB]	[DATA MSB]
[PEC]	[PEC]	[PEC]	[PEC]
[ALIVE]*	[ALIVE]*	[ALIVE]*	[ALIVE]*
Stop	Stop	Stop	Stop

* If Alive-Counter mode is enabled.

READALL Command

The READALL command returns register data from the specified register for all daisy-chain devices. The data for the first device (connected to the host) is returned last. The command sequence is shown in Table 49 and Table 50. If the received PEC byte does not match the calculated value, the UART sets the ALRTPECUP, or ALRTPECDN bit in the STATUS2 register, and also ALRTPEC bit in the STATUS1 register. All single-UART configurations set the ALRTPECUP

bit. In a dual-UART configuration, a PEC error in the UP path sets ALRTPECUP, and a PEC error in the DOWN path sets the ALRTPECDN. However, the command proceeds to the next device in the daisy-chain. A Manchester error immediately switches the data propagation from read mode to write (pass-through) mode, insuring that the Manchester error is propagated through the daisy-chain and back to the host.

Table 49. READALL Command Sequencing in Single-UART or Dual-UART Up Path (z = Number of Devices)

HOST Tx	DEVICE(n) RXL	DEVICE(n) TXU	HOST Rx
Preamble	Preamble	Preamble	Preamble
03h	03h	03h	03h
[REG ADDR]	[REG ADDR]	[DATA ADDR]	[REG ADDR]
[DC] = 0x00	[DATA LSB(n-1)]	[DATA LSB(n)]	[DATA LSB(z)] = [DATA LSB(TA)]
[PEC]	[DATA MSB(n-1)]	[DATA MSB(n)]	[DATA MSB(z)] = [DATA MSB(TA)]
[ALIVE]*	...	...	[DATA LSB(z-1)] = [DATA LSB(TA-1)]
[FD(1) C2h]	...	...	[DATA MSB(z-1)] = [DATA MSB(TA-1)]
[FD(1) D3h]	[DATA LSB(1)] = [DATA LSB(BA)]	[DATA LSB(1)] = [DATA LSB(BA)]	...
[FD(2) C2h]	[DATA MSB(1)] = [DATA MSB(BA)]	[DATA MSB(1)] = [DATA MSB(BA)]	...
[FD(2) D3h]	[DC]	[DC]	...
...	[PEC]	[PEC]	...
...	[ALIVE]*	[ALIVE]*	...
...	[FD(1) C2h]	[FD(1) C2h]	...
...	[FD(1) D3h]	[FD(1) D3h]	[DATA LSB(1)] = [DATA LSB(BA)]
...	...	...	[DATA MSB(1)] = [DATA MSB(BA)]
...	...	...	[DC]
[FD(z) C2h]	[FD(z-n) C2h]	[FD(z-n-1) C2h]	[PEC]
[FD(z) D3h]	[FD(z-n) D3h]	[FD(z-n-1) D3h]	[ALIVE]*
Stop	Stop	Stop	Stop
12+(4 x z) characters	12+(4 x z) characters	12+(4 x z) characters	12+(4 x z) characters

* If Alive-Counter mode is enabled.

Table 50. READALL Command Sequencing in Dual-UART Down Path (z = Number of Devices)

HOST Tx	DEVICE(n) RXU	DEVICE(n) TXL	HOST Rx
Preamble	Preamble	Preamble	Preamble
03h	03h	03h	03h
[REG ADDR]	[REG ADDR]	[DATA ADDR]	[REG ADDR]
[DC] = 0x00	[DATA LSB(n-1)]	[DATA LSB(n)]	[DATA LSB(z)] = [DATA LSB(BA)]
[PEC]	[DATA MSB(n-1)]	[DATA MSB(n)]	[DATA MSB(z)] = [DATA MSB(BA)]
[ALIVE]*	...	...	[DATA LSB(z-1)] = [DATA LSB(BA +1)]
[FD(1) C2h]	...	...	[DATA MSB(z-1)] = [DATA MSB(BA +1)]

Table 50. READALL Command Sequencing in Dual-UART Down Path (z = Number of Devices) (continued)

[FD(1) D3h]	[DATA LSB(1)] = [DATA LSB(TA)]	[DATA LSB(1)] = [DATA LSB(TA)]	...
[FD(2) C2h]	[DATA MSB(1)] = [DATA MSB(TA)]	[DATA MSB(1)] = [DATA MSB(TA)]	...
[FD(2) D3h]	[DC]	[DC]	...
...	[PEC]	[PEC]	...
...	[ALIVE]*	[ALIVE]*	...
...	[FD(1) C2h]	[FD(1) C2h]	...
...	[FD(1) D3h]	[FD(1) D3h]	[DATA LSB(1)] = [DATA LSB(TA)]
...	...	...	[DATA MSB(1)] = [DATA MSB(TA)]
...	...	...	[DC]
[FD(z) C2h]	[FD(z-n) C2h]	[FD(z-n-1) C2h]	[PEC]
[FD(z) D3h]	[FD(z-n) D3h]	[FD(z-n-1) D3h]	[ALIVE]*
Stop	Stop	Stop	Stop
12+(4 x z) characters	12+(4 x z) characters	12+(4 x z) characters	12+(4 x z) characters

*If Alive-Counter mode is enabled.

The fill byte values transmitted by the MAX17841 or MAX17851 interface alternate between C2h and D3h as shown. As the packet propagates through the device, the device retransmits it in the order shown in the Table 49 (device TXU column). The device knows which bytes to overwrite since its ADDRESS register contains the top and bottom device addresses, and its own device address and therefore it knows where in the data stream it belongs.

READDEVICE Command

The READDEVICE command returns a 16-bit word read from the specified register in the addressed device only. If the register address is not valid for the device, the command is ignored. The command sequence is shown in Table 51 and Table 52.

The command packet is forwarded up the daisy-chain until it reaches the addressed device. The addressed device overwrites the received fill bytes with the two bytes of register data and forwards the packet to the next device. The Alive-Counter byte (if enabled) is only incremented by the addressed device. A Manchester error immediately switches the data propagation from read mode to write (pass-through) mode, ensuring that the Manchester error is propagated through the daisy-chain and back to the host.

Table 51. READDEVICE Sequencing in Single-UART or Dual-UART Up Path

HOST Tx	DEVICE RXL	DEVICE TXU	HOST Rx
Preamble	Preamble	Preamble	Preamble
{DA[4:0], 0b101}	{DA[4:0], 0b101}	{DA[4:0], 0b101}	{DA[4:0], 0b101}
[REG ADDR]	[REG ADDR]	[REG ADDR]	[REG ADDR]
[DC]	[DC]	[DATA LSB]	[DATA LSB]
[PEC]	[PEC]	[DATA MSB]	[DATA MSB]
[ALIVE]*	[ALIVE]*	[DC]	[DC]
[FD(1) C2h]	[FD(1) C2h]	[PEC]	[PEC]
[FD(1) D3h]	[FD(1) D3h]	[ALIVE]*	[ALIVE]*
Stop	Stop	Stop	Stop
16 characters	16 characters	16 characters	16 characters

*If Alive-Counter mode is enabled.

Table 52. READDEVICE Sequencing in Dual-UART Down Path

HOST Tx	DEVICE RXU	DEVICE TXL	HOST Rx
Preamble	Preamble	Preamble	Preamble
{DA[4:0], 0b101}	{DA[4:0], 0b101}	{DA[4:0], 0b101}	{DA[4:0], 0b101}
[REG ADDR]	[REG ADDR]	[REG ADDR]	[REG ADDR]
[DC]	[DC]	[DATA LSB]	[DATA LSB]
[PEC]	[PEC]	[DATA MSB]	[DATA MSB]
[ALIVE]*	[ALIVE]*	[DC]	[DC]
[FD(1) C2h]	[FD(1) C2h]	[PEC]	[PEC]
[FD(1) D3h]	[FD(1) D3h]	[ALIVE]*	[ALIVE]*
Stop	Stop	Stop	Stop
16 characters	16 characters	16 characters	16 characters

*If Alive-Counter mode is enabled.

READBLOCK Command

The READBLOCK command returns a 18-byte read from the specified register for a block size of 1 in the addressed device only. If the register address is not valid for the device, it returns 0 for any invalid addresses. If the device address is not valid, the command will be ignored. The command sequences for a block size of 1 are shown in Table 53 and Table 54. The command sequences for a block size of 2 are shown in Table 55 and Table 56. The command packet is forwarded up the daisy-chain until it reaches the addressed device. The addressed device overwrites the received fill bytes with the two bytes of register data (from a single device) and forwards the packet to the next device. The Alive-Counter byte (if enabled) is only incremented by the addressed device. A Manchester error immediately switches the data propagation from read mode to write (pass-through) mode, ensuring that the Manchester error is propagated through the daisy-chain and back to the host.

Table 53. READBLOCK Sequencing in Single-UART or Dual-UART Up Path Block Size = 1

HOST Tx	DEVICE RXL	DEVICE TXU	HOST Rx
Preamble	Preamble	Preamble	Preamble
{BS[4:0], 3b110}	{BS[4:0], 3b110}	{BS[4:0], 3b110}	{BS[4:0], 3b110}
[DEVICE ADDR]	[DEVICE ADDR]	[DEVICE ADDR]	[DEVICE ADDR]
[REG ADDR]	[REG ADDR]	[REG ADDR]	[REG ADDR]
[DC]	[DC]	[DATA LSB]	[DATA LSB]
[PEC]	[PEC]	[DATA MSB]	[DATA MSB]
[ALIVE]*	[ALIVE]*	[DC]	[DC]
[FD(1) C2h]	[FD(1) C2h]	[PEC]	[PEC]
[FD(1) D3h]	[FD(1) D3h]	[ALIVE]*	[ALIVE]*
Stop	Stop	Stop	Stop
18 characters	18 characters	18 characters	18 characters

* If Alive-Counter mode is enabled.

Table 54. READBLOCK Sequencing in Dual-UART Down Path Block Size = 1

HOST Tx	DEVICE RXU	DEVICE TXL	HOST Rx
Preamble	Preamble	Preamble	Preamble
{BS[4:0], 3b110}	{BS[4:0], 3b110}	{BS[4:0], 3b110}	{BS[4:0], 3b110}
[DEVICE ADDR]	[DEVICE ADDR]	[DEVICE ADDR]	[DEVICE ADDR]

Table 54. READBLOCK Sequencing in Dual-UART Down Path Block Size = 1 (continued)

HOST Tx	DEVICE RXU	DEVICE TXL	HOST Rx
[REG ADDR]	[REG ADDR]	[REG ADDR]	[REG ADDR]
[DC]	[DC]	[DATA LSB]	[DATA LSB]
[PEC]	[PEC]	[DATA MSB]	[DATA MSB]
[ALIVE]*	[ALIVE]*	[DC]	[DC]
[FD(1) C2h]	[FD(1) C2h]	[PEC]	[PEC]
[FD(1) D3h]	[FD(1) D3h]	[ALIVE]*	[ALIVE]*
Stop	Stop	Stop	Stop
18 characters	18 characters	18 characters	18 characters

* If Alive-Counter mode is enabled

Table 55. READBLOCK Sequencing in Single-UART or Dual-UART Up Path Block Size = 2

HOST Tx	DEVICE RXL	DEVICE TXU	HOST Rx
Preamble	Preamble	Preamble	Preamble
{BS[4:0], 3b110}	{BS[4:0], 3b110}	{BS[4:0], 3b110}	{BS[4:0], 3b110}
[DEVICE ADDR]	[DEVICE ADDR]	[DEVICE ADDR]	[DEVICE ADDR]
[REG ADDR]	[REG ADDR]	[REG ADDR]	[REG ADDR]
[DC]	[DC]	[DATA0 LSB]	[DATA0 LSB]
[PEC]	[PEC]	[DAT0 MSB]	[DATA0 MSB]
[ALIVE]*	[ALIVE]*	[DATA1 LSB]	[DATA1 LSB]
[FD(1) C2h]	[FD(1) C2h]	[DATA1 MSB]	[DATA1 MSB]
[FD(1) D3h]	[FD(1) D3h]	[DC]	[DC]
[FD(1) C2h]	[FD(1) C2h]	[PEC]	[PEC]
[FD(1) D3h]	[FD(1) D3h]	[ALIVE]*	[ALIVE]*
Stop	Stop	Stop	Stop
22 characters	22 characters	22 characters	22 characters

* If Alive-Counter mode is enabled.

Table 56. READBLOCK Sequencing in Single-UART or Dual-UART Down Path Block Size = 2

HOST Tx	DEVICE RXU	DEVICE TXL	HOST Rx
Preamble	Preamble	Preamble	Preamble
{BS[4:0], 3b110}	{BS[4:0], 3b110}	{BS[4:0], 3b110}	{BS[4:0], 3b110}
[DEVICE ADDR]	[DEVICE ADDR]	[DEVICE ADDR]	[DEVICE ADDR]
[REG ADDR]	[REG ADDR]	[REG ADDR]	[REG ADDR]
[DC]	[DC]	[DATA0 LSB]	[DATA0 LSB]
[PEC]	[PEC]	[DAT0 MSB]	[DATA0 MSB]
[ALIVE]*	[ALIVE]*	[DATA1 LSB]	[DATA1 LSB]
[FD(1) C2h]	[FD(1) C2h]	[DATA1 MSB]	[DATA1 MSB]
[FD(1) D3h]	[FD(1) D3h]	[DC]	[DC]

Table 56. READBLOCK Sequencing in Single-UART or Dual-UART Down Path Block Size = 2 (continued)

HOST Tx	DEVICE RXU	DEVICE TXL	HOST Rx
[FD(1) C2h]	[FD(1) C2h]	[PEC]	[PEC]
[FD(1) D3h]	[FD(1) D3h]	[ALIVE]*	[ALIVE]*
Stop	Stop	Stop	Stop
22 characters	22 characters	22 characters	22 characters

* If Alive-Counter mode is enabled.

DOWNHOST Command

Only one of the DUALUART paths (Up Path or Down Path) can be granted WRITE access through using the UPHOST or DOWNHOST commands; however, both paths have read access. The path that holds the WRITE access is specified using the UARTHOST register bit. By default, only the Up Path has the WRITE access (UARTHOST = 1b1).

The DOWNHOST command is used when WRITE access is required to be passed from the Up Path (UARTHOST = 1b1) to the Down Path (UARTHOST = 1b1). Alternatively, the UPHOST command is used when WRITE access is required to be passed from the Down Path to the Up Path. The UPHOST command is detailed in a different section.

When the DOWNHOST command is sent, each device modifies the UARTHOST bit in the DEVCFG1 register to change master control and also increments the DEVCOUNT variable as it sends the command to the next device, downstream, in the chain. The final value of DEVCOUNT received by the host equals the initial DEVCOUNT + total number of devices in the chain. If the DOWNHOST command is sent on the Up Path, the command will pass through the device unmodified, leaving the UARTHOST unchanged. The ALRTDUALUART bit will also be set in the STATUS2 register, signifying that an invalid command was received. Additionally, if the DOWNHOST command is sent on the Down Path while the Down Path is designated as the master, then the command will pass through the device unmodified while leaving the UARTHOST unchanged with the Down Path indication.

Note: The DOWNHOST command is relevant only when the device is configured in DUALUART mode. Sending the DOWNHOST command outside of a DUALUART configuration does not have any effect on the device and the command is passed through, unchanging the DEVCOUNT.

Table 57. DOWNHOST Sequencing (z = Total Number of Devices)

HOST Tx	DEVICE (n) RXU	DEVICE (n) TXL	HOST Rx
Preamble	Preamble	Preamble	Preamble
09h	09h	09h	09h
00h	00h	00h	00h
{0b000,DEVCOUNT[4:0]}	{0b000,DEVCOUNT[4:0]+n-1}	{0b000,DEVCOUNT[4:0]+n}	{0b000,DEVCOUNT[4:0]+z}
Stop	Stop	Stop	Stop

UPHOST Command

Only one of the DUALUART paths (Up Path or Down Path) can be granted WRITE access through using the UPHOST or DOWNHOST commands; however, both paths have read access. The path that holds the WRITE access is specified using the UARTHOST register bit. By default, only the Up Path has the WRITE access (UARTHOST = 1b1).

The UPHOST command is used when WRITE access is required to be passed from the Down Path (UARTHOST = 1b1) to the Up Path (UARTHOST = 1b1). Alternatively, the DOWNHOST command is used when WRITE access is required to be passed from the Up Path to the Down Path. The DOWNHOST command is detailed in a different section.

When the UPHOST command is sent, each device modifies the UARTHOST bit in the DEVCFG1 register to change master control and also increments the DEVCOUNT variable as it sends the command to the next device, upstream, in the chain. The final value of DEVCOUNT received by the host equals the initial DEVCOUNT + total number of devices in the chain. If the UPHOST command is sent on the Down Path, the command will pass through the device unmodified while leaving the UARTHOST unchanged, The ALRTDUALUART bit will also be set in the STATUS2 register, signifying

that an invalid command was received. Additionally, if the UPHOST command is sent on the Up Path while the Up Path is designated as the master, then the command will pass through the device unmodified while leaving the UARTHOST unchanged with the Up Path indication.

Note: The DOWNHOST command is relevant only when the device is configured in DUALUART mode. Sending the DOWNHOST command outside of a DUALUART configuration does not have any effect on the device and the command is passed through, unchanging the DEVCOUNT.

Table 58. UPHOST Sequencing (z = Total Number of Devices)

HOST Tx	DEVICE (n) RXL	DEVICE (n) TXU	HOST Rx
Preamble	Preamble	Preamble	Preamble
08h	08h	08h	08h
00h	00h	00h	00h
{0b000,DEVCOUNT[4:0]}	{0b000,DEVCOUNT[4:0]+n-1}	{0b000,DEVCOUNT[4:0]+n}	{0b000,DEVCOUNT[4:0]+z}
Stop	Stop	Stop	Stop

ALERTPACKET Command

The MAX17854 supports the transmission of an ALERT packet from either the host microcontroller or SPI to UART Bridge. This packet contains the alert Command byte, daisy chain module alert Data Address location (DA[4:0]), Alert Status byte, and the PEC byte of the protected data. See Table 59.

The module alert location is a 32-bit value that is split into 4 transmission data packets where each bit represents the device address (DA[4:0]) defined by the HELLOALL command. The Alert Status is the 16-bit output of the STATUS1 register, subject to masking through ALRTIRQEN, as described in Table 59. As the data passes through the daisy-chain, the Module Alert Location will contain a unique identifier while the STATUS output will be logically OR'ed to communicate the alert type. This creates a method to quickly assess the module status and health with little host interaction.

Table 59. ALERTPACKET Sequencing

ALERT PACKET
Preamble
Command Byte (0x21)
Module Alert Location 1 {(DA[4:7]), (DA[0:3])}
Module Alert Location 2 {(DA[12:15]),(DA[8:11])}
Module Alert Location 3 {(DA[20:23]),(DA[16:19])}
Module Alert Location 4 {(DA[28:31]),(DA[24:27])}
[STATUS LSB]
[STATUS MSB]
[PEC]
Stop

I²C Interface

The MAX17854 features an I²C-/SMBus-compatible, 2-wire master serial interface consisting of a serial data line (SDA) and a serial clock line (SCL). The interface is enabled/active if I2CEN is set high, in which case AUX/GPIO[0] is configured as an open-drain SDA I/O, and AUX/GPIO[1] is configured as an open-drain SCL output. In this configuration, the device is capable of functioning as an I²C-compatible master and is able to read and write to any number of associated I²C-compatible slave devices connected to the 2-wire bus at clock rates of 100kHz or 400kHz.

Note that the I²C master functionality is limited: the device must be the only master on the bus and is assumed to be the only device controlling the SCL line, as no provisions for arbitration are supported. In addition, the I²C master does not support slave devices that hold the clock low to force the master into a wait state (clock stretching). Clock stretching is optional and, in fact, most slave devices do not include an SCL driver so they are unable to stretch the clock.

I²C Timing Diagram and Data Format

The I²C timing diagram is shown in Figure 59. See the *Electrical Characteristics* table for complete timing specifications.

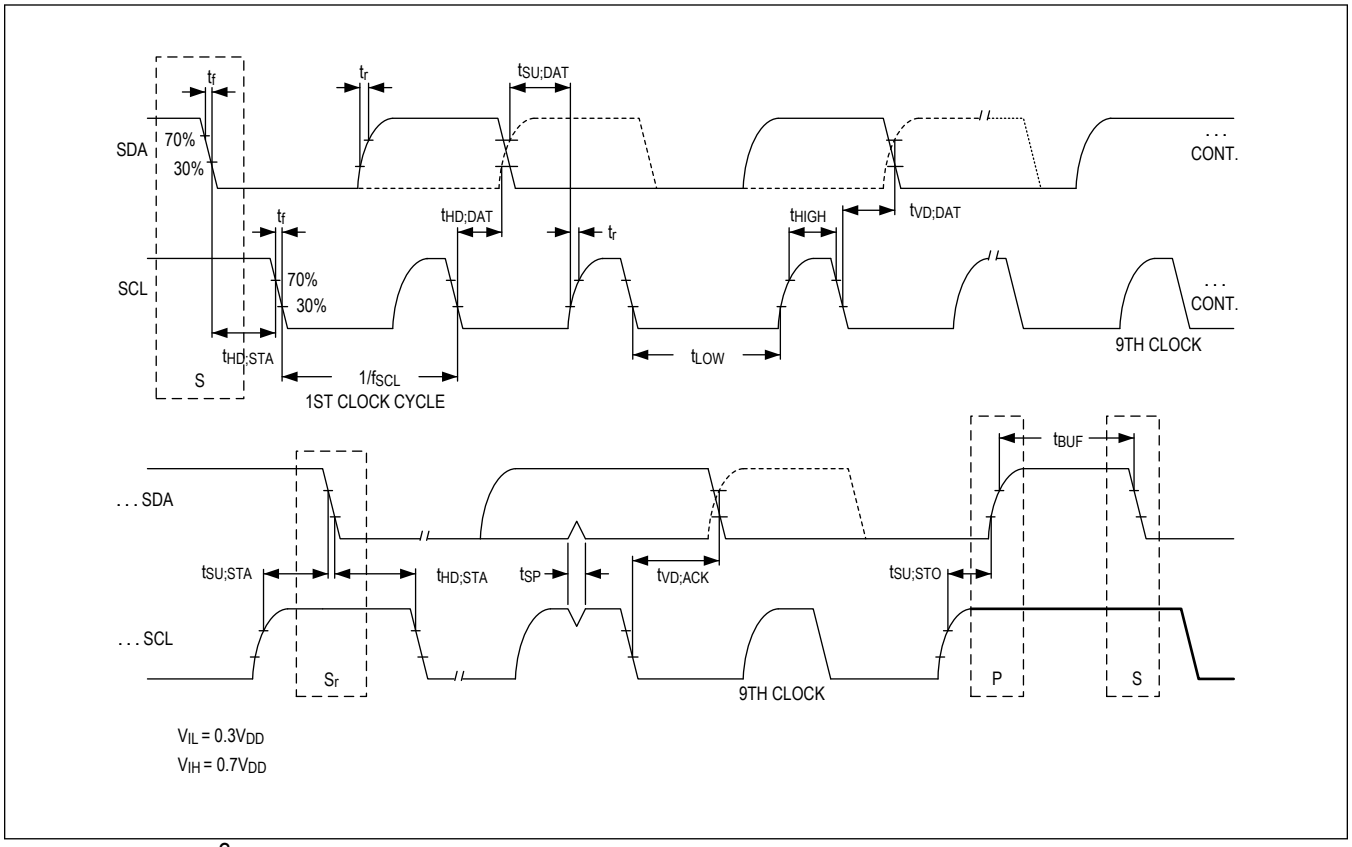


Figure 59. Standard I²C BUS Timing Diagram

I²C Start and Stop Conditions

SDA and SCL idle high when the bus is not in use. One data bit is transferred during each SCL cycle. The data on SDA must remain stable during the high period of the SCL pulse. Changing SDA while SCL is high results in control conditions being issued.

A high-to-low transition on the SDA line while SCL is high defines a START (S) condition. A low-to-high transition on the SDA line while SCL is high defines a STOP (P) condition. START and STOP conditions are always generated by the master. The bus is considered to be busy after the START condition. The bus is considered to be free again a certain time after the STOP condition. The bus stays busy if a repeated START (Sr) is generated instead of a STOP condition. In this respect, the START (S) and repeated START (Sr) conditions are functionally identical.

I²C Acknowledge and Not Acknowledge Conditions

An acknowledge (A or ACK) takes place after every byte sent/received. The acknowledge bit allows the receiver to signal the transmitter that the byte was successfully received and another byte may be sent. The master generates all clock pulses, including the acknowledge ninth clock pulse.

The ACK signal is defined as follows: the transmitter releases the SDA line during the acknowledge clock pulse so the receiver can pull the SDA line low and it remains stable low during the high period of this clock pulse. Setup and hold times must also be taken into account.

When SDA remains high during this ninth clock pulse, this is defined as the not acknowledge signal (~A or NACK). The

master will recognize a transaction failure if a slave device fails to acknowledge its address or a sent data byte. Note for all read mode transactions, the master will issue a NACK after the last byte of the transaction.

I²C Bus Construction

Pullup resistors, typically 4.7kΩ, are required on SDA and SCL. The I²C master includes slew control on the SCL and SDA output drivers, but custom slew profiles can be obtained by proper selection of pullup resistors and bus capacitance and/or the addition of inline resistors placed in series with the SCL and SDA outputs (see Figure 60). Series resistors can also protect the digital inputs from high-voltage spikes on the bus lines and minimize crosstalk and undershoot of the bus signals.

The I²C master can accommodate bus voltages higher than V_{IO} up to a limit of 5.5V; bus voltages lower than V_{IO} (V_{IO} is V_{DDL2} for this part) are not recommended and may result in significantly increased interface currents. Typically, the bus is terminated to the highest interface supply, if multiple supplies are required in the application.

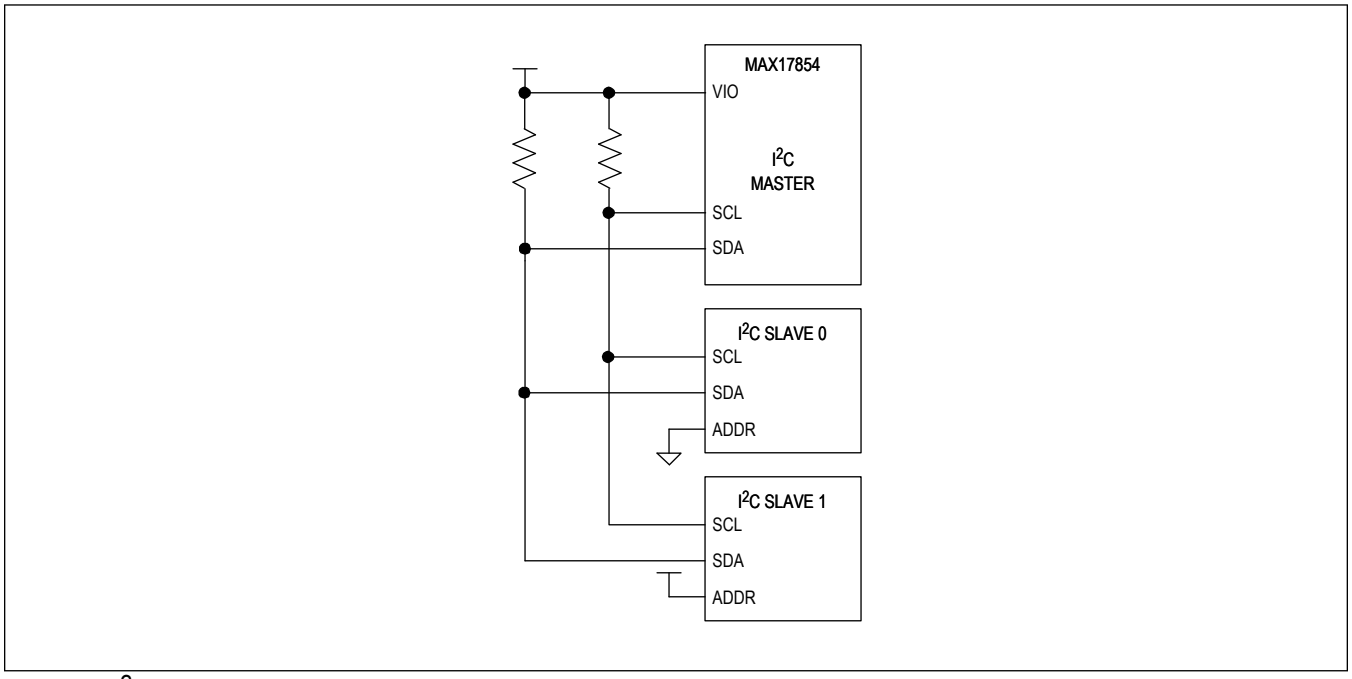


Figure 60. I²C Device Connection

I²C Master Configuration and Input Data

Prior to use, the I²C master must be configured by writing data to the registers described as follows. See the Register Map for detailed descriptions.

I2CCFG Register

I2CCFG includes all of the settings that govern the configuration and formatting of I²C read and write transactions to be performed by the master. This register can also be read back to verify contents. When communicating with slave devices of a single type, it is generally only necessary to write to the configuration register once.

I2CFSCL selects the I²C SCL frequency (0b0 = 100kHz, 0b1 = 400kHz).

I2CWALT sets the write mode data length options available. I2CWALT mode should only be used when it is necessary to send Write Mode transactions consisting only of slave addresses and a pointer (no data). Transactions of this type are sometimes required to set up pointers for use in Normal Format Read mode transactions. When I2CWALT mode is engaged, the 3-byte data length write option is replaced by a 0 byte data write option. Read length options are not impacted.

I2CRFMT selects the format used for read mode transactions (0b0 = normal, 0b1 = combined). Write mode transactions are not impacted.

I2C10BIT selects the slave address format used for all transactions (0b0 = 7 bit, 0b1 = 10 bit).

I2CPNTRLNGTH selects the number of bytes sent as the command portion of write and combined format read mode transactions (0b0 = 1 byte, 0b1 = 2 bytes). If 1-byte pointer mode is used (default, standard), both pointer bytes are available for use in I2C master transactions using I2CPNTRSEL (minimizing configuration time).

I2CALRTEN allows errors encountered during I2C transactions to be reported through ALRTI2C in the STATUS registers (0b0 = disabled, 0b1 = enabled). The alert will be cleared when I2CSTAT is read back and no new faults have been reported.

I2CANACONTEN enables analog bus contention monitoring and its associated alert component (0b0 = disabled, 0b1 = enabled).

I2CCONTEN enables digital bus contention monitoring and its associated alert component (0b0 = disabled, 0b1 = enabled).

I2CGLITCHEN enables bus glitch monitoring and its associated alert component (0b0 = disabled, 0b1 = enabled).

I2CNOISEEN enables bus noise monitoring and its associated alert component (0b0 = disabled, 0b1 = enabled).

I2CRDTREN enables redundant read mode checking and its associated alert component (0b0 = disabled, 0b1 = enabled).

I2CTOEN enables watchdog checking of I2C transactions using the 32kHz oscillator (0b0 = disabled, 0b1 = enabled).

I2CPNTR Register

This register contains I2CPBYTE1 and I2CPBYTE0 of pointer (command) data sent as the command portion of write and combined format read mode transactions. If I2CPNTRLNGTH = 0b0, either byte can be sent (selected by I2CPNTRSEL), so two I2C command transactions can be supported by writing to this register only once. If I2CPNTRLNGTH = 0b1, both bytes are sent. This register can also be read back to verify contents.

I2CWDATA Registers

The I2CWDATA1 and I2CWDATA2 registers contain 4 bytes of data that can be sent to slave devices during the data portion of Write mode transactions. Selection of which bytes and how many bytes are sent is determined by I2CDATALNGTH and I2CDATASEL. Thus for transactions of 1 or 2 bytes of data, it is possible for several Write mode transactions to be supported by writing to this register only once. This register can also be read back to verify contents.

I2C Transaction Requests and Results

Once the I2C master is properly configured and supplied with any required input data, transactions can be sent. See the Register Map for detailed descriptions.

I2CSEND Register

The I2C master generates initiates clock and data transactions on the bus in response to an accepted/qualified write to the I2CSEND command register. Each accepted/qualified write to this register initiates a transaction, unless a transaction is already in progress (in which case the new transaction request is ignored and the I2CRJCT alert component is set). Transaction progress and status can be monitored using the I2CSTATUS register. This register can also be read back to verify the specifics of the last accepted transaction.

I2CPNTRSEL selects the byte sent as the command portion of Write and combined format Read mode transactions (applicable only if I2CPNTRLNGTH = 0b0). If I2CPNTRLNGTH = 0b1 (2-byte pointer mode), this bit is ignored and both bytes are sent.

I2CDATALNGTH selects the number of data bytes to be sent in a Write mode transaction or received in a Read mode transaction.

I2CDATASEL selects the data register locations to be sent in Write mode transactions or filled during Read mode transactions. It also selects the location of the data bytes(s) to be transferred during write transactions and the target location for data byte(s) used for storage during read transactions. The selection indicates the location of the MSB of the data space used during the transaction; the number of bytes used is set by I2CDATALNGTH.

Some limitations do apply:

If I2CDATALNGTH = 0b11 (4 bytes), this selection is ignored and Bytes[3:0] are used.

If I2CDATALNGTH = 0b10 (3 bytes), this selection is ignored and Bytes[2:0] are used.

If I2CDATALNGTH = 0b01 (2 bytes), the LSB is ignored; for 0x, Bytes[1:0] are used, and for 1x, Bytes[3:2] are used.

If I2CDATALNGTH = 0b00 (1 byte), any of the four available bytes can be used.

If I2CDATALNGTH = 0b10 and I2CWALT = 0b1 (0-byte write), this selection is ignored and no bytes are used.

I2CDEVIDEXT and I2CDEVID are used to set the slave address sent during I2C transactions (I2CDEVIDEXT is only used if I2C10BIT = 0b1, otherwise it is ignored).

I2CRWB determines if the I2C transaction sent write (0) or read (1).

I2CRDATA Registers

The I2CRDATA1 and I2CRDATA2 registers contain 4 bytes (I2CRBYTE3, I2CRBYTE2, I2CRBYTE1, I2CRBYTE0) of memory that can be filled with data received from slave devices during the data portion of read mode transactions. Selection of which bytes are used in support of a Read mode transaction is determined by I2CDATALNGTH and I2CDATASEL. Thus, for transactions of 1 or 2 bytes of data, it is possible for several Read mode transactions to be supported by filling this register using multiple transactions while reading this register only once when filled. This register is read only.

Note: During Read commands, data is updated as each byte is received/acknowledged; reading back target registers during read transactions may yield corrupted results.

I2CSTAT Register

The I2CSTAT register provides information on active and completed I2C transactions.

I2CSTATUS reports the status of the last requested transaction and its resolution if completed. No Transaction (0b00) indicates no transaction has been requested since I2CSTAT was last read. Transaction in Progress (0b01) indicates the last requested transaction is in progress; this status will not be changed until the transaction terminates. Once a transaction is completed, the Transaction Complete (0b11, if successful) or Transaction Error (0b10, if unsuccessful) status is reported. A transaction error occurs if the following alert conditions are detected and enabled (I2CRJCT, I2CDEVNACK, and I2CDATANACK are always enabled). These status bits are cleared/updated when I2CSTAT is read back or when a new transaction is begun.

The remaining bits relate alert conditions if a problem was encountered.

I2CRJCT indicates one or more I2C transactions were rejected because a write to I2CSEND was attempted during an ongoing transaction. (Note that the ongoing transaction is not impacted).

I2CDEVNACK indicates the I2C transaction Device ID byte(s) were not acknowledged by a slave. This may indicate the slave is malfunctioning or not present on the bus. For Combined Format Read transactions, both slave address acknowledge pulses are required to avoid an error. The current I2C transaction will continue until completion. That is, the master will not issue a STOP bit immediately.

I2CDATANACK indicates one or more I2C transaction data byte(s) written were not acknowledged by a slave. This may indicate the slave is malfunctioning, not present on the bus, is busy, or has rejected an unsupported transaction. The current I2C transaction will continue until completion. That is, the master will not issue a STOP bit immediately.

I2CANACONT and I2CCONT indicate a bus contention condition was observed. Contention is reported when the port result does not match the value driven by the I2C master. This monitor observes the SCL port and the SDA port when driven by the I2C master. See the *I2C Bus Contention Monitor* section for more details.

I2CGLITCH indicates a bus glitch condition was observed. A glitch is reported when a port monitor reports two or more consecutive samples (125ns) that disagree with the evaluated value. This condition may also be reported if slow transition times, setup time, or hold time violations occur (outside I2C specifications). This monitor observes the SCL port and the SDA port outside specified transition intervals. See the *I2C Glitch Monitor* section for more details.

I2CNOISE indicates a noisy bus condition was observed. A noise condition is reported when a port monitor reports a large amount of samples that disagree with the evaluated value. This condition may also be reported if slow transition times, setup time, or hold time violations occur (outside I2C specifications). This monitor observes the SCL port and the

SDA port outside of specified transition intervals. See the *I²C Noise Monitor* section for more details.

I2CRDTRERR indicates the results of an I²C Redundant Read Transaction Check failed (enabled if I2CRDTREN = 0b1).

I2CTIMEOUT indicates the I²C transaction did not complete in the expected period of time (enabled if I2CTOEN = 0b1).This register is read only.

I²C Master Register Access During Active I²C Transactions

Since the I²C master register contents are in use during active I²C transactions, user interface access to the registers during ongoing I²C transactions is strictly controlled. Attempts to write or read content to/from these registers that may result in data corruption or synchronization issues are rejected and result in I2CSTAT:I2CRJCT and STATUS2:ALRTI2C being issued, notifying the user that the request has been ignored. Table 60 provides a summary of register accessibility by active I²C transaction and user transaction type. See the Register Map for complete details on all I²C master registers.

Table 60. Summary of I²C Register Access During Active I²C Transactions

I²C REGISTER	TYPE	DURING ACTIVE I²C WRITE TRANSACTIONS		DURING ACTIVE I²C READ TRANSACTIONS		COMMENT
		USER READ	USER WRITE	USER READ	USER WRITE	
I2CPNTR	R/W	Allowed	Rejected	Allowed	Rejected	Pointer data is protected during all I²C transactions
I2CWDATA1&2	R/W	Allowed	Rejected	Allowed	Rejected	Write data is protected during all I²C transactions
I2CRDATA1&2	R	Allowed	N/A	Rejected	N/A	Read data is updated during I²C Read transactions
I2CCFG	R/W	Allowed	Rejected	Allowed	Rejected	Configuration data is protected during all I²C transactions
I2CSTAT	R/W	Allowed	Rejected	Allowed	Rejected	Status data is protected during all I²C transactions
I2CSEND	R/W	Allowed	Rejected	Allowed	Rejected	Only a single I²C transaction at a time is supported

I²C Write Transactions

The I²C master initiates clock operation and data transfer on the bus in response to an accepted/qualified write to the I2CSEND command register with I2CRWB = 0b0. The master controls SCL for the entirety of the transaction. The master also controls the SDA line during all byte transfers, except those cycles reserved for acknowledge bits. The master writes data to associated slave devices by transmitting the selected slave address byte(s), followed by the command byte(s), and then the requested number of data bytes (0 to 4 byte data fields are supported in write mode). The write data comes from I2CWBYTE3, I2CWBYTE2, I2CWBYTE1, and I2CWBYTE0.

Each write mode transaction is framed by a START (S) condition and a STOP (P) condition generated by the master. After each byte sent, the addressed slave is expected to Acknowledge (A) receipt of the byte by pulling the SDA line low. The master will recognize and report a transaction failure if a slave device fails to acknowledge its address or a sent data byte, but the transaction will run to completion. In the event of a failure (I2CSTATUS = 0b10), the user may instruct the master to retry the transaction by issuing another I2CSEND command with the same content.

The following figures show I²C Write Mode Transaction examples Figure 61 using 7-bit and Figure 62 using 10-bit addressing, 1-byte pointer, and 2-byte data length (I2C10BIT = 0b0/1, I2CPNTRLENGTH = 0b0, I2CDATALNGTH = 0b01). Command/pointer widths of 1 or 2 bytes, and written data widths of 0 (command/pointer only) to 4 bytes can be achieved with alternate configuration settings. In general, it is assumed that 0-byte writes would only be used to set pointer locations for following normal format read transactions. When using 10-bit addressing, note that multiple slave devices may acknowledge Byte 1, but only the addressed slave device will acknowledge Byte 2.

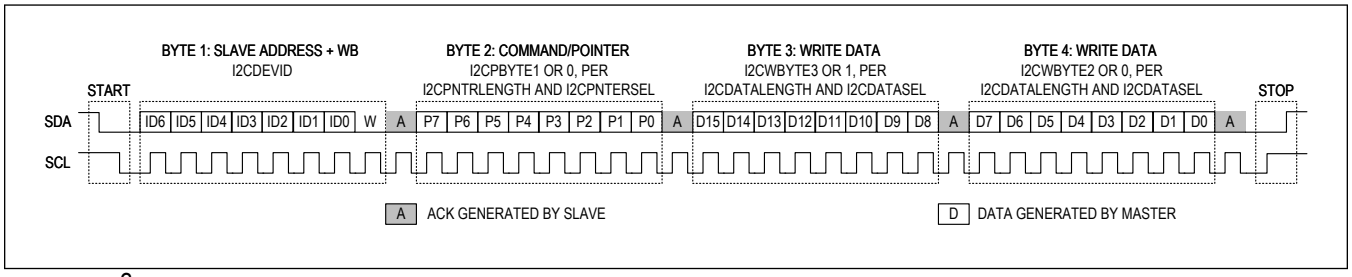


Figure 61. I²C Write Mode Transaction Example—7-Bit Address, I2C10BIT = 0

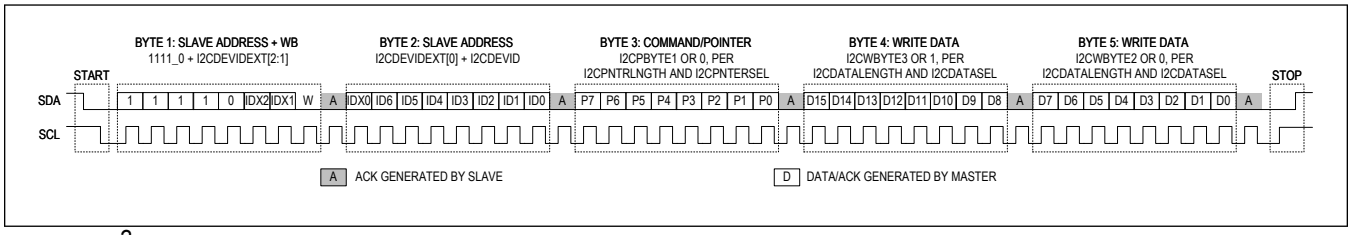


Figure 62. I²C Write Mode Transaction Example—10-Bit Address, I2C10BIT = 1

I²C Combined Format Read Transactions

In general, it is assumed that most slave devices are capable of supporting combined format read transactions, as this provides the most efficient use of the I²C master in terms of configuration and commands. Combined format read transactions are enabled when I2CRFMT = 0b1 (default).

The I²C master initiates clock operation and data transfer on the bus in response to an accepted/qualified write to the I2CSEND command register with I2CRWB = 0b1. The master controls SCL for the entirety of the transaction.

The transaction begins with a START (S) condition. The master controls the SDA line during all byte transfers of the write portion of the command (bytes preceding the REPEATED START (Sr)), except those clock cycles reserved for slave acknowledge bits. During this portion of the command, the master writes the selected pointer byte(s) to the slave, typically indicating which register contents are to be read back during the read portion of the command.

The master continues to control the SDA line during the initial byte of the read portion of the command (the byte immediately following the Sr). After the slave acknowledge bit for the initial address byte, the master shifts to receive mode and relinquish control of SDA to the slave for all incoming byte transfers. The master acknowledges each byte received from the slave by pulling SDA low during the ACK cycle following each byte transfer. A Not Acknowledge (NACK) is sent when the master reads the final byte of data from the slave, (determined by I2CDATALNGTH) before terminating the transaction with a STOP (P).

The following figures show I²C Combined Format Read Mode Transaction examples Figure 63 using 7-bit and Figure 64 using 10-bit addressing, 1-byte pointer, and 2-byte data length (I2C10BIT = 0b0/1, I2CPNTRLENGTH = 0b0, I2CDATALNGTH = 0b01. Command/pointer widths of 1 or 2 bytes and received data widths of 1 to 4 bytes can be achieved with alternate configuration settings. When using 10-bit addressing, note that multiple slave devices may acknowledge Byte 1, but only the addressed slave device will acknowledge Bytes 2, 3, and 4.

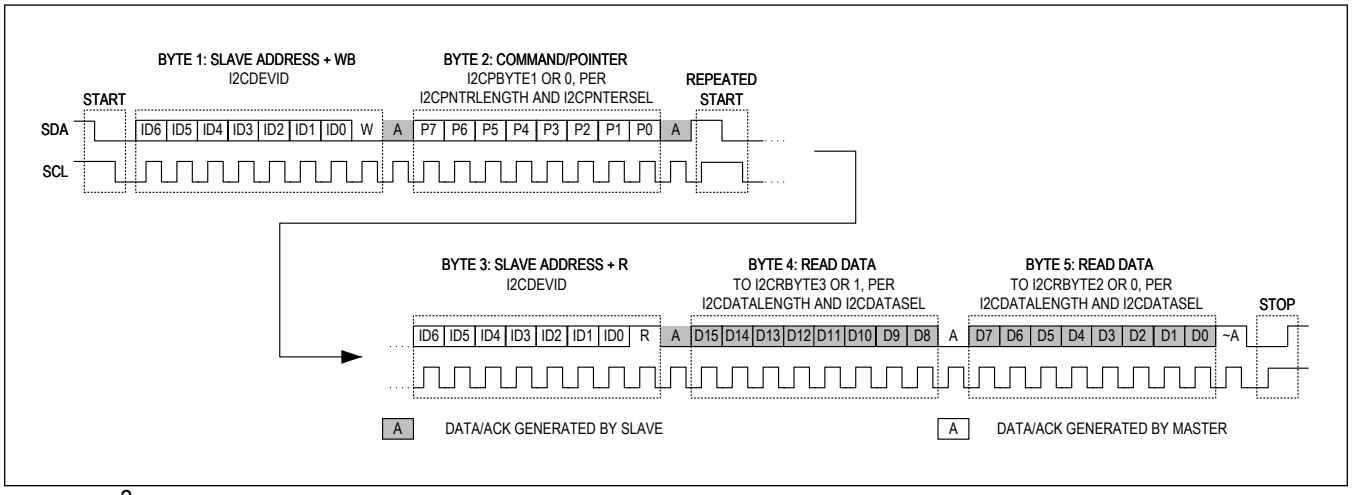


Figure 63. I²C Combined Format Read Mode Transaction Example—7-Bit Address, I2C10BIT = 0, I2CRFMT = 1

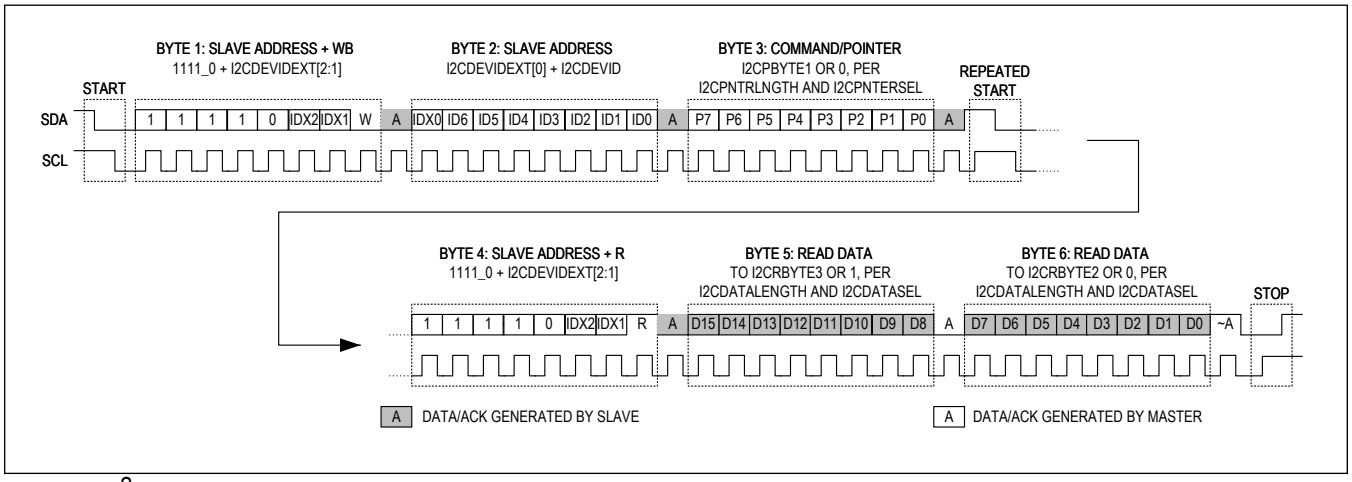


Figure 64. I²C Combined Format Read Mode Transaction Example—10-Bit Address, I2C10BIT = 1, I2CRFMT = 1

I²C Normal Format Read Transactions

In general, it is assumed that most slave devices are capable of supporting Combined Format Read Transactions, as this provides the most efficient use of the I²C master in terms of configuration and commands. However, for flexibility, the I²C master also supports Normal Format Read Mode Transactions. Note that, in a Normal Format Read Mode Transaction, there is no means of setting a pointer within the slave device to select what data is to be read back during the transaction itself. Combined format read transactions are enabled when I2CRFMT = 0b0.

Transactions of this type may be accompanied by a preceding Write Mode Transaction with no data (sending a slave address and pointer only). The I²C master can support transactions of this type with I2CWALT = 0b1 and I2CDATALENGTH = 0b10 in order to write the pointer location within a slave device.

Transactions of this type can also be used for immediate read back of a register previously written to a slave device. In this case, it is assumed that the pointer within the slave remains in the position used for the Write Mode Transaction. Therefore, if followed immediately by a Normal Format Read Mode Transaction, the data just written will be read back for confirmation.

Finally, if a slave device only has a single register location or FIFO, a pointer might not be required. Confirm exact device operation before using these transactions in an application.

7-Bit Address Transactions

The I2C master initiates clock operation and data transfer on the bus in response to an accepted/qualified write to the I2CSEND command register with I2CRWB = 0b1. The master controls SCL for the entirety of the transaction.

The transaction begins with a START (S) condition. The master controls the SDA line during the initial byte transfers associated with address portion of the transaction, except the clock cycle reserved for the slave acknowledge bit.

After the slave acknowledge bit for the initial byte, the master shifts to receive mode and relinquishes control of SDA to the slave for all incoming byte transfers. The master acknowledges each byte received from the slave by pulling SDA low during the ACK cycle following each byte transfer. A Not Acknowledge (NACK) is sent when the master reads the final byte of data from the slave (determined by I2CDATALNGTH) before terminating the transaction with a STOP (P).

The Figure 65 shows a Normal Format Read Mode Transaction example using 7-bit addressing, 1-byte pointer, and 2-byte data length (I2C10BIT = 0b0, I2CPNTRLENGTH = 0b0, I2CDATALNGTH = 0b01. Received data widths of 1 to 4 bytes can be achieved with alternate configuration settings.

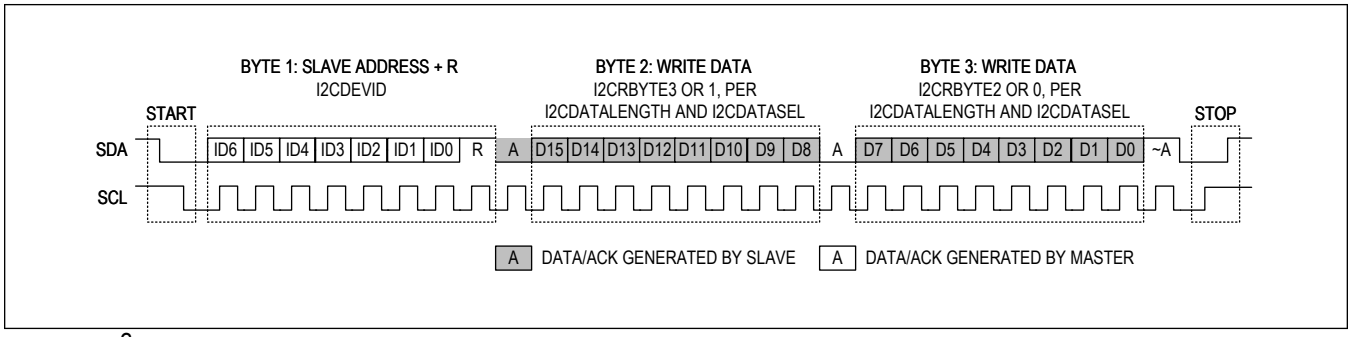


Figure 65. I2C Normal Format Read Mode Transaction Example—7-Bit Address, I2C10BIT = 0, I2CRFMT = 0

10-Bit Address Transactions

When using 10-bit addressing with I2CRFMT = 0b0, the structure of the Normal Format Read Mode Transaction is quite similar to the Combined Format transaction, except no pointer is sent during the write portion of the command. The I2C master initiates clock operation and data transfer on the bus in response to an accepted/qualified write to the I2CSEND command register with I2CRWB = 0b1. The master controls SCL for the entirety of the transaction.

The transaction begins with a START (S) condition. The master controls the SDA line during all byte transfers of the write portion of the command (bytes preceding the REPEATED START (Sr)), except those clock cycles reserved for slave acknowledge bits.

The master continues to control the SDA line during the initial byte of the read portion of the command (the byte immediately following the Sr). After the slave acknowledge bit for the initial address byte, the master shifts to receive mode and relinquishes control of SDA to the slave for all incoming byte transfers. The master acknowledges each byte received from the slave by pulling SDA low during the ACK cycle following each byte transfer. A NACK is sent when the master reads the final byte of data from the slave (determined by I2CDATALNGTH) before terminating the transaction with a STOP (P).

The Figure 66 shows an I2C Combined Format Read Mode Transaction example using 10-bit addressing, 1-byte pointer, and 2-byte data length (I2C10BIT = 0b1, I2CPNTRLENGTH = 0b0, I2CDATALNGTH = 0b01. Received data widths of 1 to 4 bytes can be achieved with alternate configuration settings. When using 10-bit addressing, note that multiple slave devices may acknowledge Byte 1, but only the addressed slave device acknowledges Bytes 2 and 3.

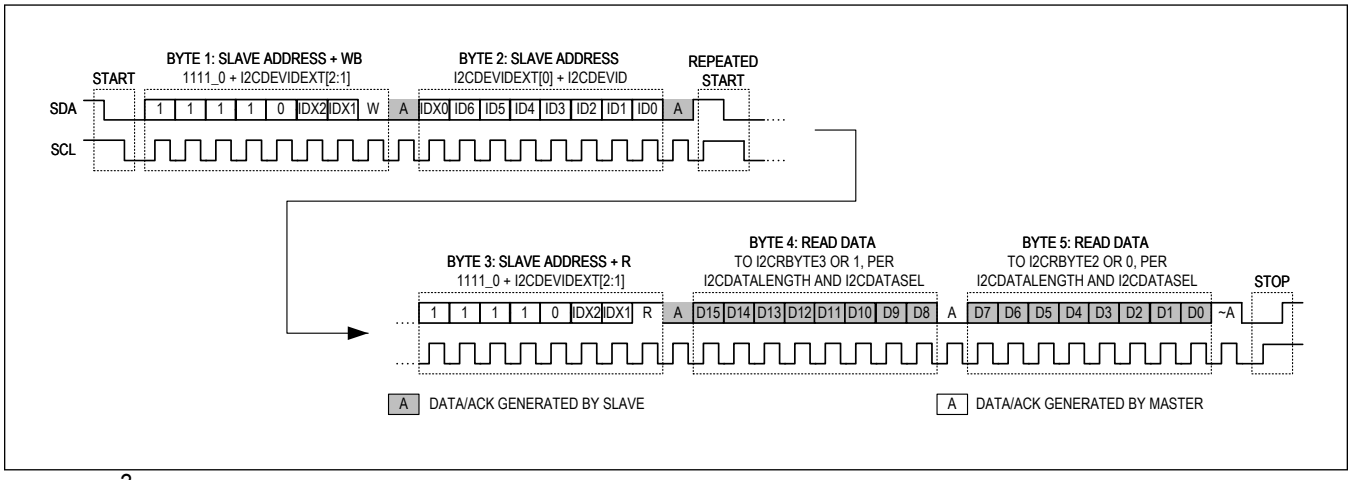


Figure 66. I²C Normal Format Read Mode Transaction Example—10-Bit Address, I2C10BIT = 1, I2CRFMT = 0

I²C Master Safety Features

The I²C master supports a variety of safety features to provide feedback on the quality of the interface transactions and the operation of the bus.

I²C Bus Contention Monitor

I2CCONT is reported when the evaluated port result does not match the value driven by the I²C master. This monitor observes the SCL port and the SDA port when driven by the I²C master. The contention monitor is always enabled. When I2CCONTEN = 0b1, STATUS2 register bit ALRTI2C is set if I2CCONT is set. When I2CCONTEN = 0b0, STATUS2 register bit ALRTI2C does not depend on the I2CCONT value.

I²C Bus Analog Contention Monitor

I2CANACONT is reported when the evaluated port result does not match the value seen on the analog filtered port. This monitor observes the SCL port and the SDA port when driven by the I²C master. The contention monitor is always enabled. When I2CANACONTEN = 0b1, STATUS2 register bit ALRTI2C is set if I2CANACONT is set. When I2CANACONTEN = 0b0, STATUS2 register bit ALRTI2C does not depend on the I2CANACONT value.

I2CANACONT vs. I2CCONT

I2CCONT monitors the raw value of the SDA/SCL ports. I2CANACONT monitors the internal analog filtered value of the SDA/SCL ports. The difference between I2CANACONT and I2CCONT is illustrated in the Figure 67 timing diagram.

The first diagram shows the fault of a weak pullup resistor on GPIO[0]. At the time evaluation (green dotted line), the raw value (observed response) is slightly above V_{IH}. However, the analog filtered value is still below V_{IH}. Thus, only I2CANACONT is set.

The second diagram shows the fault when the I²C slave prematurely pulls GPIO[0] low while the I²C master is still driving it high. Since the slave pulls GPIO[0] less than 1 analog filter time constant before the master pulls it low, the analog filtered value is still high but the raw value is low. Thus, only I2CCONT is set.

The third diagram shows the fault when GPIO[0] is stuck low. Both I2CANACONT and I2CCONT are set.

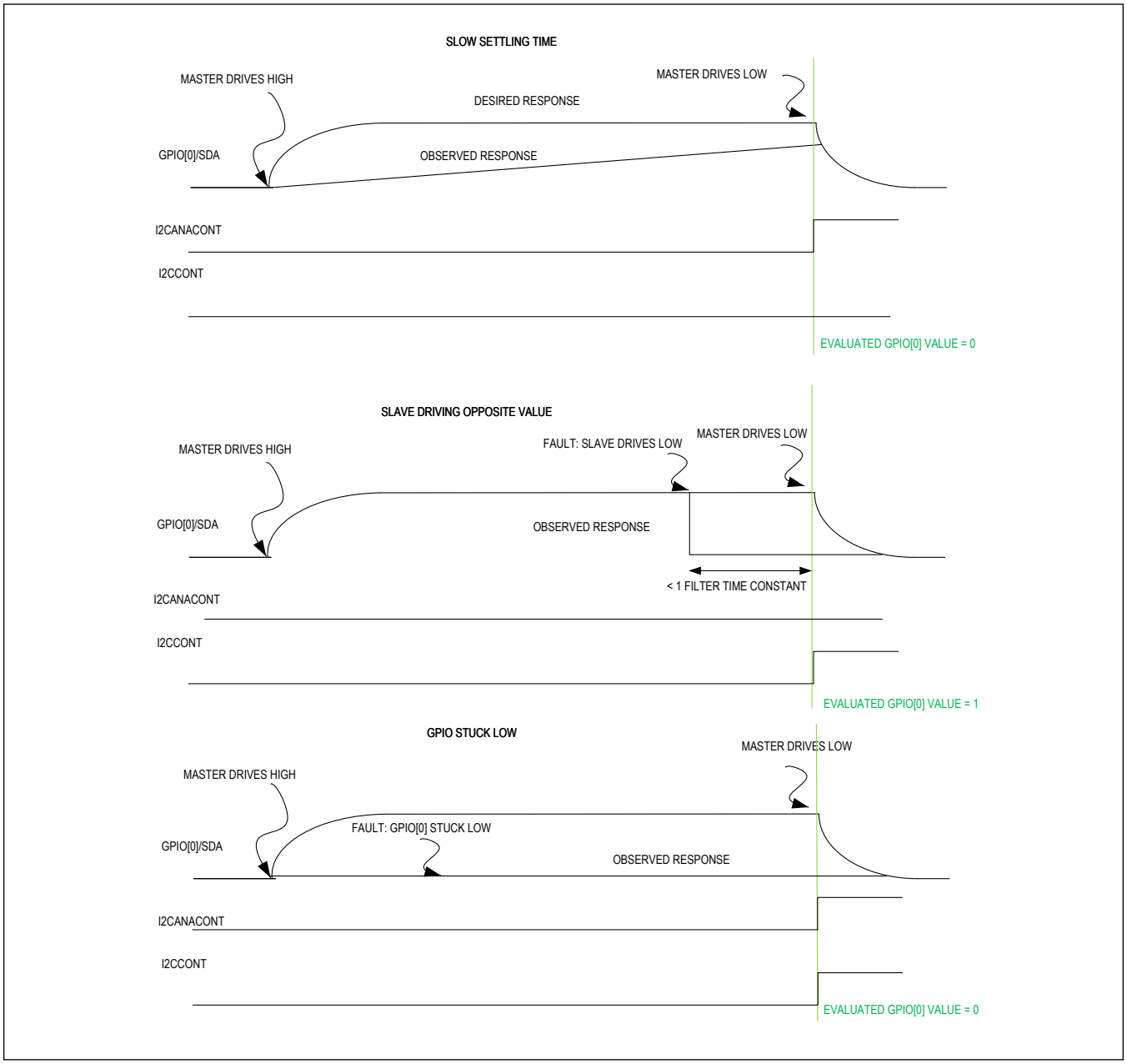


Figure 67. GPIO, I2CANACONT, and I2CCONT Timing Diagram

I²C Glitch Monitor

I2CGLITCH is reported when a port monitor reports two or more consecutive HFOSC samples that disagree with the evaluated filter value. This condition may also be reported if slow transition times, setup time, or hold time violations occur (outside I²C specifications). This monitor observes the SCL port and the SDA port outside specified transition intervals. The glitch monitor is always enabled. When I2CGLITCHEN = 0b1, STATUS2 register bit ALRTI2C is set if I2CGLTICHEN is set. When I2CGLITCHEN = 0b0, STATUS2 register bit ALRTI2C does not depend on the I2CGLITCH value.

I²C Noise Monitor

I2CNOISE condition is reported when a port monitor see more than 25% of samples that disagree with the evaluated filter value. This condition may also be reported if slow transition times, setup time, or hold time violations occur (outside I²C specifications). This monitor observes the SCL port and the SDA port outside specified transition intervals. The noise monitor is always enabled. When I2CNOISEEN = 0b1, STATUS2 register bit ALRTI2C is set if I2CNOISE is set. When I2CNOISEEN = 0b0, STATUS2 register bit ALRTI2C does not depend on the I2CNOISE value.

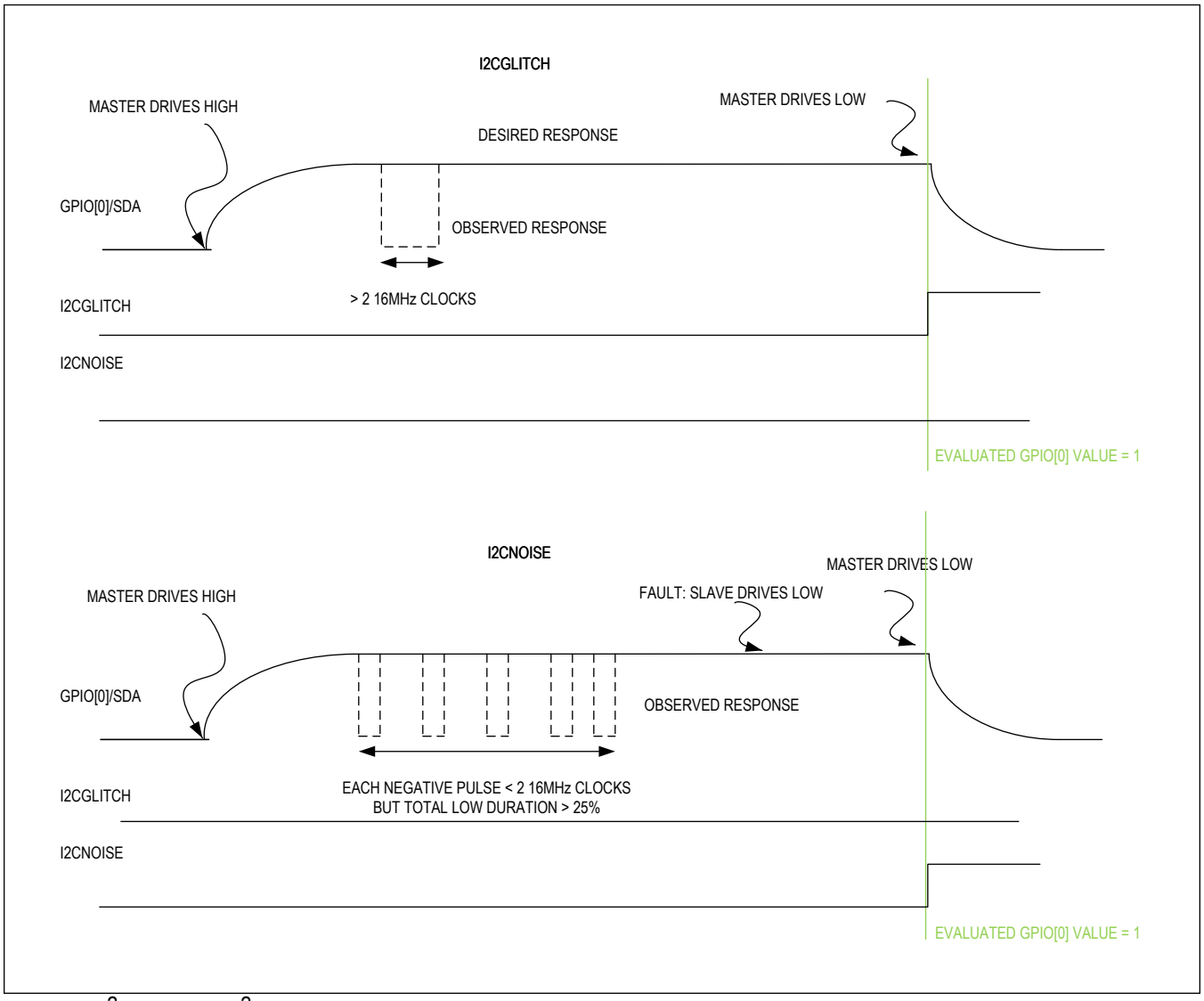


Figure 68. I²C Glitch and I²C Noise Monitor

I²C Repeated Read Checks

If Redundant Read Checking is enabled (I2CRDTREN = 0b1), all I²C Read Transactions will be automatically repeated twice in their entirety. The data received in the initial transaction is loaded into the register space specified by I2CDATALNGTH and I2CDATASEL as the transaction progresses. During the repeated transaction, the redundant data is checked against the data received in the initial transaction before the data in register space specified by I2CDATASEL is overwritten with the redundant data.

If any mismatch is found, the I2CSTATUS will read back a Transaction Error (0b10) and the I2CRDTRERR alert component bit will be set high for the transaction. While the redundant data from the repeated transaction is made available for readback in the register space specified, this data should be treated as compromised if I2CRDTRERR is set.

Note that Redundant Read Checking may not be advisable in some applications—in particular, if the slave device updates register content autonomously (and could change the data during/between the redundant transactions), or if the data requested is subject to noise (as might be the case if the read transaction triggers a measurement/observation which is read back). If used to read a FIFO with a pointer subject to increment upon readback, this method will not work. Special consideration should be given when using Normal Format Read Transactions—in particular, if slave pointers are autoincremented in response to read transactions, results may be incompatible with transactions of this type (without a preceding Write Transaction to reset the pointer to the original location). Review the operation of all slave devices carefully before using this feature.

There is no Write mode equivalent of a redundant check. Write mode transactions are best checked for success through a readback of written slave register content, assuming the slave register supports R/W access.

I²C Watchdog Timer

The I²C watchdog timer monitors all transactions for completion in the expected time required for the command. If the I²C watchdog timer is enabled (I2CTOEN = 0b1), the I²C master transaction is monitored for completion against a time out limit based on the transaction requested and mode settings. If the transaction fails to complete, the transaction will be aborted (stopped), any missing read data bytes will not be updated, I2CSTATUS will show a Transaction Error (0b10), and the I2CTIMEOUT fault indicator bit will be set high. The I²C watchdog timer counts in 32kHz clock increments—488µs for 400kHz operation and 1953µs for 100kHz operation—while I2CSEND is enabled. If terminal time is reached before completion of the current transaction, I2CSEND is cleared, the I2CTIMEOUT fault indicator bit is set, and the master returns to idle state (SDA = SCL = pulled high).

Freeing a Stuck I²C Bus

In the unlikely event of an aborted I²C transaction (due to either an I²C time out fault, or an unexpected reset of the MAX17854), it is possible for a slave device to occupy the SDA bus and hold it in a low position. This would prevent the MAX17854 from issuing new transactions until the slave device vacates the SDA bus, allowing the I²C master to send START and STOP information. If this were to occur, contention errors would be reported.

I²C Method (I2CEN = 1):

In order to recover, I²C write transactions should be sent to a nonexistent slave Device ID. The recommended transaction is a 7-bit address, single-byte data I²C Write transaction with all DEVID, PBYTE, and WBYTE content set to ones. Eventually the slave device occupying the bus will recognize the SCL activity, vacate the SDA bus, and observe the STOP condition. Contention errors will continue to be reported until the bus is freed. Normal I²C communication should then be restored, and new transactions to valid slave Device IDs can proceed.

GPIO Method (I2CENB = 0):

Alternatively, the bus can be freed by sending a stream of SCL pulses until the stuck slave device finishes its transaction and frees the bus. This can be accomplished by setting I2CEN = 0, configuring AUX0/SDA as a GPIO input (GPIOEN[0] = 1, GPIODIR[0] = 0, GPIODRV = x), and configuring AUX1/SCL as a GPIO output (GPIOEN[1] = 1, GPIODIR[1] = 1, GPIODRV = toggle). Send SCL pulses using GPIODRV[1], until the slave frees SDA (GPIORD[0] = 1 for a sustained number of SCL cycles). Once the slave vacates the bus, it will be able to observe the START/STOP conditions present in normal I²C transactions, and communication will be restored.

Alert Interface

The alert interface communicates the presence of a fault condition generated from the logical OR of the STATUS1 register, which flags any error within safety critical functionality: voltage measurements, temperature measurements, interface communication robustness, calibration, and other internal hardware diagnostics. As safety considerations may differ per platform, each of the associated alerts can be masked to provide individualized control. Additionally, the alert interface may be actively driven without an actual alert condition to validate functionality. This is done using the ALRTUSER bit in the FMEA2 register.

Alert Interface Configuration

ALERTOUT is an AC CMOS output. By default, the Alert Interface uses a single-ended, unidirectional path using the ALERTIN and ALERTOUT pins. The ALERTIN pin is configured as a single-ended UART receiver with RXP grounded (see the *UART Receiver* section for details). The ALERTOUT pin uses a single-UART transmitter as its output driver.

Alternatively, a differential alert path can be configured as using the UARTCFG bits. The UART Up Path is used for read and write commands with a direct wire return path from the last device in the chain to the µC. The Down Path is used as a differential alert path. The single-ended alert path is disabled—the ALERTOUT pin idles and the ALERTIN pin is disabled.

The Differential Alert Interface allows for robust, low-cost applications using capacitive isolation to communicate the presence of a fault. The Single-Ended Alert Interface allows for full UART flexibility using alternate isolation components (optoisolators).

Table 61. Alert Interface Configuration

UARTCFG	UART CONFIGURATION	UART UP PATH	UART DOWN PATH	SINGLE-ENDED ALERT
0b00	Single-UART Interface with External Loopback	Active	Inactive (Buffered/Pass Through)	ALERTEN Configured
0b01	Single-UART Interface with Internal Loopback	Active	Inactive (Buffered/Pass Through)	ALERTEN Configured
0b10	Single-UART Interface with Differential Alert Interface	Active	Differential Alert	Disabled (except in ALRTDCTSTEN mode)
0b11	Dual-UART Interface	Active	Active	ALERTEN Configured

If the Alert Interface is disabled, then no alerts can be communicated through the hardware interface. The ALERTIN pin remains a high impedance input and does not respond to any input signaling. Table 62 describes the configuration of the ALERTOUT output drivers for both single-ended and differential operation.

Note: Although the Alert Interface hardware can be disabled, the user may still validate alerts by reading the STATUS registers as well as verifying the UART Data-Check byte.

Table 62. Alert Output Driver Configuration

ALERTDCTSTEN	UARTCFG	ALERTOUT ACTIVE/ASSERTED	ALERTOUT INACTIVE/ DEASSERTED OR ALERTEN = 0
0	0b00, 0b01, 0b11	AC Active	GND (TXLIDLEHIZ = 0) Hi-Z (TXLIDLEHIZ = 1)
0	0b10 (Differential)	GND (TXLIDLEHIZ = 0) Hi-Z (TXLIDLEHIZ = 1)	GND (TXLIDLEHIZ = 0) Hi-Z (TXLIDLEHIZ = 1)
1	Don't Care	0	1

Alert Operation with UART Interface

The Alert Interface outputs a 2MHz continuous square wave with 50% duty cycle in the presence of a fault condition. The fault output persists for the duration of the fault and is updated at the rate determined by the scan mode. For a valid alert command to be recognized at the ALERTIN pin, the signal must be valid for 25µs and at the desired frequency. If the duration is shorter than the allocated time or at a different frequency, then this will not be recognized as fault and the signal will not be propagated to the host. See Figure 69.

In the absence of an alert, the output status depends on TXLIDLEHIZ - TXLIDLEHIZ = 1'b1, ALERTOUT is driven high-Z, and TXLIDLEHIZ = 1'b0, ALERTOUT is driven low.

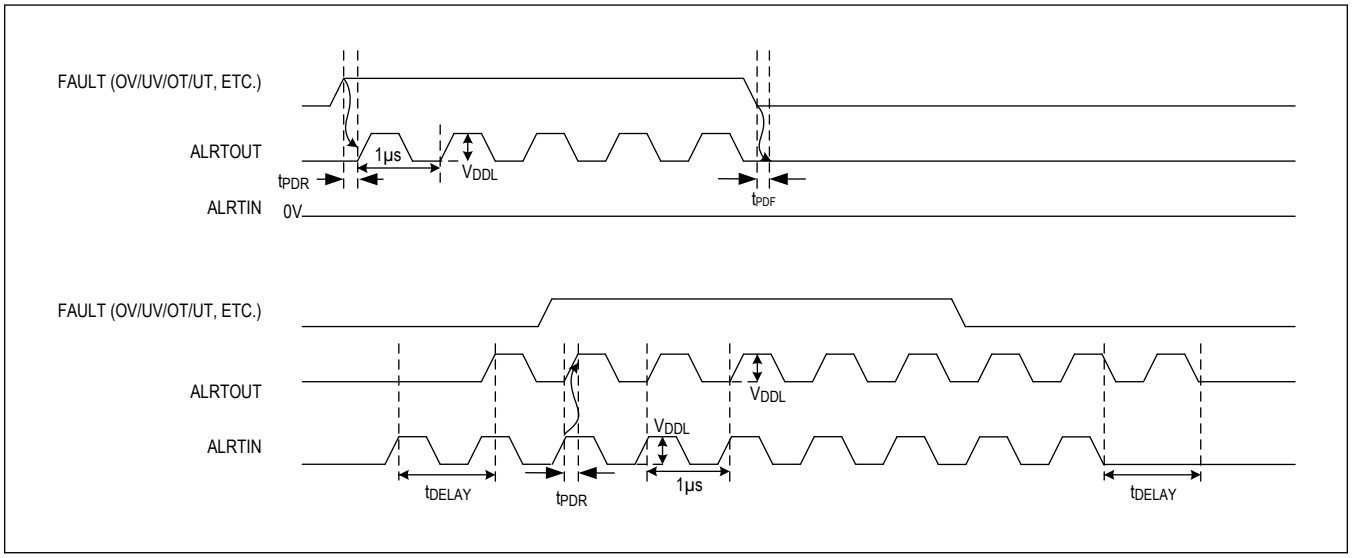


Figure 69. Alert Detection Timing Diagram

Alert Interface Masking

Alert Interface activity is based on the contents of the STATUS1 register. Individual alert conditions can be masked out of the Alert Interface using settings in ALRTIRQEN; however, the underlying alert information is always available for readback in the STATUS1 register.

Active =

(ALRTSCAN & SCANALRTEN) or ALRTRST or (ALRTMSMTCH & MSMTCHALRTEN) or

(ALRTCELLOVST & CELLOVSTALRTEN) or (ALRTCELLUVST & CELLUVSTALRTEN) or

(ALRTBLKOVST & BLKOVALRTEN) or (ALRTBLKUVST & BLKUVALRTEN) or

(ALRTAUXOVST & AUXOVSTALRTEN) or (ALRTAUXUVST & AUXUVSTALRTEN) or

(ALERTPEC & PECALRTEN) or (ALRTINTRFC & INTRFCALRTEN) or

(ALRTCAL & CALALRTEN) or (ALRTCBAL & CBALALRTEN) or

(ALRTFMEA1 & FMEA1ALRTEN) or (ALRTFMEA2 & FMEA2ALRTEN)

Note: ALRTRST indicates a POR condition, and thus cannot be masked.

ALERTPACKET STATUS Masking

The UART ALERTPACKET content is based on the contents of the STATUS1 register. Individual alert conditions can be masked out of the Alert Packet using settings in the ALRTIRQEN register; however, the underlying alert information is always available for read back in the STATUS1 register. The masking operations for each STATUS1 bit is detailed as follows:

ALRT_PKT_STAT[15] = 0

ALRT_PKT_STAT[14] = ALRTRST

ALRT_PKT_STAT[13] = (ALRTMSMTCH & MSMTCHALRTEN)

ALRT_PKT_STAT[12] = (ALRTCELLOVST & CELLOVSTALRTEN)

ALRT_PKT_STAT[11] = (ALRTCELLUVST & CELLUVSTALRTEN)

ALRT_PKT_STAT[10] = (ALRTBLKOVST & BLKOVALRTEN)

ALRT_PKT_STAT[9] = (ALRTBLKUVST & BLKUVALRTEN)

ALRT_PKT_STAT[8] = (ALRTAUXOVST & AUXOVSTALRTEN)

ALRT_PKT_STAT[7] = (ALRTAUXUVST & AUXUVSTALRTEN)

ALRT_PKT_STAT[6] = 0

ALRT_PKT_STAT[5] = (ALRTPEC & PECALRTEN)

ALRT_PKT_STAT[4] = (ALRTINTRFC & INTRFCALRTEN)

ALRT_PKT_STAT[3] = (ALRTCAL & CALALRTEN)

ALRT_PKT_STAT[2] = (ALRTCBAL & CBALALRTEN)

ALRT_PKT_STAT[1] = (ALRTFMEA1 & FMEA1ALRTEN)

ALRT_PKT_STAT[0] = (ALRTFMEA2 & FMEA2ALRTEN)

Note: STATUS1[15]:ALRTSCAN is a procedural notification bit and is intentionally not included in the ALERTPACKET data; it is available for inclusion in the Alert Interface to support interrupt-driven applications. STATUS1[14]:ALRTRST indicates a POR condition, and thus cannot be masked.

Alert Masking TOPCELL1/2

If the battery stack contains less than 14 cells and the flexible-pack configuration is not enabled, then lowest-order inputs (e.g., C1 and C0) should be utilized first and connected to the lowest common-mode signals. Any unused cell inputs should be shorted together and unused switch inputs should be shorted together. The TOPCELL1 and TOPCELL2 registers will mask all ALRTBALSW diagnostics from being reported.

All selections are supported for this function and, if TOPCELL2 is not equal to TOPCELL1, no alerts are masked.

Voltage Regulators

The MAX17854 has two linear voltage regulators: a low voltage (V_{AA}) and high voltage (V_{DDL}) regulator. The high-voltage regulator draws power from DCIN, whereas the low voltage powers off the high-voltage regulator (V_{DDL}). V_{AA} supplies power to ADC and internal digital blocks, whereas V_{DDL} powers the communication interface. The high-voltage regulator is disabled in the absence of a valid DCIN supply voltage or when the die temperature (T_{SHDN}) exceeds +145°C.

Once V_{DDL} decays below 4.5V (typ), an ALRTVDDL flag is issued in FMEA1 register as summarized in Table 64 and shown in Figure 70. It should be noted that ALRTVDDL will not be flagged until the ALRTRST bit is cleared; therefore, it is recommended that the user should clear the ALRTRST bit after the initial powerup. The low-voltage regulator POR event can be detected with the ALRTRST bit, as shown in Table 64. After a thermal shutdown, the regulator will not be enabled until T_{SHDN} < +130°C, due to hysteresis.

Table 63. High-Voltage Regulator Operation Characteristics

INPUT	V_{DCIN}
OUTPUT	V_{DDL}
DISABLE	T_{SHDN} > +145°C

Table 64. High-/Low-Voltage Regulator Diagnostic

FAULT	CONDITION	ALERT	LOCATION
V_{DDL} undervoltage	V_{DDL} < 4.5V	ALRTVDDL	STATUS1.ALRTFMEA1
V_{AA} undervoltage	V_{AA} < 1.65V	ALRTRST	STATUS1.ALRTRST

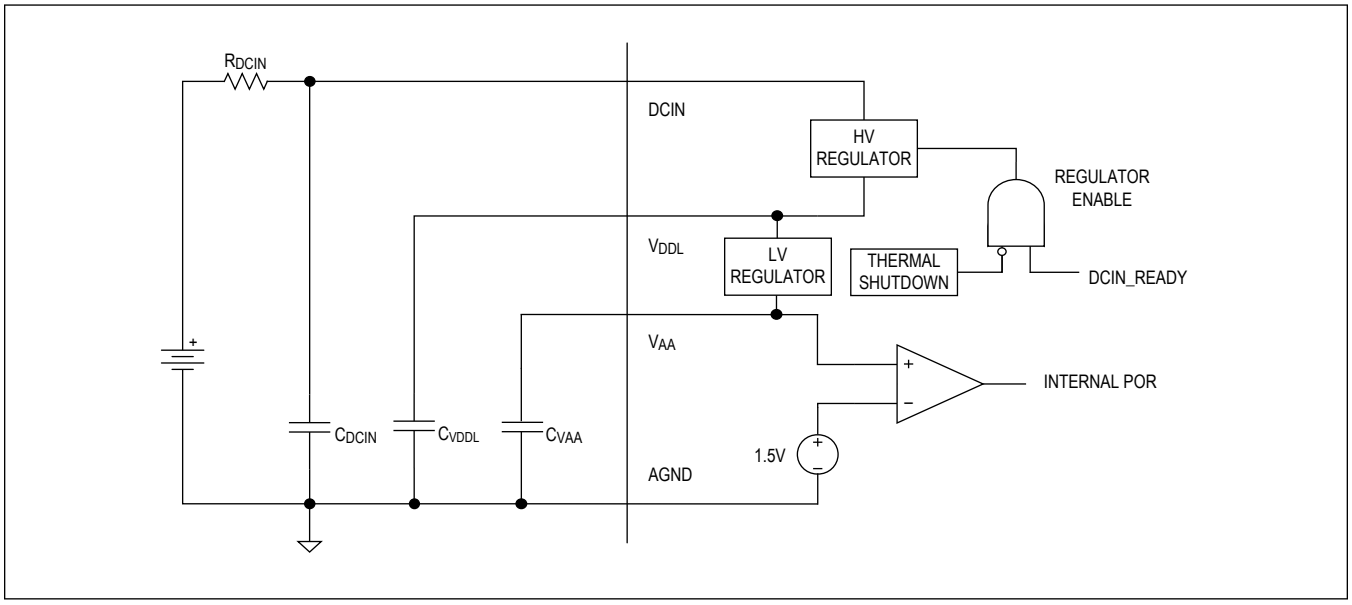


Figure 70. HV/LV Regulator and Thermal Shutdown Circuit

HV Charge Pump

The high-voltage multiplexers must be powered by a supply higher than any monitored voltage. To this end, an internal charge pump draws power from the DCIN pin to provide a high-voltage supply V_{HV}, which is regulated to $V_{DCIN} + V_{HV-DCIN}$. When the charge pump achieves regulation, $V_{HV-DCIN}$, charge pumping stops until the voltage drops by 20mV. The charge pump is automatically disabled during shutdown.

During the measurement cycle for ADC, comparator, ADC+COMP, and calibration, the charge pumping is paused to eliminate any potential impact of the charge-pump noise within the measurements. The charge pump then becomes active, operating on an 83kHz clock, during an intercharge time (defined as the time between consecutive scan sequences) that lasts for 57µs on the ADC, comparator, and ADC+COMP. During calibration, the intercharge time is reduced to 21µs. The intercharge time ensures that the charge on C_{HV} capacitor is replenished prior to the next measurement cycle.

Note: The charge pump is operational during AUXTIME, CELLDLY, and SWDLY settling periods greater than 30µs, which is considered a worst settling delay for the SW input.

Outside of an acquisition, the charge pump is clocked at 32kHz.

An undervoltage comparator detects if $V_{HV-DCIN}$ drops below V_{HVUV}. If an undervoltage condition is detected, the ALRTHVUV bitfield is set. Assertion of the ALRTHVUV bit is gated until ALRTRST is cleared for the first time following power-up.

An overvoltage comparator disables the charge pump in the case where $V_{HV} - V_{DCIN}$ exceeds V_{HVOV}. This condition is indicated by the ALRTHVOV bit in the FMEA1 register. The ALRTHVOV alert does not necessarily indicate a condition that affects measurement accuracy. HV charge pump diagnostics are summarized in Table 65.

If V_{HV} drops too low relative to the top cell inputs, there is insufficient headroom to guarantee that the HVMUX switch resistance is sufficiently low or enough headroom exists for the LSAMP1 and LSAMP2 input for an accurate acquisition of the channel. Headroom alerts are indicated with the ALRTHVDRM bit in the FMEA1 register.

The HV undervoltage and HV headroom alert functions can be verified by disabling the HV charge pump HVCPDIS = 1 and allowing V_{HV} to decay while in acquisition mode.

Table 65. HV Charge Pump Diagnostics

FAULT	CONDITION	ALERT BIT	LOCATION
V_{HV} undervoltage	$V_{HV} - V_{DCIN} < V_{HVUV}$	ALRTHVUV	FMEA1:ALRTHVUV
V_{HV} overvoltage	$V_{HV} - V_{DCIN} > V_{HVOV}$	ALRTHVOV	FMEA1:ALRTHVOV
V_{HV} low headroom	$V_{HV} - V_{TOPCELL1/2} < V_{HVHDRM}$ (max)	ALRTHVHDRM	FMEA1:ALRTHVHDRM

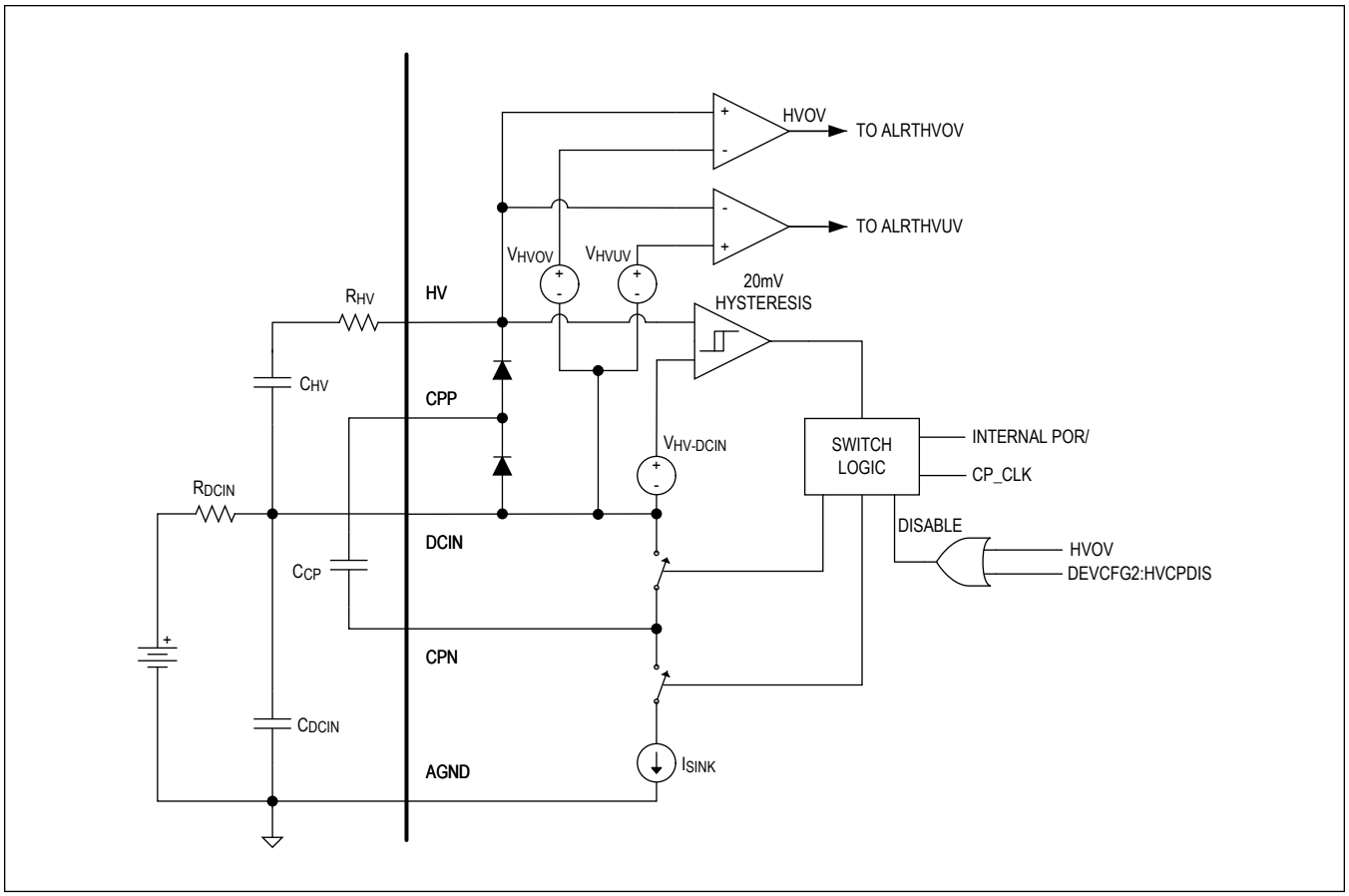


Figure 71. HV Charge Pump

Oscillators

Two factory-trimmed oscillators provide all timing requirements: HFOSC for the UART and control logic, and LFOSC for the HV charge pump and timers. A special diagnostic counter, clocked by the HFOSC signal, is employed to check the LFOSC. Every two periods of the LFOSC clock, the counter is sampled. If the count varies more than 5% from the expected value, the ALRTOSC1 bit is set as shown in Table 66. A redundant alert bit, ALRTOSC2 bit, increases the integrity level. If the HFOSC varies by more than 5%, communication errors may be indicated for the UART.

Table 66. Oscillator Diagnostics

FAULT	CONDITION	ALERT BIT	LOCATION
LFOSC	31.129kHz > f_{LFosc} > 34.406kHz	ALRTOSC1	FMEA1[15]
LFOSC	31.129kHz > f_{LFosc} > 34.406kHz	ALRTOSC2	FMEA1[14]

Diagnostics

Built-in diagnostics support ISO 26262 (ASIL) requirements by detecting specific fault conditions as shown in Table 67. The device automatically performs some of the diagnostics, while the host can perform others during initialization (e.g., at key-on) or periodically during operation as required by the application. Diagnostics performed automatically by the device are previously described in the relevant functional sections. A description of the diagnostics requiring specific configurations are provided in this section.

Note: Pin faults such as an open pin or adjacent pins shorted to each other must be detectable. Pin faults do not result in device damage but have a specific device response such as a communication error, or will be detectable through a built-in diagnostic. Analyzing the effect of pin faults is referred to as a pin FMEA. Contact Analog Devices to obtain pin FMEA results.

Table 67. Summary of Built-In Diagnostics

DIAGNOSTICS PERFORMED AUTOMATICALLY BY DEVICE WITH NO HOST INTERVENTION		
FAULT	**DIAGNOSTIC PROCEDURE**	**OUTPUT**
V_{AA} undervoltage	Continuous voltage comparison	ALRTRST
V_{HV} undervoltage	Continuous voltage comparison	ALRTHVUV
V_{HV} overvoltage	Continuous voltage comparison	ALRTHVOV
V_{HV} low headroom	Voltage comparison – updated during measurement	ALRTHVHDRM
LFOSC fault	Continuous frequency comparison	ALRTOSC1, ALRTOSC2
HFOSC fault	Communication error checking	ALRTMAN, ALRTPAR, ALRTOSC3
Communication fault	Communication error checking	ALRTPEC, ALRTMAN, ALRTPAR
Rx pin open/short	Verify Rx mode after POR	ALRTCOMMSEUn/ALRTCOMMSELn
V_{DDLx} pin open/short	Continuous voltage comparison	ALRTVDDLx
GNDLx pin open/short	Continuous voltage comparison	ALRTGNDLx
Die overtemperature	Temperature comparison	ALRTTEMP
Measurement accuracy	Accuracy comparison - updated after oversampled acquisition	ALRTCOMPACCOV/ALRTCOMPACCUV
Flexible-pack fault	Continuous fault checking of flexible-pack operation	ALRTDCINMUX

DIAGNOSTICS PERFORMED DURING ACQUISITION MODE AS SELECTED BY DIAGSEL OR SCACFG (BALSW DIAGNOSTICS)			
FAULT	**DIAGNOSTIC PROCEDURE**	**DIAGSEL[3:0] OR SCANCFG**	**OUTPUT**
Die temp (PTAT) fault	Die temperature (PTAT) diagnostic	DIAGSEL1/2 = 1h	DIAGSEL1/2[15:0] = PTAT voltage
V_{AA} voltage fault	V_{AA} verification	DIAGSEL1/2 = 2h	DIAGSEL1/2[15:0] = V_{AA} voltage
Reference voltage fault	ALTREF verification	DIAGSEL1/2 = 3h	DIAGSEL1/2[15:0] = ALTREF voltage
Comp cell signal path fault	Comp signal path verification	DIAGSEL1/2 = 4h	DIAGSEL1/2[15:0] = COMP error voltage
Cell gain calibration fault	Cell gain calibration verification	DIAGSEL1/2 = 5h	DIAGSEL1/2[15:0] = Calibration voltage (1/4)
Offset calibration fault	Offset calibration verification	DIAGSEL1/2 = 6h	DIAGSEL1/2[15:0] = Calibration offset voltage (0V)
DAC bit stuck high	DAC 3/4 scale	DIAGSEL1/2 = 7h	DIAGSEL1/2[15:0] = DAC code of 3/4 full-scale measured by ADC
DAC bit stuck low	DAC 1/4 scale	DIAGSEL1/2 = 8h	DIAGSEL1/2[15:0] = DAC code of 1/4 full-scale measured by ADC
NTC(THRM) offset calibration fault	NTC(THRM) offset calibration verification	DIAGSEL1/2 = 9h	DIAGSEL1/2[15:0] = Calibration offset error with THRM

Table 67. Summary of Built-In Diagnostics (continued)

ADC bit stuck high	Zero-scale ADC diagnostic	DIAGSEL1/2 = Ah	DIAGSEL1/2[15:0] = ADC zero scale
ADC bit stuck low	Full-scale ADC diagnostic	DIAGSEL1/2 = Bh	DIAGSEL1/2[15:0] = ADC full scale
LSAMP offset too high	LSAMP offset diagnostic	DIAGSEL1/2 = Ch	DIAGSEL1/2[15:0] (LSAMP offset voltage)
$V_{DDL2/3}$ fault	$V_{DDL2/3}$ diagnostic	DIAGSEL1/2 = Dh	DIAGSEL1/2[15:0] ($V_{DDL2/3}$ voltage)
Balancing switch short	BALSW diagnostic mode	SCANCFG = 4h	ALRTBALSW, FMEA1:ALRTBALSWSUM
Balancing switch open	BALSW diagnostic mode	SCANCFG = 5h	ALRTBALSW, FMEA1:ALRTBALSWSUM
Odd cell sense-wire open	BALSW diagnostic mode	SCANCFG = 6h	ALRTBALSW, FMEA1:ALRTBALSWSUM
Even cell sense-wire open	BALSW diagnostic mode	SCANCFG = 7h	ALRTBALSW, FMEA1:ALRTBALSWSUM
Procedural diagnostics: Contact Analog Devices for the complete listing of procedural diagnostics found in the safety manual.			

ALERTOUT Pin-to-Pin Short Diagnostic

The UART Alert DC Diagnostic Test is used to test the ALERTOUT pin for shorts to AUXIN0/GPIO0 pins. When UARTSEL = 0b1 (UART mode), this test is enabled by setting ALERTDCTSTEN bit to 0b1.

When the DC Diagnostic Test is enabled, the ALERTOUT pin will be driven low if an Alert condition is present, and driven high otherwise. The ALRTUSER bit field can be written to exercise ALRTOUT in either direction. Neighboring pins, such as AUXIN0/GPIO0, can be monitored directly or in diagnostic modes to detect a fault.

This function works in all UARTCFG modes, including the differential alert, which does not normally use the ALERTOUT pin.

CELL Pin Open Diagnostics

If an input of the MAX17854 is disconnected from the cell input through any combination of mechanical failure, the position of the failure can be detected by performing cell open diagnostics. It is recommended that comparator measurements are used for quick identification against the default threshold setting COMPOPNTH. If measurement is below the set threshold, the corresponding cell alerts are flagged in ALRTCOMPOV.

This diagnostic is enabled by setting CELLOPNDIAGSEL = 1 and performing comparator scan (SCANCFG = 0b010). Only unipolar measurements are allowed for this diagnostic and, if a cell position is set as bipolar, the corresponding cell is skipped and the alert flag is not set for that bipolar cell. Normally, in Open Diagnostic modes, pulldown current sources are enabled on all measured channels using CTSTEN for required cells. Various current configurations setting are available for the user and can be configured using DIAGCFG:CTSTDAC bit field.

Die Temperature Measurement

The die temperature measurement allows the host to compute the device temperature (T_{DIE}) as it relates to the acquisition accuracy and allows the device to automatically shut itself down when T_{DIE} > +145°C. The measurement employs a source whose voltage, V_{PTAT}, is proportional to absolute temperature (PTAT) as shown in Figure 72. The V_{PTAT} measurement is enabled by setting DIAGSEL1[3:0] or DIAGSEL2[3:0] to 0b0001, and the 14-bit measurement is stored in DIAG1 = DIAG1REG[15:2] or DIAG2 = DIAG2REG[15:2], respectively. The die temperature measurement requires a settling time of 39µs from the start of the measurement cycle until the diagnostic conversion. As long as two or more cell measurements are enabled, there will be sufficient settling time for this measurement. See the acquisition timing sections for more details.

The PTAT voltage is computed as follows:

$$V_{PTAT} = \frac{DIAG1}{16384d} \times V_{REF} \text{ or } V_{PTAT} = \frac{DIAG2}{16384d} \times V_{REF}$$

where V_{REF} = 1.25V. The measured voltage may be converted into °C as follows:

$$T_{DIE}(\text{in } ^\circ C) = \frac{V_{PTAT}}{A_{V\_PTAT}} + T_{OS\_PTAT} - 273\ ^\circ C$$

See the *Electrical Characteristics* table for A_{V_PTAT} and T_{OS_PTAT} values.

Die Temperature Alert

The die temperature is continuously monitored in an interval of 1ms to detect if the $T_{DIE} > T_{ALRTTEMP}$. In the event when die temperature is greater, ALRTTEMP bit in FMEA2 register is asserted. The only exception is that ALRTTEMP monitoring is temporarily disabled when the die temperature measurement is requested by configuring DIAGSEL1[3:0] or DIAGSEL2[3:0] = 1h. The signal path for die temperature alert and measurement is shown in Figure 72.

If ALRTTEMP is set, the host should consider the possibility that the acquisition does not meet the expected accuracy specification, or that the die temperature measurement itself may be inaccurate due to insufficient settling time (< 2 cell measurements enabled).

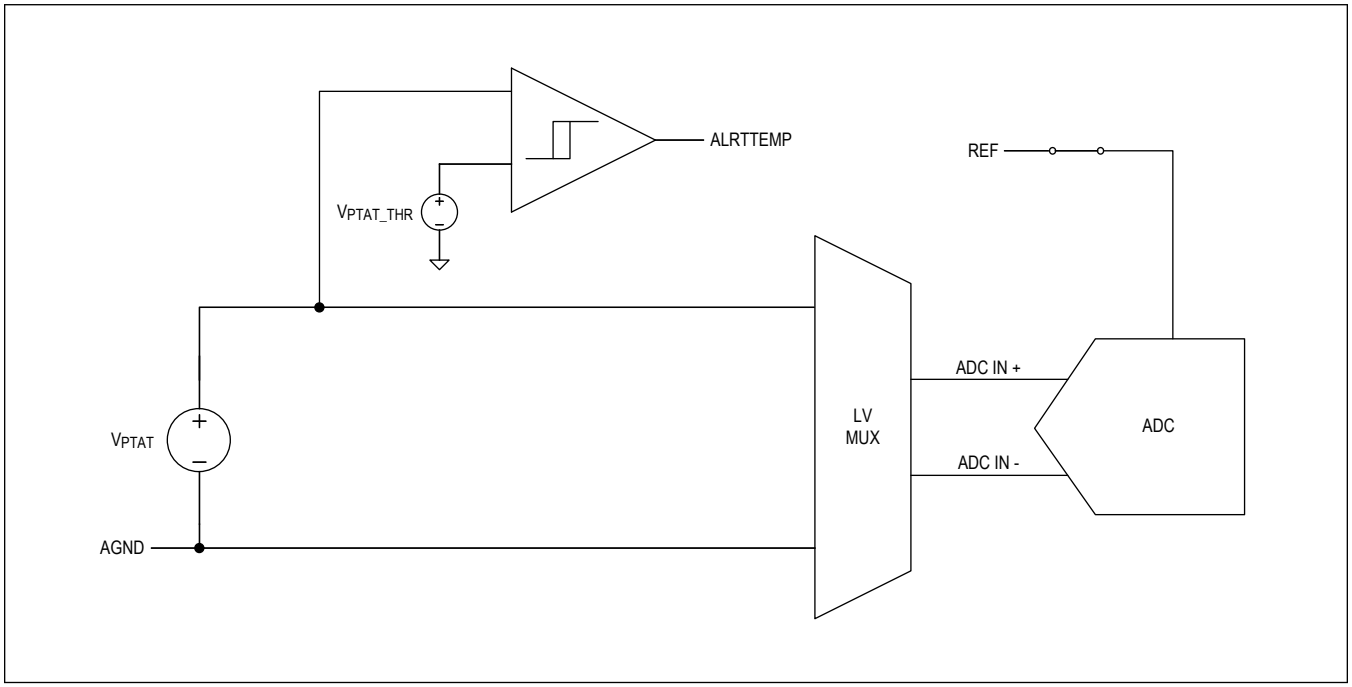


Figure 72. Die Temperature Measurement

V_{AA} Diagnostic Measurement

The V_{AA} diagnostic measurement (DIAGSEL1 or DIAGSEL2 = 0b0010) verifies that V_{AA} is within specification. This diagnostic measures V_{REF} while using V_{AA} as the ADC reference. The signal path for the V_{AA} diagnostics is as shown in Figure 73.

The voltage into the ADC is computed from the result in the DIAG1REG (or DIAG2REG) register as follows:

$$\frac{1}{4} \times V_{REF} = \frac{DIAG1REG[15:2]}{16384} \times V_{AA}$$

V_{AA} can be calculated as follows:

$$V_{AA} = \frac{1}{4} \times V_{REF} \times \frac{16384}{DIAG1REG[15:2]}$$

where V_{REF} = 1.25V.

The result for V_{AA} should fall within the range provided in the *Electrical Characteristics* table for V_{AA}.

The 14-bit ADC measurement that passes the diagnostic ranges from 0xA55 to 0xBF4 based on *Electrical Characteristics* table specs.

Note: With any sampled measurement, the signal chain noise performance must be considered within the measurement result. For consistent measurement performance, V_{AA} is recommended to be averaged within multiple system measurement cycles to mitigate the variation seen by noise.

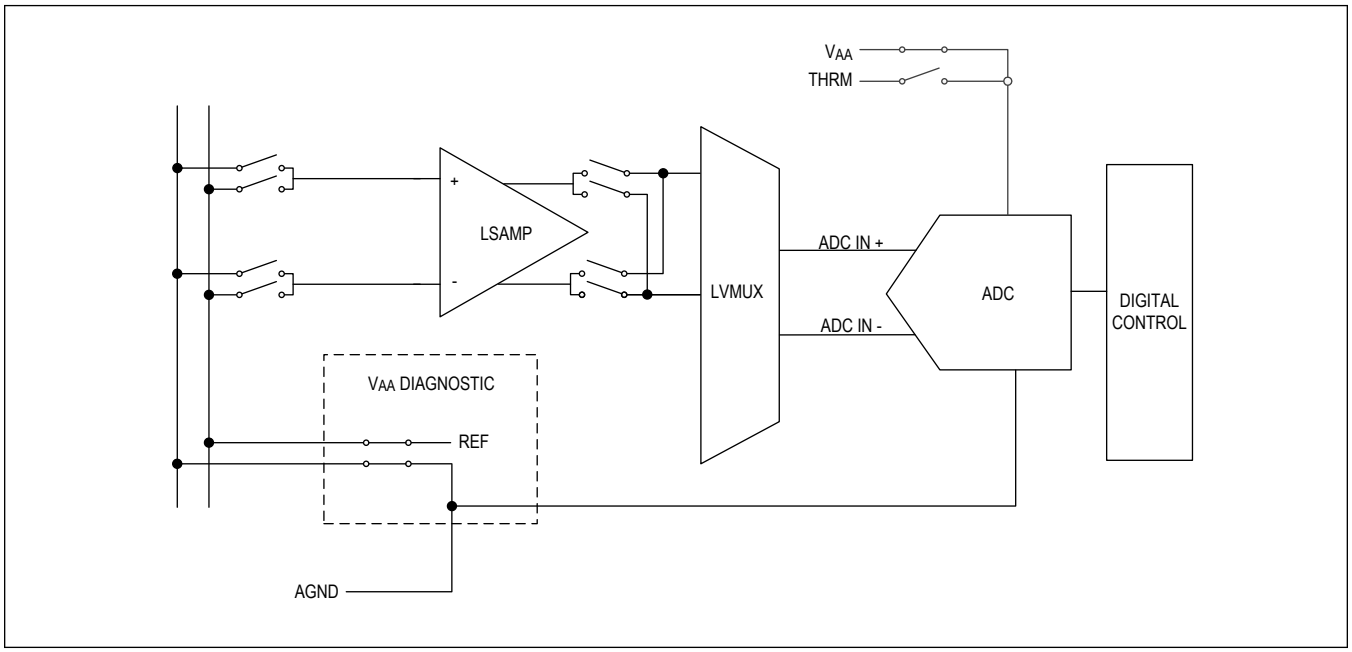


Figure 73. V_{AA} Diagnostic

ALTREF Diagnostic Measurement

The ALTREF diagnostic measurement (DIAGSEL1 or DIAGSEL2 = 0b0011) checks the primary voltage reference of the ADC by measuring the alternate reference voltage, V_{ALTREF}, while using V_{REF} as the ADC reference. The result is available in the DIAG1REG (or DIAG2REG) registers. The ALTREF voltage is computed from the result in the DIAG register as follows:

$$V_{ALTREF} = \frac{DIAG1REG[15:2]}{16384} \times V_{REF}$$

During ALTREF diagnostic measurements, the ADC is automatically set to unipolar mode. The signal path for the ALTREF diagnostic is as shown in Figure 74.

Since 0.99V < V_{ALTREF} < 1.01V and V_{ALTREF} = 1.0V (nom), the expected range for DIAG[15:2] is shown as follows.

The 14-bit ADC measurement passes the diagnostic ranges from 0x341F to 0x3247.

Note: With any sampled measurement, the signal chain noise performance must be considered within the measurement result. For consistent measurement performance, V_{ALTREF} is recommended to be averaged within multiple system measurement cycles to mitigate the variation seen by noise.

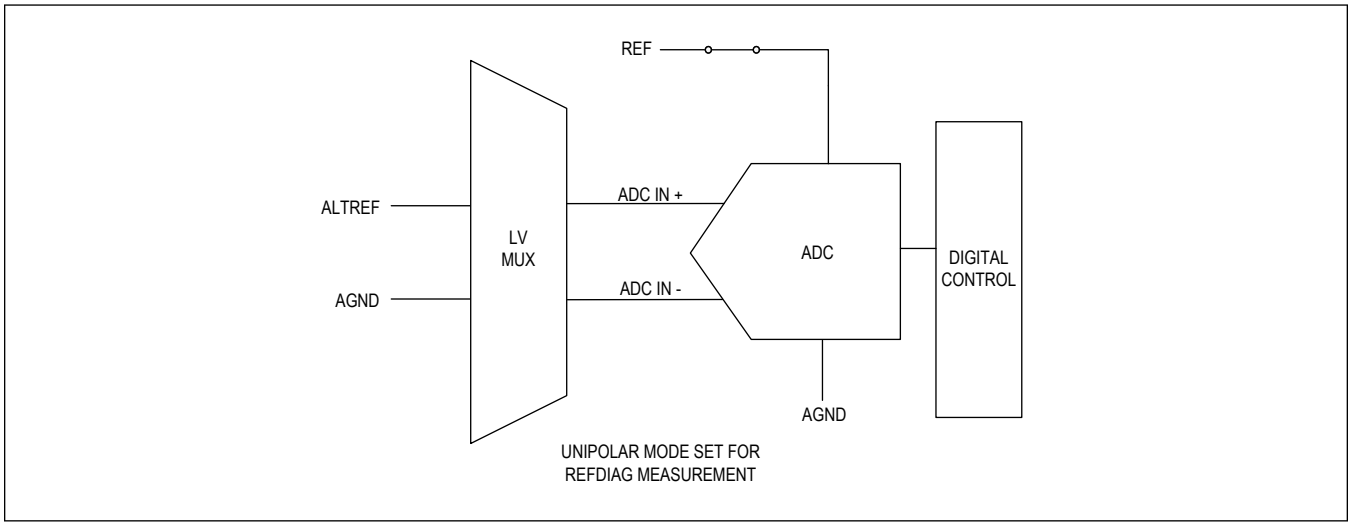


Figure 74. ALTREF Diagnostic

$V_{DDL2/3}$ Diagnostic

The $V_{DDL2/3}$ diagnostic measurement (DIAGSEL1 or DIAGSEL2 = 0b1101) checks that the $V_{DDL2/3}$ voltage is within specification. The diagnostic measures scaled $V_{DDL2/3}$ while using V_{REF} as the ADC reference. The result is available in the DIAG1REG (or DIAG2REG) registers. The $V_{DDL2/3}$ voltage is computed from the result in the DIAG register as follows:

$$V_{DDL2/3} = \frac{DIAG1REG[15:2]}{16384} \times V_{REF} \times 4.8$$

where V_{REF} = 1.25V.

The result for $V_{DDL2/3}$ should fall within the range provided in the *Electrical Characteristic* table for $V_{DDL2/3}$.

For $V_{DDL2/3}$ nominal voltage of 3.3V, the 14-bit expected range for DIAG[15:2] which passes the diagnostic is from 0x2147 to 0x24B6.

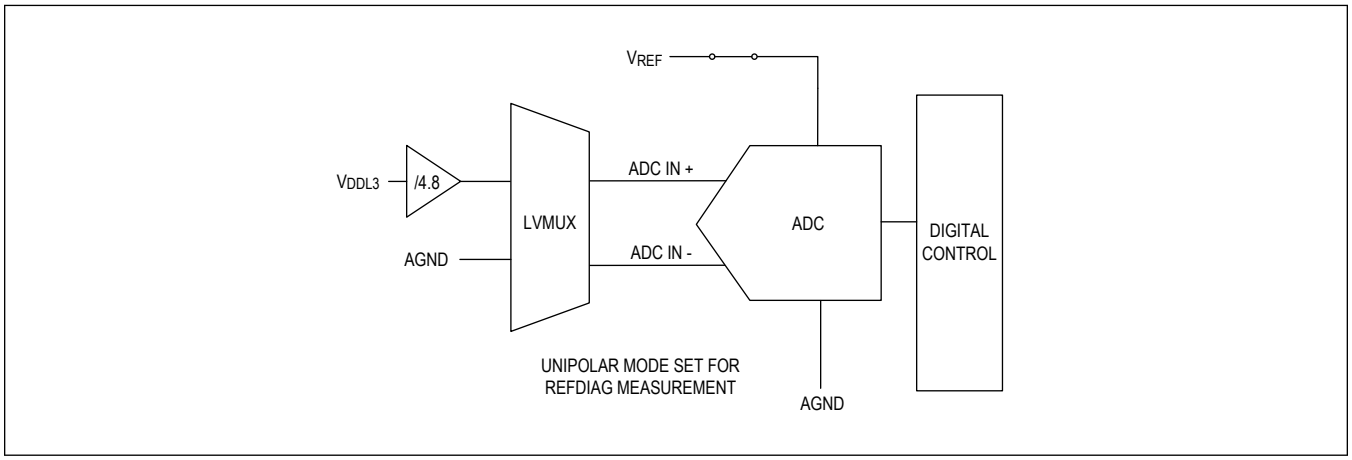


Figure 75. V_{DDL} Diagnostic

Diagnostic Measurement

The comparator signal conditioning path can be measured by the ADC, which allows for the following capabilities:

- Comparator functionality verification against specification
- Comparator thresholds calibration
- Increased comparator performance for improved specification beyond that described in the *Electrical Characteristics* table.

The functionality of the comparator signal conditioning path (shown in Figure 76) can be measured using DIAGSEL1 = 0b0100 or DIAGSEL2 = 0b0100 in the DIAGCFG register. This configuration applies an input of V_{REF} = 1.25V to the LSAMP2 while the DAC is programmed to 03FFh (DAC reference of 1.25V). The output of the comparator preamp is routed to the ADC input where it is effectively measured. The result of the ADC measurement is presented in corresponding DIAG1REG[15:2] or DIAG2REG[15:2] registers.

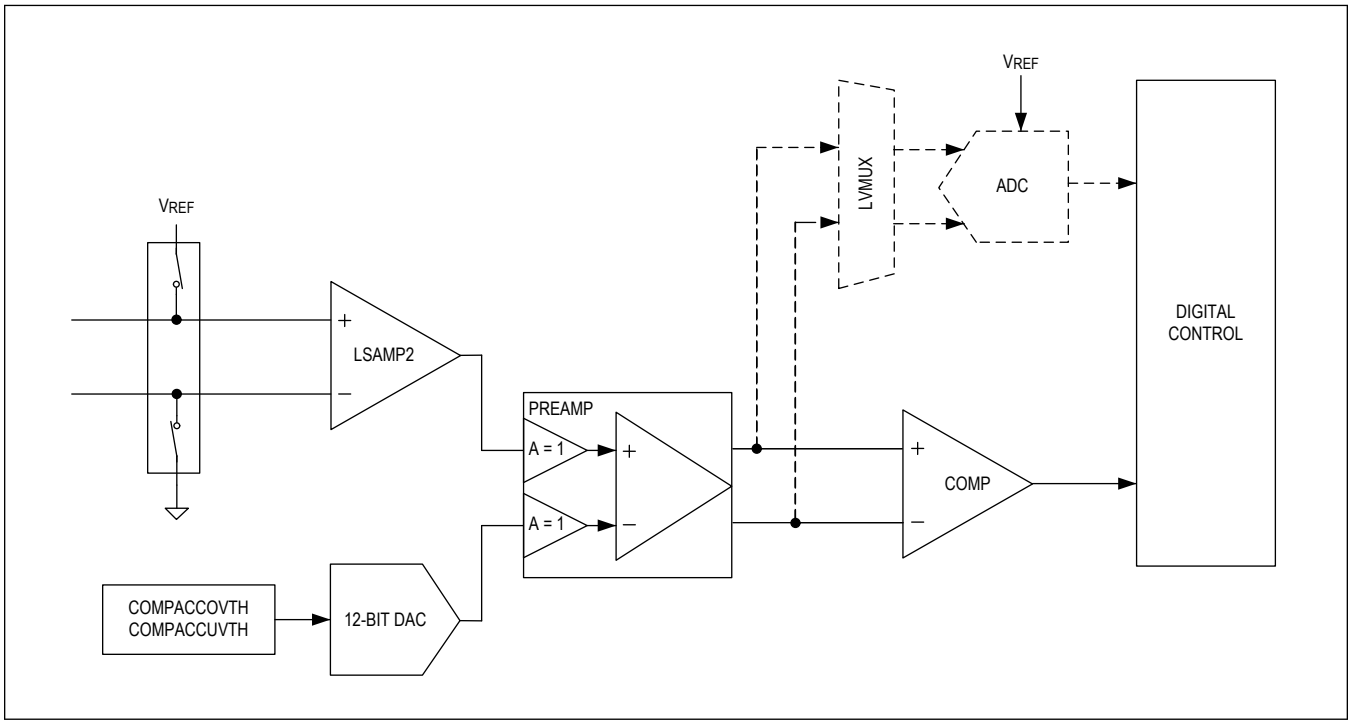


Figure 76. Comparator Signal Path to ADC

Comparator functionality is verified by comparing the DIAG register outputs against the ranges shown in Table 68.

Table 68. Comp Signal Path Diagnostic Verification Ranges

UPPER DIAGNOSTIC RANGE	LOWER DIAGNOSTIC RANGE
0x20BB	0x1F3F

In addition to verifying functionality against the specification, the DIAG register output can be used to calculate the error of the comparator cell signal path as shown in the following equation:

$$\varepsilon_{COMP\_CELLPATH} = \frac{1}{4} x \left(\frac{DIAG1REG[15:2] - 0d8195}{0d16384} \right) \cdot 5V$$

The error can then be used by the user to manually adjust the comparator OV and UV thresholds (COMPOVTH, COMPUVTH, COMPACCOVTHREG, COMPACCUVTHREG) to ensure that the thresholds are applied to the true comparator performance.

$COMPOVTH_{Adjusted} = COMPOVTH_{Desired} + Round(\varepsilon_{COMP\_CELLPATH} * 4096 / 5)$

$COMPUVTH_{Adjusted} = COMPUVTH_{Desired} + Round(\varepsilon_{COMP\_CELLPATH} * 4096 / 5)$

Note: The above threshold corrections cannot be applied to the AUX measurements since the correction includes LSAMP2 errors.

The computed error value also allows the user to specify improvement in the comparator accuracy beyond what that described in the *Electrical Specifications* table.

$$V_{OS\_COMP\_Effective} = \sqrt{\varepsilon_{COMP\_CELLPATH}^2 + 0.004^2}$$

For example, if the DIAG1 register output reads 0d8172, then the following adjustments can be applied:

$$\varepsilon_{COMP\_CELLPATH} = \frac{1}{4}\left(\frac{0d8172 - 0d8195}{0d16384}\right) \cdot 5V = -1.4mV$$

$COMPOVTH_{Adjusted} = COMPOVTH_{Desired} + Round(-1.4mV * 4096 / 5)COMPOVTH_{Adjusted} = COMPOVTH_{Desired} - 1$

$COMPUVTH_{Adjusted} = COMPUVTH_{Desired} + Round(-1.4mV * 4096 / 5)COMPUVTH_{Adjusted} = COMPUVTH_{Desired} - 1$

Comparator Accuracy Diagnostic

The COMPACCEN bit in ACQCFG register is used to test the accuracy of the comparator and is evaluated at the end of a measurement-sequence for configurations that use the comparator (SCANCFG = 001b or 010b in the SCANCTRL register) during scans. When COMPACCEN = 1, V_{REF} = 1.25V is configured as input to the LSAMP2 and the 12-bit DAC uses values from the COMPACCOVTH and COMPACCUVTH registers.

An overvoltage alert is issued by setting the ALRTCOMPACCOV bit in the FMEA2 register if the threshold value in COMPACCOVTH is violated.

If COMPACCOVTH is set to 3FFh, the comparator may set the ALRTCOMPACCOV bit (expected to be set for the ideal case).

An undervoltage alert is issued by setting the ALRTCOMPACCUV bit in the FMEA2 register if the threshold value in COMPACCUVTH is violated.

If COMPACCUVTH is set to 3FFh, the comparator may not set ALRTCOMPACCUV bit (not expected to be set for the ideal case).

The Comparator Accuracy Diagnostic signal path is shown in Figure 77.

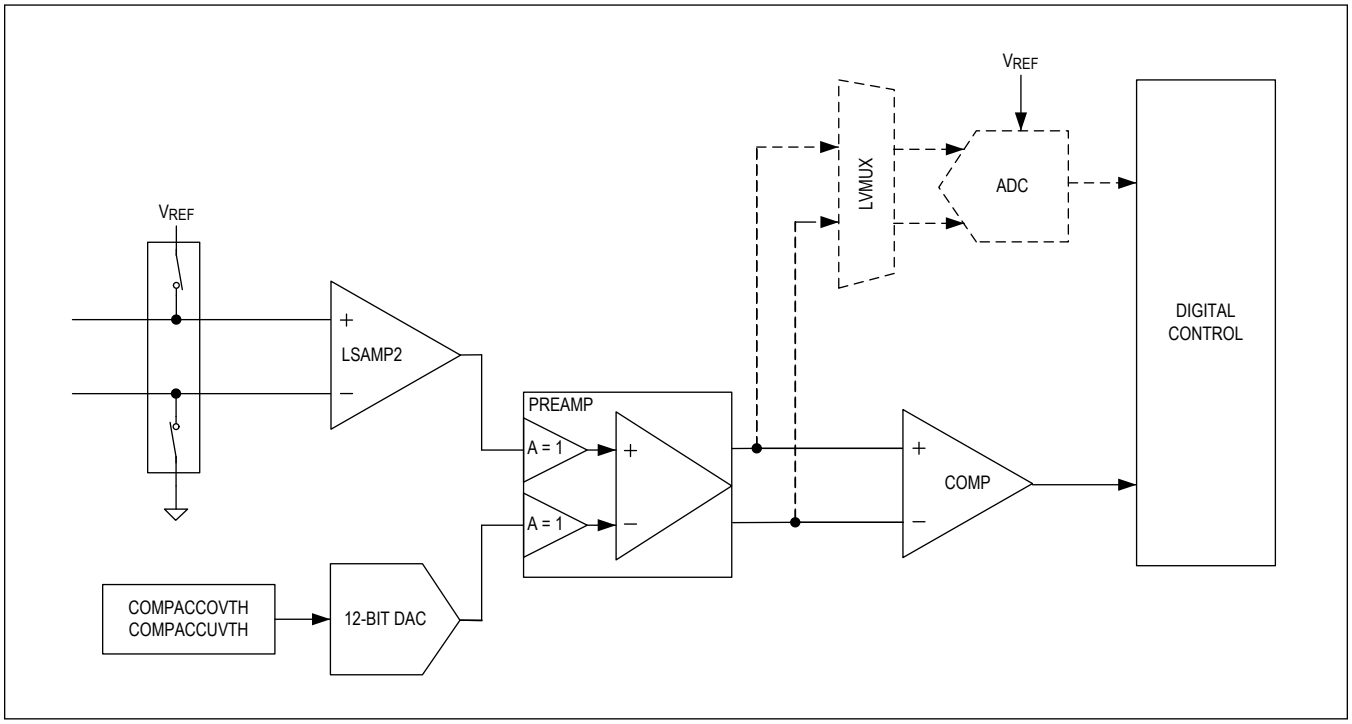


Figure 77. Comparator Accuracy Diagnostic Path

In order to eliminate false alerts, the user should adjust COMPACCOVTH and COMPACCUVTH by ±18 DAC codes.

The Comparator Accuracy Diagnostics procedure, when requested by setting COMPACCEN = 1, is run only once at the end of the last oversample of the SCAN measurement request, as indicated in Figure 78.

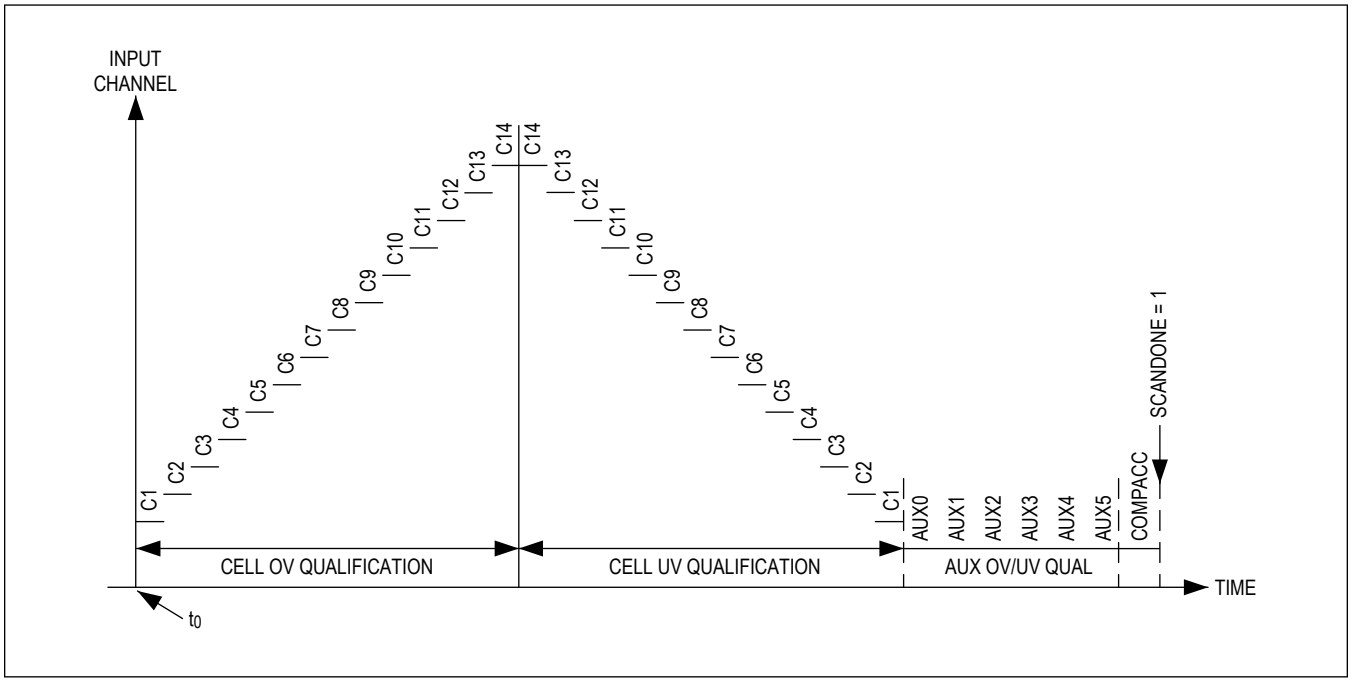


Figure 78. Comparator Accuracy End of Scan Measurement

Cell Gain Calibration Diagnostic Measurement

The cell gain calibration diagnostic verifies that on-demand calibration is functioning correctly and the ADC and LSAMP1 are operating within the specification described by the *Electrical Characteristics* table. This diagnostic is run by setting the DIAGSEL1 = 0b0101 or DIAGSEL2 = 0b0101 in the DIAGCFG register in accordance with the SCANMODE setting. Thus, if SCANMODE is configured for Pyramid mode operation when this diagnostic is run, then the sampling will occur as two conversion phases and effectively chop the offset. Similarly, if SCANMODE is configured for Ramp mode operation when this diagnostic is run, then only a single conversion phase will be implemented. This diagnostic must be run for each of the SCANMODE configurations utilized by the application to validate calibration.

The diagnostic is performed by multiplexing V_{REF} into the LSAMP1 inputs as shown in Figure 79. The OVSAMPL bitfield used during this diagnostic acquisition must be minimally configured to an oversample of 16, which ensures proper accuracy performance.

The expected result is 1/4 of full-scale voltage and can be read from the DIAG1REG [15:2] or DIAG2REG[15:2] registers. To allow for a 14-bit ADC, measurements should extend from 0xFD2 to 0x102F.

Note: This diagnostic should not be run without enabling calibration.

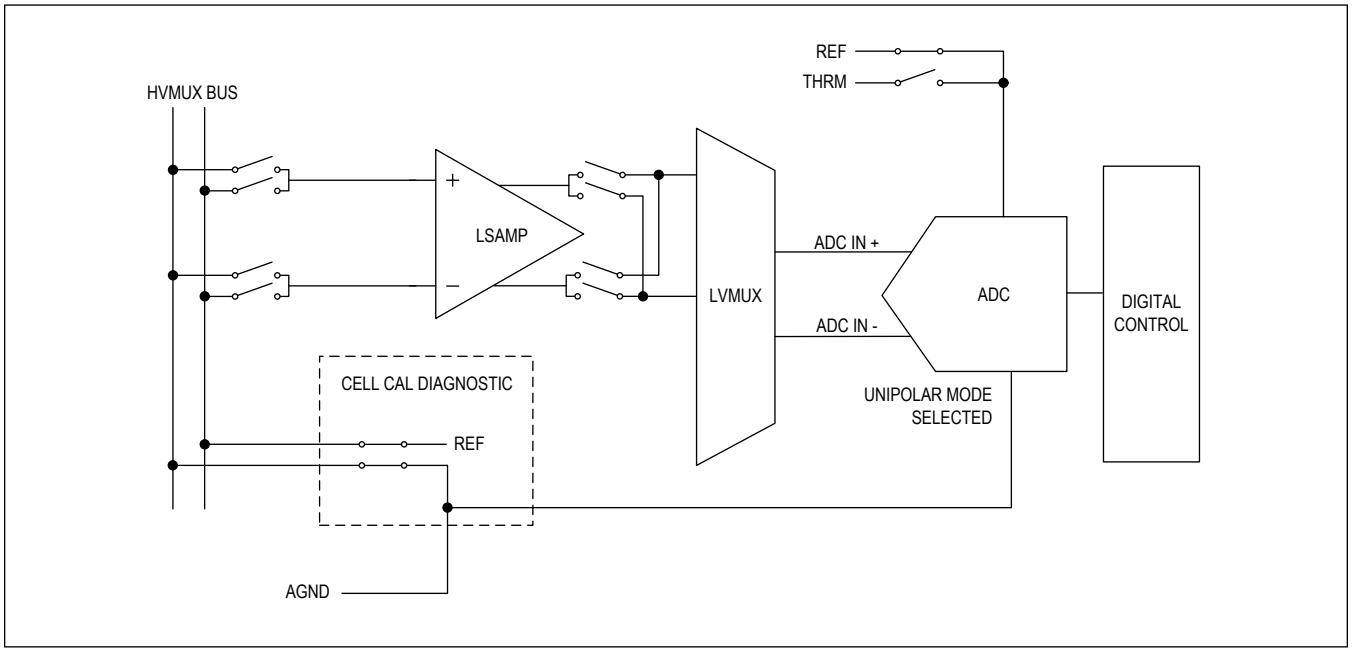


Figure 79. Cell Gain Calibration Diagnostic Measurement

Offset Calibration Diagnostic

The offset calibration diagnostic is run by setting the DIAGSEL1 = 0b0110 or DIAGSEL2 = 0b0110 in the DIAGCFG register. This diagnostic verifies that on-demand calibration is functioning correctly and operating within the *Electrical Characteristics* table specifications.

This diagnostic is configured differently depending on the SCANMODE setting in the SCANCTRL register. When configured in pyramid mode (SCANMODE = 0), the diagnostic is performed by shorting the ADC inputs and performing an acquisition with the ADC polarity overridden in bipolar mode. When configured in ramp mode (SCANMODE = 1), the diagnostic is performed by shorting the LSAMP1 inputs to ground and performing an unchopped acquisition with the ADC polarity overridden in bipolar mode. For both SCANMODE configurations, the OVSAMPL bitfield used during this diagnostic acquisition must be minimally configured to an oversample of 16, which ensures proper accuracy performance. The expected result is 0V (0x2000) and can be read from DIAG1REG [15:2] or DIAG2REG[15:2] registers.

For Pyramid mode, the 14-bit ADC measurement bound that passes this diagnostic ranges from 0x1FF6 to 0x200A.

For ramping, the 14-bit ADC measurement bound that passes this diagnostic ranges from 0x1FEA to 0x2011.

The signal path is shown in Figure 80.

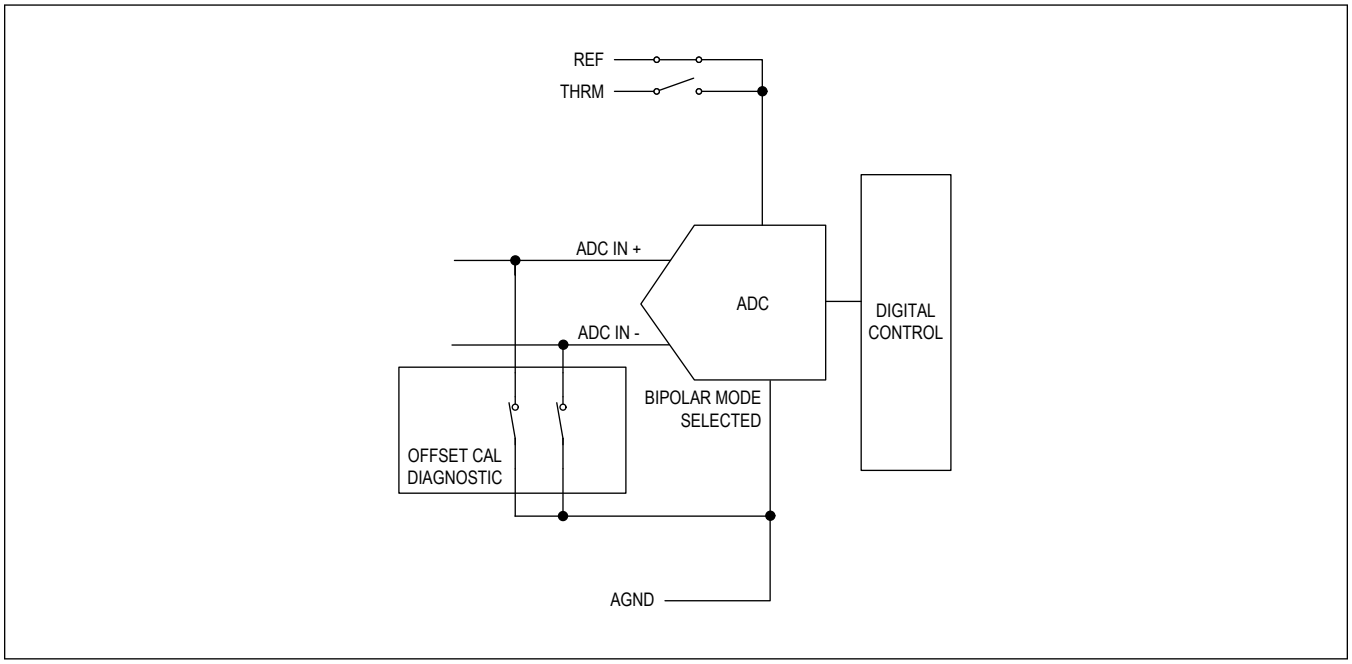


Figure 80. Offset Calibration Diagnostic

THRM Offset Calibration Diagnostic

The THRM offset calibration diagnostic is run by setting the DIAGSEL1 = 0b1001 or DIAGSEL2 = 0b1001 in the DIAGCFG register. The diagnostic verifies that on-demand calibration for the THRM case is functioning correctly and the ADC is operating within the specification detailed in the *Electrical Characteristics* table. This is performed by shorting the ADC inputs to ground with the ADC reference connected to THRM and performing an acquisition with recommendation of a minimum 16x oversample (OVSAMPL = 0b011) in bipolar mode. The signal path can be seen in Figure 81.

The expected result is 0V or DIAG1/2 [15:2] = 2000h (nom).

The 14-bit ADC measurement bound that passes this diagnostic ranges from 1F91h to 2070h.

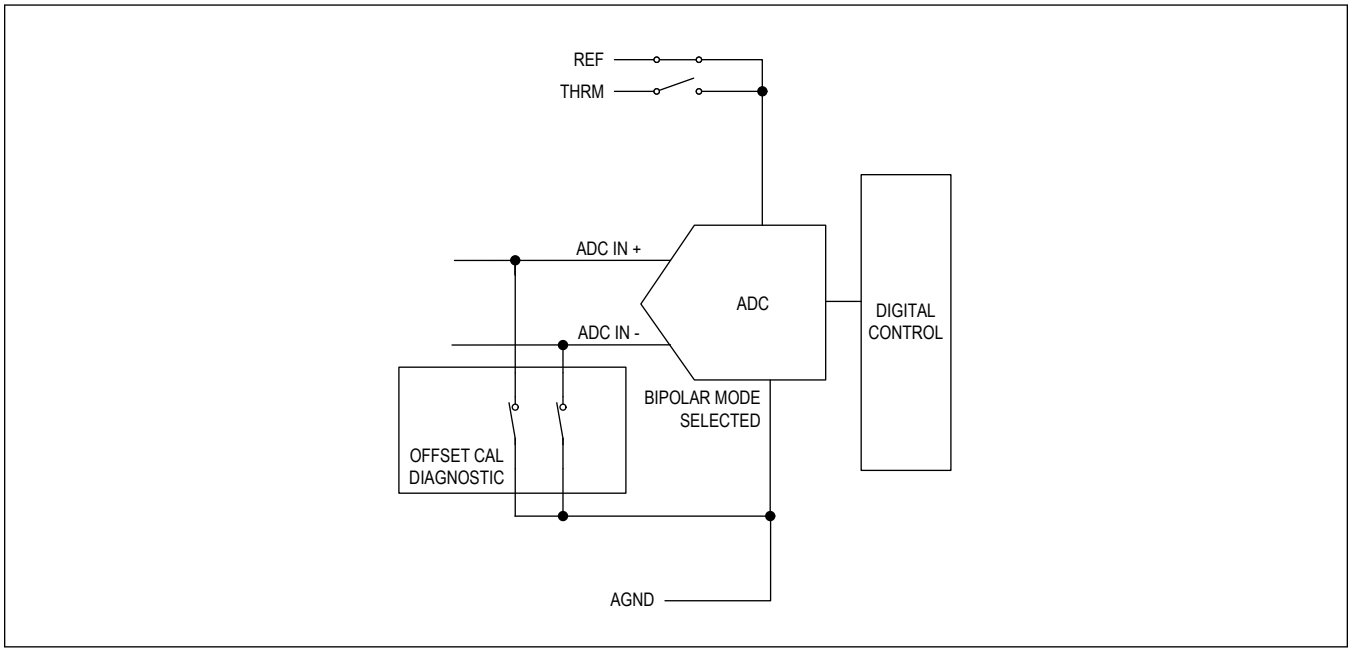


Figure 81. THRM Offset Calibration Diagnostic

LSAMP Offset Diagnostic Measurement

The LSAMP diagnostic measurement (DIAGSEL1 or DIAGSEL2 = 0b1100) measures the level-shift amplifier offset by shorting the LSAMP inputs during the diagnostic portion of the acquisition. The result is available in the DIAG1REG or DIAG2REG registers after an acquisition. For this measurement, the ADC polarity is automatically set to bipolar mode to allow accurate measurement of voltages near zero. This measurement eliminates the chopping phase to preserve the offset error. If the diagnostic measurement exceeds the valid range for V_{OS_LSAMP} as specified in the *Electrical Characteristics* table, the chopping function may not be able to cancel out all of the offset error and acquisition accuracy could be degraded accordingly. The signal path for this diagnostic is shown in Figure 82.

The LSAMP offset is computed from the result in the DIAG1 or DIAG2 as follows:

LSAMP Offset = (|DIAGn[15:2] - 2000h| / 16384d) * 5V

The 14-bit ADC measurement bound that passes this diagnostic ranges from 1FD4 to 0x202D.

The validity of measurements through LSAMP is further confirmed by the ALTREF and V_{AA} diagnostics, and by the comparison of the V_{BLK} measurement to the sum of the cell measurements.

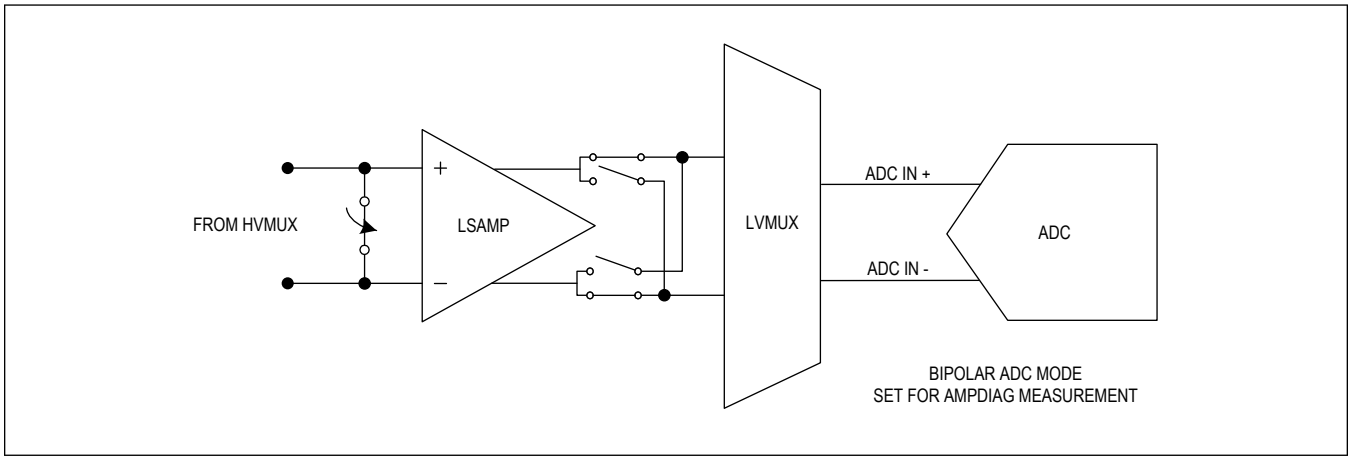


Figure 82. LSAMP Offset Diagnostic

Zero-Scale ADC Diagnostic Measurement

Stuck ADC output bits may be verified with a combination of the zero-scale and full-scale diagnostics. The zero-scale ADC diagnostic measurement (DIAGSEL1 or DIAGSEL2 = 0b1010) verifies that the ADC conversion results in 0000h (14-bit) when its input is at $-V_{AA}$ in bipolar mode (since for an input ≤ -2.5V, DIAG1/2[13:0] = 0000h). For this measurement, the ADC is automatically set to bipolar mode. The signal path for this diagnostic is shown in Figure 83.

If the user is looking for a quick combination of ADC zero-scale and full-scale to detect if ADC is stuck at some value, this can be performed as part of the end of scan by configuring ADCZSFZEN = 1 and then requesting a scan. See the acquisition timing sections for details on insertion into the scan and timing.

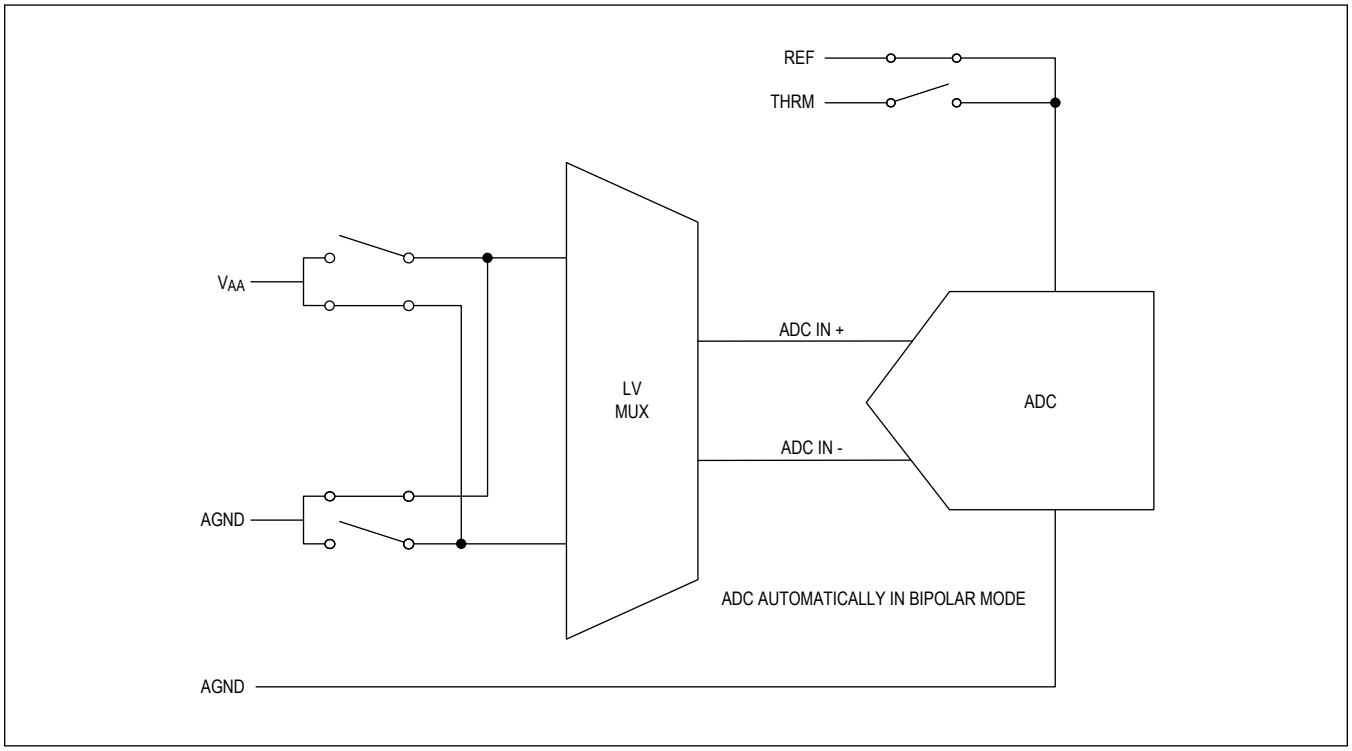


Figure 83. ADC Zero-Scale Diagnostic

Full-Scale ADC Diagnostic Measurement

Stuck ADC output bits may be verified with a combination of the zero-scale and full-scale diagnostics. The full-scale ADC diagnostic measurement (DIAGSEL1 or DIAGSEL2 = 0b1011) verifies that the ADC conversion results in 3FFFh (14-bit) when its input is at V_{AA} in bipolar mode (since for an input ≥ 2.5V, DIAG1/2[15:0] = FFFCh). For this measurement, the ADC is automatically set to bipolar mode. The signal path for this diagnostic is shown in Figure 84.

If user is looking for a quick combination of ADC zero-scale and full-scale to detect if the ADC is stuck at some value, this can be performed as part of the end of scan by configuring ADCZSFZEN = 1 and then requesting a scan. See the acquisition timing sections for details on insertion into the scan and timing.

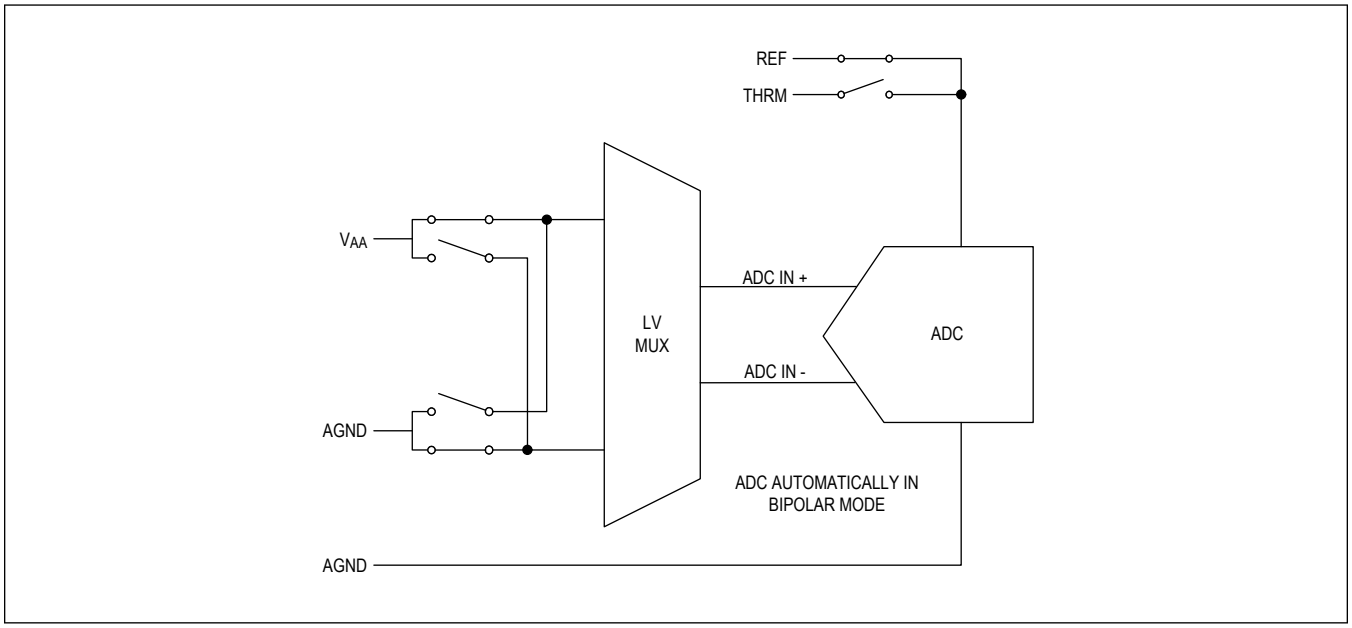


Figure 84. Full-Scale ADC Diagnostic Measurement

DAC 1/4-Scale Diagnostic

The DAC 1/4-scale diagnostic can be requested by setting DIAGSEL1 or DIAGSEL2 to 0x1000. This configures the internal DAC used to set the comparator thresholds to ~1/4 of full-scale (V_{REF}) or 0x3FF. The DAC voltage is muxltiplexed to the ADC and then compared against the bounds shown in Figure 85.

The nominal DAC and ADC voltages are:

V_{DAC} = 1023/4096 x 1.25 = 0.3122V

V_{ADC} = 0.3122/1.25 x 16383 = 4092 = 0x0FFC

The 14-bit ADC measurement bounds for passing this diagnostic range from 0x0F4D to 0x1086.

This is used in coordination with the DAC 3/4-scale diagnostic to ensure that there are no stuck bits that may cause errors with the comparator threshold settings.

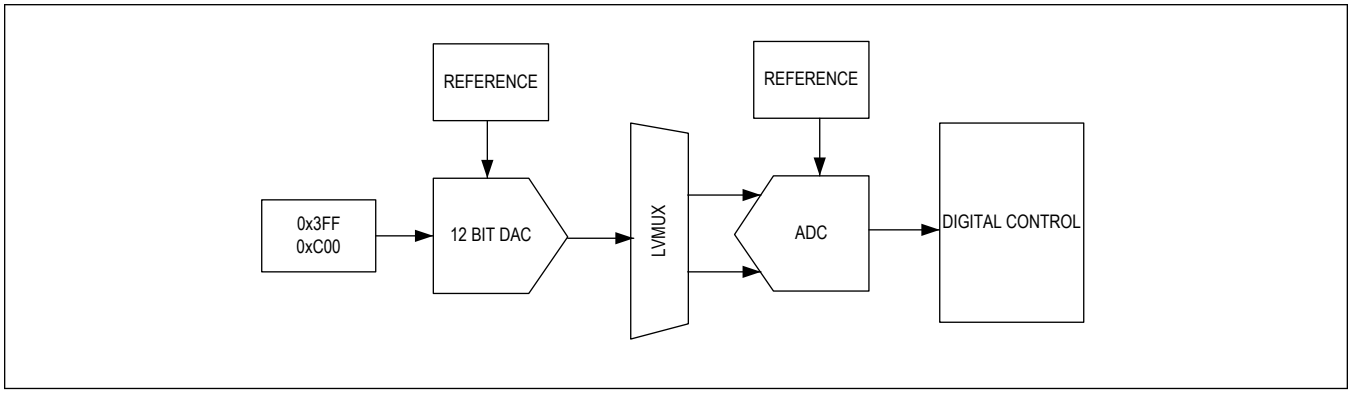


Figure 85. DAC 1/4- and 3/4-Scale Diagnostic

DAC 3/4-Scale Diagnostic

The DAC 3/4-scale diagnostic can be requested by setting DIAGSEL1 or DIAGSEL2 = 0x0111. This configures the internal DAC used to set the comparator thresholds to 3/4 of full-scale (V_{REF}) or 0C00h. The DAC voltage is multiplexed to the ADC and then compared against the following bounds.

The nominal DAC and ADC voltages are:

V_{DAC} = 3072/4096 x 1.25 = 0.9375V

V_{ADC} = 0.9375/1.25 x 16383 = 2FFFh

The 14-bit ADC measurement bounds for passing this diagnostic ranges from 0x2F06 to 0x30A4.

This is used in coordination with the DAC 1/4-scale diagnostic to ensure that there are no stuck bits that may cause errors with the comparator threshold settings.

BALSW Diagnostics

Four balancing switch diagnostic modes are available to facilitate the following diagnostics:

- Balancing switch shorted (SCANCFG[2:0] = 0b100)
- Balancing switch open (SCANCFG[2:0] = 0b101)
- Odd sense wire open (SCANCFG[2:0] = 0b110)
- Even sense wire open (SCANCFG[2:0] = 0b111)

Enabling any of these modes automatically configures several of acquisition settings (e.g., enables the ALTMUX measurement path). The host must initiate the acquisition, but the diagnostic mode automatically compares the measurements to the specific thresholds as configured through BALSHRTTHR, BALLOWTHR, or BALHIGHTHR threshold registers and sets any corresponding alerts in ALRTBALSW register field. The host presets the thresholds as determined by the minimum and maximum resistance of the switch (R_{SW}) specified in the *Electrical Characteristics* table and the intended cell-balancing current.

The Balance Switch Fault Alert register (ALRTBALSW[13:0]) is cleared at the start of a new scan request if balancing switch diagnostic mode is requested (SCANCFG = 0b100, 0b101, 0b110, or 0b111). The result from the current balancing switch diagnostic is written to ALRTBALSW[13:0] at the end of scan (SCANDONE = 1). The previous result will persist in ALRTBALSW until a new scan is requested with the balancing switch diagnostic mode enabled.

Table 69 describes which Balance Switch Diagnostic Alert thresholds contribute to ALRTBALSW in each of the four modes.

Table 69. BALSW Diagnostic

MODE	SCANCFG[2:0]	THRESHOLD	FAULT CONDITION
Balancing Switch Short	0b100	BALSHRTTHR	Data < BALSHRTTHR
Balancing Switch Open	0b101	BALLOWTHR, BALHIGHTHR	Data < BALLOWTHR, or Data > BALHIGHTHR
Cell Sense Open Odds	0b110	BALLOWTHR, BALHIGHTHR	Data < BALLOWTHR, or Data > BALHIGHTHR
Cell Sense Open Evens	0b111	BALLOWTHR, BALHIGHTHR	Data < BALLOWTHR, or Data > BALHIGHTHR

The summary status bitfield ALRTBALSWSUM is updated at the end of scan when a balancing switch diagnostic mode is enabled. ALRTBALSWSUM is a bitwise logical OR of ALRTBALSW[13:0].

ALRTBALSW is a bitwise alert status for all of the 14 channels/switches; the alert masking dependw on the TOPCELL1 and TOPCELL2 settings. The user should pay attention that if TOPCELL1 != TOPCELL2 then none of the alerts are masked. If TOPCELL1 = TOPCELL2, all the alerts above the TOPCELL1/2 position are masked. These conditions apply for all the four BALSW diagnostic SCAN requests.

The Balance Switch Diagnostic summary status ALRTBALSWSUM can be cleared if all enabled ALRTBALSW[13:0] alerts are resolved aby subsequent scan or by writing to logic 0.

Note: In Balance Switch Diagnostic mode, the ALRTOV, ALRTUV, and ALRTMSMTCH alerts are not updated, because these are only applicable during normal cell measurements.

BALSW Short Diagnostic

A short-circuit fault in the balancing path could be a short between SWn and SWn-1 as shown in Figure 86 or that a balancing FET is stuck in the conducting state. In the short-circuit state, the voltage between SWn and SWn-1 (switch voltage) is less than the voltage between Cn and Cn-1 (cell voltage).

When enabled, the balancing switch short diagnostic mode (SCANCFG[2:0] = 0b100) functions as follows:

- Disables the balancing switches automatically
- Configures the acquisition using ALTMUX path automatically
- Host initiates the acquisition on selected unipolar cells only (~POLARITYn and CELLENn)
- Compares the measurement to the threshold value BALSHRTTHR automatically (for unipolar cells only; i.e., POLARITYn = 0, see Table 70)
- If outside the threshold, sets the corresponding flag in ALRTBALSW automatically

For the best sensitivity to leakage current, set the threshold value based on the minimum cell voltage minus a small noise margin (100mV), then update the threshold value periodically or every time a measurement is taken depending on how fast the cell voltages are expected to change.

The BALSW short decision is as shown below in Table 70.

Table 70. BALSW Short Diagnostics Operation

BALSW	V_{SWn}	FAULT INDICATED?	POSSIBLE FAULT CONDITION
Off	> $V_{BALSHRTTHR}$	No	None
	< $V_{BALSHRTTHR}$	Yes	Short circuit or leakage current

An example of a BALSW short is shown below in Figure 86.

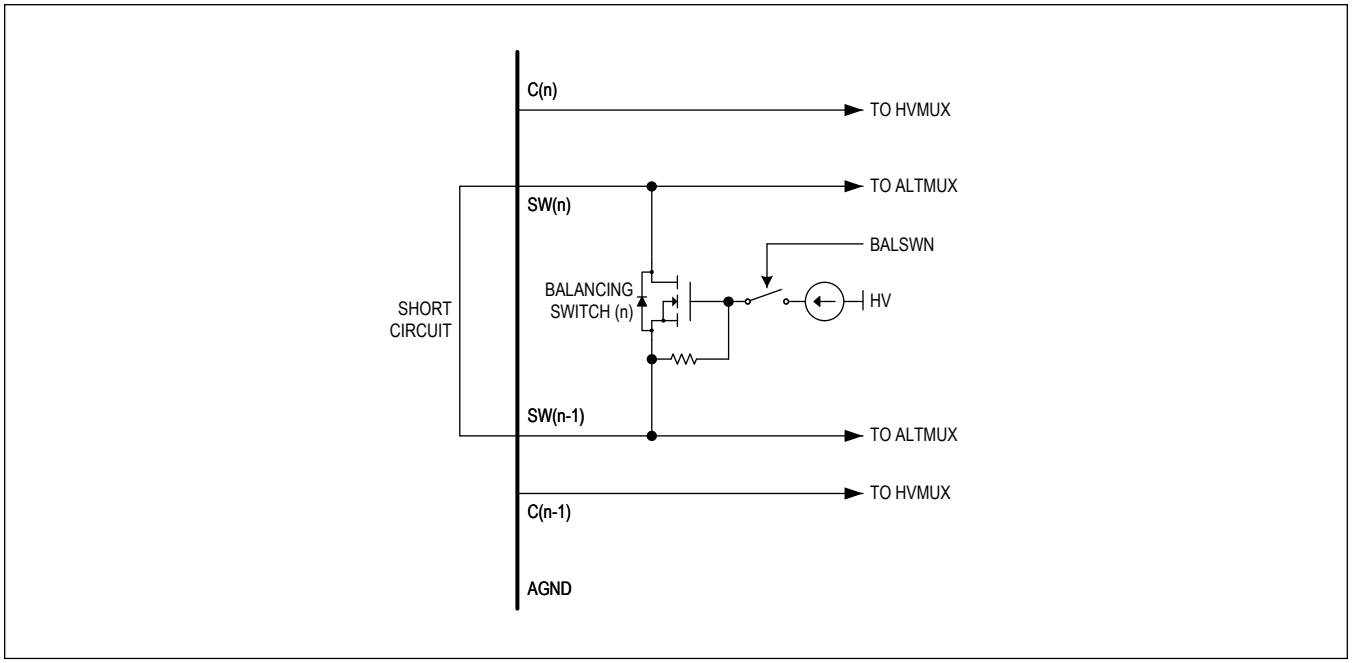


Figure 86. Balancing Switch Short

The BALSW short diagnostic procedural flow chart is shown in Figure 87.

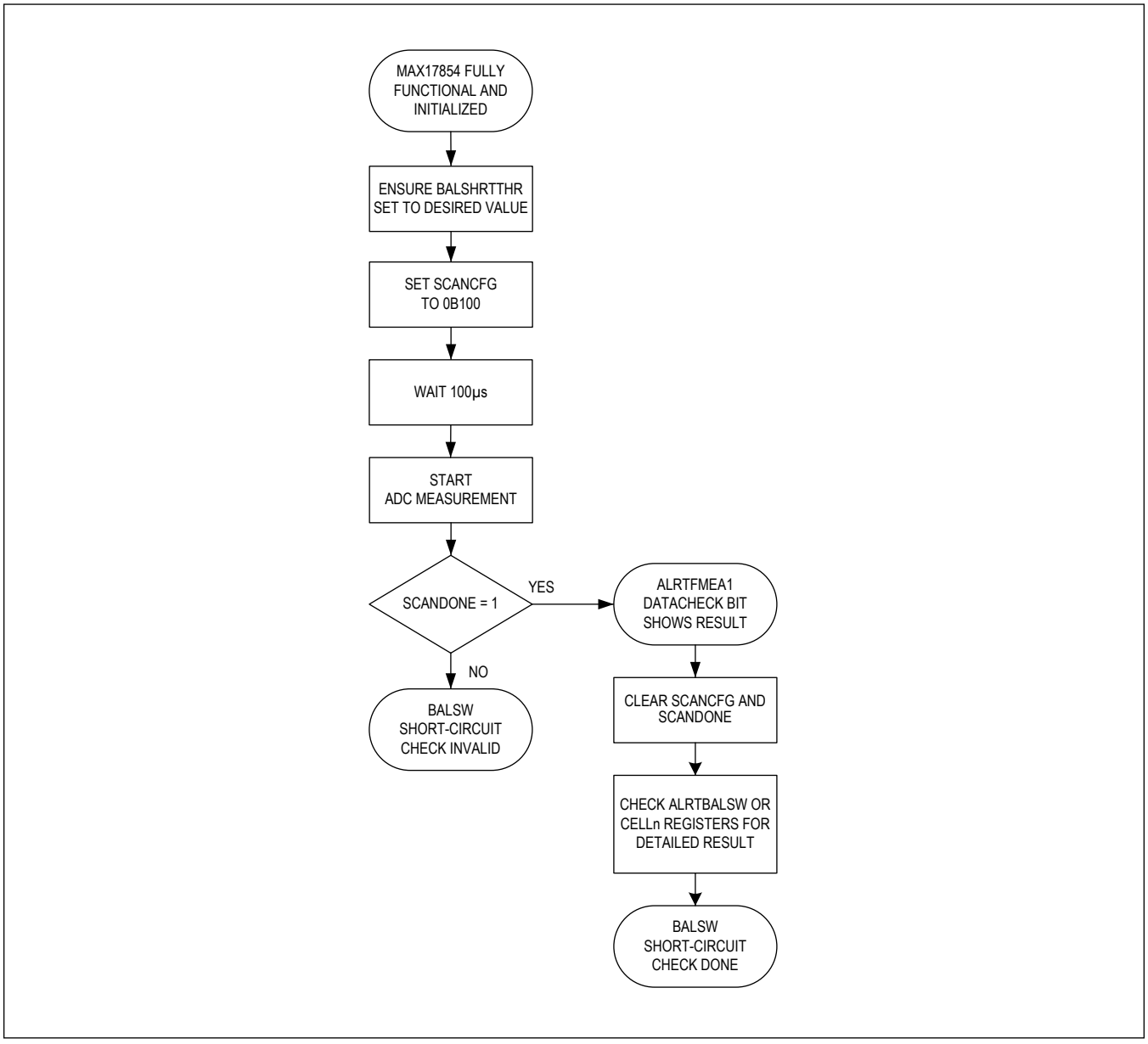


Figure 87. BALSW Short Diagnostic Chart

The BALSW short diagnostic automatically overrides the configuration settings during the measurements scan as shown in Table 71.

Table 71. BALSW Short Diagnostic Auto-Configuration

CONFIGURATION BITS	AUTOMATIC SETTING	PURPOSE
MEASUREEN1[15:14]	0b00	Disable V_{BLK} measurements
MEASUREEN1[13:0]	(~POLARITYn and CELLENn)	Enable only selected unipolar cell measurements
MEASUREEN2[5:0]	0b000000	Disable AUXn measurements

Table 71. BALSW Short Diagnostic Auto-Configuration (continued)

CONFIGURATION BITS	AUTOMATIC SETTING	PURPOSE
BALSWEN[13:0]	0x0000	Disable all balancing switches
DIAGSEL1/2	0x0	Disable all diagnostics
SCANCTRL:ALTMUXSEL	1	Enable ALTMUX measurement path
SCANCTRL:OVSAMPL	0x0	Oversample rates configured to 1

BALSW Open Diagnostic

The BALSW open diagnostic (SCANCFG[2:0] = 0b101) verifies that each enabled balancing switch is conducting (not open) as follows:

- Configures acquisition for bipolar mode (for measuring voltages near zero) automatically
- Configures acquisition for ALTMUX path automatically
- Configures acquisition to measure switch voltages for those switches enabled by BALSWENn automatically on all unipolar cell positions (~POLARITYn and BALSWENn).
  - **Note:** It is NOT necessary for the device to be in an active manual cell-balancing operation, only that BALSWEN be configured as desired.
- Host initiates acquisition
- Compares each measurement to the threshold value BALLOWTHR and BALHIGHTHR automatically; see Table 72
- If outside the threshold, set the corresponding flag in ALRTBALSW automatically

Set the thresholds by taking into account the minimum and maximum R_{SW} of the switch itself as specified in the *Electrical Characteristics* table and the balancing current for the application.

The BALSW open diagnostics operation decision is as shown in Table 72.

Table 72. BALSW Open Diagnostic Operation

BALSW	V_{SWn}	FAULT INDICATED?	POSSIBLE FAULT CONDITION
On	> $V_{BALHIGHTHR}$	Yes	Switch open circuit or overcurrent
	> $V_{BALLOWTHR}$	No	None
	< $V_{BALHIGHTHR}$		
	< $V_{BALLOWTHR}$	Yes	Path open circuit or short circuit

The BALSW open diagnostic procedural flow chart is shown in Figure 88.

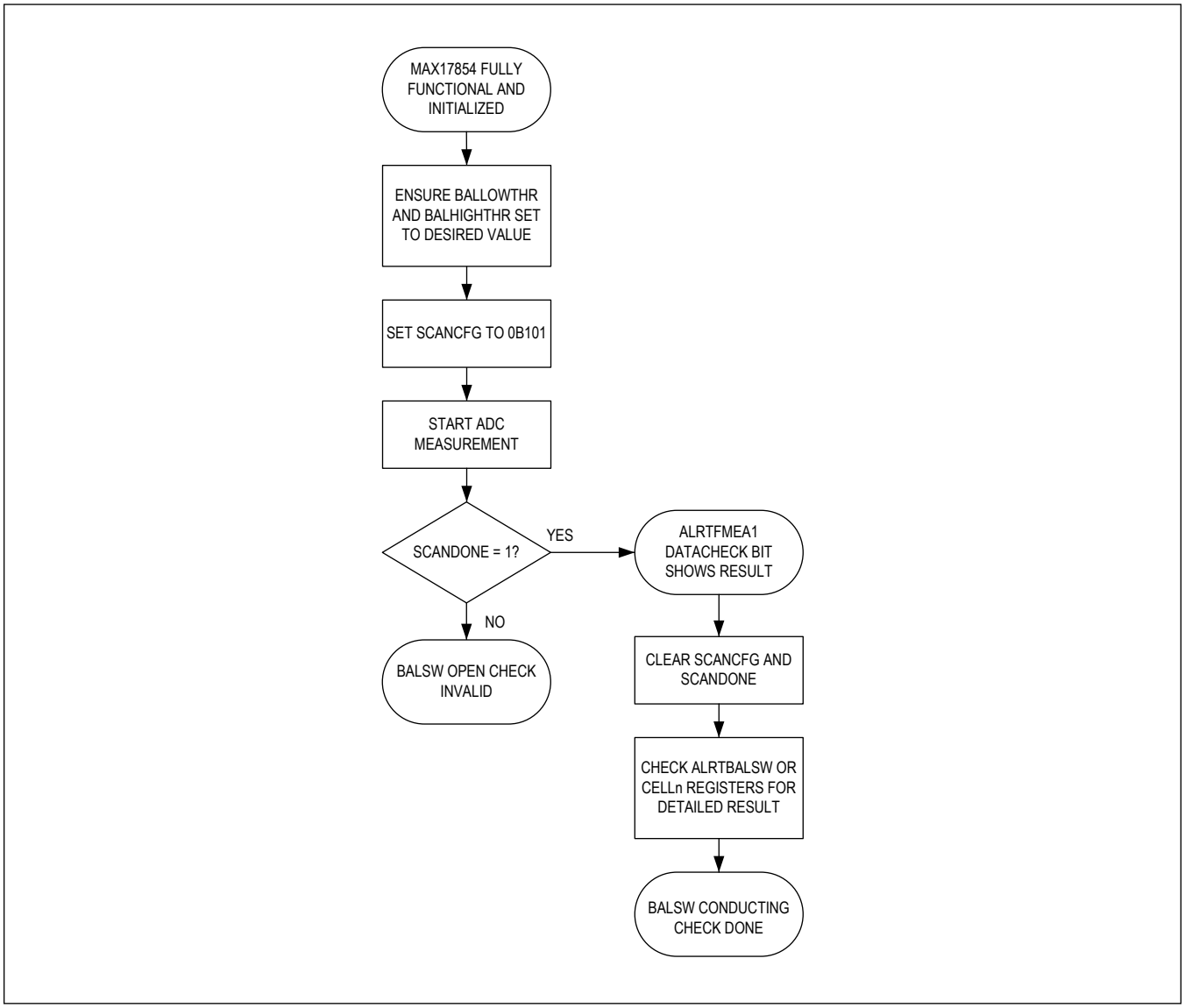


Figure 88. BALSW Open Diagnostic

The BALSW open diagnostic automatically overrides the configuration settings during the measurements scan as shown in Table 73.

Table 73. BALSW Open Diagnostic Auto-Configuration

CONFIGURATION BITS	AUTOMATIC SETTING	PURPOSE
MEASUREEN1[15:14]	0b00	Disable V_{BLK} measurements
MEASUREEN1[13:0]	BALSWENn and ~POLARITYn	Measure only active unipolar switch positions
MEASUREEN2[5:0]	0b000000	Disable AUXn measurements
DIAGSEL1/2	0x0	Disable all diagnostics
SCANCTRL:ALTMUXSEL	1	Enable ALTMUX measurement path

Table 73. BALSW Open Diagnostic Auto-Configuration (continued)

SCANCTRL:OVSAMPL	0x0	Oversample rate configured to 1

Even/Odd Sense-Wire Open Diagnostics

If enabled, the sense-wire open diagnostic modes detect if a cell sense-wire is disconnected as follows:

- Configures acquisition for bipolar mode (for measuring voltages near zero) automatically
- Closes nonadjacent switches (even or odd automatically)
- Configures acquisition to use ALTMUX path automatically
- Host waits 100µs for settling and then initiates the acquisition
- Compares the result to the BALHIGHTHR and BALLOWTHR registers automatically
- If outside thresholds, sets flags in ALRTBALSW automatically

Examples of normal and faulty operation are shown in Figure 90 through Figure 94 for examples with and without bus bars (identified by POLARITYn = 1). By examining the combined reported results from even and odd runs, the location and type of fault can be determined. Figure 89 shows the procedure performed by the MAX17854 during an Open Sense-Wire Diagnostic.

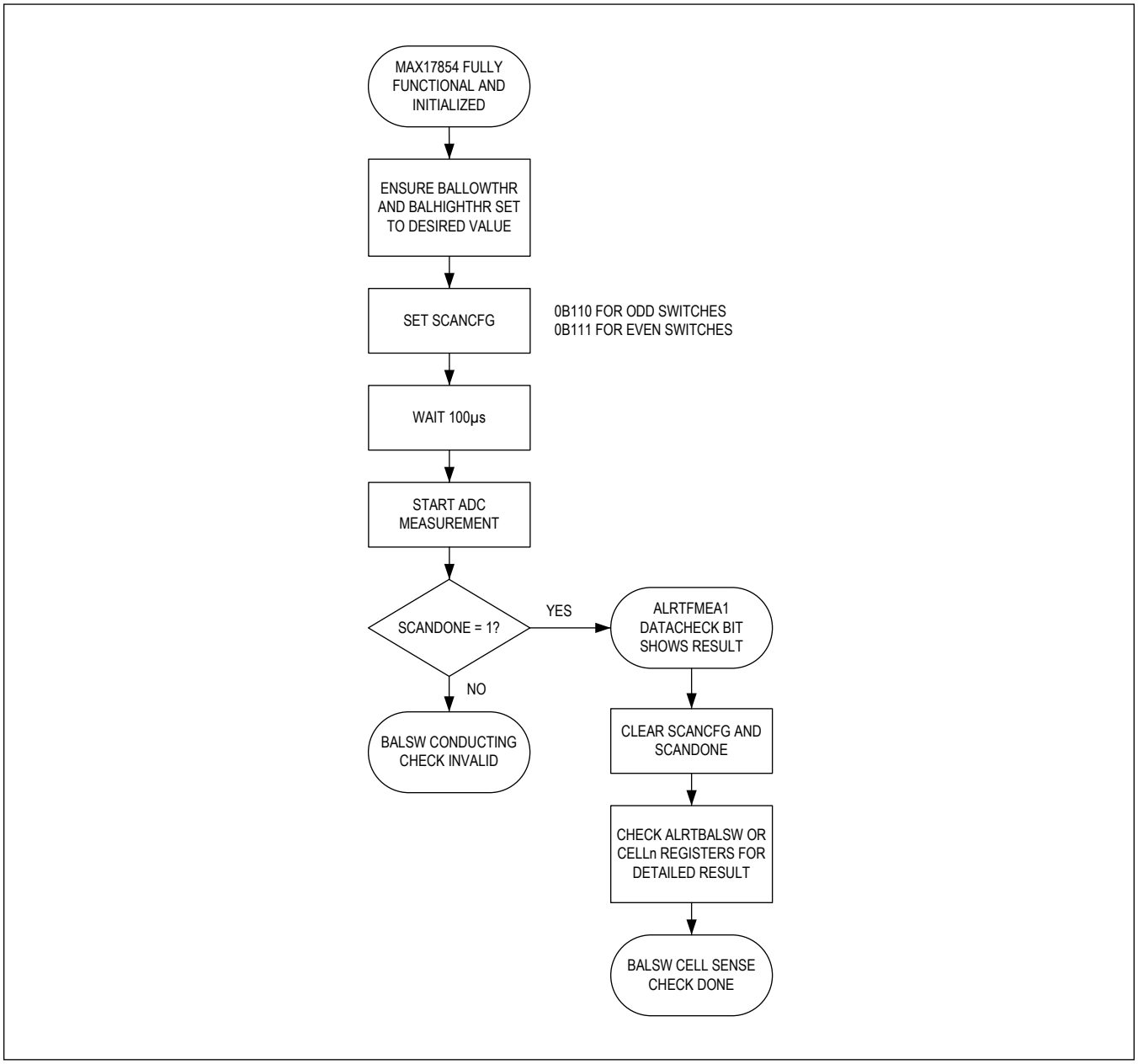


Figure 89. Sense-Wire Open Diagnostic Flow

Table 74 shows the configuration setting overrides that the MAX17854 will temporarily enforce during an Open Sense-Wire Diagnostic measurement scan.

Table 74. Sense-Wire Open Diagnostic Automatic Configuration Overrides

CONFIGURATION BIT(S)	CONFIGURATION STATE	TASK
BALSWEN[13:0]	1555h (SCANCFG[2:0] = 0b110) or 2AAAh (SCANCFG[2:0] = 0b111)	Enable odd switches Enable even switches Switch positions with POLARITYn = 1 (bipolar/bus bar) and those above TOPCELL are masked/disabled.
MEASUREEN1[15:14]	0b00	Disable V_{BLK} measurements
MEASUREEN1[13:0]	BALSWENn and ~POLARITYn)	BALSWEN[13:0] is set as per automatic overrides shown above. Measure only active switch positions per automatic BALSWEN overrides and unipolar positions.
MEASUREEN2[5:0]	0b000000	Disable AUXn measurements
DIAGSEL1/2	0x0	Disable all diagnostics
SCANCTRL:ALTMUXSEL	1	Enable ALTMUX measurement path
SCANCTRL:OVSAMPL	0x0	Oversample configured to 1

These overrides are only active during the scan, normal configured operation is restored at the end of the scan.

Examples of Normal Sense-Wire Operation

Figure 90 shows the electrical behavior during both Odd and Even Sense-Wire Open Diagnostics when no sense-wires are open or compromised.

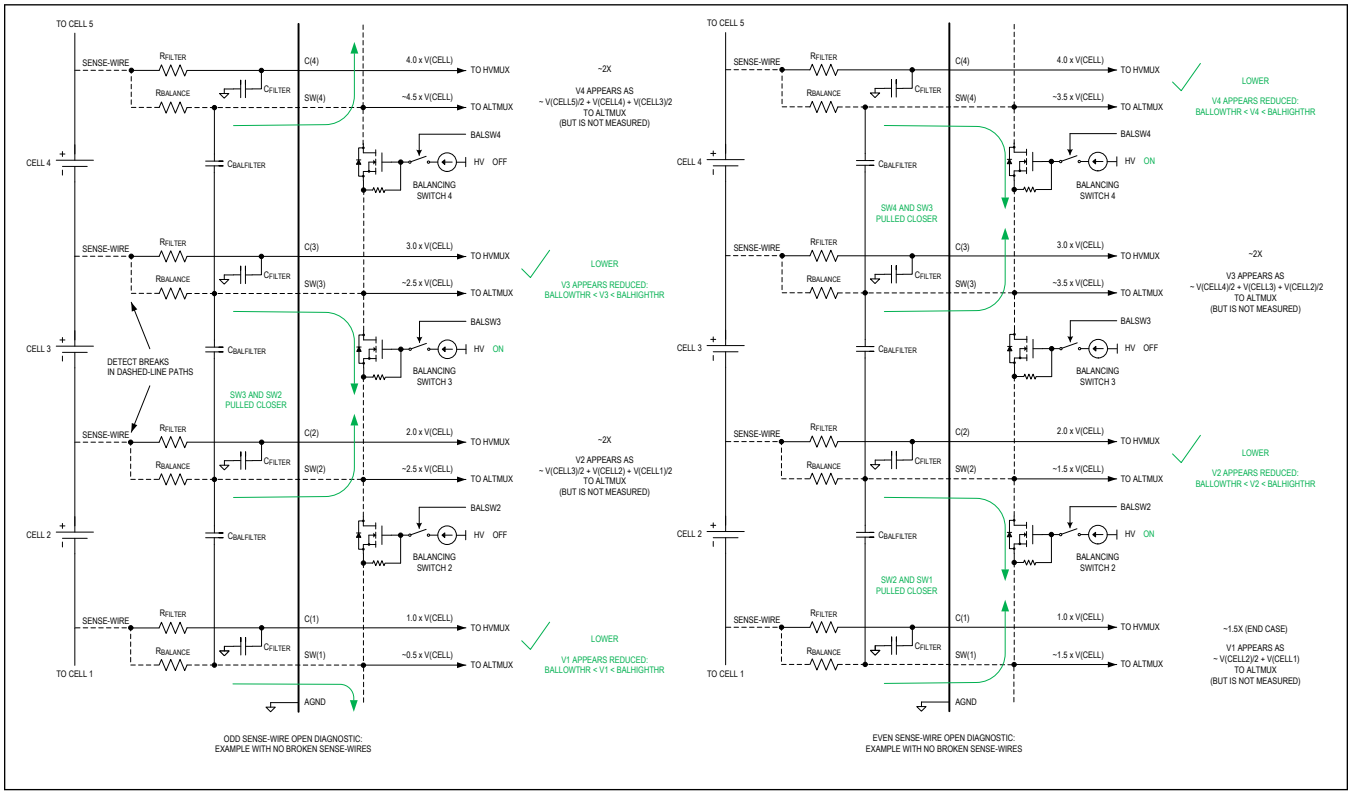


Figure 90. Cell Sense-Wire Open Diagnostic Operations - Normal Operation

Figure 91 shows the electrical behavior during both Odd and Even Sense-Wire Open Diagnostics when no sense-wires

are open or compromised, with bus bars included.

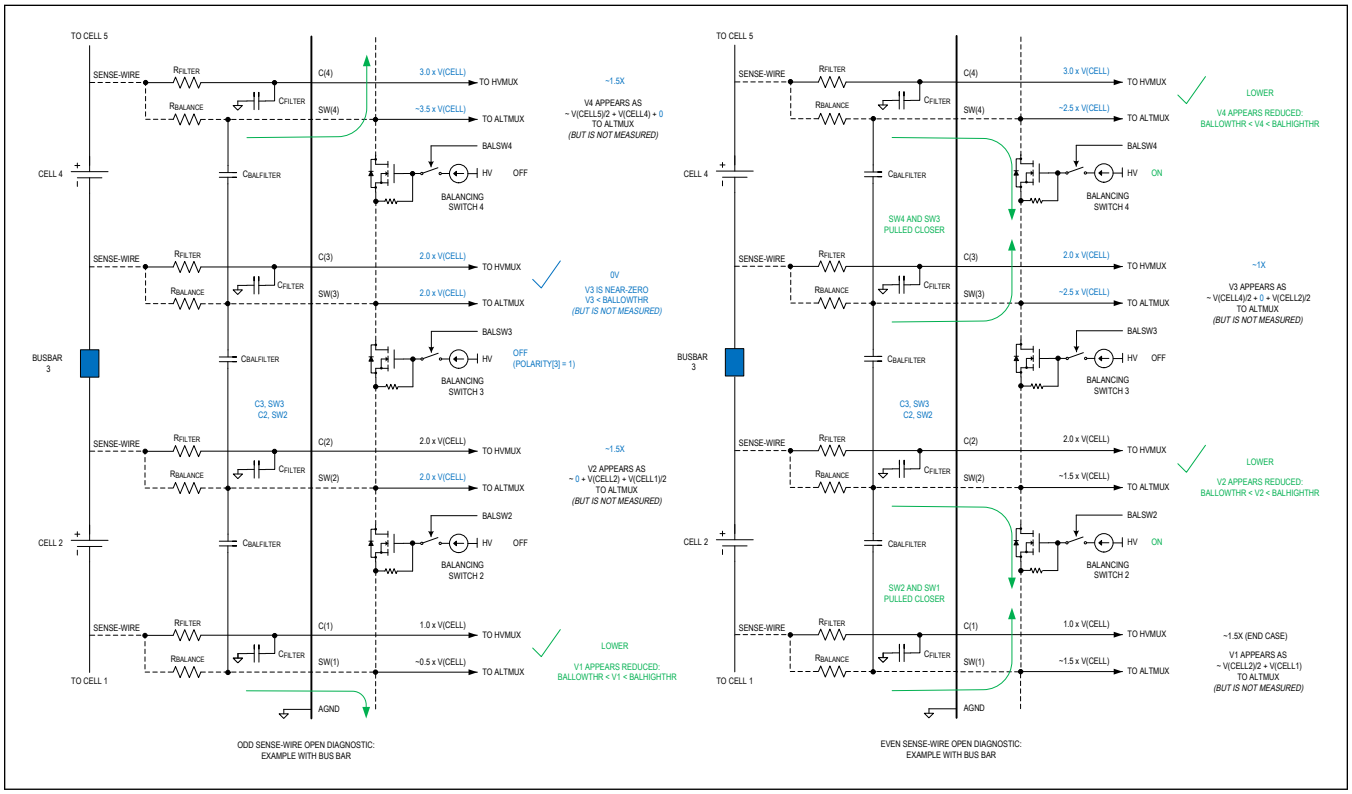


Figure 91. Cell Sense-Wire Open Diagnostic Operations - Normal Operation, Including Bus Bars

Examples of Broken Sense-Wire Fault Detection

Figure 92, Figure 93, Table 75, and Table 77 show examples of how broken sense-wires are detected and diagnosed using combinations of Odd and Even Sense-Wire Open Diagnostics.

Figure 92 shows the electrical behavior during both Odd and Even Sense-Wire Open Diagnostic sequences when a sense-wire in an odd position is broken. The alerts that will be issued as a result of the fault are also shown.

Figure 93 shows the electrical behavior during both Odd and Even Sense-Wire Open Diagnostic sequences when a sense-wire in an even position is broken. The alerts that will be issued as a result of the fault are also shown.

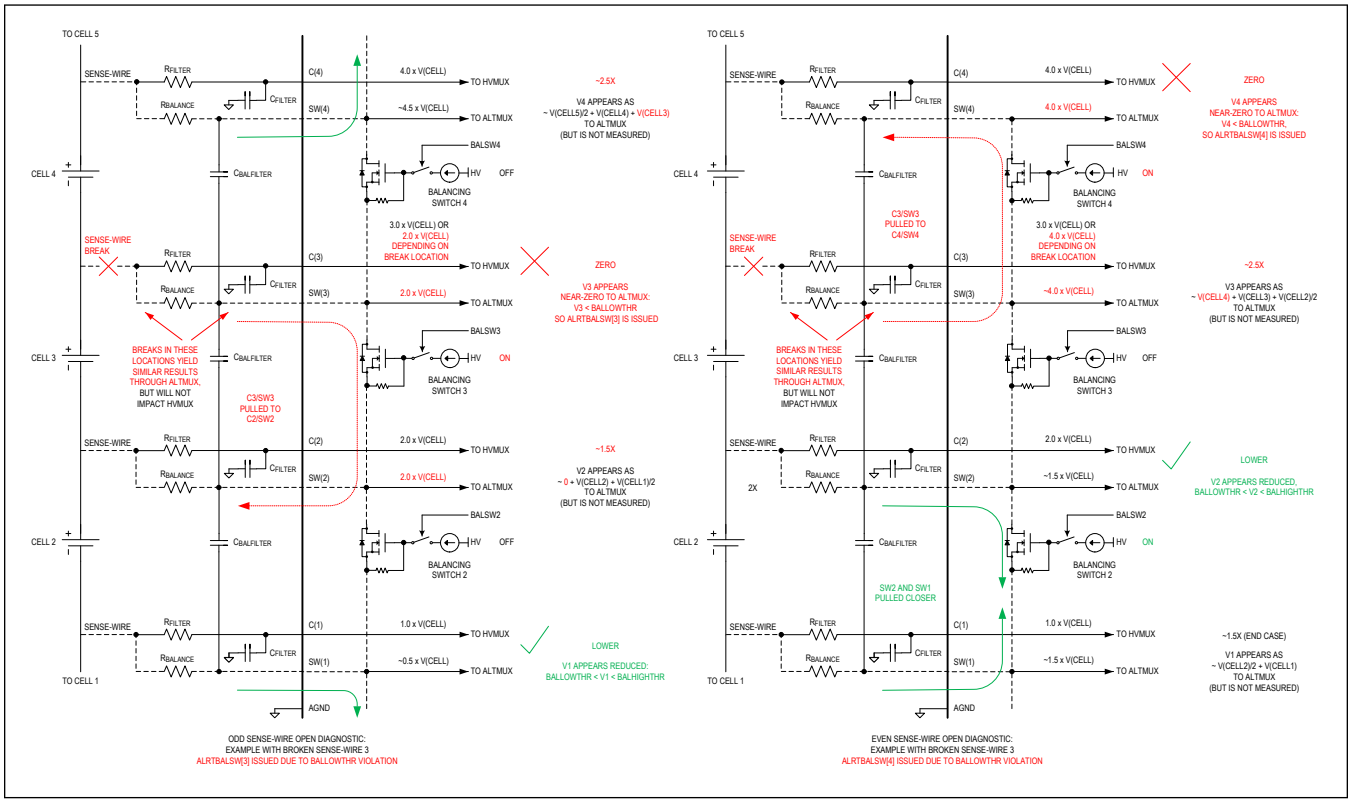


Figure 92. Cell Sense-Wire Open Diagnostic Operations - Example with Odd Sense-Wire Fault

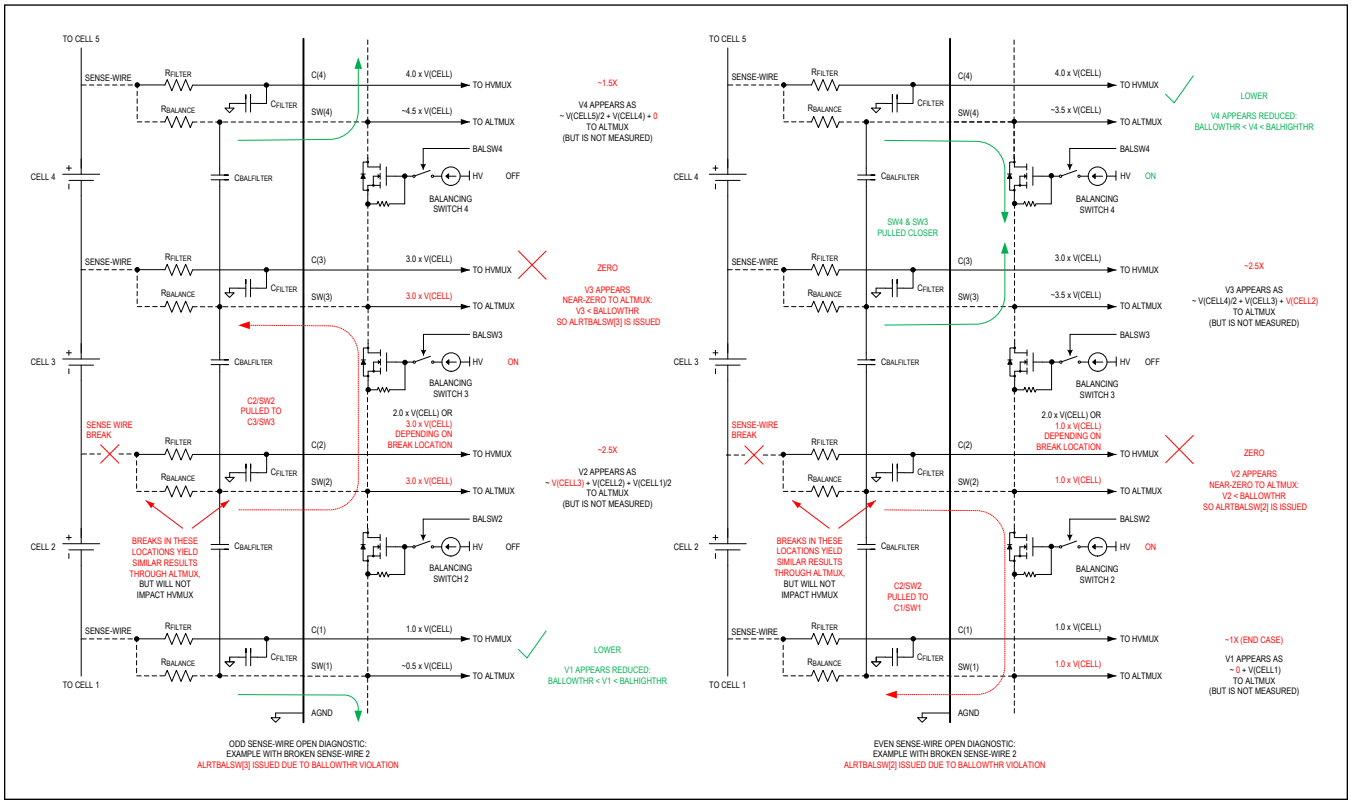


Figure 93. Cell Sense-Wire Open Diagnostic Operations - Example with Even Sense-Wire Fault

Sense-Wire Open Fault Detection Results

Table 75 shows the measurement alerts that correspond to a break in each sense-wire position during an Odd Sense-Wire Open Diagnostic. When combined with the results from an Even Sense-Wire Open Diagnostic, the exact location of the sense-wire fault can be determined.

Table 75. Odd Sense-Wire Open Measurement Results for Broken Sense-Wires

		SENSE-WIRE OPEN FAULT LOCATION														
		SW0	SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8	SW9	SW10	SW11	SW12	SW13	SW14
CELL MEASUREMENT	Cell1	LO	LO	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK
	Cell2	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM
	Cell3	OK	OK	LO	LO	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK
	Cell4	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM
	Cell5	OK	OK	OK	OK	LO	LO	OK	OK	OK	OK	OK	OK	OK	OK	OK
	Cell6	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM
	Cell7	OK	OK	OK	OK	OK	OK	LO	LO	OK	OK	OK	OK	OK	OK	OK
	Cell8	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM
	Cell9	OK	OK	OK	OK	OK	OK	OK	OK	LO	LO	OK	OK	OK	OK	OK
	Cell10	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM
	Cell11	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	LO	LO	OK	OK	OK
	Cell12	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM

Table 75. Odd Sense-Wire Open Measurement Results for Broken Sense-Wires (continued)

	Cell13	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	**LO**	**LO**	OK
	Cell14	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM

Note: OK = no error detected; LO = BALLOWTHR violation; NM = not measured; maximum result is 2.5V

Table 76 shows the measurement alerts that correspond to a break in each sense wire position during an Even Sense-Wire Open Diagnostic. When combined with the results from an Odd Sense-Wire Open Diagnostic, the exact location of the sense-wire fault can be determined.

Table 76. Even Sense-Wire Open Measurement Results for Broken Sense-Wires

		SENSE-WIRE OPEN FAULT LOCATION														
		SW0	**SW1**	**SW2**	**SW3**	**SW4**	**SW5**	**SW6**	**SW7**	**SW8**	**SW9**	**SW10**	**SW11**	**SW12**	**SW13**	**SW14**
CELL MEASUREMENT	**Cell1**	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM
	Cell2	OK	**LO**	**LO**	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK
	Cell3	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM
	Cell4	OK	OK	OK	**LO**	**LO**	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK
	Cell5	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM
	Cell6	OK	OK	OK	OK	OK	**LO**	**LO**	OK	OK	OK	OK	OK	OK	OK	OK
	Cell7	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM
	Cell8	OK	OK	OK	OK	OK	OK	OK	**LO**	**LO**	OK	OK	OK	OK	OK	OK
	Cell9	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM
	Cell10	OK	OK	OK	OK	OK	OK	OK	OK	OK	**LO**	**LO**	OK	OK	OK	OK
	Cell11	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM
	Cell12	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	**LO**	**LO**	OK	OK
	Cell13	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM
	Cell14	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	**LO**	**LO**

Note: OK = no error detected; LO = BALLOWTHR violation; NM = not measured; maximum result is 2.5V

When combined together, the two diagnostics can identify the exact location of a broken sense-wire. The combined diagnostic results are shown in Table 77.

Table 77. Odd and Even Sense-Wire Open Measurement Results Overlay for Broken Sense-Wires

		SENSE-WIRE OPEN FAULT LOCATION														
		SW0	**SW1**	**SW2**	**SW3**	**SW4**	**SW5**	**SW6**	**SW7**	**SW8**	**SW9**	**SW10**	**SW11**	**SW12**	**SW13**	**SW14**
CELL MEASUREMENT	**Cell1**	**LO**	**LO**	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK
	Cell2	OK	**LO**	**LO**	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK
	Cell3	OK	OK	**LO**	**LO**	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK
	Cell4	OK	OK	OK	**LO**	**LO**	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK
	Cell5	OK	OK	OK	OK	**LO**	**LO**	OK	OK	OK	OK	OK	OK	OK	OK	OK
	Cell6	OK	OK	OK	OK	OK	**LO**	**LO**	OK	OK	OK	OK	OK	OK	OK	OK
	Cell7	OK	OK	OK	OK	OK	OK	**LO**	**LO**	OK	OK	OK	OK	OK	OK	OK
	Cell8	OK	OK	OK	OK	OK	OK	OK	**LO**	**LO**	OK	OK	OK	OK	OK	OK
	Cell9	OK	OK	OK	OK	OK	OK	OK	OK	**LO**	**LO**	OK	OK	OK	OK	OK
	Cell10	OK	OK	OK	OK	OK	OK	OK	OK	OK	**LO**	**LO**	OK	OK	OK	OK
	Cell11	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	**LO**	**LO**	OK	OK	OK

Table 77. Odd and Even Sense-Wire Open Measurement Results Overlay for Broken Sense-Wires (continued)

	Cell12	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	**LO**	**LO**	OK	OK
	Cell13	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	**LO**	**LO**	OK
	Cell14	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	**LO**	**LO**

Note: OK = no error detected; LO = BALLOWTHR violation; maximum result is 2.5V

Examples of Broken Internal Switch/Trace Fault Detection

Figure 94 and Table 77 show examples of how broken sense wires are detected and diagnosed using combinations of Odd and Even Sense-Wire Open Diagnostics.

Figure 94 shows the electrical behavior during both Odd and Even Sense-Wire Open Diagnostic sequences when there is a fault in an internal switch or connection. The alerts that will be issued as a result of the fault are also shown.

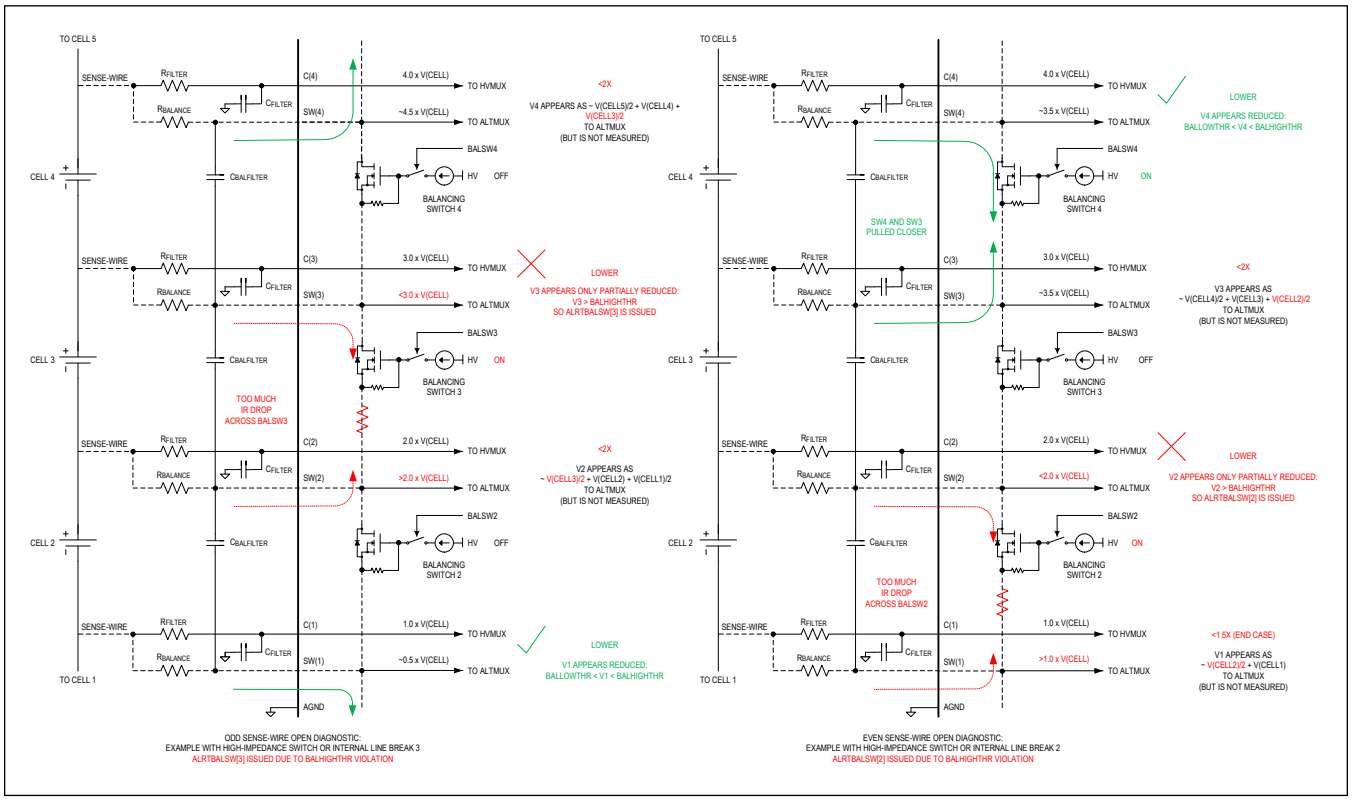


Figure 94. Cell Sense-Wire Open Diagnostic Operations - Example with Broken BALSW or Internal Trace

Broken Switch Fault Detection Results

When combined together, the two diagnostics can cover and identify the exact location of a faulty switch or internal trace. The combined diagnostic results are shown in Table 77. Notice that unlike a broken sense-wire, only a single ALRTBALSW alert is issued for faults of this type.

Table 78. Odd and Even Sense-Wire Open Measurement Results Overlay for Broken Sense-Wires

	SWITCH OR TRACE FAULT LOCATION (BALSW)

Table 78. Odd and Even Sense-Wire Open Measurement Results Overlay for Broken Sense-Wires (continued)

		1	2	3	4	5	6	7	8	9	10	11	12	13	14
CELL MEASUREMENT	Cell1	HI	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK
	Cell2	OK	HI	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK
	Cell3	OK	OK	HI	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK
	Cell4	OK	OK	OK	HI	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK
	Cell5	OK	OK	OK	OK	HI	OK	OK	OK	OK	OK	OK	OK	OK	OK
	Cell6	OK	OK	OK	OK	OK	HI	OK	OK	OK	OK	OK	OK	OK	OK
	Cell7	OK	OK	OK	OK	OK	OK	HI	OK	OK	OK	OK	OK	OK	OK
	Cell8	OK	OK	OK	OK	OK	OK	OK	HI	OK	OK	OK	OK	OK	OK
	Cell9	OK	OK	OK	OK	OK	OK	OK	OK	HI	OK	OK	OK	OK	OK
	Cell10	OK	OK	OK	OK	OK	OK	OK	OK	OK	HI	OK	OK	OK	OK
	Cell11	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	HI	OK	OK	OK
	Cell12	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	HI	OK	OK
	Cell13	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	HI	OK
	Cell14	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	HI

Note: OK = no error detected; HI = BALHIGHTHR violation; maximum result is 2.5V

ADC End of Scan Diagnostics

This diagnostic is performed at the end of a measurement sequence that is configured to use the ADC (SCANCFG = 0b000 or 0b001) when ADCZSFSEN = 1. The ADC measurements are taken in bipolar mode.

For full-scale diagnostic: $ADC_{REF} = V_{REF}$ and $ADC_{IN} = V_{AA}$

If the result from the ADC is less than FFFh (12-bit result), an alert is issued by setting the ALRTADCFS bit in the FMEA2 register.

For zero-scale diagnostic: $ADC_{REF} = V_{REF}$ and $ADC_{IN} = -V_{AA}$

If the result from the ADC is greater than 000h, an alert is issued by setting the ALRTADCZS bit in the FMEA2 register.

The DIAGSEL1 and DIAGSEL2 registers can be configured to obtain further diagnostic information regarding the ADC.

Register Map

MAX17854 User Register Map

Register Map Usage Guidelines

The Register Map (RMap) for the MAX17854 is detailed in the following section. General usage guidelines pertaining to the entire RMap are outlined here, detailing the expected usage of the RMap, including how various protocol and access issues are handled.

Interface Protocol Errors

In order for read and write transactions to be accepted, all interface protocol expectations must be met. If protocol errors occur, these will be reported through alerts in the STATUS1 and STATUS2 registers, notifying the user of the issue observed. If a protocol error occurs, none of the following behaviors will apply, because the transaction will be rejected, even if the transaction addresses a reserved register address. See the UART interface descriptions for complete details on expected interface protocols.

Reserved Registers

All user-accessible registers are contained in the address space 0x00 to 0x98. Any address/register in this space not specifically listed in the RMap should be treated as Reserved; for the MAX17854, the following addresses within the user address space are reserved: 0x2C, 0x2D, 0x2E, 0x2F, and 0x46. The address space 0x99 to 0xFF is also Reserved for Analog Devices Use Only.

If an otherwise valid attempt to read or write to a reserved register address occurs (with no protocol or CRC/PEC errors), no errors will be issued for the UART transaction. No data written to a reserved register address will be internally stored, and reserved register will always read back all zeros. If a UART Block Readback request includes any reserved register addresses, these addresses will be included in the readback data, with all zeros returned; no addresses will be skipped during UART Block Readback transactions. Users should normally avoid writing to reserved register, as the MAX17854 will not respond to such transactions.

Unused Bitfields

Within the user-accessible registers, there are many unused bitfields, denoted by a dash (-) in the RMap. During read and write transactions, PEC and CRC checks apply to all 16 bits of data, including any unused bitfields. No data written to an unused bitfield is internally stored, and unused bitfields always read back all zeros.

Reserved Bitfields

Within the RMap, there are several reserved bitfields: DEVCFG1RSRV (4 bits), DEVCFG2RSRV (5 bits); these are reserved for future use. During read and write transactions, PEC and CRC checks apply to all 16 bits of data, including any reserved bitfields. Data written to a reserved bitfield are internally stored (though the settings of these bitfields will have no effect on internal operations), and the reserved bitfields always read back their current settings.

Register Blocks and Transaction Reject Behavior

The RMap is organized into several register blocks. Each register block is subject to specific transaction rejection behaviors as detailed in the register block descriptions which follow. These behaviors ensure that register content currently in use by any requested internal process is not subject to alteration while in use. In general, the register blocks are organized and defined to provide maximum transaction efficiency while also ensuring the ultimate level of safety.

If a valid write transaction to a blocked (busy) register occurs, the transaction will be rejected, and the ALRTRJCT bit will be set, indicating the write was ignored since that register was currently being used by an ongoing internal operation. In general, user software should be written to avoid modifying register content that is currently in use, instead confirming that the internal process has completed before any modifications are written to the MAX17854.

ADDRESS	NAME	MSB							LSB
STATUS Registers									
0x00	VERSION[15:8]	MOD[11:4]							
	VERSION[7:0]	MOD[3:0]				VER[3:0]			

ADDRESS	NAME	MSB							LSB
0x01	ADDRESS[15:8]	ADDRUNLOCK	BA[4:0]					TA[4:3]	
	ADDRESS[7:0]	TA[2:0]			DA[4:0]				
0x02	STATUS1[15:8]	ALRTSCAN	ALRTRST	ALRTMSMTCH	ALRTCELLOVST	ALRTCELLUVST	ALRTBLKOVST	ALRTBLKUVST	ALRTAUXOVST
	STATUS1[7:0]	ALRTAUXUVST	–	ALRTPEC	ALRTINTRFC	ALRTCAL	ALRTCBAL	ALRTFMEA2	ALRTFMEA1
0x03	STATUS2[15:8]	ALRTPECUP	ALRTPECDN	ALRTMANUP	ALRTMANDN	ALRTPARUP	ALRTPARDN	ALRTDUALUART	–
	STATUS2[7:0]	–	–	–	–	–	ALRTI2C	–	ALRTRJCT
0x04	STATUS3[15:8]	ALRTCBTIMEOUT	ALRTCBTEMP	ALRTCBCAL	ALRTCBNTFY	ALRTCBDONE	–	–	–
	STATUS3[7:0]	–	–	–	–	–	–	–	–
0x05	FMEA1[15:8]	ALRTOSC1	ALRTOSC2	ALRTCOMMSEU1	ALRTCOMMSEL1	ALRTCOMMSEU2	ALRTCOMMSEL2	ALRTVDDL3	ALRTVDDL2
	FMEA1[7:0]	ALRTVDDL1	ALRTGNDL3	ALRTGNDL2	ALRTGNDL1	ALRTHVUV	ALRTHVHDRM	ALRTHVOV	ALRTBALSWSUM
0x06	FMEA2[15:8]	ALRTUSER	ALRTDCINMUX	ALRTAUXPRTCTSUM	ALRTTEMP	ALRTSCANTIMEOUT	–	–	–
	FMEA2[7:0]	–	–	–	–	ALRTADCZS	ALRTADCFS	ALRTCOMPACCOV	ALRTCOMPACCUV
0x07	ALRTSUM[15:8]	ALRTADCOVST	ALRTCOMPOVST	ALRTADCUVST	ALRTCOMPUVST	ALRTADCAUXOVST	ALRTCOMPAUXOVST	ALRTADCAUXUVST	ALRTCOMPAUXUVST
	ALRTSUM[7:0]	–	–	–	ALRTCALOSADC	ALRTCALOSR	ALRTCALOSTHRM	ALRTCALGAINP	ALRTCALGAINR
0x08	ALRTOVCELL[15:8]	–	–	ALRTOV[14:9]					
	ALRTOVCELL[7:0]	ALRTOV[8:1]							
0x09	ALRTUVCELL[15:8]	–	–	ALRTUV[14:9]					
	ALRTUVCELL[7:0]	ALRTUV[8:1]							
0x0A	MINMAXCELL[15:8]	–	–	–	–	MAXCELL[3:0]			
	MINMAXCELL[7:0]	–	–	–	–	MINCELL[3:0]			
0x0B	ALRTAUXPRTCTREG[15:8]	–	–	–	–	–	–	–	–
	ALRTAUXPRTCTREG[7:0]	–	–	ALRTAUXPRTCT[5:4]		ALRTAUXPRTCT[3:0]			
0x0C	ALRTAUXOVREG[15:8]	–	–	–	–	–	–	–	–
	ALRTAUXOVREG[7:0]	–	–	ALRTAUXOV[5:4]		ALRTAUXOV[3:0]			
0x0D	ALRTAUXUVREG[15:8]	–	–	–	–	–	–	–	–
	ALRTAUXUVREG[7:0]	–	–	ALRTAUXUV[5:4]		ALRTAUXUV[3:0]			
0x0E	ALRTCOMPOVREG[15:8]	–	–	ALRTCOMPOV[14:9]					

ADDRESS	NAME	MSB							LSB
	ALRTCOMPOVREG[7:0]	ALRTCOMPOV[8:1]							
0x0F	ALRTCOMPUVREG[15:8]	–	–	ALRTCOMPUV[14:9]					
	ALRTCOMPUVREG[7:0]	ALRTCOMPUV[8:1]							
0x10	ALRTCOMPAUXOVREG[15:8]	–	–	–	–	–	–	–	–
	ALRTCOMPAUXOVREG[7:0]	–	–	ALRTCOMPAUXOV[5:4]		ALRTCOMPAUXOV[3:0]			
0x11	ALRTCOMPAUXUVREG[15:8]	–	–	–	–	–	–	–	–
	ALRTCOMPAUXUVREG[7:0]	–	–	ALRTCOMPAUXUV[5:4]		ALRTCOMPAUXUV[3:0]			
0x12	ALRTBALSWREG[15:8]	–	–	ALRTBALSW[13:8]					
	ALRTBALSWREG[7:0]	ALRTBALSW[7:0]							
0x13	SWACTION[15:8]	–	–	–	–	–	–	–	–
	SWACTION[7:0]	–	–	–	–	–	–	–	SWPOR
GENERAL CONFIGURATION Registers									
0x14	DEVCFG1[15:8]	UARTCFG[1:0]		TXUIDLEHIZ	TXLIDLEHIZ	DEVCFG1RSRV[1:0]		ALIVECNTEN	UARTHOST
	DEVCFG1[7:0]	DEVCFG1RSRV	DEVCFG1RSRV	DEVCFG1RSRV	DEVCFG1RSRV	UARTDCEN	NOPEC	ALERTEN	DBLBUFEN
0x15	DEVCFG2[15:8]	IIRFC[2:0]			–	DEVCFG2RSRV[3:0]			
	DEVCFG2[7:0]	–	HVCPDIS	FORCEPOR	ALERTDCTSTEN	–	DEVCFG2RSRV	SCANTODIS	CBTODIS
0x16	AUXGPIOCFG[15:8]	I2CEN	–	GPIOEN[5:4]		GPIOEN[3:0]			
	AUXGPIOCFG[7:0]	–	–	GPIODIR[5:4]		GPIODIR[3:0]			
0x17	GPIOCFG[15:8]	–	–	GPIODRV[5:4]		GPIODRV[3:0]			
	GPIOCFG[7:0]	–	–	GPIORD[5:4]		GPIORD[3:0]			
0x18	PACKCFG[15:8]	FLXPCKEN2	FLXPCKEN1	FLXPCKSCAN	–	TOPBLOCK[3:0]			
	PACKCFG[7:0]	TOPCELL2[3:0]				TOPCELL1[3:0]			
ALERT CONFIGURATION Registers									
0x19	ALRTIRQEN[15:8]	SCANALRTEN	–	MSMTCHALRTEN	CELLOVSTALRTEN	CELLUVSTALRTEN	BLKOVSTALRTEN	BLKUVSTALRTEN	AUXOVSTALRTEN
	ALRTIRQEN[7:0]	AUXUVSTALRTEN	–	PECALRTEN	INTRFCALRTEN	CALALRTEN	CBALALRTEN	FMEA2ALRTEN	FMEA1ALRTEN
0x1A	ALRTOVEN[15:8]	–	BLKOVALRTEN	OVALRTEN[14:9]					
	ALRTOVEN[7:0]	OVALRTEN[8:1]							
0x1B	ALRTUVEN[15:8]	–	BLKUVALRTEN	UVALRTEN[14:9]					
	ALRTUVEN[7:0]	UVALRTEN[8:1]							
0x1C	ALRTAUXOVEN[15:8]	–	–	–	–	–	–	–	–

ADDRESS	NAME	MSB							LSB
	ALRTAUXOVEN[7:0]	–	–	AUXOVALRTEN[5:4]		AUXOVALRTEN[3:0]			
0x1D	ALRTAUXUVEN[15:8]	–	–	–	–	–	–	–	–
	ALRTAUXUVEN[7:0]	–	–	AUXUVALRTEN[5:4]		AUXUVALRTEN[3:0]			
0x1E	ALRTCALTST[15:8]	–	–	–	–	–	–	–	–
	ALRTCALTST[7:0]	–	–	–	CALOSADCALRTFRC	CALOSRALRTFRC	CALOSTHRMALRTFRC	CALGAINPALRTFRC	CALGAINRALRTFRC
THRESHOLD Registers									
0x1F	OVTHCLRREG[15:8]	OVTHCLR[13:6]							
	OVTHCLRREG[7:0]	OVTHCLR[5:0]						–	–
0x20	OVTHSETREG[15:8]	OVTHSET[13:6]							
	OVTHSETREG[7:0]	OVTHSET[5:0]						–	–
0x21	UVTHCLRREG[15:8]	UVTHCLR[13:6]							
	UVTHCLRREG[7:0]	UVTHCLR[5:0]						–	–
0x22	UVTHSETREG[15:8]	UVTHSET[13:6]							
	UVTHSETREG[7:0]	UVTHSET[5:0]						–	–
0x23	MSMTCHREG[15:8]	MSMTCH[13:6]							
	MSMTCHREG[7:0]	MSMTCH[5:0]						–	–
0x24	BIPOVTHCLRREG[15:8]	BIPOVTHCLR[13:6]							
	BIPOVTHCLRREG[7:0]	BIPOVTHCLR[5:0]						–	–
0x25	BIPOVTHSETREG[15:8]	BIPOVTHSET[13:6]							
	BIPOVTHSETREG[7:0]	BIPOVTHSET[5:0]						–	–
0x26	BIPUVTHCLRREG[15:8]	BIPUVTHCLR[13:6]							
	BIPUVTHCLRREG[7:0]	BIPUVTHCLR[5:0]						–	–
0x27	BIPUVTHSETREG[15:8]	BIPUVTHSET[13:6]							
	BIPUVTHSETREG[7:0]	BIPUVTHSET[5:0]						–	–
0x28	BLKOVTHCLRREG[15:8]	BLKOVTHCLR[13:6]							
	BLKOVTHCLRREG[7:0]	BLKOVTHCLR[5:0]						–	–
0x29	BLKOVTHSETREG[15:8]	BLKOVTHSET[13:6]							
	BLKOVTHSETREG[7:0]	BLKOVTHSET[5:0]						–	–
0x2A	BLKUVTHCLRREG[15:8]	BLKUVTHCLR[13:6]							
	BLKUVTHCLRREG[7:0]	BLKUVTHCLR[5:0]						–	–
0x2B	BLKUVTHSETREG[15:8]	BLKUVTHSET[13:6]							
	BLKUVTHSETREG[7:0]	BLKUVTHSET[5:0]						–	–
0x30	AUXROVTHCLRREG[15:8]	AUXROVTHCLR[13:6]							

ADDRESS	NAME	MSB							LSB
	AUXROVTHCLRREG[7:0]	AUXROVTHCLR[5:0]						–	–
0x31	AUXROVTHSETREG[15:8]	AUXROVTHSET[13:6]							
	AUXROVTHSETREG[7:0]	AUXROVTHSET[5:0]						–	–
0x32	AUXRUVTHCLRREG[15:8]	AUXRUVTHCLR[13:6]							
	AUXRUVTHCLRREG[7:0]	AUXRUVTHCLR[5:0]						–	–
0x33	AUXRUVTHSETREG[15:8]	AUXRUVTHSET[13:6]							
	AUXRUVTHSETREG[7:0]	AUXRUVTHSET[5:0]						–	–
0x34	AUXAOVTHCLRREG[15:8]	AUXAOVTHCLR[13:6]							
	AUXAOVTHCLRREG[7:0]	AUXAOVTHCLR[5:0]						–	–
0x35	AUXAOVTHSETREG[15:8]	AUXAOVTHSET[13:6]							
	AUXAOVTHSETREG[7:0]	AUXAOVTHSET[5:0]						–	–
0x36	AUXAUVTHCLRREG[15:8]	AUXAUVTHCLR[13:6]							
	AUXAUVTHCLRREG[7:0]	AUXAUVTHCLR[5:0]						–	–
0x37	AUXAUVTHSETREG[15:8]	AUXAUVTHSET[13:6]							
	AUXAUVTHSETREG[7:0]	AUXAUVTHSET[5:0]						–	–
0x38	COMPOVTHREG[15:8]	COMPOVTH[11:4]							
	COMPOVTHREG[7:0]	COMPOVTH[3:0]				–	–	–	–
0x39	COMPUVTHREG[15:8]	COMPUVTH[11:4]							
	COMPUVTHREG[7:0]	COMPUVTH[3:0]				–	–	–	–
0x3A	COMPAUXROVTHREG[15:8]	COMPAUXROVTH[11:4]							
	COMPAUXROVTHREG[7:0]	COMPAUXROVTH[3:0]				–	–	–	–
0x3B	COMPAUXRUVTHREG[15:8]	COMPAUXRUVTH[11:4]							
	COMPAUXRUVTHREG[7:0]	COMPAUXRUVTH[3:0]				–	–	–	–
0x3C	COMPAUXAOVTHREG[15:8]	COMPAUXAOVTH[11:4]							
	COMPAUXAOVTHREG[7:0]	COMPAUXAOVTH[3:0]				–	–	–	–
0x3D	COMPAUXAUVTHREG[15:8]	COMPAUXAUVTH[11:4]							

ADDRESS	NAME	MSB							LSB
	COMPAUXAUVTHREG[7:0]	COMPAUXAUVTH[3:0]				–	–	–	–
DIAGNOSTIC THRESHOLD Registers									
0x3E	COMPOPNTHREG[15:8]	COMPOPNTH[11:4]							
	COMPOPNTHREG[7:0]	COMPOPNTH[3:0]				–	–	–	–
0x3F	COMPAUXROPNTHREG[15:8]	COMPAUXROPNTH[11:4]							
	COMPAUXROPNTHREG[7:0]	COMPAUXROPNTH[3:0]				–	–	–	–
0x40	COMPAUXAOPNTHREG[15:8]	COMPAUXAOPNTH[11:4]							
	COMPAUXAOPNTHREG[7:0]	COMPAUXAOPNTH[3:0]				–	–	–	–
0x41	COMPACCOVTHREG[15:8]	COMPACCOVTH[11:4]							
	COMPACCOVTHREG[7:0]	COMPACCOVTH[3:0]				–	–	–	–
0x42	COMPACCUVTHREG[15:8]	COMPACCUVTH[11:4]							
	COMPACCUVTHREG[7:0]	COMPACCUVTH[3:0]				–	–	–	–
0x43	BALSHRTTHRREG[15:8]	BALSHRTTHR[13:6]							
	BALSHRTTHRREG[7:0]	BALSHRTTHR[5:0]						–	–
0x44	BALLOWTHRREG[15:8]	BALLOWTHR[13:6]							
	BALLOWTHRREG[7:0]	BALLOWTHR[5:0]						–	–
0x45	BALHIGHTHRREG[15:8]	BALHIGHTHR[13:6]							
	BALHIGHTHRREG[7:0]	BALHIGHTHR[5:0]						–	–
CELL DATA Registers									
0x47	CELL1REG[15:8]	CELL1[13:6]							
	CELL1REG[7:0]	CELL1[5:0]						–	–
0x48	CELL2REG[15:8]	CELL2[13:6]							
	CELL2REG[7:0]	CELL2[5:0]						–	–
0x49	CELL3REG[15:8]	CELL3[13:6]							
	CELL3REG[7:0]	CELL3[5:0]						–	–
0x4A	CELL4REG[15:8]	CELL4[13:6]							
	CELL4REG[7:0]	CELL4[5:0]						–	–
0x4B	CELL5REG[15:8]	CELL5[13:6]							
	CELL5REG[7:0]	CELL5[5:0]						–	–
0x4C	CELL6REG[15:8]	CELL6[13:6]							
	CELL6REG[7:0]	CELL6[5:0]						–	–
0x4D	CELL7REG[15:8]	CELL7[13:6]							
	CELL7REG[7:0]	CELL7[5:0]						–	–

ADDRESS	NAME	MSB							LSB
0x4E	CELL8REG[15:8]	CELL8[13:6]							
	CELL8REG[7:0]	CELL8[5:0]						–	–
0x4F	CELL9REG[15:8]	CELL9[13:6]							
	CELL9REG[7:0]	CELL9[5:0]						–	–
0x50	CELL10REG[15:8]	CELL10[13:6]							
	CELL10REG[7:0]	CELL10[5:0]						–	–
0x51	CELL11REG[15:8]	CELL11[13:6]							
	CELL11REG[7:0]	CELL11[5:0]						–	–
0x52	CELL12REG[15:8]	CELL12[13:6]							
	CELL12REG[7:0]	CELL12[5:0]						–	–
0x53	CELL13REG[15:8]	CELL13[13:6]							
	CELL13REG[7:0]	CELL13[5:0]						–	–
0x54	CELL14REG[15:8]	CELL14[13:6]							
	CELL14REG[7:0]	CELL14[5:0]						–	–
0x55	BLOCKREG[15:8]	VBLOCK[13:6]							
	BLOCKREG[7:0]	VBLOCK[5:0]						–	–
TOTAL DIAG AUX DATA Registers									
0x56	TOTALREG[15:8]	TOTAL[15:8]							
	TOTALREG[7:0]	TOTAL[7:0]							
0x57	DIAG1REG[15:8]	DIAG1[13:6]							
	DIAG1REG[7:0]	DIAG1[5:0]						–	–
0x58	DIAG2REG[15:8]	DIAG2[13:6]							
	DIAG2REG[7:0]	DIAG2[5:0]						–	–
0x59	AUX0REG[15:8]	AUX0[13:6]							
	AUX0REG[7:0]	AUX0[5:0]						–	–
0x5A	AUX1REG[15:8]	AUX1[13:6]							
	AUX1REG[7:0]	AUX1[5:0]						–	–
0x5B	AUX2REG[15:8]	AUX2[13:6]							
	AUX2REG[7:0]	AUX2[5:0]						–	–
0x5C	AUX3REG[15:8]	AUX3[13:6]							
	AUX3REG[7:0]	AUX3[5:0]						–	–
0x5D	AUX4REG[15:8]	AUX4[13:6]							
	AUX4REG[7:0]	AUX4[5:0]						–	–
0x5E	AUX5REG[15:8]	AUX5[13:6]							
	AUX5REG[7:0]	AUX5[5:0]						–	–
SCAN SETTINGS Registers									
0x5F	POLARITYCTRL[15:8]	MINMAX POL	–	POLARITY[14:9]					
	POLARITYCTRL[7:0]	POLARITY[8:1]							
0x60	AUXREFCTRL[15:8]	–	–	–	–	–	–	–	–
	AUXREFCTRL[7:0]	–	–	AUXREFSEL[5:4]		AUXREFSEL[3:0]			
0x61	AUXTIMEREG[15:8]	–	–	–	–	–	–	AUXTIME[9:8]	
	AUXTIMEREG[7:0]	AUXTIME[7:0]							

ADDRESS	NAME	MSB							LSB
0x62	ACQCFG[15:8]	ADCZSFSEN	ADCCALEN	COMPACCEN	FOSR[1:0]		THRMMODE[1:0]		–
	ACQCFG[7:0]	–	–	–	–	–	–	–	–
0x63	BALSWDLY[15:8]	CELLDLY[7:0]							
	BALSWDLY[7:0]	SWDLY[7:0]							
SCAN CONTROL Registers									
0x64	MEASUREEN1[15:8]	–	BLOCKEN	CELLEN[14:9]					
	MEASUREEN1[7:0]	CELLEN[8:1]							
0x65	MEASUREEN2[15:8]	SCANIIRINIT	–	–	–	–	–	–	–
	MEASUREEN2[7:0]	–	–	AUXEN[5:4]		AUXEN[3:0]			
0x66	SCANCTRL[15:8]	SCANDONE	SCANTIMEOUT	DATARDY	AUTOBALSWDIS	ALRTFILTSEL	AMENDFILT	RDFILT	SCANCFG[2]
	SCANCTRL[7:0]	SCANCFG[1:0]		OVSAMPL[2:0]			ALTMUXSEL	SCANMODE	SCAN
DIAGNOSTIC SETTINGS Registers									
0x67	ADCTEST1AREG[15:8]	ADCTSTEN	–	–	–	ADCTEST1A[11:8]			
	ADCTEST1AREG[7:0]	ADCTEST1A[7:0]							
0x68	ADCTEST1BREG[15:8]	–	–	–	–	ADCTEST1B[11:8]			
	ADCTEST1BREG[7:0]	ADCTEST1B[7:0]							
0x69	ADCTEST2AREG[15:8]	–	–	–	–	ADCTEST2A[11:8]			
	ADCTEST2AREG[7:0]	ADCTEST2A[7:0]							
0x6A	ADCTEST2BREG[15:8]	–	–	–	–	ADCTEST2B[11:8]			
	ADCTEST2BREG[7:0]	ADCTEST2B[7:0]							
DIAGNOSTIC CONTROL Registers									
0x6B	DIAGCFG[15:8]	CTSTDAC[3:0]				CTSTSRC	MUXDIAGBUS	MUXDIAGPAIR	MUXDIAGEN
	DIAGCFG[7:0]	DIAGSEL2[3:0]				DIAGSEL1[3:0]			
0x6C	CTSTCFG[15:8]	CELLOPNDIAGSEL	CTSTEN[14:8]						
	CTSTCFG[7:0]	CTSTEN[7:0]							
0x6D	AUXTSTCFG[15:8]	–	–	–	–	–	–	–	–
	AUXTSTCFG[7:0]	–	–	AUXTSTEN[5:4]		AUXTSTEN[3:0]			
0x6E	DIAGGENCFG[15:8]	AUXDIAGSEL[2:0]			–	–	–	–	–
	DIAGGENCFG[7:0]	–	–	–	–	–	–	–	–
CELL BALANCING Registers									
0x6F	BALSWCTRL[15:8]	CBRESTART	–	BALSWEN[14:9]					
	BALSWCTRL[7:0]	BALSWEN[8:1]							
0x70	BALEXP1[15:8]	–	–	–	–	–	–	CBEXP1[9:8]	
	BALEXP1[7:0]	CBEXP1[7:0]							
0x71	BALEXP2[15:8]	–	–	–	–	–	–	CBEXP2[9:8]	

ADDRESS	NAME	MSB							LSB
	BALEXP2[7:0]	CBEXP2[7:0]							
0x72	BALEXP3[15:8]	–	–	–	–	–	–	CBEXP3[9:8]	
	BALEXP3[7:0]	CBEXP3[7:0]							
0x73	BALEXP4[15:8]	–	–	–	–	–	–	CBEXP4[9:8]	
	BALEXP4[7:0]	CBEXP4[7:0]							
0x74	BALEXP5[15:8]	–	–	–	–	–	–	CBEXP5[9:8]	
	BALEXP5[7:0]	CBEXP5[7:0]							
0x75	BALEXP6[15:8]	–	–	–	–	–	–	CBEXP6[9:8]	
	BALEXP6[7:0]	CBEXP6[7:0]							
0x76	BALEXP7[15:8]	–	–	–	–	–	–	CBEXP7[9:8]	
	BALEXP7[7:0]	CBEXP7[7:0]							
0x77	BALEXP8[15:8]	–	–	–	–	–	–	CBEXP8[9:8]	
	BALEXP8[7:0]	CBEXP8[7:0]							
0x78	BALEXP9[15:8]	–	–	–	–	–	–	CBEXP9[9:8]	
	BALEXP9[7:0]	CBEXP9[7:0]							
0x79	BALEXP10[15:8]	–	–	–	–	–	–	CBEXP10[9:8]	
	BALEXP10[7:0]	CBEXP10[7:0]							
0x7A	BALEXP11[15:8]	–	–	–	–	–	–	CBEXP11[9:8]	
	BALEXP11[7:0]	CBEXP11[7:0]							
0x7B	BALEXP12[15:8]	–	–	–	–	–	–	CBEXP12[9:8]	
	BALEXP12[7:0]	CBEXP12[7:0]							
0x7C	BALEXP13[15:8]	–	–	–	–	–	–	CBEXP13[9:8]	
	BALEXP13[7:0]	CBEXP13[7:0]							
0x7D	BALEXP14[15:8]	–	–	–	–	–	–	CBEXP14[9:8]	
	BALEXP14[7:0]	CBEXP14[7:0]							
0x7E	BALAUTOUVTHR[15:8]	CBUVTHR[13:6]							
	BALAUTOUVTHR[7:0]	CBUVTHR[5:0]						–	CBUVMINCELL
0x7F	BALDLYCTRL[15:8]	–	–	–	–	–	–	CBNTFYCFG[1:0]	
	BALDLYCTRL[7:0]	–	–	–	–	–	CBCALDLY[2:0]		
0x80	BALCTRL[15:8]	CBACTIVE[1:0]		CBMODE[2:0]			CBIIRINIT	HOLDSHDNL[1:0]	
	BALCTRL[7:0]	CBDUTY[3:0]				CBDONEALRTEN	CBTEMPEN	CBMEASEN[1:0]	
0x81	BALSTAT[15:8]	CBACTIVE_M1[1:0]		CBUNIT[1:0]		CBCNTR[1:0]		CBTIMER[9:8]	
	BALSTAT[7:0]	CBTIMER[7:0]							
0x82	BALUVSTAT[15:8]	CBACTIVE_M2[1:0]		CBUVSTAT[14:9]					
	BALUVSTAT[7:0]	CBUVSTAT[8:1]							
0x83	BALDATA[15:8]	CBACTIVE_M3[1:0]		DATARDY_M	–	–	–	–	–
	BALDATA[7:0]	–	–	–	–	–	–	–	CBSCAN
I2C MASTER Registers									
0x84	I2CPNTR[15:8]	I2CPBYTE1[7:0]							

ADDRESS	NAME	MSB							LSB
	I2CPNTR[7:0]	I2CPBYTE0[7:0]							
0x85	I2CWDATA1[15:8]	I2CWBYTE3[7:0]							
	I2CWDATA1[7:0]	I2CWBYTE2[7:0]							
0x86	I2CWDATA2[15:8]	I2CWBYTE1[7:0]							
	I2CWDATA2[7:0]	I2CWBYTE0[7:0]							
0x87	I2CRDATA1[15:8]	I2CRBYTE3[7:0]							
	I2CRDATA1[7:0]	I2CRBYTE2[7:0]							
0x88	I2CRDATA2[15:8]	I2CRBYTE1[7:0]							
	I2CRDATA2[7:0]	I2CRBYTE0[7:0]							
0x89	I2CCFG[15:8]	I2CFSCL	I2CWALT	I2CRFMT	I2C10BIT	I2CPNTRLNGTH	I2CALRTEN	–	–
	I2CCFG[7:0]	–	–	I2CANACONTEN	I2CCONTEN	I2CGLITCHEN	I2CNOISEEN	I2CRDTREN	I2CTOEN
0x8A	I2CSTAT[15:8]	I2CSTATUS[1:0]		–	–	–	–	–	I2CRJCT
	I2CSTAT[7:0]	I2CDEVNACK	I2CDATANACK	I2CANACONT	I2CCONT	I2CGLITCH	I2CNOISE	I2CRDTRERR	I2CTIMEOUT
0x8B	I2CSEND[15:8]	I2CPNTRSEL	I2CDATALNGTH[1:0]		I2CDATASEL[1:0]		I2CDEVIDEXT[2:0]		
	I2CSEND[7:0]	I2CDEVID[6:0]							I2CRWB
ROM SUPPORT Registers									
0x8C	ID1[15:8]	DEVID[15:8]							
	ID1[7:0]	DEVID[7:0]							
0x8D	ID2[15:8]	DEVID[31:24]							
	ID2[7:0]	DEVID[23:16]							
0x8E	ID3[15:8]	OTP2[7:0]							
	ID3[7:0]	DEVID[39:32]							
0x8F	OTP3REG[15:8]	OTP3[15:8]							
	OTP3REG[7:0]	OTP3[7:0]							
0x90	OTP4REG[15:8]	OTP4[1:0]		ALTREF_OTP[13:8]					
	OTP4REG[7:0]	ALTREF_OTP[7:0]							
0x91	OTP5REG[15:8]	OTP5[15:8]							
	OTP5REG[7:0]	OTP5[7:0]							
0x92	OTP6REG[15:8]	OTP6[15:8]							
	OTP6REG[7:0]	OTP6[7:0]							
0x93	OTP7REG[15:8]	OTP7[15:8]							
	OTP7REG[7:0]	OTP7[7:0]							
0x94	OTP8REG[15:8]	OTP8[15:8]							
	OTP8REG[7:0]	OTP8[7:0]							
0x95	OTP9REG[15:8]	OTP9[15:8]							
	OTP9REG[7:0]	OTP9[7:0]							
0x96	OTP10REG[15:8]	OTP10[15:8]							
	OTP10REG[7:0]	OTP10[7:0]							
0x97	OTP11REG[15:8]	OTP11[15:8]							

ADDRESS	NAME	MSB							LSB
	OTP11REG[7:0]	OTP11[7:0]							
0x98	OTP12REG[15:8]	ROMCRC[7:0]							
	OTP12REG[7:0]	OTP12[7:0]							

Register Details

VERSION (0x00)

VERSION is a read-only accessible register that returns information on the device.

BIT	15	14	13	12	11	10	9	8
Field	MOD[11:4]							
Reset								
Access Type	Read Only							

BIT	7	6	5	4	3	2	1	0
Field	MOD[3:0]				VER[3:0]			
Reset					0x4			
Access Type	Read Only				Read Only			

BITFIELD	BITS	DESCRIPTION
MOD	15:4	Device Model Number 0x854 = MAX17854 Read only.
VER	3:0	Si Version Current Version = 0x4 Read only.

ADDRESS (0x01)

ADDRESS is a read- and write-accessible register that sets the first, last, and device address used by a device in a UART chain .

BIT	15	14	13	12	11	10	9	8
Field	ADDRUNLOCK	BA[4:0]					TA[4:3]	
Reset	0b1	0b0_0000					0b0_0000	
Access Type	Write, Read, Ext	Write, Read, Ext					Write, Read, Ext	

BIT	7	6	5	4	3	2	1	0
Field	TA[2:0]			DA[4:0]				
Reset	0b0_0000			0b0_0000				
Access Type	Write, Read, Ext			Write, Read, Ext				

BITFIELD	BITS	DESCRIPTION
ADDRUNLOCK	15	UART Device Address Unlock 0 = Normal Operation (following HELLOALL) 1 = Disable write-protection of device address DA[4:0], allowing re-sends of HELLOALL to reassign device addresses without POR (also POR default). Cleared only by HELLOALL command (writes to 0 are ignored). This bitfield is unaffected in the event of a SWPOR (software POR) request by the host. ***Note:*** *This bit should normally be written to 0 when populating BA and TA content; it should only be necessary to set this bit if the user believes the original DA content populated by the HELLOALL command is corrupted.*
BA	14:10	Bottom Device Address in a UART Chain Address of the device at the bottom of the daisy-chain. If the host sends an initial address other than 0x00 in the HELLOALL command through the UART Up Path (assign/increment), then the host must write that bottom address (as well as the expected top address) to all devices in the daisy-chain with a WRITEALL command to this bitfield. READALL commands and Alert Packets require that BA[4:0], TA[4:0], and DA[4:0] be correct in order for the data-check and PEC features to function as intended. This bitfield is unaffected in the event of a SWPOR (software POR) request by the host.
TA	9:5	Top Device Address in a UART Chain Address of the device connected to the top of the daisy-chain. If the host sends an initial address in the HELLOALL command through the UART Down Path (assign/decrement), then the host must write that top address (as well as the expected bottom address) to all devices in the daisy-chain with a WRITEALL command to this bitfield. READALL commands and Alert Packets require that BA[4:0], TA[4:0], and DA[4:0] be correct in order for the data-check and PEC features to function as intended. This bitfield is unaffected in the event of a SWPOR (software POR) request by the host.

BITFIELD	BITS	DESCRIPTION
DA	4:0	Device Address Device address written only by the HELLOALL command as it propagates through the daisy-chain. If HELLOALL is issued through the UART Up Path, this bitfield is accepted and then automatically incremented by each device. If HELLOALL is issued through the UART Down Path, this bitfield is accepted and then automatically decremented by each device. The host must choose an initial (bottom) address 0x00 or greater and ensure the resulting top address will not exceed the maximum address of 0x1F during the propagation of the HELLOALL command through the Up Path. Likewise, the host must choose an initial (top) address 0x1F or lower and ensure that the resulting bottom address will be 0x00 or greater after propagation of the HELLOALL command through the Down Path. Writing has no effect; only a HELLOALL command executed while ADDRUNLOCK = 1 will update this content. This bitfield is unaffected in the event of a SWPOR (software POR) request by the host.

STATUS1 (0x02)

STATUS1 is a read- and write-accessible register that relates the current status of the device. STATUS1 also contains summary information on STATUS2, STATUS3, and FMEA registers, and other selected registers indicating if additional readback checks are required.

BIT	15	14	13	12	11	10	9	8
Field	ALRTSCAN	ALRTRST	ALRTMSMTCH	ALRTCELLOVST	ALRTCELLUVST	ALRTBLKOVST	ALRTBLKUVST	ALRTAUXOVST
Reset	0b0	0b1	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Only	Write 0 to Clear, Read	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BIT	7	6	5	4	3	2	1	0
Field	ALRTAUXUVST	–	ALRTPEC	ALRTINTRFC	ALRTCAL	ALRTCBAL	ALRTFMEA2	ALRTFMEA1
Reset	0b0	–	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Only	–	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION
ALRTSCAN	15	Scan Done Alert 0 = No Measurement Requested or Measurement in Progress (default) 1 = Measurement Complete Cleared if SCANCRTL:SCANDONE is removed. Read only.

BITFIELD	BITS	DESCRIPTION
ALRTRST	14	Reset Alert Indicates a power-on-reset event occurred. UART users should clear this alert after power-on and after a successful HELLOALL transaction in order to detect future resets. Cleared only by writing to logic 0. Writing to a logic 1 has no effect.
ALRTMSMTCH	13	Cell Voltage Mismatch Alert Indicates V_{MAX} - V_{MIN} > V_{MSMTCH} threshold. Read MINMAXCELL for detailed information on which channels are involved to aide diagnosis. Cleared at next acquisition if the condition is false. Read only.
ALRTCELLOVST	12	Cell Overvoltage Status Summary Alert Bitwise logical OR of ALRTOV[14:1] and ALRTCOMPOV[14:1]. Read ALRTSUM for information on whether the ADC, comparator, or both circuits detected the fault to aide diagnosis. Cleared on next acquisition, if all enabled overvoltage conditions are resolved. Read only.
ALRTCELLUVST	11	Cell Undervoltage Status Summary Alert Bitwise logical OR of ALRTUV[14:1] and ALRTCOMPUV[14:1]. Read ALRTSUM for information on whether the ADC, comparator, or both circuits detected the fault to aide diagnosis. Cleared on next acquisition, if all enabled undervoltage conditions are resolved. Read only.
ALRTBLKOVST	10	Block Overvoltage Status Alert Indicates the latest block voltage measurement exceeded the threshold set by BLKOVTHSET. Cleared on next block voltage acquisition, if condition is resolved. Read only.
ALRTBLKUVST	9	Block Undervoltage Status Alert Indicates the latest block voltage measurement was below the threshold set by BLKUVTHSET. Cleared on next block voltage acquisition, if condition is resolved. Read only.

BITFIELD	BITS	DESCRIPTION
ALRTAUXOVST	8	Auxiliary Overvoltage (Cold) Status Summary Alert Logical OR of ALRTAUXOV[5:0] and ALRTCOMPAUXOV[5:0] auxiliary alerts. Read ALRTSUM for information on whether the ADC, comparator, or both circuits detected the fault to aide diagnosis. Cleared on next acquisition, if all enabled overvoltage conditions are resolved. Read only.
ALRTAUXUVST	7	Auxiliary Undervoltage (Hot) Status Summary Alert Logical OR of ALRTAUXUV[5:0] and ALRTCOMPAUXUV[5:0] auxiliary alerts. Read ALRTSUM for information on whether the ADC, comparator, or both circuits detected the fault to aide diagnosis. Cleared on next acquisition, if all enabled undervoltage conditions are resolved. Read only.
ALRTPEC	5	PEC (CRC) Alert Indicates a received UART character/transaction contained a PEC/CRC error and was ignored as a result. Logical OR of (ALRTPECUP, ALRTPECDN). Cleared if component alerts are resolved in STATUS2:ALRTPECUP/DN, see component bitfield descriptions for details. Read only.
ALRTINTRFC	4	Interface Specific Error Alert Indicates that an error specific to the selected interface: UART user interface and/or I^2C master interface (if enabled) has occurred. Bitwise OR of (ALRTMANUP/DN, ALRTPARUP/DN, ALRTDUALART, ALRTRJCT, ALRTI2C). ALRTPEC holds a dedicated position in the STATUS register (assertion of ALRTPEC will not assert ALRTINTRFC). If this alert bit is set, the specific error(s) can be read and cleared using the STATUS2 register.
ALRTCAL	3	Calibration Fault Alert Logical OR of all calibration alerts (ALRTCALOSADC, ALRTCALOSR, ALERTCALOSTHRM, ALRTCALGAINP, ALRTCALGAINR). Cleared if component alerts are resolved in ALRTSUM; see ALRTSUM and ALRTIRQEN for details. Read only. If a calibration error occurs during an Automated Cell-Balancing or Discharge operation, the operation will end and issue CBACTIVE = 11 and ALRTCBCAL, notifying the user of the termination.

BITFIELD	BITS	DESCRIPTION
ALRTCBAL	2	Cell-Balancing Status Alert 0 = Cell-Balancing Inactive/Normal 1 = Cell-Balancing Complete/Fault Logical OR of all enabled/unmasked cell-balancing alerts (ALRTCBTIMEOUT, ALRTCBTEMP, ALRTCBCAL, ALRTCBNTFY, ALRTCBDONE). Cleared if component alerts are resolved in STATUS3; see STATUS3 and ALRTIRQEN for details. Read only.
ALRTFMEA2	1	FMEA2 Condition Summary Alert Bitwise logical OR of FMEA2[15:0]. Read only.
ALRTFMEA1	0	FMEA1 Condition Summary Alert Bitwise logical OR of FMEA1[15:0]. Read only.

STATUS2 (0x03)

STATUS2 is a read- and write-accessible register that contains summary information on alerts related to interface and communication faults.

BIT	15	14	13	12	11	10	9	8
Field	ALRTPECUP	ALRTPECDN	ALRTMANUP	ALRTMANDN	ALRTPARUP	ALRTPARDN	ALRTDUALUART	–
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	–
Access Type	Write 0 to Clear, Read	Write 0 to Clear, Read	Write 0 to Clear, Read	Write 0 to Clear, Read	Write 0 to Clear, Read	Write 0 to Clear, Read	Write 0 to Clear, Read	–

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	ALRTI2C	–	ALRTRJCT
Reset	–	–	–	–	–	0b0	–	0b0
Access Type	–	–	–	–	–	Read Only	–	Write 0 to Clear, Read

BITFIELD	BITS	DESCRIPTION
ALRTPECUP	15	UART Up Interface Packet Error Check Alert Indicates a character/transaction recieved by the UART Up Interface contained a PEC error and was ignored as a result. Cleared only by writing to logic 0. Writing to a logic 1 has no effect.
ALRTPECDN	14	UART Down Interface Packet Error Check Alert Indicates a character/transaction recieved by the UART Down Interface contained a PEC error and was ignored as a result. Cleared only by writing to logic 0. Writing to a logic 1 has no effect. Applies only to parts operating using the dual-UART interface (UARTCFG = 11).

BITFIELD	BITS	DESCRIPTION
ALRTMANUP	13	UART Up Interface Manchester-Encoding Error Indicates that a character received by the UART Up Interface (through RXL) contained a Manchester error. Cleared only by writing to logic 0. Writing to a logic 1 has no effect.
ALRTMANDN	12	UART Down Interface Manchester-Encoding Error Indicates that a character received by the UART Down Interface (through RXU) contained a Manchester error. Cleared only by writing to logic 0. Writing to a logic 1 has no effect. Applies only to parts operating using the dual-UART interface (UARTCFG = 11).
ALRTPARUP	11	UART Up Interface Parity Error Indicates that a character received by the UART Up Interface (through RXL) contained a parity error. Cleared only by writing to logic 0. Writing to a logic 1 has no effect.
ALRTPARDN	10	UART Down Interface Parity Error Indicates that a character received by the UART Down Interface (through RXU) contained a parity error. Cleared only by writing to logic 0. Writing to a logic 1 has no effect. Applies only to parts operating using the dual-UART interface (UARTCFG = 11).
ALRTDUALUART	9	Dual-UART Fault Alert 0 = No Dual-UART Fault Detected 1 = Invalid Dual-UART Command Received ALRTDUALUART indicates one or more of the following conditions occurred: A WRITEDEVICE or WRITEALL command sent through a path not configured as host was ignored (only the host path accepts writes). An UPHOST command was issued and ignored on the downstream UART path. An DOWNHOST command was issued and ignored on the upstream UART path. These conditions are checked only when UARTCFG = DUAL (11). Cleared only by writing to logic 0. Writing to a logic 1 has no effect.

BITFIELD	BITS	DESCRIPTION
ALRTI2C	2	I^2C Master Fault Alert Logical OR of I2CSTAT[8:0] error indicator bits, subject to masking by I2CCFG:I2CALRTEN. Cleared only when unmasked component alerts are resolved in the I2CSTAT register. Read only.
ALRTRJCT	0	Protected Command Rejection Alert 0 = Normal Operation 1 = Invalid Command Rejected during an active scan or cell-balancing operation ALRTRJCT is issued when an invalid write to a protected register is received during an active/gating scan or cell-balancing operation. The invalid command will be ignored. Cleared only by writing to logic 0. Writing to a logic 1 has no effect.

STATUS3 (0x04)

STATUS3 is a read- and write-accessible register that contains summary information on alerts related to automated cell-balancing operations.

BIT	15	14	13	12	11	10	9	8
Field	ALRTCBTIMEOUT	ALRTCBTEMP	ALRTCBCAL	ALRTCBNTFY	ALRTCBDONE	–	–	–
Reset	0b0	0b0	0b0		0b0	–	–	–
Access Type	Write 0 to Clear, Read	Write 0 to Clear, Read	Write 0 to Clear, Read	Write 0 to Clear, Read	Write 0 to Clear, Read	–	–	–

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION
ALRTCBTIMEOUT	15	Cell-Balancing Timeout Alert 0 = Cell-Balancing Disabled or in Progress 1 = Cell-Balancing Operation Halted due to Timeout Fault ALRTCBTIMEOUT is issued when a discharge or automated cell-balancing operation is halted due to an internal logic fault condition triggering the watchdog timer. This alert is automatically enabled if CBTODIS = 0. Cleared only by writing to logic 0. Writing to a logic 1 has no effect.

BITFIELD	BITS	DESCRIPTION
ALRTCBTEMP	14	Cell-Balancing Thermal Alert 0 = Cell-Balancing Disabled or in Progress 1 = Cell-Balancing Operation Halted due to Thermal Fault ALRTCBTEMP is issued when a manual, discharge, or automated cell-balancing operation is halted due to a thermal fault condition. This alert is automatically enabled if CBTEMPEN = 1. Cleared only by writing to logic 0 after the automated cell-balancing operation which generated the alert has been completed or otherwise ended. Writing to a logic 1 has no effect.
ALRTCBCAL	13	Cell-Balancing Calibration Alert 0 = Cell-Balancing Disabled or in Progress 1 = Cell-Balancing Operation Halted due to Calibration Fault ALRTCBCAL is issued when a discharge, or automated cell-balancing operation is halted due to an embedded calibration fault condition. Cleared only by writing to logic 0 after the automated cell-balancing operation which generated the alert has been completed or otherwise ended. Writing to a logic 1 has no effect.
ALRTCBNTFY	12	Cell-Balancing Notification Alert 0 = No Cell-Balancing Progression Notification Present 1 = Cell-Balancing Progression Notification ALRTCBNTFY is periodically issued during discharge and automated cell-balancing operations to confirm normal progression of the operation. This alert is enabled and configured by CBNTFYCFG. Cleared only by writing to logic 0. Writing to a logic 1 has no effect.
ALRTCBDONE	11	Cell-Balancing Complete Alert 0 = Cell-Balancing Disabled or in Progress 1 = Cell-Balancing Operation Complete ALRTCBDONE is issued when a manual, discharge, or automated cell-balancing operation completes due to a normal timed or undervoltage exit condition. Cleared only by writing to logic 0. Writing to a logic 1 has no effect.

FMEA1 (0x05)

FMEA1 is a read- and write-accessible register that relates current information on possible fault conditions.

BIT	15	14	13	12	11	10	9	8
Field	ALRTOSC1	ALRTOSC2	ALRTCOMMSEU1	ALRTCOMMSEL1	ALRTCOMMSEU2	ALRTCOMMSEL2	ALRTVDDL3	ALRTVDDL2
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write 0 to Clear, Read	Write 0 to Clear, Read	Read Only	Read Only	Read Only	Read Only	Write 0 to Clear, Read	Write 0 to Clear, Read

BIT	7	6	5	4	3	2	1	0
Field	ALRTVDDL1	ALRTGNDL3	ALRTGNDL2	ALRTGNDL1	ALRTHVUV	ALRTHVHDRM	ALRTHVOV	ALRTBALSWSUM
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write 0 to Clear, Read	Write 0 to Clear, Read	Write 0 to Clear, Read	Write 0 to Clear, Read	Write 0 to Clear, Read	Write 0 to Clear, Read	Write 0 to Clear, Read	Write, Read, Ext

BITFIELD	BITS	DESCRIPTION
ALRTOSC1	15	LFOSC Fault Alert Indicates that the LFOSC frequency is not within ±5% of its expected value when measured against the HFOSC oscillator. The status is updated every two cycles (LFOSC). Cleared only by writing to logic 0 if the condition has been resolved. Writing to a logic 1 has no effect.
ALRTOSC2	14	32kHz Oscillator Fault Alert (Redundant) Identical to ALRTOSC1 - redundant alert with independent latch. Cleared only by writing to logic 0 if the condition has been resolved. Writing to a logic 1 has no effect.
ALRTCOMMSEU1	13	UART Upper Port Single-Ended Alert Indicates that the UART has placed the upper port receiver in single-ended mode based on the first preamble received after POR. This bit is not set until the ALRTRST bit is cleared. Read only.
ALRTCOMMSEL1	12	UART Lower Port Single-Ended Alert Indicates that the UART has placed the lower port receiver in single-ended mode based on the first preamble received after POR. This bit is not set until the ALRTRST bit is cleared. Read only.
ALRTCOMMSEU2	11	UART Upper Port Single-Ended Redundant Alert Same as ALRTCOMMSEU1 (redundant alert) except that it sets before ALRTRST is cleared. Read only.
ALRTCOMMSEL2	10	UART Lower Port Single-Ended Redundant Alert Same as ALRTCOMMSEL1 (redundant alert) except that it sets before ALRTRST is cleared. Read only.
ALRTVDDL3	9	V_{DDL3} Fault Alert Indicates $V_{DDL3} < V_{VDDL2/3\_OC}$. This bit is not set until the ALRTRST bit is cleared. Cleared only by writing to logic 0 if condition is resolved. Writing to a logic 1 has no effect.
ALRTVDDL2	8	V_{DDL2} Fault Alert Indicates $V_{DDL2} < V_{VDDL2/3\_OC}$. This bit is not set until the ALRTRST bit is cleared. Cleared only by writing to logic 0 if condition is resolved. Writing to a logic 1 has no effect.
ALRTVDDL1	7	V_{DDL1} Fault Alert Indicates $V_{DDL1} < V_{VDDL1\_OC}$. This bit is not set until the ALRTRST bit is cleared. Cleared only by writing to logic 0 if condition is resolved. Writing to a logic 1 has no effect.

BITFIELD	BITS	DESCRIPTION
ALRTGNDL3	6	GNDL3 Fault Alert Indicates an open circuit on the GNDL3 pin. This bit is not set until the ALRTRST bit is cleared. Cleared only by writing to logic 0. Writing to a logic 1 has no effect.
ALRTGNDL2	5	GNDL2 Fault Alert Indicates an open circuit on the GNDL2 pin. This bit is not set until the ALRTRST bit is cleared. Cleared only by writing to logic 0. Writing to a logic 1 has no effect.
ALRTGNDL1	4	GNDL1 Fault Alert Indicates an open circuit on the GNDL1 pin. This bit is not set until the ALRTRST bit is cleared. Cleared only by writing to logic 0. Writing to a logic 1 has no effect.
ALRTHVUV	3	HV Undervoltage Fault Alert Indicates $V_{HV} < V_{HVUV}$. This bit is not set until the ALRTRST bit is cleared. Cleared only by writing to logic 0. Writing to a logic 1 has no effect.
ALRTHVHDRM	2	HV Headroom Fault Alert Indicates that $V_{HV} - V_{TOPCELL1/2}$ was too low during the acquisition for an accurate measurement. Checked only during measurement activity. Cleared only by writing to logic 0. Writing to a logic 1 has no effect.
ALRTHVOV	1	HV Overvoltage Fault Alert Indicates that $V_{HV} - V_{DCIN} > V_{HVOV}$. This bit is not set until the ALRTRST bit is cleared. Cleared only by writing to logic 0. Writing to a logic 1 has no effect.
ALRTBALSWSUM	0	Balance Switch Fault Alert Summary Bitwise logical OR of ALRTBALSW[13:0]. Updated at the end of a BALSWDIAG scan. Cleared if all enabled ALRTBALSW alerts are resolved or by writing to logic 0. Writing to a logic 1 has no effect.

FMEA2 (0x06)

FMEA1 is a read- and write-accessible register that relates current information on possible fault conditions.

BIT	15	14	13	12	11	10	9	8
Field	ALRTUSER	ALRTDCINMUX	ALRTAUXPRTCTSUM	ALRTTEMP	ALRTSCANTIMEOUT	–	–	–
Reset	0b0	0b0	0b0	0b0	0b0	–	–	–
Access Type	Write, Read	Write 0 to Clear, Read	Read Only	Write 0 to Clear, Read	Read Only	–	–	–

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	ALRTADCZS	ALRTADCFS	ALRTCOMPACCOV	ALRTCOMPACCUV
Reset	–	–	–	–	0b0	0b0	0b0	0b0
Access Type	–	–	–	–	Write 0 to Clear, Read	Write 0 to Clear, Read	Write 0 to Clear, Read	Write 0 to Clear, Read

BITFIELD	BITS	DESCRIPTION
ALRTUSER	15	User-Defined Alert (Diagnostic) Used to test the Alert Interface. Asserted by writing to logic 1. The resulting alert will be relayed through the Alert Interface/UART DCByte and can be read back using the FMEA2 command. Cleared by writing to logic 0 (default).
ALRTDCINMUX	14	DCIN MUX Fault Alert 0 = No DCINMUX Fault Detected (default) 1 = DCINMUX Fault Detected A high condition indicates the enabled DCINMUX is not functioning properly in a flexible-pack application. Connections will be made by diodes, and performance may be impacted, and/or other related faults may be issued. This alert is enabled if the DCINMUX is enabled (FLXPACKEN = 1) after STATUS1:ALRTRST has been cleared. The PACKCFG register makes selections on which SW[n] input is used for DCIN supply and which C[n] is used for V_{BLK} measurements in flexible-pack applications. Cleared only by writing to logic 0 if condition has been resolved. Writing to a logic 1 has no effect.
ALRTAUXPRTCTSUM	13	Auxiliary Protection Fault Alert Summary Logical OR of all enabled ALRTAUXPRTCT bits, indicating one or more AUXINn inputs is in a fault mode with input protection engaged. These alerts are enabled for all AUX/GPIO pins currently configured as AUXINn inputs. This bit will only be cleared when the ALRTAUXPRTCT register is cleared; see the ALRTAUXPRTCT register for specific details. Read only.
ALRTTEMP	12	Die Overtemperature Fault Alert Indicates that T_{DIE} > +115°C (+120°C, typ). Cleared only by writing to logic 0. Writing to a logic 1 has no effect. If a thermal alert occurs during an automated cell-balancing or discharge operation, the operation will end and issue CBACTIVE = 11 and ALRTCBTEMP, notifying the user of the termination.
ALRTSCANTIMEOUT	11	Scan Timeout Alert 0 = Scan Not Requested or Progressing Normally (default) 1 = Scan Operation Halted due to Timeout Fault ALRTSCANTIMEOUT is a copy of SCANTIMEOUT. This alert is automatically enabled if SCANTODIS = 0. Cleared only by writing SCANCTRL:SCANTIMEOUT to 0. Read only.

BITFIELD	BITS	DESCRIPTION
ALRTADCZS	3	ADC Zero-Scale BIST Alert 0 = ADC Zero-Scale BIST Passed 1 = ADC Zero-Scale BIST Failed Reports the result of the ADC zero-scale BIST measurement performed during the last acquisition. Tests the SAR ADC DAC, comparator, and logic components. Enabled using ADCZSFSEN. Cleared only by writing to logic 0. Writing to a logic 1 has no effect. ***Note:*** *If detailed results are desired, use the Zero-Scale ADC Detailed Diagnostic.*
ALRTADCFS	2	ADC Full-Scale BIST Alert 0 = ADC Full-Scale BIST Passed 1 = ADC Full-Scale BIST Failed Reports the result of the ADC full-scale BIST measurement performed during the last acquisition. Tests the SAR ADC DAC, comparator, and logic components. Enabled using ADCZSFSEN. Cleared only by writing to logic 0. Writing to a logic 1 has no effect. ***Note:*** *If detailed results are desired, use the Full-Scale ADC Diagnostic.*
ALRTCOMPACCOV	1	End-of-Sequence Comparator Accuracy Diagnostic Overvoltage Alert 0 = COMP Accuracy OV Test Passed 1 = COMP Accuracy OV Test Failed Result of the end-of-sequence comparator accuracy overvoltage diagnostic, if enabled (SCANCFG = 001 or 010, and COMPACCEN = 1). Cleared only by writing to logic 0. Writing to a logic 1 has no effect.
ALRTCOMPACCUV	0	End-of-Sequence Comparator Accuracy Diagnostic Undervoltage Alert 0 = COMP Accuracy UV Test Passed 1 = COMP Accuracy UV Test Failed Result of the end-of-sequence comparator accuracy undervoltage diagnostic if enabled (SCANCFG = 001 or 010, and COMPACCEN = 1). Cleared only by writing to logic 0. Writing to a logic 1 has no effect.

ALRTSUM (0x07)

ALRTSUM is a read-accessible register that relates added, detailed information on the current status of the device, breaking out several summary bits in STATUS1.

BIT	15	14	13	12	11	10	9	8
Field	ALRTADCOVST	ALRTCOMPOVST	ALRTADCUVST	ALRTCOMPUVST	ALRTADCAUXOVST	ALRTCOMPAUXOVST	ALRTADCAUXUVST	ALRTCOMPAUXUVST
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	ALRTCALOSADC	ALRTCALOSR	ALRTCALOSTHRM	ALRTCALGAINP	ALRTCALGAINR
Reset	–	–	–	0b0	0b0	0b0	0b0	0b0
Access Type	–	–	–	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION
ALRTADCOVST	15	Cell ADC Overvoltage Alert Status Summary Bitwise logical OR of ALRTOV[14:1], based on ADC measurements. Cleared on next acquisition, if all enabled overvoltage conditions are resolved. Read only.
ALRTCOMPOVST	14	Comparator Cell Overvoltage Alert Status Summary Bitwise logical OR of ALRTCOMPOV[14:1], based on redundant comparator monitoring. Cleared on next acquisition, if all enabled overvoltage conditions are resolved. Read only.
ALRTADCUVST	13	Cell ADC Undervoltage Alert Status Summary Bitwise logical OR of ALRTUV[14:1], based on ADC measurements. Cleared on next acquisition, if all enabled undervoltage conditions are resolved. Read only.
ALRTCOMPUVST	12	Comparator Cell Undervoltage Alert Status Summary Bitwise logical OR of ALRTCOMPUV[14:1], based on redundant comparator monitoring. Cleared on next acquisition, if all enabled undervoltage conditions are resolved. Read only.
ALRTADCAUXOVST	11	Auxiliary ADC Overvoltage (Cold) Alert Status Summary Logical OR of ALRTAUXOV[5:0], based on ADC measurements. Cleared on next acquisition, if all enabled overvoltage conditions are resolved. Read only.
ALRTCOMPAUXOVST	10	Comparator Auxiliary Overvoltage (Cold) Alert Status Summary Logical OR of ALRTCOMPAUXOV[5:0], based on redundant comparator monitoring. Cleared on next acquisition, if all enabled overvoltage conditions are resolved. Read only.
ALRTADCAUXUVST	9	Auxiliary ADC Undervoltage (Hot) Alert Logical OR of ALRTAUXUV[5:0], based on ADC measurements. Cleared on next acquisition, if all enabled undervoltage conditions are resolved. Read only.
ALRTCOMPAUXUVST	8	Comparator Auxiliary Undervoltage (Hot) Alert Status Summary Logical OR of ALRTCOMPAUXUV[5:0], based on redundant comparator monitoring. Cleared on next acquisition, if all enabled undervoltage conditions are resolved. Read only.

BITFIELD	BITS	DESCRIPTION
ALRTCALOSADC	4	ADC Offset Calibration Alert 0 = ADC Offset Calibration Valid 1 = ADC Offset Calibration Fault ALRTCALOSADC indicates the ADC offset calibration operation returned a result outside expected boundaries. Cleared when a later calibration operation or write to CALOSADC returns an expected result. Read only.
ALRTCALOSR	3	Ramp LSA + ADC Offset Calibration Alert 0 = LSA + ADC Offset Calibration Valid 1 = LSA + ADC Offset Calibration Fault ALRTCALOSR indicates the LSA + ADC offset calibration operation returned a result outside expected boundaries. Cleared when a later calibration operation or write to CALOSR returns an expected result. Read only.
ALRTCALOSTHRM	2	ADC Ratiometric Offset Calibration Alert 0 = Ratiometric ADC Offset Calibration Valid 1 = Ratiometric ADC Offset Calibration Fault ALRTCALOSTHRM indicates the ratiometric ADC offset calibration operation returned a result outside expected boundaries. Cleared when a later calibration operation or write to CALOSTHRM returns an expected result. Read only.
ALRTCALGAINP	1	Pyramid Gain Calibration Alert 0 = Pyramid Gain Calibration Valid 1 = Pyramid Calibration Fault ALRTCALGAINP indicates the gain calibration operation returned a result outside expected boundaries. Cleared when a later calibration operation or write to CALGAINP returns an expected result. Read only.
ALRTCALGAINR	0	Ramp Gain Calibration Alert 0 = Ramp Gain Calibration Valid 1 = Ramp Calibration Fault ALRTCALGAINR indicates the gain calibration operation returned a result outside expected boundaries. Cleared when a later calibration operation or write to CALGAINR returns an expected result. Read only.

ALRTOVCELL (0x08)

ALRTOVCELL is a read-accessible register that relates current information on cell overvoltage fault alerts based on ADC measurements.

BIT	15	14	13	12	11	10	9	8
Field	–	–	ALRTOV[14:9]					
Reset	–	–	0x0000					
Access Type	–	–	Read Only					

BIT	7	6	5	4	3	2	1	0
Field	ALRTOV[8:1]							
Reset	0x0000							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
ALRTOV	13:0	Cell Overvoltage Fault Alert ALRTOV[n] indicates $V_{CELLN} > V_{OV}$ (OVTHSET threshold for POLARITY = 0, BIPOVTHSET for POLARITY = 1); evaluated/enabled if OVALRTEN[n] = 1. Cleared on next acquisition, if the overvoltage condition is resolved. Read only.

ALRTUVCELL (0x09)

ALRTOVCELL is a read-accessible register that relates current information on cell undervoltage fault alerts based on ADC measurements.

BIT	15	14	13	12	11	10	9	8
Field	–	–	ALRTUV[14:9]					
Reset	–	–	0x0000					
Access Type	–	–	Read Only					

BIT	7	6	5	4	3	2	1	0
Field	ALRTUV[8:1]							
Reset	0x0000							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
ALRTUV	13:0	Cell Undervoltage Fault Alert ALRTOV[n] indicates $V_{CELLN} < V_{UV}$ (UVTHSET threshold for POLARITY = 0, BIPUVTHSET for POLARITY = 1); evaluated/enabled if UVALRTEN[n] = 1. Cleared on next acquisition, if the undervoltage condition is resolved. Read only.

MINMAXCELL (0x0A)

MINMAX is a read-accessible register that relates the cell locations with the highest and lowest values measured.

BIT	15	14	13	12	11	10	9	8
Field	–	–	–	–	MAXCELL[3:0]			
Reset	–	–	–	–	0x0			
Access Type	–	–	–	–	Read Only			

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	MINCELL[3:0]			
Reset	–	–	–	–	0x0			
Access Type	–	–	–	–	Read Only			

BITFIELD	BITS	DESCRIPTION
MAXCELL	11:8	Maximum Voltage Cell Cell number [14:1] of the maximum cell voltage enabled/observed (for all CELLENn = 1) in the last scan (SCAN = 1) based on ALU/IIR data as selected by RDFILT. This bitfield is not updated for data requests made with SCAN = 0. If multiple cells have the same maximum value, this field contains the lowest cell number reporting that result. ***Note:*** *This operation works on unipolar or bipolar measurement sets, as selected by MINMAXPOL. If MINMAXPOL is set such that no measurements in the scan meet the criteria (e.g., MINMAXPOL = 1 (bipolar), but POLARITY[14:1] = 0000h), a result of Fh will be returned (indicating no valid result was found).* Read only.
MINCELL	3:0	Minimum Voltage Cell Cell number [14:1] of the minimum cell voltage enabled/observed (for all CELLENn = 1) in the last scan (SCAN = 1) based on ALU/IIR data as selected by RDFILT. This bitfield is not updated for data requests made with SCAN = 0. If multiple cells have the same minimum value, this field contains the lowest cell number reporting that result. ***Note:*** *This operation works on unipolar or bipolar measurement sets, as selected by MINMAXPOL. If MINMAXPOL is set such that no measurements in the scan meet the criteria (e.g., MINMAXPOL = 1 (bipolar), but POLARITY[14:1] = 0000h), a result of Fh will be returned (indicating no valid result was found).* Read only.

ALRTAUXPRTCTREG (0x0B)

ALRTAUXPRTCT is a read-accessible register that relates current information on auxiliary input protection fault alerts.

BIT	15	14	13	12	11	10	9	8
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–

BIT	7	6	5	4	3	2	1	0
Field	–	–	ALRTAUXPRTCT[5:4]		ALRTAUXPRTCT[3:0]			
Reset	–	–	0x00		0x00			
Access Type	–	–	Read Only		Read Only			

BITFIELD	BITS	DESCRIPTION
ALRTAUXPRTCT	5:4	Auxiliary Protection Fault Alert ALRTAUXPRTCT[n] indicates $V_{AUX[n]} > V_{AA}$; the alert is evaluated/enabled on each AUX/GPIO pin configured as an AUXINn input (see AUXGPIOCFG). Once the fault condition is detected on a pin, the AUXINn input switch is disabled to protect internal circuitry. AUXINn measurements and alerts for that pin will be invalid until proper operating conditions are restored. Cleared only if the condition is resolved upon a retry, or if the affected pin is no longer configured as an AUXINn input (disabling the protection circuit). In order to retry AUX operation and clear the fault condition, rewrite the desired configuration to the AUXGPIOCFG register (it is not necessary to toggle the configuration). Read only.
ALRTAUXPRTCT	3:0	Auxiliary Protection Fault Alert ALRTAUXPRTCT[n] indicates $V_{AUX[n]} > V_{AA}$; the alert is evaluated/enabled on each AUX/GPIO pin configured as an AUXINn input (see AUXGPIOCFG). Once the fault condition is detected on a pin, the AUX[n] input switch is disabled to protect internal circuitry. AUX[n] measurements and alerts for that pin will be invalid until proper operating conditions are restored. Cleared only if the condition is resolved upon a retry, or if the affected pin is no longer configured as an AUXINn input (disabling the protection circuit). In order to retry AUX operation and clear the fault condition, rewrite the desired configuration to the AUXGPIOCFG register (it is not necessary to toggle the configuration). Read only.

ALRTAUXOVREG (0x0C)

ALRTAUXOV is a read-accessible register that relates current information on auxiliary overvoltage (cold) fault alerts.

BIT	15	14	13	12	11	10	9	8
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–

BIT	7	6	5	4	3	2	1	0
Field	–	–	ALRTAUXOV[5:4]		ALRTAUXOV[3:0]			
Reset	–	–	0x0		0x0			
Access Type	–	–	Read Only		Read Only			

BITFIELD	BITS	DESCRIPTION
ALRTAUXOV	5:4	Auxiliary Overvoltage (Cold) Fault Alert ALRTAUXOV[n] indicates $V_{AUXINn} > V_{AUXOVTHSET}$; evaluated/enabled if AUXOVALRTEN[n] = 1. Cleared on next acquisition, if the overvoltage condition is resolved. Read only.

BITFIELD	BITS	DESCRIPTION
ALRTAUXOV	3:0	Auxiliary Overvoltage (Cold) Fault Alert ALRTAUXOV[n] indicates V_{AUXINn} > $V_{AUXOVTHSET}$; evaluated/enabled if AUXOVALRTEN[n] = 1. Cleared on next acquisition, if the overvoltage condition is resolved. Read only.

ALRTAUXUVREG (0x0D)

ALRTAUXUV is a read-accessible register that relates current information on auxiliary undervoltage fault (hot) alerts.

BIT	15	14	13	12	11	10	9	8
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–

BIT	7	6	5	4	3	2	1	0
Field	–	–	ALRTAUXUV[5:4]		ALRTAUXUV[3:0]			
Reset	–	–	0x0		0x0			
Access Type	–	–	Read Only		Read Only			

BITFIELD	BITS	DESCRIPTION
ALRTAUXUV	5:4	Auxiliary Undervoltage (Hot) Fault Alert ALRTAUXUV[n] indicates V_{AUXINn} < $V_{AUXUVTHSET}$; evaluated/enabled if AUXUVALRTEN[n] = 1. Cleared on next acquisition, if the undervoltage condition is resolved. Read only.
ALRTAUXUV	3:0	Auxiliary Undervoltage (Hot) Fault Alert ALRTAUXUV[n] indicates V_{AUXINn} < $V_{AUXUVTHSET}$; evaluated/enabled if AUXUVALRTEN[n] = 1. Cleared on next acquisition, if the undervoltage condition is resolved. Read only.

ALRTCOMPOVREG (0x0E)

ALRTCOMPOV is a read-accessible register that relates current information on cell overvoltage fault alerts based on the redundant comparator.

BIT	15	14	13	12	11	10	9	8
Field	–	–	ALRTCOMPOV[14:9]					
Reset	–	–	0x0000					
Access Type	–	–	Read Only					

BIT	7	6	5	4	3	2	1	0
Field	ALRTCOMPOV[8:1]							
Reset	0x0000							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
ALRTCOMPOV	13:0	Cell Overvoltage Fault Comparator Alert ALRTCOMPOV[n] indicates $V_{CELL[n]} > V_{COMPOVTH}$ (Comparator Overvoltage Threshold); evaluated/enabled if OVALRTEN[n] = 1. Cleared on next comparator acquisition, if the overvoltage condition is resolved. Read only.

ALRTCOMPUVREG (0x0F)

ALRTCOMPUV is a read-accessible register that relates current information on cell undervoltage fault alerts based on the redundant comparator.

BIT	15	14	13	12	11	10	9	8
Field	–	–	ALRTCOMPUV[14:9]					
Reset	–	–	0x0000					
Access Type	–	–	Read Only					

BIT	7	6	5	4	3	2	1	0
Field	ALRTCOMPUV[8:1]							
Reset	0x0000							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
ALRTCOMPUV	13:0	Cell Undervoltage Fault Comparator Alert ALRTCOMPUV[n] indicates $V_{CELL[n]} < V_{COMPUVTH}$ (Comparator Undervoltage Threshold); evaluated/enabled if UVALRTEN[n] = 1. Cleared on next comparator acquisition, if the undervoltage condition is resolved. Read only.

ALRTCOMPAUXOVREG (0x10)

ALRTCOMPAUXOV is a read-accessible register that relates current information on auxiliary overvoltage fault (cold) alerts based on the redundant comparator.

BIT	15	14	13	12	11	10	9	8
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–

BIT	7	6	5	4	3	2	1	0
Field	–	–	ALRTCOMPAUXOV[5:4]		ALRTCOMPAUXOV[3:0]			
Reset	–	–	0x0		0x0			
Access Type	–	–	Read Only		Read Only			

BITFIELD	BITS	DESCRIPTION
ALRTCOMPAUXOV	5:4	Auxiliary Overvoltage (Cold) Fault Comparator Alert ALRTCOMPAUXOV[n] indicates $V_{AUXINn} > V_{COMPOVTH}$ (Comparator Overvoltage Threshold, Cold); evaluated/enabled if AUXOVALRTEN[n] = 1. Cleared on next comparator acquisition, if the overvoltage condition is resolved. Read only.
ALRTCOMPAUXOV	3:0	Auxiliary Overvoltage (Cold) Fault Comparator Alert ALRTCOMPAUXOV[n] indicates $V_{AUXINn} > V_{COMPOVTH}$ (Comparator Overvoltage Threshold, Cold); evaluated/enabled if AUXOVALRTEN[n] = 1. Cleared on next comparator acquisition, if the overvoltage condition is resolved. Read only.

ALRTCOMPAUXUVREG (0x11)

ALRTCOMPAUXUV is a read-accessible register that relates current information on auxiliary undervoltage fault (hot) alerts based on the redundant comparator.

BIT	15	14	13	12	11	10	9	8
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–

BIT	7	6	5	4	3	2	1	0
Field	–	–	ALRTCOMPAUXUV[5:4]		ALRTCOMPAUXUV[3:0]			
Reset	–	–	0x0		0x0			
Access Type	–	–	Read Only		Read Only			

BITFIELD	BITS	DESCRIPTION
ALRTCOMPAUXUV	5:4	Auxiliary Undervoltage (Hot) Fault Comparator Alert ALRTCOMPAUXUV[n] indicates $V_{AUXINn} < V_{COMPUVTH}$ (Comparator Undervoltage Threshold, Hot); evaluated/enabled if AUXUVALRTEN[n] = 1. Cleared on next acquisition, if the undervoltage condition is resolved. Read only.
ALRTCOMPAUXUV	3:0	Auxiliary Undervoltage (Hot) Fault Comparator Alert ALRTCOMPAUXUV[n] indicates $V_{AUXINn} < V_{COMPUVTH}$ (Comparator Undervoltage Threshold, Hot); evaluated/enabled if AUXUVALRTEN[n] = 1. Cleared on next acquisition, if the undervoltage condition is resolved. Read only.

ALRTBALSWREG (0x12)

ALRTBALSW is a read-accessible register that relates current summary information on balancing switch fault alerts.

BIT	15	14	13	12	11	10	9	8
Field	–	–	ALRTBALSW[13:8]					
Reset	–	–	0x0000					
Access Type	–	–	Read Only					

BIT	7	6	5	4	3	2	1	0
Field	ALRTBALSW[7:0]							
Reset	0x0000							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
ALRTBALSW	13:0	Balance Switch Fault Alert ALRTBALSW[n] indicates the corresponding measurement result fails the threshold specified by the Balance Switch Diagnostic modes (SCANCFG = 100 through 111). Testing and faults above the TOPCELL1/2 position are automatically masked out of this register (see PACKCFG:TOPCELL1&2 for complete details). Cleared on next acquisition, if the condition is resolved. Read only.

SWACTION (0x13)

SWACTION is a read- and write-accessible register that contains bits allowing software exit and reset requests. These requests are not recommended for general use, but may be of use in case of error.

BIT	15	14	13	12	11	10	9	8
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	SWPOR
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Write, Read, Pulse

BITFIELD	BITS	DESCRIPTION
SWPOR	0	Software POR Request 0 = Normal Operation (default, no effect) 1 = Initiates Software POR event Always reads logic 0.

DEVCFG1 (0x14)

DEVCNFG1 is a read- and write-accessible register that governs the configuration of the device interface operation.

BIT	15	14	13	12	11	10	9	8
Field	UARTCFG[1:0]		TXUIDLEHIZ	TXLIDLEHIZ	DEVCFG1RSRV[1:0]		ALIVECNTEN	UARTHOST
Reset	0b11		0b0	0b0	0b00		0b0	0b1
Access Type	Write, Read, Ext		Write, Read, Ext	Write, Read, Ext	Write, Read, Ext		Write, Read, Ext	Read Only

BIT	7	6	5	4	3	2	1	0
Field	DEVCFG1RSRV	DEVCFG1RSRV	DEVCFG1RSRV	DEVCFG1RSRV	UARTDCEN	NOPEC	ALERTEN	DBLBUFEN
Reset	0b0	0b0	0b0	0b0	0b1	0b0	0b0	0b0
Access Type	Write, Read, Ext	Write, Read, Ext	Write, Read, Ext	Write, Read, Ext	Write, Read	Write, Read, Ext	Write, Read, Ext	Write, Read

BITFIELD	BITS	DESCRIPTION
UARTCFG	15:14	UART Interface Configuration 00 - Single-UART Interface with External Loopback 01 - Single-UART Interface with Internal Loopback 10 - Single-UART Interface with Differential Alert Interface 11 - Dual-UART Interface (default) Single UART options with Loopback (modes 0x): The UART Up Path is used for read and write commands and the Down Path is used as a return (pass-through) path. If an internal loopback path is desired, the internal shunt should only be engaged on the last device in the chain using mode 01. Alert Interface is single-ended (using the ALERTIN and ALERTOUT pins) since the Down Path is engaged for UART communications. Single UART with Differential Alert Interface (mode 10): The UART Up Path is used for read and write commands with a direct wire return path from the last device in the chain to the µC. The Down Path is used as a differential Alert path. The single-ended Alert path is disabled - the ALERTOUT port will idle and the ALERTIN port will be disabled. Dual UART Interface: Both the Up and Down Interfaces are used for UART communication. Only the host path (selected using UPHOST or DOWNHOST commands, and indicated by HOSTUART) accepts write commands, while both paths can accept read commands. The Alert Interface is single-ended (using the ALERTIN and ALERTOUT pins) since the Down Path is engaged for UART communications. For all the above options, the UART Up Path uses the RXL->TXU ports, and the UART Down Path uses the TXL->RXU ports. This bitfield is unaffected in the event of a SWPOR (software POR) request by the host. ***Note:*** *The device hardware must be preconfigured to support the correct operational mode. The device powers up in the Dual-UART mode to ensure any hardware configuration can configure the device. If the incorrect operating mode is configured, the UART master should cease communications (and possibly issue a FORCEPOR) to reset the device to default status through SHDNL assertion.*
TXUIDLEHIZ	13	UART Upper Tx Idle Mode Selection 0 = TXU Drivers Idle in Logic 0 (default) 1 = TXU Drivers Idle in High-Z Leave in default state for normal operation. This bitfield is unaffected in the event of a SWPOR (software POR) request by the host.

BITFIELD	BITS	DESCRIPTION
TXLIDLEHIZ	12	UART Lower TX Idle Mode Selection 0 = TXL Drivers Idle in Logic 0 (default) 1 = TXL Drivers Idle in High-Z Leave in default state for normal operation. This bitfield is unaffected in the event of a SWPOR (software POR) request by the host.
DEVCFG1RSRV	11:10	Reserved. Reads back the value written.
ALIVECNTEN	9	Enable UART Interface Alive Counter 0 = Do not send Alive-Counter byte (default). 1 = Enables inclusion of Alive-Counter byte at end of all write and read packets.
UARTHOST	8	UART Host Mode Indicator Bit 0 = UART Down Path is Host 1 = UART Up Path is Host (default) Signfies which UART path is currently configured as the host. Down Host mode is only accessible if UARTCFG = DUAL (11). The host mode is selected using UPHOST and DOWNHOST commands. Read only. This bitfield is unaffected in the event of a SWPOR (software POR) request by the host.
DEVCFG1RSRV	7	Reserved. Reads back the value written.
DEVCFG1RSRV	6	Reserved. Reads back the value written.
DEVCFG1RSRV	5	Reserved. Reads back the value written.
DEVCFG1RSRV	4	Reserved. Reads back the value written.
UARTDCEN	3	UART Data Check Byte Enable (Interface Option) 0 - Data Check Byte Not Supported 1 - Data Check Byte Required (default)
NOPEC	2	UART PEC/CRC Disable 0 = PEC/CRC Enabled (default) 1 = PEC/CRC Disabled Determines if Packet Error Checking is enforced using the UART interface. If this bit is set, the PEC characters should be omitted from the UART packet/ command.

BITFIELD	BITS	DESCRIPTION
ALERTEN	1	Alert Interface Enable 0 = Alert Interface is Disabled (Default) 1 = Alert Interface is Enabled If disabled: - If UARTCFG = 0x or 11 (Single-Ended Alert), the ALERTOUT port will idle high-Z and the ALERTIN port will be disabled/ignored. - If UARTCFG = 10 (Differential Alert), the UART Down Path will idle as set by TXLIDLEHIZ. If enabled, the device will initiate alerts based on STATUS1 content, as well as pass through any alerts received from/to the daisy-chain. This bit is unaffected in the event of SWPOR (software POR) request by host.
DBLBUFEN	0	Double-Buffer Mode Enable 0 = Normal Operation (default) 1 = Double-Buffered Operation Enables the Double-Buffer mode. This mode automatically transfers data from the ALU/IIR to the data registers at the start of the next acquisition instead of at the end of an acquisition. *This mode may be used so the host can start a second acquisition and then begin reading the data from the first acquisition (during the second acquisition). This works even if the first data read transactions take longer than the second acquisition to complete; simply hold off on a third acquisition until the first acquisition data is retrieved. Launching a third acquisition will move the data from the second acquisition to the data registers for readback during the third acquisition, and so forth.*

DEVCFG2 (0x15)

DEVCNFG2 is a read- and write-accessible register that governs the configuration of the device filtering, several top-level diagnostic modes, and timeout monitors.

BIT	15	14	13	12	11	10	9	8
Field	IIRFC[2:0]			–	DEVCFG2RSRV[3:0]			
Reset	0b010			–	0b0000			
Access Type	Write, Read			–	Write, Read			

BIT	7	6	5	4	3	2	1	0
Field	–	HVCPDIS	FORCEPOR	ALERTDCTSTEN	–	DEVCFG2RSRV	SCANTODIS	CBTODIS
Reset	–	0b0	0b0	0b0	–	0b0	0b0	0b0
Access Type	–	Write, Read	Write, Read	Write, Read	–	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
IIRFC	15:13	IIR Filter Coefficient Selection 000 = 0.125 001 = 0.250 010 = 0.375 (default) 011 = 0.500 100 = 0.625 101 = 0.750 110 = 0.875 111 = 1.000 (filter off) This setting determines the weight of the current measurement result vs. the previously accumulated results in the IIR filter. A setting of 1.0 effectively disables the filter.
DEVCFG2RSRV	11:8	Reserved. Reads back the value written.
HVCPDIS	6	HV Charge Pump Disable 0 = Normal Operation (default) 1 = Disable HV Charge Pump Used for ALRTHVUV diagnostic. If the HV charge pump is disabled in normal operation, measurement errors will result due to an V_{HV} undervoltage condition.
FORCEPOR	5	Force POR Event 0 = Normal Operation (default) 1 = Enables hard POR by pulling down SHDNL internally. If cleared before the POR occurs, the active pulldown on SHDNL will be removed. ***Note:*** *This bit is used to accelerate a complete POR event issued by SHDNL falling. In UART applications, it is possible that UART activity will fight or overcome the SHDNL pulldown. For best results, cease UART communications when using this mode.*
ALERTDCTSTEN	4	UART Alert DC Diagnostic Test Enable 0 = UART Alert DC Testing Disabled (Default) 1 = UART Alert DC Testing Enabled Used to place the ALRTOUT pin in a DC diagnostic mode for use in testing for shorts to GPIO/AUX0. If enabled, the ALRTOUT pin will be driven low if an alert condition is present, and driven high otherwise. ALRTUSER can be written to exercise ALRTOUT in either direction. Neighboring pins such as AUX/GPIO[0] can be monitored directly or in diagnostic modes to detect a fault. This function works in all UARTCFG modes, including 10 (Differential Alert), which does not normally use the ALRTOUT pin.
DEVCFG2RSRV	2	Reserved. Reads back the value written.
SCANTODIS	1	Scan Timeout Disable 0 = Normal Operation (default) 1 = Disables the acquisition watchdog, but does not clear the SCANTIMEOUT flag in the SCANCTRL register if it is set.
CBTODIS	0	Cell-Balancing Timeout Disable 0 = Normal Operation (default) 1 = Disables the cell-balancing watchdog, but does not clear the ALRTCBTIMEOUT flag in the STATUS3 register if it was previously set.

AUXGPIOCFG (0x16)

AUXGPIOCFG is a read- and write-accessible register that governs the configuration of the AUX/GPIO multifunction pins.

BIT	15	14	13	12	11	10	9	8
Field	I2CEN	–	GPIOEN[5:4]		GPIOEN[3:0]			
Reset	0b0	–	0x3		0xF			
Access Type	Write, Read, Ext	–	Write, Read, Ext		Write, Read, Ext			

BIT	7	6	5	4	3	2	1	0
Field	–	–	GPIODIR[5:4]		GPIODIR[3:0]			
Reset	–	–	0x0		0x0			
Access Type	–	–	Write, Read, Ext		Write, Read, Ext			

BITFIELD	BITS	DESCRIPTION
I2CEN	15	Digital I^2C Mode Enable 0 = Normal Configured Operation (default) 1 = I^2C Master Operation If I2CEN is set high, AUX/GPIO[0] is configured as the SDA open-drain I/O and AUX/GPIO[1] is configured as the SCL open-drain output driver for use as an I^2C master. If this bit is set, all remaining selections in AUXGPIOCFG, GPIO, and MEASUREEN2 will be ignored for AUX/GPIO[1:0].
GPIOEN	13:12	Digital GPIO Mode Enable 0 = Analog Input (AUX) Mode (High-Z) 1 = Digital GPIO Mode (default) GPIOEN[n] configures the corresponding AUX/GPIO[n] pin for operation in the selected mode.
GPIOEN	11:8	Digital GPIO Mode Enable 0 = Analog Input (AUX) Mode (High-Z) 1 = Digital GPIO Mode (default) GPIOEN[n] configures the corresponding AUX/GPIO[n] pin for operation in the selected mode. ***Note:*** *If I2CEN = 1, GPIOEN[1:0] are ignored, but will still read back the user setting.*
GPIODIR	5:4	Digital GPIO Direction Selection 0 = Digital Input Mode (High-Z, default) 1 = Digital Output Mode GPIODIR[n] configures the direction of the corresponding AUX/GPIO[n] pin. This setting is only applicable if GPIOEN[n] = 1 (Digital GPIO mode enabled). In digital input mode (GPIOEN = 1 and GPIODIR = 0), a 2MΩ pulldown (R_{GPIO}) will be enabled to prevent the GPIO input from floating. In digital output mode (GPIOEN = 1 and GPIODIR = 1, the GPIO input circuitry will continue to operate, allowing direct observation of the port status.

BITFIELD	BITS	DESCRIPTION
GPIODIR	3:0	Digital GPIO Direction Selection 0 = Digital Input Mode (High-Z, default) 1 = Digital Output Mode GPIODIR[n] configures the direction of the corresponding AUX/GPIO[n] pin. This setting is only applicable if GPIOEN[n] = 1 (Digital GPIO mode enabled). In digital input mode (GPIOEN = 1 and GPIODIR = 0), a 2MΩ pulldown (R_{GPIO}) will be enabled to prevent the GPIO input from floating. In digital output mode (GPIOEN = 1 and GPIODIR = 1), the GPIO input circuitry will continue to operate, allowing direct observation of the port status. ***Note:*** *If I2CEN = 1, GPIODIR[1:0] is ignored, but will still read back the user setting.*

GPIOCFG (0x17)

GPIO is a read- and write-accessible register that governs the output state of GPIO outputs and reads back the input state of GPIO inputs.

BIT	15	14	13	12	11	10	9	8
Field	–	–	GPIODRV[5:4]		GPIODRV[3:0]			
Reset	–	–	0x0		0b0			
Access Type	–	–	Write, Read, Ext		Write, Read, Ext			

BIT	7	6	5	4	3	2	1	0
Field	–	–	GPIORD[5:4]		GPIORD[3:0]			
Reset	–	–	0x0		0x0			
Access Type	–	–	Read Only		Read Only			

BITFIELD	BITS	DESCRIPTION
GPIODRV	13:12	Digital GPIO Output State 0 = Output Logic 0 (default) 1 = Output Logic 1 GPIODRV[n] sets the output logic state direction of the corresponding AUX/GPIO[n] pin. This setting is only applicable if GPIOEN[n] = 1 and GPIODIR[n] = 1 (Digital GPIO Output mode enabled).
GPIODRV	11:8	Digital GPIO Output State 0 = Output Logic 0 (default) 1 = Output Logic 1 GPIODRV[n] sets the output logic state direction of the corresponding AUX/GPIO[n] pin. This setting is only applicable if GPIOEN[n] = 1 and GPIODIR[n] = 1 (Digital GPIO Output mode enabled). ***Note:*** *If I2CEN = 1, GPIODRV[1:0] is ignored, but will still read back the user setting.*

BITFIELD	BITS	DESCRIPTION
GPIORD	5:4	Digital GPIO Input State Indicator 0 = Logic 0 (default) 1 = Logic 1 GPIORD[n] indicates the current logic state of each active GPIO[n] input buffer. Data is only relevant if GPIOEN[n] = 1 (all digital GPIO pins are monitored in Input or Output mode), otherwise zero will be read back. The logic state is sampled at the end of the parity bit of the register address byte during a read transaction. Read only.
GPIORD	3:0	Digital GPIO Input State Indicator 0 = Logic 0 (default) 1 = Logic 1 GPIORD[n] indicates the current logic state of each active GPIO[n] input buffer. Data is only relevant if GPIOEN[n] = 1 (all digital GPIO pins are monitored in Input or Output mode), otherwise 0 will be read back. The logic state is sampled at the end of the parity bit of the register address byte during a read transaction. Read only. ***Note:*** *If I2CEN = 1, GPIORD[1:0] is no longer valid and will read back 00.*

PACKCFG (0x18)

PCKCFG is a read- and write-accessible register that configures the part such that the top most cell and block used in the application is known. Details of flexible-pack applications are also configured within this register.

BIT	15	14	13	12	11	10	9	8
Field	FLXPCKEN2	FLXPCKEN1	FLXPCKSCAN	–	TOPBLOCK[3:0]			
Reset	0b1	0b1	0b1	–	0xF			
Access Type	Write, Read	Write, Read	Write, Read	–	Write, Read			

BIT	7	6	5	4	3	2	1	0
Field	TOPCELL2[3:0]				TOPCELL1[3:0]			
Reset	0xF				0xF			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION
FLXPCKEN2	15	Flexible-Pack Enable 2 0 = Flexible-Pack Functions Disabled 1 = Flexible-Pack Selection of Top Cell and Top Block Enabled (default) Indicates the flexible-pack support is engaged (DCINMUX and V_{BLKMUX}), selecting the internal power and block routing path when the DCIN pin is not supplied externally. This selection is protected by a redundant bitfield. FLXPCKEN1 and FLXPCKEN2 must agree, resulting in a valid internal FLXPCKEN1/2 selection. If the two bitfields do not agree, the internal FLXPCKEN1/2 selection will be mapped to 1 (enabled, default) and DCINMUX selection will be mapped to the OFF position. SWn selection is determined by TOPCELL1/2 (based on TOPCELL1&2). Valid selections range from Cell 8 (0x8) to Cell 14 (0xE). If an unsupported selection (0x0 to 0x7, 0xF) is made in TOPCELL1/2, the DCINMUX selection switches are disabled, but the DCINMUX common switch is enabled (this is the default condition). In this condition, DCIN is initially pulled to a diode below the highest SWn input and there is no interference if DCIN is externally supplied. Block selection is determined by TOPBLOCK. Valid cell selections range from Cell 8 (0x8) to Cell 14 (0xE). If an unsupported selection (0x0~0x7, 0xF) is made in TOPBLOCK, the V_{BLKP} port is selected.
FLXPCKEN1	14	Flexible-Pack Enable 1 (Redundant Bitfield) 0 = Flexible-Pack Functions Disabled 1 = Flexible-Pack Selection of Top Cell and Top Block Enabled (default) See FLXPCKEN2 for complete details on operation and redundant bitfield checking.
FLXPCKSCAN	13	Flexible-Pack Scan Configuration 0 = Flexible-Pack ALTMUX Scan Unmodified 1 = Flexible-Pack ALTMUX Scan Modified with Additional 30µs Delay before Acquisition of TOPCELL1/2 (default) FLEXPCKSCAN will configure the measurement sequence such that for any scan with ALTMUXSEL = 1, there will be 30µs delay prior to sampling the TOPCELL1/2 voltage regardless of SCANMODE. This delay affords the SW[TOPCELL1/2] input time to settle for an accurate diagnostic measurement when DCIN loading is temporarily suspended in flexible-pack configurations. Impacts scan sequences where FLXPCKEN1/2 = 1 and TOPCELL1/2 is set to a supported value (0x8 to 0xE), and ALTMUXSEL = 1 (effective value). Ignored otherwise.
TOPBLOCK	11:8	Top Block Selection Configures the top block position if a selection other than the V_{BLK} pin is chosen. Used to properly determine the connection point for the V_{BLOCK} resistive divider. TOPBLOCK[3:0] selects the Cn pin to be connected to the V_{BLOCK} resistive divider. 0xF (default) selects the V_{BLK} pin. Selections 0x0 through 0x7 are not supported and will be mapped to 0xF (V_{BLK}, default). TOPBLOCK may differ from TOPCELL1/2 if there are bus bars installed in channels above the top cell. TOPBLOCK is ignored if FLXPCKEN1/2 = 0.

BITFIELD	BITS	DESCRIPTION
TOPCELL2	7:4	Top Cell Selection 2 Configures the top cell position if less than 14 channels are used. Used to properly mask the ALRTBALSW diagnostic alerts (always) and to make DCINMUX selections when FLXPCKEN1/2 = 1. This selection is protected by a redundant bitfield. TOPCELL1 and TOPCELL2 must agree, resulting in a valid internal TOPCELL1/2 selection. If the two bitfields do not agree, no ALRTBALSW alerts are masked, and the internal DCINMUX selection will be mapped to the OFF position. 0xF (default) removes all ALRTBALSW masking, and places DCINMUX in the OFF position. Flexible-Pack Behavior TOPCELL1/2 selects the SW pin to be connected to the DCIN pin. Selections 0x8 to 0xE map to SW[8] to SW[14]. Selections 0x0 to 0x7 and 0xF are not supported and will be mapped to an OFF position. In the OFF position, DCIN is initially pulled to a diode below the highest SWn input. Masking Behavior TOPCELL1/2 also sets masking behavior in ALRTBALSW diagnostics. All selections are supported for this function.
TOPCELL1	3:0	Top Cell Selection 1 (Redundant Bitfield) Configures the top cell position if less than 14 channels are used. Used to properly mask the ALRTBALSW diagnostic alerts (always) and to make DCINMUX selections when FLXPCKEN1/2 = 1. See TOPCELL2 for complete details on operation and redundant bitfield checking.

ALRTIRQEN (0x19)

ALRTIRQEN is a read- and write-accessible register that selects which STATUS1 alerts trigger interrupts through the ALERT interface port(s), and are included in notifications through the DCByte and Alert Packet. Note the information in the STATUS1 register itself (or any component terms rolled up into STATUS1) is not masked/disabled by these settings, allowing the underlying data to always be available through STATUS1 readback.

BIT	15	14	13	12	11	10	9	8
Field	SCANALRTEN	–	MSMTCHALRTEN	CELLOVSTALRTEN	CELLUVSTALRTEN	BLKOVSTALRTEN	BLKUVSTALRTEN	AUXOVSTALRTEN
Reset	0b0	–	0b1	0b1	0b1	0b1	0b1	0b1
Access Type	Write, Read	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BIT	7	6	5	4	3	2	1	0
Field	AUXUVSTALRTEN	–	PECALRTEN	INTRFCALRTEN	CALALRTEN	CBALALRTEN	FMEA2ALRTEN	FMEA1ALRTEN
Reset	0b1	–	0b1	0b1	0b1	0b1	0b1	0b1
Access Type	Write, Read	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
SCANALRTEN	15	Scan Complete Alert Enable 0 = ALRTSCAN Masked (default) 1 = ALRTSCAN Enabled Disabled by default since this is not a safety feature, but a notification option. Applies to the Alert Interface only in order to support interrupt-driven applications; ALRTSCAN is never included in the UART DCByte and Alert Packet .
MSMTCHALRTEN	13	Cell Voltage Mismatch Alert Enable 0 = ALRTMSMTCH Masked 1 = ALRTMSMTCH Enabled (default) Applies to the Alert Interface, UART DCByte, and Alert Packet .
CELLOVSTALRTEN	12	Cell Overvoltage Status Summary Alert Enable 0 = ALRTCELLOVST Masked 1 = ALRTCELLOVST Enabled (default) Applies to the Alert Interface, UART DCByte, and Alert Packet .
CELLUVSTALRTEN	11	Cell Undervoltage Status Summary Alert Enable 0 = ALRTCELLUVST Masked 1 = ALRTCELLUVST Enabled (default) Applies to the Alert Interface, UART DCByte, and Alert Packet .
BLKOVSTALRTEN	10	Block Overvoltage Status Alert Enable 0 = ALRTBLKOVST Masked 1 = ALRTBLKOVST Enabled (default) Applies to the Alert Interface, UART DCByte, and Alert Packet .
BLKUVSTALRTEN	9	Block Undervoltage Status Alert Enable 0 = ALRTBLKUVST Masked 1 = ALRTBLKUVST Enabled (default) Applies to the Alert Interface, UART DCByte, and Alert Packet .
AUXOVSTALRTEN	8	Auxiliary Overvoltage Status Summary Alert Enable 0 = ALRTAUXOVST Masked 1 = ALRTAUXOVST Enabled (default) Applies to the Alert Interface, UART DCByte, and Alert Packet .
AUXUVSTALRTEN	7	Auxiliary Undervoltage Status Summary Alert Enable 0 = ALRTAUXUVST Masked 1 = ALRTAUXUVST Enabled (default) Applies to the Alert Interface, UART DCByte, and Alert Packet .
PECALRTEN	5	Packet Error Check (CRC) Alert Enable 0 = ALRTPEC masked 1 = ALRTPEC enabled (default) Applies to the Alert Interface, UART Alert Packet ; ALRTPEC is not included in the UART DCByte.
INTRFCALRTEN	4	Interface Specific Error Alert Enable 0 = ALRTINTRFC Masked 1 = ALRTINTRFC Enabled (default) Applies to the Alert Interface, UART DCByte, and Alert Packet .

BITFIELD	BITS	DESCRIPTION
CALALRTEN	3	Calibration Fault Alert Enable 0 = ALRTCAL Masked 1 = ALRTCAL Enabled (default) Applies to the Alert Interface, UART DCByte, and Alert Packet .
CBALALRTEN	2	Cell-Balancing Status Alert Enable 0 = ALRTCBAL Masked 1 = ALRTCBAL Enabled (default) Applies to the Alert Interface, UART DCByte, and Alert Packet .
FMEA2ALRTEN	1	FMEA2 Condition Summary Alert Enable 0 = ALRTFMEA2 Masked 1 = ALRTFMEA2 Enabled (default) Applies to the Alert Interface, UART DCByte, and Alert Packet .
FMEA1ALRTEN	0	FMEA1 Condition Summary Alert Enable 0 = ALRTFMEA1 Masked 1 = ALRTFMEA1 Enabled (default) Applies to the Alert Interface, UART DCByte, and Alert Packet .

ALRTOVEN (0x1A)

ALRTOVEN is a read- and write-accessible register that enables overvoltage fault checks on selected input channels during scans using either the ADC or comparator.

BIT	15	14	13	12	11	10	9	8
Field	–	BLKOVALRTEN	OVALRTEN[14:9]					
Reset	–	0b0	0x0000					
Access Type	–	Write, Read	Write, Read					

BIT	7	6	5	4	3	2	1	0
Field	OVALRTEN[8:1]							
Reset	0x0000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BLKOVALRTEN	14	Block Overvoltage Fault Check Enable BLKOVALRTEN enables overvoltage fault checking on ADC block measurements against threshold BLKOVTHSET. Clearing also clears the associated block alert.
OVALRTEN	13:0	Overvoltage Fault Check Enable OVALRTEN[n] enables overvoltage fault checking on CELL[n] against threshold OVTHSET (ADC) and COMPOVTH (comparator). Clearing also clears the associated cell alert in ALRTOVCELL and ALRTCOMPOVREG.

ALRTUVEN (0x1B)

ALRTUVEN is a read- and write-accessible register that enables undervoltage fault checks on selected input channels during scans using either the ADC or comparator.

BIT	15	14	13	12	11	10	9	8
Field	–	BLKUVALRTEN	UVALRTEN[14:9]					
Reset	–	0b0	0x0000					
Access Type	–	Write, Read	Write, Read					

BIT	7	6	5	4	3	2	1	0
Field	UVALRTEN[8:1]							
Reset	0x0000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BLKUVALRTEN	14	Block Undervoltage Fault Check Enable BLKUVALRTEN enables undervoltage fault checking on ADC block measurements against threshold BLKUVTHSET. Clearing also clears the associated block alert.
UVALRTEN	13:0	Undervoltage Fault Check Enable UVALRTEN[n] enables undervoltage fault checking on CELL[n] against threshold UVTHSET (ADC) and COMPUVTH (comparator). Clearing also clears the associated cell alert in ALRTOVCELL and ALRTCOMPOVREG.

ALRTAUXOVEN (0x1C)

ALRTAUXOVEN is a read- and write-accessible register that enables auxiliary overvoltage (cold) fault checks on selected auxiliary channels during scans using either the ADC or comparator.

BIT	15	14	13	12	11	10	9	8
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–

BIT	7	6	5	4	3	2	1	0
Field	–	–	AUXOVALRTEN[5:4]		AUXOVALRTEN[3:0]			
Reset	–	–	0x0		0x00			
Access Type	–	–	Write, Read, Ext		Write, Read, Ext			

BITFIELD	BITS	DESCRIPTION
AUXOVALRTEN	5:4	Auxiliary Overvoltage (Cold) Fault Check Enable AUXOVALRTEN[n] enables overvoltage (cold) fault checking on AUX[n] against the ratiometric/absolute threshold AUXROVTHSET/AUXAOVTHSET (ADC) and COMPAUXROVTH/COMPAUXAOVTH (comparator), as selected by AUXREFSEL[n]. Clearing also clears the associated alert. ***Note:*** *If the respective GPIOEN bit is set (GPIO mode), this bit is ignored, but will still read back the user setting.*

BITFIELD	BITS	DESCRIPTION
AUXOVALRTEN	3:0	Auxiliary Overvoltage (Cold) Fault Check Enable AUXOVALRTEN[n] enables overvoltage (cold) fault checking on AUX[n] against the ratiometric/absolute threshold AUXROVTHSET/AUXAOVTHSET (ADC) and COMPAUXROVTH/COMPAUXAOVTH (comparator), as selected by AUXREFSEL[n]. Clearing also clears the associated alert. ***Note:*** *If the I2CEN bit (digital I^2C mode, applies to [1:0] only) or the respective GPIOEN bit is set (GPIO mode), this bit is ignored, but will still read back the user setting.*

ALRTAUXUVEN (0x1D)

ALRTAUXUVEN is a read- and write-accessible register that enables auxiliary undervoltage (hot) fault checks on selected auxiliary channels using either the ADC or comparator.

BIT	15	14	13	12	11	10	9	8
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–

BIT	7	6	5	4	3	2	1	0
Field	–	–	AUXUVALRTEN[5:4]		AUXUVALRTEN[3:0]			
Reset	–	–	0x0		0x0			
Access Type	–	–	Write, Read, Ext		Write, Read, Ext			

BITFIELD	BITS	DESCRIPTION
AUXUVALRTEN	5:4	Auxiliary Undervoltage (Hot) Fault Check Enable AUXUVALRTEN[n] enables undervoltage (hot) fault checking on AUX[n] against the ratiometric/absolute threshold AUXRUVTHSET/AUXAUVTHSET (ADC) and COMPAUXRUVTH/COMPAUXAUVTH (comparator), as selected by AUXREFSEL[n]. Clearing also clears the associated alert. ***Note:*** *If the respective GPIOEN bit is set (GPIO mode), this bit is ignored, but will still read back the user setting.*
AUXUVALRTEN	3:0	Auxiliary Undervoltage (Hot) Fault Check Enable AUXUVALRTEN[n] enables undervoltage (hot) fault checking on AUX[n] against the ratiometric/absolute threshold AUXRUVTHSET/AUXAUVTHSET (ADC) and COMPAUXRUVTH/COMPAUXAUVTH (comparator), as selected by AUXREFSEL[n]. Clearing also clears the associated alert. ***Note:*** *If the I2CEN bit (digital I^2C mode, applies to [1:0] only), or the respective GPIOEN bit is set (GPIO mode), this bit is ignored, but will still read back the user setting.*

ALRTCALTST (0x1E)

ALRTCALTST is a read- and write-accessible register that allows the user to force calibration alerts to test readback and interrupt logic. The forced alert(s) will remain forced until this register is written back to zeros (assuming the existing

calibration data is with range).

BIT	15	14	13	12	11	10	9	8
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	CALOSADCALRTFRC	CALOSRALRTFRC	CALOSTHRMALRTFRC	CALGAINPALRTFRC	CALGAINRALRTFRC
Reset	–	–	–	0b0	0b0	0b0	0b0	0b0
Access Type	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
CALOSADCALRTFRC	4	ADC Offset Calibration Alert Force 0 = ALRTCALOSADC Normal Operation (default) 1 = ALRTCALOSADC Forced if Unmasked Used to test alert functionality.
CALOSRALRTFRC	3	Ramp LSA + ADC Offset Calibration Alert Force 0 = ALRTCALOSR Normal Operation (default) 1 = ALRTCALOSR Forced if Unmasked Used to test alert functionality.
CALOSTHRMALRTFRC	2	Ratiometric ADC Offset Calibration Alert Force 0 = ALRTCALOSTHRM Normal Operation (default) 1 = ALRTCALOSTHRM Forced if Unmasked Used to test alert functionality.
CALGAINPALRTFRC	1	Pyramid Gain Calibration Alert Force 0 = ALRTCALGAINP Normal Operation (default) 1 = ALRTCALGAINP Forced if Unmasked Used to test alert functionality.
CALGAINRALRTFRC	0	Ramp Gain Calibration Alert Force 0 = ALRTCALGAINR Normal Operation (default) 1 = ALRTCALGAINR Forced if Unmasked Used to test alert functionality.

OVTHCLRREG (0x1F)

OVTHCLR is a read- and write-accessible register that selects the cell overvoltage alert clear threshold used with unipolar ADC measurements.

BIT	15	14	13	12	11	10	9	8
Field	OVTHCLR[13:6]							
Reset	0x3FFF							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	OVTHCLR[5:0]						–	–
Reset	0x3FFF						–	–
Access Type	Write, Read						–	–

BITFIELD	BITS	DESCRIPTION
OVTHCLR	15:2	Unipolar Cell Overvoltage Alert Clear Threshold 14-bit threshold value at/below which ALRTOV alerts will be cleared/ deasserted for unipolar cell measurements. ***Note:*** *For proper operation, this value should always be less than or equal to OVTHSET.*

OVTHSETREG (0x20)

OVTHSET is a read- and write-accessible register that selects the cell overvoltage alert set threshold used with unipolar ADC measurements.

BIT	15	14	13	12	11	10	9	8
Field	OVTHSET[13:6]							
Reset	0x3FFF							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	OVTHSET[5:0]						–	–
Reset	0x3FFF						–	–
Access Type	Write, Read						–	–

BITFIELD	BITS	DESCRIPTION
OVTHSET	15:2	Unipolar Cell Overvoltage Alert Set Threshold 14-bit threshold value above which ALRTOV alerts will be set/asserted for unipolar cell measurements. A value of 0x3FFF effectively disables overvoltage checking.

UVTHCLRREG (0x21)

UVTHCLR is a read- and write-accessible register that selects the cell undervoltage alert clear threshold used with unipolar ADC measurements.

BIT	15	14	13	12	11	10	9	8
Field	UVTHCLR[13:6]							
Reset	0x0000							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	UVTHCLR[5:0]						–	–
Reset	0x0000						–	–
Access Type	Write, Read						–	–

BITFIELD	BITS	DESCRIPTION
UVTHCLR	15:2	Unipolar Cell Undervoltage Alert Clear Threshold 14-bit threshold value at/above which ALRTUV alerts will be cleared/ deasserted for unipolar cell measurements. ***Note:*** *For proper operation, this value should always be greater than or equal to UVTHSET.*

UVTHSETREG (0x22)

UVTHSET is a read- and write-accessible register that selects the cell undervoltage alert set threshold used with unipolar ADC measurements.

BIT	15	14	13	12	11	10	9	8
Field	UVTHSET[13:6]							
Reset	0x0000							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	UVTHSET[5:0]						–	–
Reset	0x0000						–	–
Access Type	Write, Read						–	–

BITFIELD	BITS	DESCRIPTION
UVTHSET	15:2	Unipolar Cell Undervoltage Alert Set Threshold 14-bit threshold value below which ALRTUV alerts will be set/asserted for unipolar cell measurements. A value of 0x0000 effectively disables undervoltage checking.

MSMTCHREG (0x23)

MSMTCH is a read- and write-accessible register that selects the cell voltage mismatch alert threshold used with ADC cell scan measurements.

BIT	15	14	13	12	11	10	9	8
Field	MSMTCH[13:6]							
Reset	0x3FFF							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	MSMTCH[5:0]						–	–
Reset	0x3FFF						–	–
Access Type	Write, Read						–	–

BITFIELD	BITS	DESCRIPTION
MSMTCH	15:2	Cell Voltage Mismatch Alert Threshold 14-bit threshold value; if the difference between maximum and minimum cell voltages exceeds this value, ALRTMSMTCH will be set/asserted. Whether only unipolar ADC measurements (POLARITYn = 0) are included in mismatch calculations or all measurements are included is determined by POLARITYCTRL:MINMAXPOL.

BIPOVTHCLRREG (0x24)

BIPOVTHCLR is a read- and write-accessible register that selects the cell overvoltage alert clear threshold used with bipolar ADC measurements.

BIT	15	14	13	12	11	10	9	8
Field	BIPOVTHCLR[13:6]							
Reset	0x3FFF							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	BIPOVTHCLR[5:0]						–	–
Reset	0x3FFF						–	–
Access Type	Write, Read						–	–

BITFIELD	BITS	DESCRIPTION
BIPOVTHCLR	15:2	Bipolar Cell Overvoltage Alert Clear Threshold 14-bit threshold value at/below which ALRTOV alerts will be cleared/ deasserted for bipolar cell measurements. Bipolar format. ***Note:*** *For proper operation, this value should always be less than or equal to BIPOVTHSET.*

BIPOVTHSETREG (0x25)

BIPOVTHSET is a read- and write-accessible register that selects the cell overvoltage alert set threshold used with bipolar ADC measurements.

BIT	15	14	13	12	11	10	9	8
Field	BIPOVTHSET[13:6]							
Reset	0x3FFF							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	BIPOVTHSET[5:0]						–	–
Reset	0x3FFF						–	–
Access Type	Write, Read						–	–

BITFIELD	BITS	DESCRIPTION
BIPOVTHSET	15:2	Bipolar Cell Overvoltage Alert Set Threshold 14-bit threshold value above which ALRTOV alerts will be set/asserted for bipolar cell measurements. Bipolar format. A value of 0x3FFF effectively disables overvoltage checking.

BIPUVTHCLRREG (0x26)

BIPUVTHCLR is a read- and write-accessible register that selects the cell undervoltage alert clear threshold used with bipolar ADC measurements.

BIT	15	14	13	12	11	10	9	8
Field	BIPUVTHCLR[13:6]							
Reset	0x0000							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	BIPUVTHCLR[5:0]						–	–
Reset	0x0000						–	–
Access Type	Write, Read						–	–

BITFIELD	BITS	DESCRIPTION
BIPUVTHCLR	15:2	Bipolar Cell Undervoltage Alert Clear Threshold 14-bit threshold value at/above which ALRTUV alerts will be cleared/ deasserted for bipolar cell measurements. Bipolar format. ***Note:*** *For proper operation, this value should always be greater than or equal to BIPUVTHSET.*

BIPUVTHSETREG (0x27)

BIPUVTHSET is a read- and write-accessible register that selects the cell undervoltage alert set threshold used with bipolar ADC measurements.

BIT	15	14	13	12	11	10	9	8
Field	BIPUVTHSET[13:6]							
Reset	0x0000							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	BIPUVTHSET[5:0]						–	–
Reset	0x0000						–	–
Access Type	Write, Read						–	–

BITFIELD	BITS	DESCRIPTION
BIPUVTHSET	15:2	Bipolar Cell Undervoltage Alert Set Threshold 14-bit threshold value below which ALRTUV alerts will be set/asserted for bipolar cell measurements. Bipolar format. A value of 0x0000 effectively disables undervoltage checking.

BLKOVTHCLRREG (0x28)

BLKOVTHCLR is a read- and write-accessible register that selects the block overvoltage alert clear threshold used with ADC measurements.

BIT	15	14	13	12	11	10	9	8
Field	BLKOVTHCLR[13:6]							
Reset	0x3FFF							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	BLKOVTHCLR[5:0]						–	–
Reset	0x3FFF						–	–
Access Type	Write, Read						–	–

BITFIELD	BITS	DESCRIPTION
BLKOVTHCLR	15:2	Block Overvoltage Alert Clear Threshold 14-bit threshold value at/below which the ALRTBLKOV alert will be cleared/ deasserted. ***Note:*** *For proper operation, this value should always be less than or equal to BLKOVTHSET.*

BLKOVTHSETREG (0x29)

BLKOVTHSET is a read- and write-accessible register that selects the block overvoltage alert set threshold used with ADC measurements.

BIT	15	14	13	12	11	10	9	8
Field	BLKOVTHSET[13:6]							
Reset	0x3FFF							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	BLKOVTHSET[5:0]						–	–
Reset	0x3FFF						–	–
Access Type	Write, Read						–	–

BITFIELD	BITS	DESCRIPTION
BLKOVTHSET	15:2	Block Overvoltage Alert Set Threshold 14-bit threshold value above which the ALRTBLKOV alert will be set/asserted. A value of 0x3FFF effectively disables overvoltage checking.

BLKUVTHCLRREG (0x2A)

BLKUVTHCLR is a read- and write-accessible register that selects the block undervoltage alert clear threshold used with ADC measurements.

BIT	15	14	13	12	11	10	9	8
Field	BLKUVTHCLR[13:6]							
Reset	0x0000							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	BLKUVTHCLR[5:0]						–	–
Reset	0x0000						–	–
Access Type	Write, Read						–	–

BITFIELD	BITS	DESCRIPTION
BLKUVTHCLR	15:2	Block Undervoltage Alert Clear Threshold 14-bit threshold value at/above which the ALRTBLKUV alert will be cleared/ deasserted. ***Note:*** *For proper operation, this value should always be greater than or equal to BLKUVTHSET.*

BLKUVTHSETREG (0x2B)

BLKUVTHSET is a read- and write-accessible register that selects the block undervoltage alert set threshold used with ADC measurements.

BIT	15	14	13	12	11	10	9	8
Field	BLKUVTHSET[13:6]							
Reset	0x0000							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	BLKUVTHSET[5:0]						–	–
Reset	0x0000						–	–
Access Type	Write, Read						–	–

BITFIELD	BITS	DESCRIPTION
BLKUVTHSET	15:2	Block Undervoltage Alert Set Threshold 14-bit threshold value below which the ALRTBLKUV alert will be set/asserted. A value of 0x0000 effectively disables undervoltage checking.

AUXROVTHCLRREG (0x30)

AUXROVTHCLR is a read- and write-accessible register that selects the overvoltage (cold) alert clear threshold used with ratiometric auxiliary ADC measurements.

BIT	15	14	13	12	11	10	9	8
Field	AUXROVTHCLR[13:6]							
Reset	0x3FFF							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	AUXROVTHCLR[5:0]						–	–
Reset	0x3FFF						–	–
Access Type	Write, Read						–	–

BITFIELD	BITS	DESCRIPTION
AUXROVTHCLR	15:2	Ratiometric Auxiliary Overvoltage (Cold) Alert Clear Threshold 14-bit overvoltage (cold) clear threshold value, at/below which ALRTAUXOV alerts will be cleared/deasserted. This threshold is applied for Auxiliary measurements where AUXREFSELn = 0 (ratiometric). ***Note:*** *For proper operation, this value should always be less than or equal to AUXROVTHSET.*

AUXROVTHSETREG (0x31)

AUXROVTHSET is a read- and write-accessible register that selects the overvoltage (cold) alert set threshold used with ratiometric auxiliary ADC measurements.

BIT	15	14	13	12	11	10	9	8
Field	AUXROVTHSET[13:6]							
Reset	0x3FFF							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	AUXROVTHSET[5:0]						–	–
Reset	0x3FFF						–	–
Access Type	Write, Read						–	–

BITFIELD	BITS	DESCRIPTION
AUXROVTHSET	15:2	Ratiometric Auxiliary Overvoltage (Cold) Alert Set Threshold 14-bit overvoltage (cold) set threshold value, above which ALRTAUXOV alerts will be asserted. This threshold is applied for Auxiliary measurements where AUXREFSELn = 0 (ratiometric). A value of 0x3FFF effectively disables overvoltage checking.

AUXRUVTHCLRREG (0x32)

AUXRUVTHCLR is a read- and write-accessible register that selects the undervoltage (hot) alert clear threshold used with ratiometric auxiliary ADC measurements.

BIT	15	14	13	12	11	10	9	8
Field	AUXRUVTHCLR[13:6]							
Reset	0x0000							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	AUXRUVTHCLR[5:0]						–	–
Reset	0x0000						–	–
Access Type	Write, Read						–	–

BITFIELD	BITS	DESCRIPTION
AUXRUVTHCLR	15:2	Ratiometric Auxiliary Undervoltage (Hot) Alert Clear Threshold 14-bit undervoltage (hot) clear threshold value, at/above which ALRTAUXUV alerts will be cleared/deasserted. This threshold is applied for Auxiliary measurements where AUXREFSELn = 0 (ratiometric). ***Note:*** *For proper operation, this value should always be greater than or equal to AUXRUVTHSET.*

AUXRUVTHSETREG (0x33)

AUXRUVTHSET is a read- and write-accessible register that selects the undervoltage (hot) alert set threshold used with ratiometric auxiliary ADC measurements.

BIT	15	14	13	12	11	10	9	8
Field	AUXRUVTHSET[13:6]							
Reset	0x0000							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	AUXRUVTHSET[5:0]						–	–
Reset	0x0000						–	–
Access Type	Write, Read						–	–

BITFIELD	BITS	DESCRIPTION
AUXRUVTHSET	15:2	Ratiometric Auxiliary Undervoltage (Hot) Alert Set Threshold 14-bit undervoltage (hot) set threshold value, below which ALRTAUXUV alerts will be asserted. This threshold is applied for Auxiliary measurements where AUXREFSELn = 0 (ratiometric). A value of 0x0000 effectively disables undervoltage checking.

AUXAOVTHCLRREG (0x34)

AUXOVTHCLR is a read- and write-accessible register that selects the overvoltage alert clear threshold used with absolute auxiliary ADC measurements.

BIT	15	14	13	12	11	10	9	8
Field	AUXAOVTHCLR[13:6]							
Reset	0x3FFF							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	AUXAOVTHCLR[5:0]						–	–
Reset	0x3FFF						–	–
Access Type	Write, Read						–	–

BITFIELD	BITS	DESCRIPTION
AUXAOVTHCLR	15:2	Absolute Auxiliary Overvoltage Alert Clear Threshold 14-bit overvoltage clear threshold value, at/below which ALRTAUXOV alerts will be cleared/deasserted. This threshold is applied for Auxiliary measurements where AUXREFSELn = 1 (absolute). ***Note:*** *For proper operation, this value should always be less than or equal to AUXAOVTHSET.*

AUXAOVTHSETREG (0x35)

AUXAOVTHSET is a read- and write-accessible register that selects the overvoltage alert set threshold used with absolute auxiliary ADC measurements.

BIT	15	14	13	12	11	10	9	8
Field	AUXAOVTHSET[13:6]							
Reset	0x3FFF							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	AUXAOVTHSET[5:0]						–	–
Reset	0x3FFF						–	–
Access Type	Write, Read						–	–

BITFIELD	BITS	DESCRIPTION
AUXAOVTHSET	15:2	Auxiliary Overvoltage Alert Set Threshold 14-bit overvoltage set threshold value, above which ALRTAUXOV alerts will be asserted. This threshold is applied for Auxiliary measurements where AUXREFSELn = 1 (absolute). A value of 0x3FFF effectively disables overvoltage checking.

AUXAUVTHCLRREG (0x36)

AUXAUVTHCLR is a read- and write-accessible register that selects the undervoltage alert clear threshold used with absolute auxiliary ADC measurements.

BIT	15	14	13	12	11	10	9	8
Field	AUXAUVTHCLR[13:6]							
Reset	0x0000							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	AUXAUVTHCLR[5:0]						–	–
Reset	0x0000						–	–
Access Type	Write, Read						–	–

BITFIELD	BITS	DESCRIPTION
AUXAUVTHCLR	15:2	Absolute Auxiliary Undervoltage Alert Clear Threshold 14-bit undervoltage clear threshold value, at/above which ALRTAUXUV alerts will be cleared/deasserted. This threshold is applied for Auxiliary measurements where AUXREFSELn = 1 (absolute). ***Note:*** *For proper operation, this value should always be greater than or equal to AUXAUVTHSET.*

AUXAUVTHSETREG (0x37)

AUXAUVTHSET is a read- and write-accessible register that selects the undervoltage alert set threshold used with absolute auxiliary ADC measurements.

BIT	15	14	13	12	11	10	9	8
Field	AUXAUVTHSET[13:6]							
Reset	0x0000							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	AUXAUVTHSET[5:0]						–	–
Reset	0x0000						–	–
Access Type	Write, Read						–	–

BITFIELD	BITS	DESCRIPTION
AUXAUVTHSET	15:2	Absolute Auxiliary Undervoltage Alert Set Threshold 14-bit undervoltage set threshold value, below which ALRTAUXUV alerts will be asserted. This threshold is applied for Auxiliary measurements where AUXREFSELn = 1 (absolute). A value of 0x0000 effectively disables undervoltage checking.

COMPOVTHREG (0x38)

COMPOVTH is a read- and write-accessible register that selects the cell overvoltage alert threshold for the redundant comparator.

BIT	15	14	13	12	11	10	9	8
Field	COMPOVTH[11:4]							
Reset	0xFFF							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	COMPOVTH[3:0]				–	–	–	–
Reset	0xFFF				–	–	–	–
Access Type	Write, Read				–	–	–	–

BITFIELD	BITS	DESCRIPTION
COMPOVTH	15:4	Comparator Cell Overvoltage Alert Threshold 12-bit threshold value of a 5V input range above which ALRTCOMPOV alerts will be set/asserted by comparator scans. A value of 0xFFF effectively disables overvoltage checking. ***Note:*** *For proper operation, this value should always be greater than or equal to COMPUVTH.*

COMPUVTHREG (0x39)

COMPUVTH is a read- and write-accessible register that selects the cell undervoltage alert threshold for the redundant comparator.

BIT	15	14	13	12	11	10	9	8
Field	COMPUVTH[11:4]							
Reset	0x000							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	COMPUVTH[3:0]				–	–	–	–
Reset	0x000				–	–	–	–
Access Type	Write, Read				–	–	–	–

BITFIELD	BITS	DESCRIPTION
COMPUVTH	15:4	Comparator Cell Undervoltage Alert Threshold 12-bit threshold value of a 5V input range below which ALRTCOMPUV alerts will be set/asserted by comparator scans. A value of 0x000 effectively disables undervoltage checking. ***Note:*** *For proper operation, this value should always be less than or equal to COMPOVTH.*

COMPAUXROVTHREG (0x3A)

COMPAUXROVTH is a read- and write-accessible register that selects the overvoltage (cold) alert threshold applied during ratiometric auxiliary comparator measurements.

BIT	15	14	13	12	11	10	9	8
Field	COMPAUXROVTH[11:4]							
Reset	0xFFF							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	COMPAUXROVTH[3:0]				–	–	–	–
Reset	0xFFF				–	–	–	–
Access Type	Write, Read				–	–	–	–

BITFIELD	BITS	DESCRIPTION
COMPAUXROVTH	15:4	Comparator Ratiometric Auxiliary Overvoltage (Cold) Alert Threshold 12-bit overvoltage (cold) threshold value of a input range of V_{AA} above which ALRTCOMPAUXOV alerts will be set/asserted by comparator scans. This threshold is applied for auxiliary measurements where AUXREFSELn = 0 (ratiometric). A value of 0xFFF effectively disables overvoltage checking. ***Note:*** *For proper operation, this value should always be greater than or equal to COMPAUXRUVTH.*

COMPAUXRUVTHREG (0x3B)

COMPAUXRUVTH is a read- and write-accessible register that selects the undervoltage (hot) alert threshold applied during ratiometric auxiliary comparator measurements.

BIT	15	14	13	12	11	10	9	8
Field	COMPAUXRUVTH[11:4]							
Reset	0x000							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	COMPAUXRUVTH[3:0]				–	–	–	–
Reset	0x000				–	–	–	–
Access Type	Write, Read				–	–	–	–

BITFIELD	BITS	DESCRIPTION
COMPAUXRUVTH	15:4	Comparator Ratiometric Auxiliary Undervoltage (Hot) Alert Threshold 12-bit undervoltage (hot) threshold value of a input range of V_{AA} below which ALRTCOMPAUXUV alerts will be set/asserted by comparator scans. This threshold is applied for auxiliary measurements where AUXREFSELn = 0 (ratiometric). A value of 0x000 effectively disables undervoltage checking. ***Note:*** *For proper operation, this value should always be less than or equal to COMPAUXROVTH.*

COMPAUXAOVTHREG (0x3C)

COMPAUXAOVTH is a read- and write-accessible register that selects the overvoltage alert threshold applied during absolute auxiliary comparator measurements.

BIT	15	14	13	12	11	10	9	8
Field	COMPAUXAOVTH[11:4]							
Reset	0xFFF							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	COMPAUXAOVTH[3:0]				–	–	–	–
Reset	0xFFF				–	–	–	–
Access Type	Write, Read				–	–	–	–

BITFIELD	BITS	DESCRIPTION
COMPAUXAOVTH	15:4	Comparator Absolute Auxiliary Overvoltage Alert Threshold 12-bit overvoltage threshold value of an input range of V_{REF} above which ALRTCOMPAUXOV alerts will be set/asserted by comparator scans. This threshold is applied for auxiliary measurements where AUXREFSELn = 1 (absolute). A value of 0xFFF effectively disables overvoltage checking. ***Note:*** *For normal operation, this value should always be greater than or equal to COMPAUXAUVTH.*

COMPAUXAUVTHREG (0x3D)

COMPAUXAUVTH is a read- and write-accessible register that selects the undervoltage alert threshold applied during absolute auxiliary comparator measurements.

BIT	15	14	13	12	11	10	9	8
Field	COMPAUXAUVTH[11:4]							
Reset	0x000							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	COMPAUXAUVTH[3:0]				–	–	–	–
Reset	0x000				–	–	–	–
Access Type	Write, Read				–	–	–	–

BITFIELD	BITS	DESCRIPTION
COMPAUXAUVTH	15:4	Comparator Absolute Auxiliary Undervoltage Alert Threshold 12-bit undervoltage threshold value of an input range of V_{REF} below which ALRTCOMPAUXUV alerts will be set/asserted by comparator scans. This threshold is applied for auxiliary measurements where AUXREFSELn = 1 (absolute). A value of 0x000 effectively disables undervoltage checking. ***Note:*** *For proper operation, this value should always be less than or equal to COMPAUXAOVTH.*

COMPOPNTHREG (0x3E)

COMPOPNTH is a read- and write-accessible register that selects the undervoltage alert threshold applied to unipolar cell inputs in Open Diagnostic mode.

BIT	15	14	13	12	11	10	9	8
Field	COMPOPNTH[11:4]							
Reset	0x000							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	COMPOPNTH[3:0]				–	–	–	–
Reset	0x000				–	–	–	–
Access Type	Write, Read				–	–	–	–

BITFIELD	BITS	DESCRIPTION
COMPOPNTH	15:4	Comparator Cell Open Undervoltage Alert Threshold 12-bit threshold of a 5V input range below which ALRTCOMPUV alerts will be set/asserted by comparator scans performed on unipolar cell inputs in Open Diagnostic mode (see CTSTCFG:CELLOPNDIAGSEL). A value of 0x000 effectively disables open undervoltage checking.

COMPAUXROPNTHREG (0x3F)

COMPAUXROPNTH is a read- and write-accessible register that selects the undervoltage alert threshold applied to ratiometric auxiliary inputs in Open Diagnostic mode.

BIT	15	14	13	12	11	10	9	8
Field	COMPAUXROPNTH[11:4]							
Reset	0x000							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	COMPAUXROPNTH[3:0]				–	–	–	–
Reset	0x000				–	–	–	–
Access Type	Write, Read				–	–	–	–

BITFIELD	BITS	DESCRIPTION
COMPAUXROPNTH	15:4	Comparator Ratiometric Auxiliary Open Undervoltage Alert Threshold 12-bit undervoltage threshold value of an input range of V_{AA} below which ALRTCOMPAUXUV alerts will be set/asserted by comparator scans performed on ratiometric auxiliary inputs in Open Diagnostic mode (see DIAGGENCFG:AUXDIAGSEL). This threshold is applied for auxiliary measurements where AUXREFSELn = 0 (ratiometric). A value of 0x000 effectively disables undervoltage checking.

COMPAUXAOPNTHREG (0x40)

COMPAUXAOPNTH is a read- and write-accessible register that selects the undervoltage alert threshold applied to absolute auxiliary inputs in Open Diagnostic Mode.

BIT	15	14	13	12	11	10	9	8
Field	COMPAUXAOPNTH[11:4]							
Reset	0x000							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	COMPAUXAOPNTH[3:0]				–	–	–	–
Reset	0x000				–	–	–	–
Access Type	Write, Read				–	–	–	–

BITFIELD	BITS	DESCRIPTION
COMPAUXAOPNTH	15:4	Comparator Absolute Auxiliary Open Undervoltage Alert Threshold 12-bit undervoltage threshold value of an input range of V_{REF} below which ALRTCOMPAUXUV alerts will be set/asserted by comparator scans performed on absolute auxiliary inputs in Open Diagnostic Mode (see DIAGGENCFG:AUXDIAGSEL). This threshold is applied for auxiliary measurements where AUXREFSELn = 1 (absolute). A value of 0x000 effectively disables undervoltage checking.

COMPACCOVTHREG (0x41)

COMPACCOVTH is a read- and write-accessible register that selects the overvoltage alert threshold applied during comparator accuracy diagnostics.

BIT	15	14	13	12	11	10	9	8
Field	COMPACCOVTH[11:4]							
Reset	0xFFF							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	COMPACCOVTH[3:0]				–	–	–	–
Reset	0xFFF				–	–	–	–
Access Type	Write, Read				–	–	–	–

BITFIELD	BITS	DESCRIPTION
COMPACCOVTH	15:4	End-of-Sequence Comparator Accuracy Diagnostic Overvoltage Alert Threshold 12-bit overvoltage threshold value of a 5V input range used to validate the accuracy of the comparator at the end of any measurement sequence using the comparator, if enabled (SCANCFG = 001 or 010 and COMPACCEN = 1). Tested for the Cell Signal Path with $COMP_{IN}$ = V_{REF} through LSA2 (gain = 1/4) and DAC_{REF} = V_{REF}. A value above COMPACCOVTH will result in the ALRTCOMPACCOV bit being set/asserted. 0x3FF is the ideal value. A precise value can be selected based on information from the Comparator Cell Signal Path Fault diagnostic. A value of 0xFFF effectively disables overvoltage checking (default).

COMPACCUVTHREG (0x42)

COMPACCUVTH is a read- and write-accessible register that selects the undervoltage alert threshold applied during comparator accuracy diagnostics.

BIT	15	14	13	12	11	10	9	8
Field	COMPACCUVTH[11:4]							
Reset	0x000							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	COMPACCUVTH[3:0]				–	–	–	–
Reset	0x000				–	–	–	–
Access Type	Write, Read				–	–	–	–

BITFIELD	BITS	DESCRIPTION
COMPACCUVTH	15:4	End-of-Sequence Comparator Accuracy Diagnostic Undervoltage Alert Threshold 12-bit undervoltage threshold value of a 5V input range used to validate the accuracy of the comparator at the end of any measurement sequence using the comparator, if enabled (SCANCFG = 001 or 010, and COMPACCEN = 1). Tested for the cell signal path with $COMP_{IN}$ = V_{REF} through LSA2 (gain = 1/4) and DAC_{REF} = V_{REF}. A value below COMPACCUVTH will result in the ALRTCOMPACCUV bit being set/asserted. 0x3FF is the ideal value. A precise value can be selected based on information from the Comparator Cell Signal Path Fault diagnostic. A value of 0x000 effectively disables undervoltage checking (default).

BALSHRTTHRREG (0x43)

BALSHRTTHR is a read- and write-accessible register that selects alert threshold used during the Balance Switch Short Diagnostic mode.

BIT	15	14	13	12	11	10	9	8
Field	BALSHRTTHR[13:6]							
Reset	0x0000							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	BALSHRTTHR[5:0]						–	–
Reset	0x0000						–	–
Access Type	Write, Read						–	–

BITFIELD	BITS	DESCRIPTION
BALSHRTTHR	15:2	Balance Switch Short Diagnostic Alert Threshold 14-bit undervoltage threshold used for the balancing switch short-circuit diagnostic test (SCANCFG = 100). Unipolar format. For BALSW Short Diagnostics, only cells with (POLARITYn = 0 and CELLENn = 1) are measured and checked. The unipolar ADC cell voltage results taken in this mode are compared against the threshold; if any result is below the threshold, it is flagged as a balancing switch alert (ALRTBALSW). Results above the threshold are considered normal. The threshold should be set by the system controller prior to making a diagnostic measurement.

BALLOWTHRREG (0x44)

BALLOWTHR is a read- and write-accessible register that selects alert low threshold used during the Balance Switch Open Diagnostic mode.

BIT	15	14	13	12	11	10	9	8
Field	BALLOWTHR[13:6]							
Reset	0x0000							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	BALLOWTHR[5:0]						–	–
Reset	0x0000						–	–
Access Type	Write, Read						–	–

BITFIELD	BITS	DESCRIPTION
BALLOWTHR	15:2	Balance Switch Open Diagnostic Alert Low Threshold 14-bit undervoltage threshold used for the balancing switch conducting and cell sense wire diagnostic tests (SCANCFG = 101, 110, and 111). Bipolar format, typically a small positive value is selected. For BALSW Open Diagnostics, only cells with (POLARITYn = 0 and BALSWENn = 1) are measured and checked. For Cell Sense Open Odd/Even Diagnostics, only odd/even cells at/below TOPCELL1/2 with POLARITYn = 0 and are measured and checked. The bipolar ADC cell results in this mode are compared against the threshold; if any result is below the threshold, it is flagged as a balancing switch alert (ALRTBALSW). Results above the threshold are considered normal. The threshold should be set by the system controller prior to making a diagnostic measurement.

BALHIGHTHRREG (0x45)

BALHIGHTHR is a read- and write-accessible register that selects alert high threshold used during the Balance Switch Open Diagnostic mode.

BIT	15	14	13	12	11	10	9	8
Field	BALHIGHTHR[13:6]							
Reset	0x0000							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	BALHIGHTHR[5:0]						–	–
Reset	0x0000						–	–
Access Type	Write, Read						–	–

BITFIELD	BITS	DESCRIPTION
BALHIGHTHR	15:2	Balance Switch Open Diagnostic Alert High Threshold 14-bit overvoltage threshold used for the balancing switch conducting and cell sense wire diagnostic tests (SCANCFG = 101, 110, 111). Bipolar format, typically a moderate positive value, is selected based on external resistor characteristics. For BALSW Open Diagnostics, only cells with (POLARITYn = 0 and BALSWENn = 1) are measured and checked. For Cell Sense Open Odd/Even Diagnostics, only odd/even cells at/below TOPCELL1/2 with POLARITYn = 0 and are measured and checked. The bipolar ADC cell results in this mode are compared against the threshold; if any result is above the threshold, it is flagged as a balancing switch alert (ALRTBALSW). Results below the threshold are considered normal. The threshold should be set by the system controller prior to making a diagnostic measurement.

CELL1REG (0x47)

CELLn is a read-accessible register that holds the current value for each individual cell measurement result.

BIT	15	14	13	12	11	10	9	8
Field	CELL1[13:6]							
Reset	0x0000							
Access Type	Read Only							

BIT	7	6	5	4	3	2	1	0
Field	CELL1[5:0]						–	–
Reset	0x0000						–	–
Access Type	Read Only						–	–

BITFIELD	BITS	DESCRIPTION
CELL1	15:2	Cell Voltage Measurement Result CELLn[13:0] contains the 14-bit measurement result for CELLn. Full-scale input range of 5V. If CELLEN = 0 and the measurement was skipped during the latest ADC scan, no internal data is updated and ALU/IIR readback will be determined by RDFILT. Read only.

CELL2REG (0x48)

CELLn is a read-accessible register that holds the current value for each individual cell measurement result.

BIT	15	14	13	12	11	10	9	8
Field	CELL2[13:6]							
Reset	0x0000							
Access Type	Read Only							

BIT	7	6	5	4	3	2	1	0
Field	CELL2[5:0]						–	–
Reset	0x0000						–	–
Access Type	Read Only						–	–

BITFIELD	BITS	DESCRIPTION
CELL2	15:2	Cell Voltage Measurement Result CELLn[13:0] contains the 14-bit measurement result for CELLn. Full-scale input range of 5V. If CELLEN = 0 and the measurement was skipped during the latest ADC scan, no internal data is updated and ALU/IIR readback will be determined by RDFILT. Read only.

CELL3REG (0x49)

CELLn is a read-accessible register that holds the current value for each individual cell measurement result.

BIT	15	14	13	12	11	10	9	8
Field	CELL3[13:6]							
Reset	0x0000							
Access Type	Read Only							

BIT	7	6	5	4	3	2	1	0
Field	CELL3[5:0]						–	–
Reset	0x0000						–	–
Access Type	Read Only						–	–

BITFIELD	BITS	DESCRIPTION
CELL3	15:2	Cell Voltage Measurement Result CELLn[13:0] contains the 14-bit measurement result for CELLn. Full-scale input range of 5V. If CELLEN = 0 and the measurement was skipped during the latest ADC scan, no internal data is updated and ALU/IIR readback will be determined by RDFILT. Read only.

CELL4REG (0x4A)

CELLn is a read-accessible register that holds the current value for each individual cell measurement result.

BIT	15	14	13	12	11	10	9	8
Field	CELL4[13:6]							
Reset	0x0000							
Access Type	Read Only							

BIT	7	6	5	4	3	2	1	0
Field	CELL4[5:0]						–	–
Reset	0x0000						–	–
Access Type	Read Only						–	–

BITFIELD	BITS	DESCRIPTION
CELL4	15:2	Cell Voltage Measurement Result CELLn[13:0] contains the 14-bit measurement result for CELLn. Full scale input range of 5V. If CELLEN = 0 and the measurement was skipped during the latest ADC scan, no internal data is updated and ALU/IIR readback will be determined by RDFILT. Read only.

CELL5REG (0x4B)

CELLn is a read-accessible register that holds the current value for each individual cell measurement result.

BIT	15	14	13	12	11	10	9	8
Field	CELL5[13:6]							
Reset	0x0000							
Access Type	Read Only							

BIT	7	6	5	4	3	2	1	0
Field	CELL5[5:0]						–	–
Reset	0x0000						–	–
Access Type	Read Only						–	–

BITFIELD	BITS	DESCRIPTION
CELL5	15:2	Cell Voltage Measurement Result CELLn[13:0] contains the 14-bit measurement result for CELLn. Full-scale input range of 5V. If CELLEN = 0 and the measurement was skipped during the latest ADC scan, no internal data is updated and ALU/IIR readback will be determined by RDFILT. Read only.

CELL6REG (0x4C)

CELLn is a read-accessible register that holds the current value for each individual cell measurement result.

BIT	15	14	13	12	11	10	9	8
Field	CELL6[13:6]							
Reset	0x0000							
Access Type	Read Only							

BIT	7	6	5	4	3	2	1	0
Field	CELL6[5:0]						–	–
Reset	0x0000						–	–
Access Type	Read Only						–	–

BITFIELD	BITS	DESCRIPTION
CELL6	15:2	Cell Voltage Measurement Result CELLn[13:0] contains the 14-bit measurement result for CELLn. Full-scale input range of 5V. If CELLEN = 0 and the measurement was skipped during the latest ADC scan, no internal data is updated and ALU/IIR readback will be determined by RDFILT. Read only.

CELL7REG (0x4D)

CELLn is a read-accessible register that holds the current value for each individual cell measurement result.

BIT	15	14	13	12	11	10	9	8
Field	CELL7[13:6]							
Reset	0x0000							
Access Type	Read Only							

BIT	7	6	5	4	3	2	1	0
Field	CELL7[5:0]						–	–
Reset	0x0000						–	–
Access Type	Read Only						–	–

BITFIELD	BITS	DESCRIPTION
CELL7	15:2	Cell Voltage Measurement Result CELLn[13:0] contains the 14-bit measurement result for CELLn. Full-scale input range of 5V. If CELLEN = 0 and the measurement was skipped during the latest ADC scan, no internal data is updated and ALU/IIR readback will be determined by RDFILT. Read only.

CELL8REG (0x4E)

CELLn is a read-accessible register that holds the current value for each individual cell measurement result.

BIT	15	14	13	12	11	10	9	8
Field	CELL8[13:6]							
Reset	0x0000							
Access Type	Read Only							

BIT	7	6	5	4	3	2	1	0
Field	CELL8[5:0]						–	–
Reset	0x0000						–	–
Access Type	Read Only						–	–

BITFIELD	BITS	DESCRIPTION
CELL8	15:2	Cell Voltage Measurement Result CELLn[13:0] contains the 14-bit measurement result for CELLn. Full-scale input range of 5V. If CELLEN = 0 and the measurement was skipped during the latest ADC scan, no internal data is updated and ALU/IIR readback will be determined by RDFILT. Read only.

CELL9REG (0x4F)

CELLn is a read-accessible register that holds the current value for each individual cell measurement result.

BIT	15	14	13	12	11	10	9	8
Field	CELL9[13:6]							
Reset	0x0000							
Access Type	Read Only							

BIT	7	6	5	4	3	2	1	0
Field	CELL9[5:0]						–	–
Reset	0x0000						–	–
Access Type	Read Only						–	–

BITFIELD	BITS	DESCRIPTION
CELL9	15:2	Cell Voltage Measurement Result CELLn[13:0] contains the 14-bit measurement result for CELLn. Full-scale input range of 5V. If CELLEN = 0 and the measurement was skipped during the latest ADC scan, no internal data is updated and ALU/IIR readback will be determined by RDFILT. Read only.

CELL10REG (0x50)

CELLn is a read-accessible register that holds the current value for each individual cell measurement result.

BIT	15	14	13	12	11	10	9	8
Field	CELL10[13:6]							
Reset	0x0000							
Access Type	Read Only							

BIT	7	6	5	4	3	2	1	0
Field	CELL10[5:0]						–	–
Reset	0x0000						–	–
Access Type	Read Only						–	–

BITFIELD	BITS	DESCRIPTION
CELL10	15:2	Cell Voltage Measurement Result CELLn[13:0] contains the 14-bit measurement result for CELLn. Full-scale input range of 5V. If CELLEN = 0 and the measurement was skipped during the latest ADC scan, no internal data is updated and ALU/IIR readback will be determined by RDFILT. Read only.

CELL11REG (0x51)

CELLn is a read-accessible register that holds the current value for each individual cell measurement result.

BIT	15	14	13	12	11	10	9	8
Field	CELL11[13:6]							
Reset	0x0000							
Access Type	Read Only							

BIT	7	6	5	4	3	2	1	0
Field	CELL11[5:0]						–	–
Reset	0x0000						–	–
Access Type	Read Only						–	–

BITFIELD	BITS	DESCRIPTION
CELL11	15:2	Cell Voltage Measurement Result CELLn[13:0] contains the 14-bit measurement result for CELLn. Full-scale input range of 5V. If CELLEN = 0 and the measurement was skipped during the latest ADC scan, no internal data is updated and ALU/IIR readback will be determined by RDFILT. Read only.

CELL12REG (0x52)

CELLn is a read-accessible register that holds the current value for each individual cell measurement result.

BIT	15	14	13	12	11	10	9	8
Field	CELL12[13:6]							
Reset	0x0000							
Access Type	Read Only							

BIT	7	6	5	4	3	2	1	0
Field	CELL12[5:0]						–	–
Reset	0x0000						–	–
Access Type	Read Only						–	–

BITFIELD	BITS	DESCRIPTION
CELL12	15:2	Cell Voltage Measurement Result CELLn[13:0] contains the 14-bit measurement result for CELLn. Full-scale input range of 5V. If CELLEN = 0 and the measurement was skipped during the latest ADC scan, no internal data is updated and ALU/IIR readback will be determined by RDFILT. Read only.

CELL13REG (0x53)

CELLn is a read-accessible register that holds the current value for each individual cell measurement result.

BIT	15	14	13	12	11	10	9	8
Field	CELL13[13:6]							
Reset	0x0000							
Access Type	Read Only							

BIT	7	6	5	4	3	2	1	0
Field	CELL13[5:0]						–	–
Reset	0x0000						–	–
Access Type	Read Only						–	–

BITFIELD	BITS	DESCRIPTION
CELL13	15:2	Cell Voltage Measurement Result CELLn[13:0] contains the 14-bit measurement result for CELLn. Full-scale input range of 5V. If CELLEN = 0 and the measurement was skipped during the latest ADC scan, no internal data is updated and ALU/IIR readback will be determined by RDFILT. Read only.

CELL14REG (0x54)

CELLn is a read-accessible register that holds the current value for each individual cell measurement result.

BIT	15	14	13	12	11	10	9	8
Field	CELL14[13:6]							
Reset	0x0000							
Access Type	Read Only							

BIT	7	6	5	4	3	2	1	0
Field	CELL14[5:0]						–	–
Reset	0x0000						–	–
Access Type	Read Only						–	–

BITFIELD	BITS	DESCRIPTION
CELL14	15:2	Cell Voltage Measurement Result CELLn[13:0] contains the 14-bit measurement result for CELLn. Full-scale input range of 5V. If CELLEN = 0 and the measurement was skipped during the latest ADC scan, no internal data is updated and ALU/IIR readback will be determined by RDFILT. Read only.

BLOCKREG (0x55)

BLOCK is a read-accessible register that holds the current value for the total block measurement result.

BIT	15	14	13	12	11	10	9	8
Field	VBLOCK[13:6]							
Reset	0x0000							
Access Type	Read Only							

BIT	7	6	5	4	3	2	1	0
Field	VBLOCK[5:0]						–	–
Reset	0x0000						–	–
Access Type	Read Only						–	–

BITFIELD	BITS	DESCRIPTION
VBLOCK	15:2	Block Voltage Measurement Result VBLOCK[13:0] contains the 14-bit measurement result for VBLK. Full-scale input range of 65V. If BLOCKEN = 0 and the measurement was skipped during the latest ADC scan, no internal data is updated and ALU/IIR readback will be determined by RDFILT. Read only.

TOTALREG (0x56)

TOTAL is a read-accessible register that holds the current value for the sum of all enabled measurement results within the stack.

BIT	15	14	13	12	11	10	9	8
Field	TOTAL[15:8]							
Reset	0x0000							
Access Type	Read Only							

BIT	7	6	5	4	3	2	1	0
Field	TOTAL[7:0]							
Reset	0x0000							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
TOTAL	15:0	Total Cell Voltage Measurement Result TOTAL[15:0] contains the 16-bit sum of all cell measurement results enabled during the last scan by MEASUREEN1. Full-scale range is 0.0 to 80.0V with a 1.22mV LSB (unipolar). Read only. *Note the following behavior:* *Since disabled measurements retain their last results, it is possible there will be data in the result registers that was not included in the TOTAL result calculated for the last scan.* *If cell and bus bar (unipolar and bipolar) measurements are mixed within a scan, the summation will be handled accordingly.* *Totals below 0V cannot be supported and will be clipped at 0x0000 (this may apply to scans using only bipolar measurements).*

DIAG1REG (0x57)

DIAG1 is a read-only register that contains the diagnostic result requested by the DIAGCFG:DIAGSEL1 selection taken during the last ADC acquisition.

BIT	15	14	13	12	11	10	9	8
Field	DIAG1[13:6]							
Reset	0x0000							
Access Type	Read Only							

BIT	7	6	5	4	3	2	1	0
Field	DIAG1[5:0]						–	–
Reset	0x0000						–	–
Access Type	Read Only						–	–

BITFIELD	BITS	DESCRIPTION
DIAG1	15:2	DIAG1 contains the 14-bit measurement result for the diagnostic selected by DIAGCFG:DIAGSEL1.

DIAG2REG (0x58)

DIAG2 is a read-only register that contains the diagnostic result requested by the DIAGCFG:DIAGSEL2 selection taken during the last ADC acquisition.

BIT	15	14	13	12	11	10	9	8
Field	DIAG2[13:6]							
Reset	0x0000							
Access Type	Read Only							

BIT	7	6	5	4	3	2	1	0
Field	DIAG2[5:0]						–	–
Reset	0x0000						–	–
Access Type	Read Only						–	–

BITFIELD	BITS	DESCRIPTION
DIAG2	15:2	DIAG2 contains the 14-bit measurement result for the diagnostic selected by DIAGCFG:DIAGSEL2.

AUX0REG (0x59)

AUXn is a read-accessible register that holds the current value for each enabled individual auxiliary measurement result.

BIT	15	14	13	12	11	10	9	8
Field	AUX0[13:6]							
Reset	0x0000							
Access Type	Read Only							

BIT	7	6	5	4	3	2	1	0
Field	AUX0[5:0]						–	–
Reset	0x0000						–	–
Access Type	Read Only						–	–

BITFIELD	BITS	DESCRIPTION
AUX0	15:2	Auxiliary Voltage Measurement Result AUXn[13:0] contains the 14-bit measurement result for AUXn. Full-scale input range of V_{AA} for ratiometric operation, V_{REF} for absolute operation. If the port is not configured as an AUXINn input (see AUXGPIOCFG), the result will read back 0x0000 for the unused channel. Otherwise if AUXEN = 0 and the measurement was skipped during the latest ADC scan, the previously determined result will remain. Read only.

AUX1REG (0x5A)

AUXn is a read-accessible register that holds the current value for each enabled individual auxiliary measurement result.

BIT	15	14	13	12	11	10	9	8
Field	AUX1[13:6]							
Reset	0x0000							
Access Type	Read Only							

BIT	7	6	5	4	3	2	1	0
Field	AUX1[5:0]						–	–
Reset	0x0000						–	–
Access Type	Read Only						–	–

BITFIELD	BITS	DESCRIPTION
AUX1	15:2	Auxiliary Voltage Measurement Result AUXn[13:0] contains the 14-bit measurement result for AUXn. Full-scale input range of V_{AA} for ratiometric operation, V_{REF} for absolute operation. If the port is not configured as an AUXINn input (see AUXGPIOCFG), the result will read back 0x0000 for the unused channel. Otherwise if AUXEN = 0 and the measurement was skipped during the latest ADC scan, the previously determined result will remain. Read only.

AUX2REG (0x5B)

AUXn is a read-accessible register that holds the current value for each enabled individual auxiliary measurement result.

BIT	15	14	13	12	11	10	9	8
Field	AUX2[13:6]							
Reset	0x0000							
Access Type	Read Only							

BIT	7	6	5	4	3	2	1	0
Field	AUX2[5:0]						–	–
Reset	0x0000						–	–
Access Type	Read Only						–	–

BITFIELD	BITS	DESCRIPTION
AUX2	15:2	Auxiliary Voltage Measurement Result AUXn[13:0] contains the 14-bit measurement result for AUXn. Full-scale input range of V_{AA} for ratiometric operation, V_{REF} for absolute operation. If the port is not configured as an AUXINn input (see AUXGPIOCFG), the result will read back 0x0000 for the unused channel. Otherwise if AUXEN = 0 and the measurement was skipped during the latest ADC scan, the previously determined result will remain. Read only.

AUX3REG (0x5C)

AUXn is a read-accessible register that holds the current value for each enabled individual auxiliary measurement result.

BIT	15	14	13	12	11	10	9	8
Field	AUX3[13:6]							
Reset	0x0000							
Access Type	Read Only							

BIT	7	6	5	4	3	2	1	0
Field	AUX3[5:0]						–	–
Reset	0x0000						–	–
Access Type	Read Only						–	–

BITFIELD	BITS	DESCRIPTION
AUX3	15:2	Auxiliary Voltage Measurement Result AUXn[13:0] contains the 14-bit measurement result for AUXn. Full-scale input range of V_{AA} for ratiometric operation, V_{REF} for absolute operation. If the port is not configured as an AUXINn input (see AUXGPIOCFG), the result will read back 0x0000 for the unused channel. Otherwise if AUXEN = 0 and the measurement was skipped during the latest ADC scan, the previously determined result will remain. Read only.

AUX4REG (0x5D)

AUXn is a read-accessible register that holds the current value for each enabled individual auxiliary measurement result.

BIT	15	14	13	12	11	10	9	8
Field	AUX4[13:6]							
Reset	0x0000							
Access Type	Read Only							

BIT	7	6	5	4	3	2	1	0
Field	AUX4[5:0]						–	–
Reset	0x0000						–	–
Access Type	Read Only						–	–

BITFIELD	BITS	DESCRIPTION
AUX4	15:2	Auxiliary Voltage Measurement Result AUXn[13:0] contains the 14-bit measurement result for AUXn. Full-scale input range of V_{AA} for ratiometric operation, V_{REF} for absolute operation. If the port is not configured as an AUXINn input (see AUXGPIOCFG), the result will readback 0x0000 for the unused channel. Otherwise, if AUXEN = 0 and the measurement was skipped during the latest ADC scan, the previously determined result will remain. Read only.

AUX5REG (0x5E)

AUXn is a read-accessible register that holds the current value for each enabled individual auxiliary measurement result.

BIT	15	14	13	12	11	10	9	8
Field	AUX5[13:6]							
Reset	0x0000							
Access Type	Read Only							

BIT	7	6	5	4	3	2	1	0
Field	AUX5[5:0]						–	–
Reset	0x0000						–	–
Access Type	Read Only						–	–

BITFIELD	BITS	DESCRIPTION
AUX5	15:2	Auxiliary Voltage Measurement Result AUXn[13:0] contains the 14-bit measurement result for AUXn. Full-scale input range of V_{AA} for ratiometric operation, V_{REF} for absolute operation. If the port is not configured as an AUXINn input (see AUXGPIOCFG), the result will read back 0x0000 for the unused channel. Otherwise, if AUXEN = 0 and the measurement was skipped during the latest ADC scan, the previously determined result will remain. Read only.

POLARITYCTRL (0x5F)

POLARITYCTRL is a read- and write-accessible register that governs the measurement type used during scans. In general, unipolar mode indicates a cell, and bipolar mode indicates a bus bar.

BIT	15	14	13	12	11	10	9	8
Field	MINMAXPOL	–	POLARITY[14:9]					
Reset	0b0	–	0x0000					
Access Type	Write, Read	–	Write, Read					

BIT	7	6	5	4	3	2	1	0
Field	POLARITY[8:1]							
Reset	0x0000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
MINMAXPOL	15	MIN/MAX Operating Mode 0 = Only Unipolar Cell Measurements are Included in MINCELL, MAXCELL, and ALRTMSMTCH Calculations (default) 1 = Only Bipolar Cell Measurements are Included in MINCELL, MAXCELL, and ALRTMSMTCH Calculations (useful in fuel cell applications)

BITFIELD	BITS	DESCRIPTION
POLARITY	13:0	Cell Measurement Polarity Selection 0 = Unipolar 0 to 5V Input Range (default) 1 = Bipolar -2.5V to 2.5V Input Bipolar cells will be fault masked during BALSWDIAG ADC measurement scans. MINMAXPOL determines whether bipolar cells are included in MIN/MAXCELL and ALRTMSMTCH calculations. Bipolar cell measurements will be checked against BIPOVTH and BIPUVTH thresholds rather than OVTH and UVTH thresholds. Bipolar cells will not be included in comparator measurement scans: ALRTCOMPOV, ALRTCOMPUV, alerts will not be triggered.

AUXREFCTRL (0x60)

AUXREFCTRL is a read- and write-accessible register that governs the reference range used for enabled auxiliary channels during ADC and COMP acquisition sequences.

BIT	15	14	13	12	11	10	9	8
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–

BIT	7	6	5	4	3	2	1	0
Field	–	–	AUXREFSEL[5:4]		AUXREFSEL[3:0]			
Reset	–	–	0x0		0x0			
Access Type	–	–	Write, Read, Ext		Write, Read, Ext			

BITFIELD	BITS	DESCRIPTION
AUXREFSEL	5:4	Auxiliary Input Reference Selection 0 = Ratiometric, REF = V_{THRM} (default) 1 = Absolute, REF = V_{REF} = 1.25V This bit selects the reference used and which set of AUX OV, UV, and OPN thresholds are used during ADC and comparator acquisition sequences. ***Note:*** *If the respective GPIOEN bit is set (GPIO mode), this bit is ignored, but it will still read back the user setting.*
AUXREFSEL	3:0	Auxiliary Input Reference Selection 0 = Ratiometric, REF = V_{THRM} (default) 1 = Absolute, REF = V_{REF} = 1.25V This bit selects the reference used and which set of AUX OV, UV, and OPN thresholds are used during ADC and comparator acquisition sequences. ***Note:*** *If the I2CEN bit (Digital I^2C mode, applies to [1:0] only), or the respective GPIOEN bit is set (GPIO mode), this bit is ignored, but will still read back the user setting.*

AUXTIMEREG (0x61)

AUXTIMEREG is a read- and write-accessible register that governs the settling time allowed for biasing AUX/GPIO pins prior to measurements.

BIT	15	14	13	12	11	10	9	8
Field	–	–	–	–	–	–	AUXTIME[9:8]	
Reset	–	–	–	–	–	–	0x000	
Access Type	–	–	–	–	–	–	Write, Read	

BIT	7	6	5	4	3	2	1	0
Field	AUXTIME[7:0]							
Reset	0x000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
AUXTIME	9:0	AUX Preconversion Settling TIme Configures the preconversion settling time for all enabled AUXn inputs from 0µs (default) up to 6.138ms according to the equation: t_{Settle} = (AUXTIME[9:0]) * 6µs This is to allow extra settling time if the application circuit requires it, since the THRM voltage is not driven out until the start of the acquisition (in auto mode). This time is inserted at the beginning of each requested scan. If AUXTIME has not expired, but no other scan measurement is active, the HVCP will be refreshed during AUXTIME.

ACQCFG (0x62)

ACQCFG is a read- and write-accessible register that governs several aspects of the measurement and acquisition procedure.

BIT	15	14	13	12	11	10	9	8
Field	ADCZSFSEN	ADCCALEN	COMPACCEN	FOSR[1:0]		THRMMODE[1:0]		–
Reset	0b0	0b0	0b0	0b00		0b00		–
Access Type	Write, Read	Write, Read	Write, Read	Write, Read		Write, Read		–

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION
ADCZSFSEN	15	End-of-Sequence ADC Stuck-at-Fault Diagnostic Enable 0 = Disable ADC ZS/FS Diagnostics (default) 1 = Enable ADC ZS/FS Diagnostics If enabled, at the end of any measurement sequence using the ADC (SCANCFG != 010), the ADC will automatically be tested with overdriven inputs designed to force outputs to zero-scale and full-scale. Any result other than 0x000 or 0xFFF will be reported through ALRTADCZS and ALRTADCFS, respectively.

BITFIELD	BITS	DESCRIPTION
ADCCALEN	14	ADC Calibration Enable 0 = Calibration Not Applied to Scan Results 1 = Calibration Applied to Scan Results *Does not impact comparator operations.*
COMPACCEN	13	End-of-Sequence Comparator Accuracy Diagnostic Enable 0 = Disable COMPACC Diagnostics (default) 1 = Enable COMPACC Diagnostics If enabled, at the end of any measurement sequence using the comparator (SCANCFG = 001 or 010), the comparator will automatically be tested with $COMP_{IN} = V_{REF}$ through the LSA2 path (gain = 1/4) and $DAC_{REF} = V_{REF}$ against bracketing thresholds COMPACCOVTHR and COMPACCUVTHR. If an unexpected result is found, ALRTCOMPACCOV or ALRTCOMPACCUV will be issued.
FOSR	12:11	Oversampling Frequency Selection 00 = f_{OSR} = Frequency Determined by Selected Features 01 = f_{OSR} = 1.60kHz, Useful for 50Hz Rejection 1x = f_{OSR} = 1.92kHz, Useful for 60Hz Rejection For ADC and comparator scans, f_{OSR} sets a specific effective sampling frequency for use with oversampled acquisitions (OVSAMPL > 000). This can be used to place nulls at n x (f_{OSR}/OSR) to help reject noise at a given frequency. For example, with f_{OSR} = 1.60kHz and OSR = 32, noise at 50Hz and its harmonics can be attenuated. Selection of 00 results in an arbitrary but maximum effective sampling frequency determined solely by the number of channels and diagnostics selected for measurement, in addition to analog overhead operations (such as HVCP refresh). Worst case is estimated at 2.2kHz with all features enabled.
THRMMODE	10:9	Thermistor Bias Control Mode Controls application of V_{AA} to the THRM pin through the internal switch to bias external thermistors for measurement. 0x - Automatic Mode (Switch ON During Acquisition Mode) 10 - Manual Off Mode (Switch Always OFF) 11 - Manual On Mode (Switch Always ON)

BALSWDLY (0x63)

BALSWDLY is a read- and write-accessible register that selects the delay intervals used within Manual and Automated Cell-Balancing operations when ADC measurements are requested.

BIT	15	14	13	12	11	10	9	8
Field	CELLDLY[7:0]							
Reset	0x00							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	SWDLY[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
CELLDLY	15:8	Cell-Balancing Cell Path Recovery Delay Selection Time delay for C[n] (HVMUX) recovery from voltage drop during cell balancing prior to ADC measurement. Values of 0µs (default) to 24.480ms can be realized (96µs step size). This delay is used in Manual Cell-Balancing modes when using AUTOBALSWDIS = 1 and ALTMUXSEL = 0. Also used in Automatic Cell-Balancing and Discharge modes after each pair of even and odd discharge cycles when CBMEASEN = 1x and ALTMUXSEL = 0.
SWDLY	7:0	Cell-Balancing Switch Path Recovery Delay Selection Time delay for SW[n] (ALTMUX) recovery from voltage drop during cell balancing prior to ADC measurement. Values of 0µs (default) to 24.480ms can be realized (96µs step size). This delay is used in Manual Cell-Balancing modes when using AUTOBALSWDIS = 1 and ALTMUXSEL = 1. Also used in Automatic Cell-Balancing and Discharge modes after each pair of even and odd discharge cycles when CBMEASEN = 1x and ALTMUXSEL = 1.

MEASUREEN1 (0x64)

MEASUREEN1 is a read- and write-accessible register that governs the channels measured during ADC and COMP acquisition sequences.

BIT	15	14	13	12	11	10	9	8
Field	–	BLOCKEN	CELLEN[14:9]					
Reset	–	0b0	0x0000					
Access Type	–	Write, Read	Write, Read					

BIT	7	6	5	4	3	2	1	0
Field	CELLEN[8:1]							
Reset	0x0000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BLOCKEN	14	Block Voltage Measurement Enable 0 = Disable V_{BLK}/TOPBLOCK Measurement and Automatic Divider Connection (default) 1 = Enable V_{BLK}/TOPBLOCK Measurement and Automatic Divider Connection Applies to ADC scans only; block is not subject to comparator measurements. In addition to enabling the ADC measurement, BLOCKEN will automatically engage the V_{BLOCK} resistive divider for the duration of the scan. ***Note:*** *In flexible-pack applications (FLXPCKEN1/2 = 1), the resistive divider is connected to a selected Cn pin, and the resulting bias current will impact the Cn result. Therefore, in flexible-pack applications, it is generally recommended to set BLOCKEN = 1 only for scans with ALTMUXSEL = 1.*

BITFIELD	BITS	DESCRIPTION
CELLEN	13:0	Cell Voltage Measurement Enable 0 = Disable CELLn Measurement (default) 1 = Enable CELLn Measurement Enables measurement of the respective cell in Acquisition mode.

MEASUREEN2 (0x65)

MEASUREEN2 is a read- and write-accessible register that governs the auxiliary channels measured during ADC and COMP acquisition sequences, as well as IIR initialization.

BIT	15	14	13	12	11	10	9	8
Field	SCANIIRINIT	–	–	–	–	–	–	–
Reset	0b0	–	–	–	–	–	–	–
Access Type	Write, Read	–	–	–	–	–	–	–

BIT	7	6	5	4	3	2	1	0
Field	–	–	AUXEN[5:4]		AUXEN[3:0]			
Reset	–	–	0x0		0x0			
Access Type	–	–	Write, Read, Ext		Write, Read, Ext			

BITFIELD	BITS	DESCRIPTION
SCANIIRINIT	15	Sequencer IIR Initialization Request 0 = IIR Filter Continuation (default) 1 = IIR Filter Initialized In Continuation mode, the current value in the IIR accumulators is kept (presumably from previous cell measurements) and sequencer measurements are amended normally. In Initialization mode, the IIR accumulators will be reinitialized to the first measurement taken, and further cell-balancing measurements are amended normally.
AUXEN	5:4	Auxiliary Input Measurement Enable 0 = Auxiliary ADC Measurement Disabled (default) 1 = Auxiliary ADC Measurement Enabled Enables measurement of the respective auxiliary inputs in Acquisition mode. ***Note:*** *If the respective GPIOEN bit is set (GPIO mode), this bit is ignored, but will still read back the user setting.*
AUXEN	3:0	Auxiliary Input Measurement Enable 0 = Auxiliary ADC Measurement Disabled (default) 1 = Auxiliary ADC Measurement Enabled Enables measurement of the respective auxiliary inputs in Acquisition mode. ***Note:*** *If the I2CEN bit (Digital I^2C mode, applies to [1:0] only) or the respective GPIOEN bit is set (GPIO mode), this bit is ignored, but will still read back the user setting.*

SCANCTRL (0x66)

SCANCTRL is a read- and write-accessible register which governs the internal measurement acquisitions (scan) requested of the device. The register also manages the handling of data generated as a result of any scan request.

ADC scans are used for precision measurements of cell and auxiliary voltages.

COMP scans are used for periodic safety/redundancy checking of ADC results and, in some cases, enhanced communication efficiency.

On-Demand Calibration will run an internal calibration of the ADC and update the Calibration Data registers. All ADC measurements requested by Scan and Diagnostic Configuration and Control settings will be ignored.

Balance Switch and Cell Sense-Wire Open ADC Diagnostic scans are a special class of ADC scan. Use of these settings temporarily overrides other Scan and Diagnostic Configuration and Control settings. See the BALSW Diagnostics section for details.

BIT	15	14	13	12	11	10	9	8
Field	SCANDONE	SCANTIMEOUT	DATARDY	AUTOBALSWDIS	ALRTFILTSEL	AMENDFILT	RDFILT	SCANCFG[2]
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b000
Access Type	Write 0 to Clear, Read	Write 0 to Clear, Read	Write, Read, Ext	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BIT	7	6	5	4	3	2	1	0
Field	SCANCFG[1:0]		OVSAMPL[2:0]			ALTMUXSEL	SCANMODE	SCAN
Reset	0b000		0b000			0b0	0b0	0b0
Access Type	Write, Read		Write, Read			Write, Read	Write, Read	Write, Read, Pulse

BITFIELD	BITS	DESCRIPTION
SCANDONE	15	Acquisition Complete Indicator Bit 0 = Indicates an SCAN Acquisition is in Progress if Requested 1 = Indicates the SCAN Acquisition has Completed Once a SCAN acquisition is completed, the device will set this bit high to indicate completion. This bit is cleared by writing to 0. When this bit is high, further acquisitions requested using SCAN will be ignored. Writing to logic 1 has no internal effect.
SCANTIMEOUT	14	Scan Timeout Indicator Bit Indicates the acquisition did not complete in the expected period of time. The timeout threshold depends on the oversampling configuration. If a SCANTIMEOUT is issued, the resulting partial data should be treated as suspect and ignored. In applications using the IIR, SCANIIRINIT should be issued to avoid any corruption resulting from the timeout event. The acquisition watchdog can be disabled by setting SCANTODIS in the DEVCFG2 register. Cleared by writing to logic 0 to allow detection of future timeout events. Writing to logic 1 has no internal effect.

BITFIELD	BITS	DESCRIPTION
DATARDY	13	Data Ready Indicator Bit Indicates the measurement data from the acquisition has been transferred from the ALU to the data registers and may now be read. Data for all measurement registers and MIN/MAX/TOTAL is transferred at the same time. Cleared by writing to logic 0 to allow detection of the next data transfer. Writing to logic 1 has no internal effect.
AUTOBALSWDIS	12	Automatic Balancing Switch Disable 0 = Cell-Balancing Operations not Impacted by Measurement Sequences (default) 1 = Cell-Balancing Manual Operations Temporarily Disabled during Measurement Sequences Enables automatic suspension of active manual cell-balancing operations during measurement sequences. The delay for cell recovery settling time and for the diagnostic recovery is selected automatically based on the ALTMUXSEL setting for the sequence as follows: 0 = CELLDLY is used 1 = SWDLY is used
ALRTFILTSEL	11	Alert Filtering Selection 0 = Alert Issuance Based on Raw Sequencer Results (default) 1 = Alert Issuance Based on IIR Filter Results Determines whether the cell and block alerts are issued based on raw sequencer outputs (oversampling still applies) or IIR filtered outputs. If mode 1 is selected, MEASUREEN2:SCANIIRINIT should be used with the first scan to avoid triggering false alerts due to the IIR settling behavior. ***Note:*** *This bit is ignored for measurement scans taken in automated cell-balancing modes (ALRTFILTSEL = 1 is used).*
AMENDFILT	10	Amend IIR Filter Enable 0 = ADC result is not included in the IIR accumalator (default). 1 = ADC result is included in the IIR accumulator. When set high, for ADC outputs that have IIR filters/accumulators, the new ADC conversion in the ALU is automatically scaled and transferred into the IIR accumulator at the end of the sequence. This is most often used for normal measurement sequences. When set low, the new ADC conversion in the ALU is not transferred into the IIR accumulator at the end of the sequence. This is most often used for diagnostic measurement sequences where the ADC result would corrupt the settled normal data. ***Note:*** *This bit is ignored for measurement scans taken in automated cell-balancing modes (AMENDFILT = 1 is used).*
RDFILT	9	Read IIR Filter Selection 0 = Unfiltered ADC data is loaded into the output data registers (default). 1 = IIR Filtered ADC data is loaded into the output data registers. This bit chooses the source for data loaded to the cell and block registers for readback. The setting of this bit at the time of a measurement scan request (SCAN = 1) also determines the source data (filtered/unfiltered) used for TOTAL, MINCELL, MAXCELL, MSMTCH, and all OV/UV alert computations.

BITFIELD	BITS	DESCRIPTION
SCANCFG	8:6	Scan Configuration Selects the type of scan to be performed based on the selections below. FOSR selection applies to all scans where oversampling applies. 000 = ADC only Scan 001 = ADC + COMP Scan (Pyramid only) 010 = COMP only Scan (Pyramid only) 011 = On-Demand Calibration 100 = Balancing Switch Short 101 = Balancing Switch Open 110 = Cell Sense Open Odds 111 = Cell Sense Open Evens Some of these selections are formatted by other register content. Some of these selections will temporarily modify/override other register content. See the register descriptions for further details. For COMP scans, polarity is always defaulted to unipolar, any cell measurements requested in bipolar mode will be skipped. On-Demand Calibration executes an automated routine that will update the contents of the CALOSADC, CALOSR, CALOSTHRM, CALGAINP, and CALGAINR correction coefficients. No other measurements are taken during this operation. ***Note:*** *This bitfield is ignored for measurement scans taken in Automated Cell-Balancing modes (SCANCFG = 000 is used).*
OVSAMPL	5:3	Oversampling Selection for ADC Acquisitions 000 = Single Acquisition 001 = 4x Oversampling 010 = 8x Oversampling 011 = 16x Oversampling 100 = 32x Oversampling 101 = 64x Oversampling 11x = 128x Oversampling ***Note:*** *This bitfield is ignored during calibration (SCANCFG = 011) scans. This bitfield is ignored for measurement scans taken in Automated Cell-Balancing modes (OVSAMPL = 011 is used).*
ALTMUXSEL	2	Cell Measurement Path Selection 0 = HVMUX Signal Path (default) 1 = ALTMUX Signal Path See the Diagnostics section. ***Note:*** *Where ALTMUX settings disagree with SCANCFG (BALSWDIAG), SCANCFG takes precedence.*
SCANMODE	1	ADC Scan Mode Selection 0 = Pyramid Scan Mode (default) 1 = Ramp Scan Mode Ramp Scan mode is not supported for scans using the comparator or calibration scan requests - the setting will be ignored in these modes. ***Note:*** *This bit is ignored for measurement scans taken in Automated Cell-Balancing modes (SCANMODE = 0 is used).*

BITFIELD	BITS	DESCRIPTION
SCAN	0	Scan (Measurement Sequence) Request 0 - Used to initiate a data transfer and/or setup measurement conditions without initiating a measurement sequence 1 - Used to request a new measurement sequence (scan) and initiate a data transfer Acts as a strobe bit and therefore does not need to be cleared (self-clearing). Always reads logic 0. Writes to SCANCTRL with SCAN = 1 requesting new scans are ignored if a scan is already in progress, or if SCANDONE is high. In this case, the content written to SCANCTRL[15:1] will be accepted, but the conflicting scan will not be executed and ALRTRJCT will be issued, notifying the user of the conflict. ***Note:*** *The intended use of this bit is to enter/exit BALSWDIAG modes using SCANCFG, and allow the alternate conditions to settle prior to requesting the measurement (with a subsequent write to SCANCRTL with SCAN = 1). This bit can also be used to realize a variety of data move options (see DBLBUFEN and RDFILT for details) or to clear SCANDONE, SCANTIMEOUT, and DATARDY bits without requesting a measurement sequence/scan.*

ADCTEST1AREG (0x67)

ADCTEST1A is a read- and write-accessible register that contains user-specified arguments used in ALU diagnostics.

BIT	15	14	13	12	11	10	9	8
Field	ADCTSTEN	–	–	–	ADCTEST1A[11:8]			
Reset	0b0	–	–	–	0x000			
Access Type	Write, Read	–	–	–	Write, Read			

BIT	7	6	5	4	3	2	1	0
Field	ADCTEST1A[7:0]							
Reset	0x000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
ADCTSTEN	15	ADC/ALU Self Test Mode Enable 0 = Normal Operation (default) 1 = Enables the ALU Test Mode This mode feeds 12-bit data from the ADCTEST registers directly into the ALU instead of the ADC conversion data. Scans can then be performed, confirming proper operation of the ALU and calibration MAC. Notes: No calibration coefficients will be applied to ensure deterministic results (Gain = 1.0, Offset = 0.0). ADCTESTEN is ignored for On-Demand Calibration scans (SCANCFG = 011) to avoid miscalibration, and all scans performed during Automated Cell-Balancing modes to avoid inaccurate balancing results.

BITFIELD	BITS	DESCRIPTION
ADCTEST1A	11:0	ALU ADC Input Arguement 1A User-specified test data for the ALU diagnostic (ADCTESTEN = 1). This 12-bit data is fed into the ALU during the first conversion of odd-numbered samples (e.g., first sample).

ADCTEST1BREG (0x68)

ADCTEST1B is a read- and write-accessible register that contains user-specified arguments used in ALU diagnostics.

BIT	15	14	13	12	11	10	9	8
Field	–	–	–	–	ADCTEST1B[11:8]			
Reset	–	–	–	–	0x000			
Access Type	–	–	–	–	Write, Read			

BIT	7	6	5	4	3	2	1	0
Field	ADCTEST1B[7:0]							
Reset	0x000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
ADCTEST1B	11:0	ALU ADC Input Arguement 1B User-specified test data for the ALU diagnostic (ADCTEST = 1). This 12-bit data is fed into the ALU during the second conversion of odd-numbered samples (e.g., first sample).

ADCTEST2AREG (0x69)

ADCTEST2A is a read- and write-accessible register that contains user-specified arguments used in ALU diagnostics.

BIT	15	14	13	12	11	10	9	8
Field	–	–	–	–	ADCTEST2A[11:8]			
Reset	–	–	–	–	0x000			
Access Type	–	–	–	–	Write, Read			

BIT	7	6	5	4	3	2	1	0
Field	ADCTEST2A[7:0]							
Reset	0x000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
ADCTEST2A	11:0	ALU ADC Input Arguement 2A User-specified test data for the ALU diagnostic (ADCTEST = 1). This 12-bit data is fed into the ALU during the first conversion of even-numbered samples in oversampling mode.

ADCTEST2BREG (0x6A)

ADCTEST2B is a read- and write-accessible register that contains user-specified arguments used in ALU diagnostics.

BIT	15	14	13	12	11	10	9	8
Field	–	–	–	–	ADCTEST2B[11:8]			
Reset	–	–	–	–	0x000			
Access Type	–	–	–	–	Write, Read			

BIT	7	6	5	4	3	2	1	0
Field	ADCTEST2B[7:0]							
Reset	0x000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
ADCTEST2B	11:0	ALU ADC Input Arguement 2B User-specified test data for the ALU diagnostic (ADCTEST = 1). This 12-bit data is fed into the ALU during the second conversion of even-numbered samples in oversampling mode.

DIAGCFG (0x6B)

DIAGCFG is a read- and write-accessible register that governs diagnostic source and mode options applied to the internal measurement acquisitions (scans).

BIT	15	14	13	12	11	10	9	8
Field	CTSTDAC[3:0]				CTSTSRC	MUXDIAGBUS	MUXDIAGPAIR	MUXDIAGEN
Reset	0x0				0b0	0b0	0b0	0b0
Access Type	Write, Read				Write, Read	Write, Read	Write, Read	Write, Read

BIT	7	6	5	4	3	2	1	0
Field	DIAGSEL2[3:0]				DIAGSEL1[3:0]			
Reset	0x0				0x0			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION
CTSTDAC	15:12	Current Level Configuration for all enabled test sources per the following table (6.25µA LSB for Cn, AUXIN, 3.125µA LSB for HVMUX)

CTSTDAC	TEST SOURCE	CURRENT
[3:0]	Cn, AUXIN	HVMUX
0x0	6.25µA	3.125µA
0x1	12.50µA	6.250µA
0x2	18.75µA	9.375µA
...	...	...
0xD	87.5µA	43.75µA
0xE	93.75µA	46.875µA
0xF	100µA	50µA

BITFIELD	BITS	DESCRIPTION
CTSTSRC	11	Test Current Source Polarity 0 = Sink Current to GND (default) 1 = Source Current from V_{DDL} ***Note:*** *Polarity selection applies to AUX test current sources only.*
MUXDIAGBUS	10	Selects the HVMUX output to which the HVMUX test current source is connected, if MUXDIAGPAIR is enabled. 0 = Output Used for Even Cells, C0, and AGND 1 = Output Used for Odd Cells and REF, and ALTREF
MUXDIAGPAIR	9	MUX Diagnostic Bus Configuration 0 = Both HVMUX test current sources are connected to both HVMUX outputs. (default) 1 = A single HVMUX test current source is connected to only one HVMUX output (as selected by MUXDIAGBUS).
MUXDIAGEN	8	HVMUX Test Current Source(s) Enable 0 = Disable (default) 1 = Enable The current level is configured by CSTDAC and the connectivity is configured by MUXDIAGPAIR and MUXDIAGBUS
DIAGSEL2	7:4	Acquisition Diagnostic2 Measurement Selection 0000 = No Diagnostic Requested 0001 = Die Temperature ($ADC_{IN} = V_{PTAT}$, $ADC_{REF} = V_{REF}$). 0010 = V_{AA} ($ADC_{IN} = V_{REF}$ through LSAmp, $ADC_{REF} = V_{AA}$) 0011 = Cell Signal Path ADC Fault, V_{ALTREF} ($ADC_{IN} = V_{ALTREF}$ (1V), $ADC_{REF} = V_{REF}$) 0100 = Comparator Cell Signal Path Fault ($ADC_{IN} = V_{REF}$ through LSAmp2 - V_{DAC} at DAC_{CODE} = 0x400 (1/4), $ADC_{REF} = DAC_{REF} = V_{REF}$, bipolar mode) 0101 = Cell Calibration ($ADC_{IN} = V_{REF}$ through LSAmp, $ADC_{REF} = V_{REF}$). Calibration gain and offset coefficients and chopping applied according to SCANMODE selection. 0110 = Offset Calibration (ADC_{IN} = Short (Pyramid) or ADC_{IN} = Short through LSAmp (ramp), $ADC_{REF} = V_{REF}$, bipolar mode). Calibration offset coefficients applied according to SCANMODE selection. 0111 = 3/4-Scale DAC Test (DAC = 0xC00 $ADC_{IN} = V_{DAC}$, $ADC_{REF} = DAC_{REF} = V_{REF}$). 1000 = 1/4-Scale DAC Test (DAC = 0x3FF $ADC._{IN} = V_{DAC}$, $ADC_{REF} = DAC_{REF} = V_{REF}$). 1001 = THRM Offset Calibration (ADC_{IN} = short, $ADC_{REF} = V_{THRM}$, bipolar mode). CALOSTHRM coefficient applied. 1101 = $V_{DDL2/3}$ ($ADC_{IN} = V_{DDL2/3}$ through LSAmp, $ADC_{REF} = V_{REF}$) Selects the second diagnostic measurement appended to the acquisition, with the result stored in DIAG2. Appropriate calibrations (or factory defaults if ADCALEN = 0) and chopping are applied as needed. *Detailed Diagnostics* *1010 = Zero-Scale ADC Test (0x0000, $ADC_{IN} = -V_{AA}$, $ADC_{REF} = V_{REF}$, bipolar mode), full result available through DIAG.* *1011 = Full-Scale ADC Test (0x3FFC, $ADC_{IN} = V_{AA}$, $ADC_{REF} = V_{REF}$, bipolar mode), full result available through DIAG.* *1100 = LSAMP Offset ($ADC_{IN} = V_{LSA\_0V}$, $ADC_{REF} = V_{REF}$. bipolar mode)* *Detailed diagnostics are normally performed at the end of an acquisition (with the exception of LSAMP offset, which is covered by the V_{ALTREF} diagnostic), and the pass/fail results are available in the FMEA2 BIST alerts. However, if it is deemed necessary to examine detailed results, these can be made available in the DIAG2 register using the modes above.*

BITFIELD	BITS	DESCRIPTION
DIAGSEL1	3:0	Acquisition Diagnostic1 Measurement Selection 0000 = No Diagnostic Requested 0001 = Die Temperature (ADC_{IN} = V_{PTAT}, ADC_{REF} = V_{REF}). 0010 = V_{AA} (ADC_{IN} = V_{REF} through LSAmp, ADC_{REF} = V_{AA}) 0011 = Cell Signal Path ADC Fault, V_{ALTREF} (ADC_{IN} = V_{ALTREF} (1V), ADC_{REF} = V_{REF}) 0100 = Comparator Cell Signal Path Fault (ADC_{IN} = V_{REF} through LSAmp2 - V_{DAC} at DAC_{CODE} = 0x400 (1/4), ADC_{REF} = DAC_{REF} = V_{REF}, bipolar mode) 0101 = Cell Calibration (ADC_{IN} = V_{REF} through LSAmp, ADC_{REF} = V_{REF}). Calibration gain and offset coefficients and chopping applied according to SCANMODE selection. 0110 = Offset Calibration (ADC_{IN} = Short (Pyramid) or ADC_{IN} = Short through LSAmp (ramp), ADC_{REF} = V_{REF}, bipolar mode). Calibration offset coefficients applied according to SCANMODE selection. 0111 = 3/4-Scale DAC Test (DAC = 0xC00 ADC_{IN} = V_{DAC}, ADC_{REF} = DAC_{REF} = V_{REF}). 1000 = 1/4-Scale DAC Test (DAC = 0x3FF $ADC._{IN}$ = V_{DAC}, ADC_{REF} = DAC_{REF} = V_{REF}). 1001 = THRM Offset Calibration (ADC_{IN} = Short, ADC_{REF} = V_{THRM}, bipolar mode). CALOSTHRM coefficient applied. 1101 = $V_{DDL2/3}$ (ADC_{IN} = $V_{DDL2/3}$ through LSAmp, ADC_{REF} = V_{REF}) Selects the first diagnostic measurement appended to the acquisition, with the result stored in DIAG1. Appropriate calibrations (or factory defaults if ADCALEN = 0) and chopping are applied as needed. *Detailed Diagnostics* *1010 = Zero-Scale ADC Test (0x0000, ADC_{IN} = -V_{AA}, ADC_{REF} = V_{REF}, bipolar mode), full result available through DIAG.* *1011 = Full-Scale ADC Test (0x3FFC, ADC_{IN} = V_{AA}, ADC_{REF} = V_{REF}, bipolar mode), full result available through DIAG.* *1100 = LSAMP Offset (ADC_{IN} = V_{LSA_0V}, ADC_{REF} = V_{REF}. bipolar mode)* *Detailed diagnostics are normally performed at the end of an acquisition (with the exception of LSAMP offset, which is covered by the V_{ALTREF} diagnostic), and the pass/fail results are available in the FMEA2 BIST alerts. However, if it is deemed necessary to examine detailed results, these can be made available in the DIAG1 register using the modes above.*

CTSTCFG (0x6C)

CTSTCFG is a read- and write-accessible register that controls the application of diagnostic current sources to selected cell input channels.

BIT	15	14	13	12	11	10	9	8
Field	CELLOPNDIAGSEL	CTSTEN[14:8]						
Reset	0b0	0x0000						
Access Type	Write, Read	Write, Read						
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	CTSTEN[7:0]							
Reset	0x0000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
CELLOPNDIAGSEL	15	Cell Open Diagnostic Mode Selection 0 - Normal Operation (default) 1 - Open Diagnostic Operation In Normal mode (0), measured CELLn channels are selected by CELLEN and measured with standard thresholds on a per channel basis for both ADC and comparator acquisition sequences. In Open Diagnostic mode (1), measured CELLn channels are selected by (CELLENn & !POLARITYn) on a per channel basis. Only low-side comparator checks will be performed using alternate Open (OPN) thresholds. Normally in Open Diagnostic modes, pulldown current sources are enabled on all measured channels using CTSTEN, and only comparator measurements are selcected (SCANCFG = 010). This mode is most often used with an appropriate Auxiliary Open Diagnostic mode (AUXDIAGSEL = 010 or 011).
CTSTEN	14:0	Cell Diagnostic Current Source Enable Enables the current sources connected to the corresponding cell inputs for diagnostic testing. The current level is configured by the CTSTDAC in the DIAGCFG register.

AUXTSTCFG (0x6D)

AUXTSTCFG is a read- and write-accessible register that controls the application of diagnostic modes and current sources to selected auxiliary input channels.

BIT	15	14	13	12	11	10	9	8
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–

BIT	7	6	5	4	3	2	1	0
Field	–	–	AUXTSTEN[5:4]		AUXTSTEN[3:0]			
Reset	–	–	0x0		0x0			
Access Type	–	–	Write, Read, Ext		Write, Read, Ext			

BITFIELD	BITS	DESCRIPTION
AUXTSTEN	5:4	Auxiliary Diagnostic Current Source Enable Enables the current sources connected to the corresponding auxiliary input for diagnostic testing. The current level is configured by DIAGCFG:CTSTDAC, and the current direction is configured by DIAGCFG:CTSTSRC. ***Note:*** *If the respective GPIOEN bit is set (GPIO mode), this bit is ignored, but will still read back the user setting.*

BITFIELD	BITS	DESCRIPTION
AUXTSTEN	3:0	Auxiliary Diagnostic Current Source Enable Enables the current sources connected to the corresponding auxiliary input for diagnostic testing. The current level is configured by DIAGCFG:CTSTDAC, and the current direction is configured by DIAGCFG:CTSTSRC. ***Note:*** *If the I2CEN bit (Digital I^2C mode, applies to [1:0] only) or the respective GPIOEN bit is set (GPIO mode), this bit is ignored, but will still read back the user setting.*

DIAGGENCFG (0x6E)

DIAGGENCFG is a read- and write-accessible register that controls the application of general diagnostic modes to the selected input paths.

BIT	15	14	13	12	11	10	9	8
Field	AUXDIAGSEL[2:0]			–	–	–	–	–
Reset	0b000			–	–	–	–	–
Access Type	Write, Read			–	–	–	–	–

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION
AUXDIAGSEL	15:13	AUX Diagnostic Mode Selection 00x - Normal Operation (default) 010 - AUX Accelerated Discharge Operation (ratiometric only) 011 - THRM Output Connected to AGND 1xx - Reserved for Analog Devices Use Only Control bits used for AUXINn pin diagnostic testing. Only ports configured as AUXINn inputs are tested.

BALSWCTRL (0x6F)

BALSWCTRL is a read- and write-accessible register that governs the behavior of the Charge-Balancing Switches in Manual and Auto Cell-Balancing modes.

Write access to this register is blocked during Automated Cell-Balancing operations (CBMODE = 001, 1xx).

BIT	15	14	13	12	11	10	9	8
Field	CBRESTART	–	BALSWEN[14:9]					
Reset	0b0	–	0x0000					
Access Type	Write, Read, Pulse	–	Write, Read, Ext					

BIT	7	6	5	4	3	2	1	0
Field	BALSWEN[8:1]							
Reset	0x0000							
Access Type	Write, Read, Ext							

BITFIELD	BITS	DESCRIPTION
CBRESTART	15	Watchdog Timer Restart for Manual Mode 0 - CBTIMER continues to run. 1 - CBTIMER is reset to zero. Acts as a strobe bit and therefore does not need to be cleared. Always reads logic 0. Accessible and applies in Manual mode only. Writing 1 to CBRESTART after cell-balancing timer expiration has no effect. To perform another Manual mode cell-balancing event, the user must issue a separate write to the BALCTRL register.
BALSWEN	13:0	Balance Switch Enable BALSWEN[n] enables the balancing switch (allowing conduction) between SWn and SWn-1, balancing CELLn.

BALEXP1 (0x70)

BALEXPn is a read- and write-accessible register that holds the Cell-Balancing Expiration Time for CELLn (using the switch across SWn and SWn-1).

BALEXP1 sets the Expiration Time for all Group Auto Cell-Balancing and Discharge modes and the watchdog timeout for Manual Cell-Balancing mode.

Write access to this register is blocked during all cell-balancing operations (CBMODE != 000).

BIT	15	14	13	12	11	10	9	8
Field	–	–	–	–	–	–	CBEXP1[9:8]	
Reset	–	–	–	–	–	–	0x000	
Access Type	–	–	–	–	–	–	Write, Read, Ext	

BIT	7	6	5	4	3	2	1	0
Field	CBEXP1[7:0]							
Reset	0x000							
Access Type	Write, Read, Ext							

BITFIELD	BITS	DESCRIPTION
CBEXP1	9:0	Cell-Balancing Expiration Time Cell-Balancing Expiration Time for CELLn; unit (LSB = hour, minute, or second) determined by CBMODE. CBEXP1 is used as the master/watchdog timeout setting for Manual, Discharge, and Auto Group Cell-Balancing modes. Value 0x3FF operates balancing indefinitely (no timer expiration). Default value 0x000 disables cell balancing (preconfigured timer expiration).

BALEXP2 (0x71)

BALEXPn is a read- and write-accessible register that holds the Cell-Balancing Expiration Time for CELLn (using the switch across SWn and SWn-1). Used in Individual Automated Cell-Balancing modes only.

Write access to this register is blocked during Automated Cell-Balancing operations (CBMODE = 1xx).

BIT	15	14	13	12	11	10	9	8
Field	–	–	–	–	–	–	CBEXP2[9:8]	
Reset	–	–	–	–	–	–	0x000	
Access Type	–	–	–	–	–	–	Write, Read, Ext	

BIT	7	6	5	4	3	2	1	0
Field	CBEXP2[7:0]							
Reset	0x000							
Access Type	Write, Read, Ext							

BITFIELD	BITS	DESCRIPTION
CBEXP2	9:0	Cell-Balancing Expiration Time Cell-Balancing Expiration Time for CELLn; unit (LSB = hour, minute, or second) determined by CBMODE. Value 0x3FF operates balancing indefinitely (no timer expiration). Default value 0x000 disables cell balancing (preconfigured timer expiration).

BALEXP3 (0x72)

BALEXPn is a read- and write-accessible register that holds the Cell-Balancing Expiration Time for CELLn (using the switch across SWn and SWn-1). Used in Individual Automated Cell-Balancing modes only.

Write access to this register is blocked during Automated Cell-Balancing operations (CBMODE = 1xx).

BIT	15	14	13	12	11	10	9	8
Field	–	–	–	–	–	–	CBEXP3[9:8]	
Reset	–	–	–	–	–	–	0x000	
Access Type	–	–	–	–	–	–	Write, Read, Ext	

BIT	7	6	5	4	3	2	1	0
Field	CBEXP3[7:0]							
Reset	0x000							
Access Type	Write, Read, Ext							

BITFIELD	BITS	DESCRIPTION
CBEXP3	9:0	Cell-Balancing Expiration Time Cell-Balancing Expiration Time for CELLn; unit (LSB = hour, minute, or second) determined by CBMODE. Value 0x3FF operates balancing indefinitely (no timer expiration). Default value 0x000 disables cell balancing (preconfigured timer expiration).

BALEXP4 (0x73)

BALEXPn is a read- and write-accessible register that holds the Cell-Balancing Expiration Time for CELLn (using the switch across SWn and SWn-1). Used in Individual Automated Cell-Balancing modes only.

Write access to this register is blocked during Automated Cell-Balancing operations (CBMODE = 1xx).

BIT	15	14	13	12	11	10	9	8
Field	–	–	–	–	–	–	CBEXP4[9:8]	
Reset	–	–	–	–	–	–	0x000	
Access Type	–	–	–	–	–	–	Write, Read, Ext	

BIT	7	6	5	4	3	2	1	0
Field	CBEXP4[7:0]							
Reset	0x000							
Access Type	Write, Read, Ext							

BITFIELD	BITS	DESCRIPTION
CBEXP4	9:0	Cell-Balancing Expiration Time Cell-Balancing Expiration Time for CELLn; unit (LSB = hour, minute, or second) determined by CBMODE. Value 0x3FF operates balancing indefinitely (no timer expiration). Default value 0x000 disables cell balancing (preconfigured timer expiration).

BALEXP5 (0x74)

BALEXPn is a read- and write-accessible register that holds the Cell-Balancing Expiration Time for CELLn (using the switch across SWn and SWn-1). Used in individual Automated Cell-Balancing modes only.

Write access to this register is blocked during Automated Cell-Balancing operations (CBMODE = 1xx).

BIT	15	14	13	12	11	10	9	8
Field	–	–	–	–	–	–	CBEXP5[9:8]	
Reset	–	–	–	–	–	–	0x000	
Access Type	–	–	–	–	–	–	Write, Read, Ext	

BIT	7	6	5	4	3	2	1	0
Field	CBEXP5[7:0]							
Reset	0x000							
Access Type	Write, Read, Ext							

BITFIELD	BITS	DESCRIPTION
CBEXP5	9:0	Cell-Balancing Expiration Time Cell-Balancing Expiration Time for CELLn; unit (LSB = hour, minute, or second) determined by CBMODE. Value 0x3FF operates balancing indefinitely (no timer expiration). Default value 0x000 disables cell balancing (preconfigured timer expiration).

BALEXP6 (0x75)

BALEXPn is a read- and write-accessible register that holds the Cell-Balancing Expiration Time for CELLn (using the switch across SWn and SWn-1). Used in individual Automated Cell-Balancing modes only.

Write access to this register is blocked during Automated Cell-Balancing operations (CBMODE = 1xx).

BIT	15	14	13	12	11	10	9	8
Field	–	–	–	–	–	–	CBEXP6[9:8]	
Reset	–	–	–	–	–	–	0x000	
Access Type	–	–	–	–	–	–	Write, Read, Ext	

BIT	7	6	5	4	3	2	1	0
Field	CBEXP6[7:0]							
Reset	0x000							
Access Type	Write, Read, Ext							

BITFIELD	BITS	DESCRIPTION
CBEXP6	9:0	Cell-Balancing Expiration Time Cell-Balancing Expiration Time for CELLn; unit (LSB = hour, minute, or second) determined by CBMODE. Value 0x3FF operates balancing indefinitely (no timer expiration). Default value 0x000 disables cell balancing (preconfigured timer expiration).

BALEXP7 (0x76)

BALEXPn is a read- and write-accessible register that holds the Cell-Balancing Expiration Time for CELLn (using the switch across SWn and SWn-1). Used in Individual Automated Cell-Balancing modes only.

Write access to this register is blocked during Automated Cell-Balancing operations (CBMODE = 1xx).

BIT	15	14	13	12	11	10	9	8
Field	–	–	–	–	–	–	CBEXP7[9:8]	
Reset	–	–	–	–	–	–	0x000	
Access Type	–	–	–	–	–	–	Write, Read, Ext	

BIT	7	6	5	4	3	2	1	0
Field	CBEXP7[7:0]							
Reset	0x000							
Access Type	Write, Read, Ext							

BITFIELD	BITS	DESCRIPTION
CBEXP7	9:0	Cell-Balancing Expiration Time Cell-Balancing Expiration Time for CELLn; unit (LSB = hour, minute, or second) determined by CBMODE. Value 0x3FF operates balancing indefinitely (no timer expiration). Default value 0x000 disables cell balancing (preconfigured timer expiration).

BALEXP8 (0x77)

BALEXPn is a read- and write-accessible register that holds the Cell-Balancing Expiration Time for CELLn (using the switch across SWn and SWn-1). Used in Individual Automated Cell-Balancing modes only.

Write access to this register is blocked during Automated Cell-Balancing operations (CBMODE = 1xx).

BIT	15	14	13	12	11	10	9	8
Field	–	–	–	–	–	–	CBEXP8[9:8]	
Reset	–	–	–	–	–	–	0x000	
Access Type	–	–	–	–	–	–	Write, Read, Ext	

BIT	7	6	5	4	3	2	1	0
Field	CBEXP8[7:0]							
Reset	0x000							
Access Type	Write, Read, Ext							

BITFIELD	BITS	DESCRIPTION
CBEXP8	9:0	Cell-Balancing Expiration Time Cell-Balancing Expiration Time for CELLn; unit (LSB = hour, minute, or second) determined by CBMODE. Value 0x3FF operates balancing indefinitely (no timer expiration). Default value 0x000 disables cell balancing (preconfigured timer expiration).

BALEXP9 (0x78)

BALEXPn is a read- and write-accessible register that holds the Cell-Balancing Expiration Time for CELLn (using the switch across SWn and SWn-1). Used in Individual Automated Cell-Balancing modes only.

Write access to this register is blocked during Automated Cell-Balancing operations (CBMODE = 1xx).

BIT	15	14	13	12	11	10	9	8
Field	–	–	–	–	–	–	CBEXP9[9:8]	
Reset	–	–	–	–	–	–	0x000	
Access Type	–	–	–	–	–	–	Write, Read, Ext	

BIT	7	6	5	4	3	2	1	0
Field	CBEXP9[7:0]							
Reset	0x000							
Access Type	Write, Read, Ext							

BITFIELD	BITS	DESCRIPTION
CBEXP9	9:0	Cell-Balancing Expiration Time Cell-Balancing Expiration Time for CELLn; unit (LSB = hour, minute, or second) determined by CBMODE. Value 0x3FF operates balancing indefinitely (no timer expiration). Default value 0x000 disables cell balancing (preconfigured timer expiration).

BALEXP10 (0x79)

BALEXPn is a read- and write-accessible register that holds the Cell-Balancing Expiration Time for CELLn (using the switch across SWn and SWn-1). Used in individual Automated Cell-Balancing modes only.

Write access to this register is blocked during Automated Cell-Balancing operations (CBMODE = 1xx).

BIT	15	14	13	12	11	10	9	8
Field	–	–	–	–	–	–	CBEXP10[9:8]	
Reset	–	–	–	–	–	–	0x000	
Access Type	–	–	–	–	–	–	Write, Read, Ext	

BIT	7	6	5	4	3	2	1	0
Field	CBEXP10[7:0]							
Reset	0x000							
Access Type	Write, Read, Ext							

BITFIELD	BITS	DESCRIPTION
CBEXP10	9:0	Cell-Balancing Expiration Time Cell-Balancing Expiration Time for CELLn; unit (LSB = hour, minute, or second) determined by CBMODE. Value 0x3FF operates balancing indefinitely (no timer expiration). Default value 0x000 disables cell balancing (preconfigured timer expiration).

BALEXP11 (0x7A)

BALEXPn is a read- and write-accessible register that holds the Cell-Balancing Expiration Time for CELLn (using the switch across SWn and SWn-1). Used in individual Automated Cell-Balancing modes only.

Write access to this register is blocked during Automated Cell-Balancing operations (CBMODE = 1xx).

BIT	15	14	13	12	11	10	9	8
Field	–	–	–	–	–	–	CBEXP11[9:8]	
Reset	–	–	–	–	–	–	0x000	
Access Type	–	–	–	–	–	–	Write, Read, Ext	

BIT	7	6	5	4	3	2	1	0
Field	CBEXP11[7:0]							
Reset	0x000							
Access Type	Write, Read, Ext							

BITFIELD	BITS	DESCRIPTION
CBEXP11	9:0	Cell-Balancing Expiration Time Cell-Balancing Expiration Time for CELLn; unit (LSB = hour, minute, or second) determined by CBMODE. Value 0x3FF operates balancing indefinitely (no timer expiration). Default value 0x000 disables cell balancing (preconfigured timer expiration).

BALEXP12 (0x7B)

BALEXPn is a read- and write-accessible register that holds the Cell-Balancing Expiration Time for CELLn (using the switch across SWn and SWn-1). Used in individual Automated Cell-Balancing modes only.

Write access to this register is blocked during Automated Cell-Balancing operations (CBMODE = 1xx).

BIT	15	14	13	12	11	10	9	8
Field	–	–	–	–	–	–	CBEXP12[9:8]	
Reset	–	–	–	–	–	–	0x000	
Access Type	–	–	–	–	–	–	Write, Read, Ext	

BIT	7	6	5	4	3	2	1	0
Field	CBEXP12[7:0]							
Reset	0x000							
Access Type	Write, Read, Ext							

BITFIELD	BITS	DESCRIPTION
CBEXP12	9:0	Cell-Balancing Expiration Time Cell-Balancing Expiration Time for CELLn; unit (LSB = hour, minute, or second) determined by CBMODE. Value 0x3FF operates balancing indefinitely (no timer expiration). Default value 0x000 disables cell balancing (preconfigured timer expiration).

BALEXP13 (0x7C)

BALEXPn is a read- and write-accessible register that holds the Cell-Balancing Expiration Time for CELLn (using the switch across SWn and SWn-1). Used in Individual Automated Cell-Balancing modes only.

Write access to this register is blocked during Automated Cell-Balancing operations (CBMODE = 1xx).

BIT	15	14	13	12	11	10	9	8
Field	–	–	–	–	–	–	CBEXP13[9:8]	
Reset	–	–	–	–	–	–	0x000	
Access Type	–	–	–	–	–	–	Write, Read, Ext	

BIT	7	6	5	4	3	2	1	0
Field	CBEXP13[7:0]							
Reset	0x000							
Access Type	Write, Read, Ext							

BITFIELD	BITS	DESCRIPTION
CBEXP13	9:0	Cell-Balancing Expiration Time Cell-Balancing Expiration Time for CELLn; unit (LSB = hour, minute, or second) determined by CBMODE. Value 0x3FF operates balancing indefinitely (no timer expiration). Default value 0x000 disables cell balancing (preconfigured timer expiration).

BALEXP14 (0x7D)

BALEXPn is a read- and write-accessible register that holds the Cell-Balancing Expiration Time for CELLn (using the switch across SWn and SWn-1). Used in Individual Automated Cell-Balancing modes only.

Write access to this register is blocked during Automated Cell-Balancing operations (CBMODE = 1xx).

BIT	15	14	13	12	11	10	9	8
Field	–	–	–	–	–	–	CBEXP14[9:8]	
Reset	–	–	–	–	–	–	0x000	
Access Type	–	–	–	–	–	–	Write, Read, Ext	

BIT	7	6	5	4	3	2	1	0
Field	CBEXP14[7:0]							
Reset	0x000							
Access Type	Write, Read, Ext							

BITFIELD	BITS	DESCRIPTION
CBEXP14	9:0	Cell-Balancing Expiration Time Cell-Balancing Expiration Time for CELLn; unit (LSB = hour, minute, or second) determined by CBMODE. Value 0x3FF operates balancing indefinitely (no timer expiration). Default value 0x000 disables cell balancing (preconfigured timer expiration).

BALAUTOUVTHR (0x7E)

BALAUTOUVTHR is a read- and write-accessible register that selects the cell undervoltage exit threshold for the ADC when used in Automated Cell-Balancing operations.

A write to this register allows direct setting or automatic selection of this threshold.

Write access to this register is blocked during Automated Cell-Balancing operations (CBMODE = 1xx). Also, during active measurement scans, all writes with CBUVMINCELL = 1 will be blocked and will result in ALRTRJCT being issued (since the MINCELL data may be altered as a result of the scan in progress).

A read from this register will display the current value of the threshold and the method used for its selection.

BIT	15	14	13	12	11	10	9	8
Field	CBUVTHR[13:6]							
Reset	0x3FFF							
Access Type	Write, Read, Ext							

BIT	7	6	5	4	3	2	1	0
Field	CBUVTHR[5:0]						–	CBUVMINCELL
Reset	0x3FFF						–	0b0
Access Type	Write, Read, Ext						–	Write, Read, Ext

BITFIELD	BITS	DESCRIPTION
CBUVTHR	15:2	Cell-Balancing Undervoltage Threshold 14-bit ADC threshold,of a 5V input range, below which Cell-Balancing operations will be suspended on each CELL. Default of 0x3FFF, ensures no cell balancing will occur without prior configuration.
CBUVMINCELL	0	Cell-Balancing Undervoltage Threshold Selection 0 = User-Defined CBUVTHR 1 = MINCELL-Defined CBUVTHR In mode 0, the value written to CBUVTHR during a valid write to BALAUTOUVTHR will be loaded to CBUVTHR. In mode 1, the current value in the CELLn register corresponding to the MINCELL address will be automatically loaded to CBUVTHR during a valid write to BALAUTOUVTHR (and the content in CBUVTHR during the write will be ignored). ***Note:*** *Automated Cell Balancing with CBUVTHR checking is only supported for unipolar cell measurements. If CBUVMINCELL = 1 is written while MINMAXPOL = 1, CBUVTHR will be set to 0x3FFF\h as a result.*

BALDLYCTRL (0x7F)

BALDLYCTRL is a read- and write-accessible register that selects the delay/timing intervals used within Automated Cell-Balancing operations.

Write access to this register is blocked during Automated Cell-Balancing operations (CBMODE = 001, 1xx).

BIT	15	14	13	12	11	10	9	8
Field	–	–	–	–	–	–	CBNTFYCFG[1:0]	
Reset	–	–	–	–	–	–	0b00	
Access Type	–	–	–	–	–	–	Write, Read, Ext	

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	CBCALDLY[2:0]		
Reset	–	–	–	–	–	0b000		
Access Type	–	–	–	–	–	Write, Read, Ext		

BITFIELD	BITS	DESCRIPTION
CBNTFYCFG	9:8	Cell-Balancing Notification Alert Configuration 00 = Disable Cell-Balancing Notification Alert (default) 01 = Nofication Issued every 1hr 10 = Nofication Issued every 2hr 11 = Nofication Issued every 4hr In Automatic and Discharge modes, the Cell-Balancing Notification Alert (ALRTCBNTFY) can be issued to confirm normal progression of automated operations. The frequency of issuance is selected as described above, in real time (i.e., not CBDUTY-adjusted). Notification alerts will continue to be issued during HOLDSHDNL.

BITFIELD	BITS	DESCRIPTION
CBCALDLY	2:0	Cell-Balancing Calibration Period Selection In Automatic and Discharge modes, after each pair of Even and Odd Cell-Balancing periods, a supervisory ADC measurement is taken (and checked against CBUVTHR, if enabled/applicable). CBCALDLY allows a calibration operation to be substituted in place of a measurement at the frequency indicted below. A value of 000 (default) disables CAL operations (only ADC operations are performed). 000 - Periodic Calibration Disabled 001 - 2 (every other) cycle 010 - 4 (every fourth) cycle 011 - 8 cycles 100 - 12 cycles 101 - 16 cycles 110 - 24 cycles 111 - 32 cycles If CBMEASEN = 0x (ADC/CAL measurements disabled), this bitfield is ignored and has no effect.

BALCTRL (0x80)

BALCTRL is a read- and write-accessible register that initiates and controls all internal cell-balancing modes and operations.

Any write to this register to a mode other than CBMODE = 000 (disable) will restart the CBTIMER at 0 and launch the requested mode of operation.

BIT	15	14	13	12	11	10	9	8
Field	CBACTIVE[1:0]		CBMODE[2:0]			CBIIRINIT	HOLDSHDNL[1:0]	
Reset	0b00		0b000			0b0	0b00	
Access Type	Read Only		Write, Read, Ext			Write, Read	Write, Read	

BIT	7	6	5	4	3	2	1	0
Field	CBDUTY[3:0]				CBDONEALRTEN	CBTEMPEN	CBMEASEN[1:0]	
Reset	0x0				0b0	0b0	0x0	
Access Type	Write, Read				Write, Read	Write, Read	Write, Read	

BITFIELD	BITS	DESCRIPTION
CBACTIVE	15:14	Cell-Balancing Timer Active Indicator 00 = Cell Balancing is Disabled (default) 01 = Cell-Balancing Operations are Active 10 = Cell Balancing Completed Normally due to Reaching CBUVTHR or CBEXP Exit Conditions 11 = Cell Balancing Halted Unexpectedly due to Thermal Exit (ALRTCBTEMP), Time Out (ALRTCBTIMEOUT), or Calibration Fault (ALRTCBCAL) Conditions Read only.

BITFIELD	BITS	DESCRIPTION
CBMODE	13:11	Cell-Balancing Mode Selection 000 = Cell Balancing Disabled (default) 001 = Emergency/EOL Discharge by Hour 010 = Manual Cell Balancing by Second 011 = Manual Cell Balancing by Minute 100 = Auto Individual Cell Balancing by Second 101 = Auto Individual Cell Balancing by Minute 110 = Auto Group Cell Balancing by Second 111 = Auto Group Cell Balancing by Minute
CBIIRINIT	10	Cell-Balancing IIR Initialization Request 0 = IIR Filter Continuation (default) 1 = IIR Filter Initialized If enabled, the IIR filter contents will be initialized during the first measurement scan and CBUVTHR checks will be suspended for 16 measurement scans, giving the IIR time to settle.
HOLDSHDNL	9:8	SHDNL Hold Mode Enable 00 = No Hold (default) 01 = SHDNL Held High for the Duration of Automated Cell Balancing or Discharge Operations 10 = SHDNL Held High for Duration of Automated Cell Balancing or Discharge Operations, plus 5min or 6.25% of the Maximum Applicable CBEXP Interval (whichever is greater) 11 = SHDNL Held High for Duration of Automated Cell Balancing or Discharge Operations, and until Removed
CBDUTY	7:4	Cell-Balancing Duty Cycle Sets the active duty-cycle within each t_{CBEO} period. 0000 = 6.25% (default) 0001 = 12.5% ... 1110 = 93.75% 1111 = 100%, less NOL and measurement/calibration overhead.
CBDONEALRTEN	3	Cell-Balancing Complete Alert Enable 0 = ALRTCBDONE Masked in STATUS1:ALRTCBAL (default) 1 = ALRTCBDONE Included in STATUS1:ALRTCBAL Masking of this alert component allows the user the choice to be notified only for unexpected exits, or normal completions as well.
CBTEMPEN	2	Cell-Balancing Thermal Exit Enable 0 = Cell Balancing Not Impacted by ALRTTEMP (default) 1 = Cell Balancing Halts in Response to ALRTTEMP
CBMEASEN	1:0	Cell-Balancing Measurement Enable 0x = Embedded ADC/CAL Measurements and CBUVTHR Checking Disabled (default) 10 = Embedded ADC/CAL Measurements Enabled, CBUVTHR Checking Disabled 11 = Embedded ADC/CAL Measurements Enabled, CBUVTHR Checking Enabled ***Note:*** *Automated Cell Balancing with CBUVTHR checking is only supported for unipolar cell measurements.*

BALSTAT (0x81)

BALSTAT is a read-accessible register that allows the monitoring of any Automated Cell-Balancing operations currently in progress.

Once a CBMODE is initiated, all status bits persist and are cleared only when CBMODE is written to 000 (disabled) or when a new CBMODE operation is initiated through CBSTART.

BIT	15	14	13	12	11	10	9	8
Field	CBACTIVE_M1[1:0]		CBUNIT[1:0]		CBCNTR[1:0]		CBTIMER[9:8]	
Reset	0b00		0b00		0b00		0x000	
Access Type	Read Only		Read Only		Read Only		Read Only	

BIT	7	6	5	4	3	2	1	0
Field	CBTIMER[7:0]							
Reset	0x000							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
CBACTIVE_M1	15:14	Cell-Balancing Timer Active Indicator (Mirror) 00 = Cell Balancing is Disabled (default) 01 = Cell-Balancing Operations are Active 10 = Cell Balancing Completed Normally due to Reaching CBUVTHR or CBEXP Exit Conditions 11 = Cell Balancing Halted Unexpectedly due to Thermal Exit (ALRTCBTEMP), Timeout (ALRTCBTIMEOUT), or Calibration Fault (ALRTCBCAL) Conditions Read only.
CBUNIT	13:12	Cell-Balancing Timer Unit Indicator 00 = Cell Balancing is Disabled (default) 01 = CBTIMER Measures Seconds 10 = CBTIMER Measures Minutes 11 = CBTIMER Measures Hours Allows confirmation of Cell-Balancing Timer operating mode (LSB weight). Read only,
CBCNTR	11:10	Cell-Balancing Active Counter 1Hz counter that can be read to verify CBTIMER operation/activity when the CBTIMER is operated in minute or hour modes. The counter counts from 0 to 3, rolling over to 0 approximately every 4 seconds in all active cell-balancing modes (CBMODE != 000). Read only. ***Notes:*** *During Hold SHDNL extension periods (HOLDSHDNL = 1x), CBCNTR will continue to run.* *If the governing CBEXP setting is set to 0x3FF (infinite), this counter will continue to run, even though it has no impact on the active cell-balancing mode.*

BITFIELD	BITS	DESCRIPTION
CBTIMER	9:0	Cell-Balancing Timer Value Reads the current cell-balancing timer value in seconds, minutes, or hours, depending on CBMODE, as indicated by CBUNIT. Read only. ***Notes:*** *During SHDNL hold/extension periods (HOLDSHDNL = 1x), CBTIMER will read back the governing expiration time (CBEXP), indicating that the requested balancing operation has completed.* *If the governing CBEXP setting is set to 0x3FF (infinite), this timer will still run and roll over, even though it has no impact on the active cell-balancing mode.*

BALUVSTAT (0x82)

BALUVSTAT is a read-accessible register that relates current summary information on the cell voltages vs. the CBUVTHR undervoltage threshold.

BIT	15	14	13	12	11	10	9	8
Field	CBACTIVE_M2[1:0]		CBUVSTAT[14:9]					
Reset	0b00		0x0000					
Access Type	Read Only		Read Only					

BIT	7	6	5	4	3	2	1	0
Field	CBUVSTAT[8:1]							
Reset	0x0000							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
CBACTIVE_M2	15:14	Cell-Balancing Timer Active Indicator (Mirror) 00 = Cell Balancing is Disabled (default) 01 = Cell-Balancing Operations are Active 10 = Cell Balancing Completed Normally due to Reaching CBUVTHR or CBEXP Exit Conditions 11 = Cell Balancing Halted Unexpectedly due to Thermal Exit (ALRTCBTEMP), Timeout (ALRTCBTIMEOUT), or Calibration Fault (ALRTCBCAL) Conditions Read only.
CBUVSTAT	13:0	Cell-Balancing CBUVTHR Check Status CBUVSTAT[n] = 1 indicates the corresponding CELLn result falls below the threshold specified by CBUVTHR and that Cell-Balancing operations on that cell have ended. Cleared only when CBMODE is written to 000 (disabled) or when a new CBMODE operation is initiated through a write to BALCTRL. Read only. ***Note:*** *Automated Cell Balancing with CBUVTHR checking is only supported for unipolar cell measurements in locations with BALSWENn = 1. The user must also ensure CELLENn = 1 and POLARITYn = 0 to allow the required measurement updates; if the measurement is not supported, balancing of the cell automatically ends with a CBUVSTATn = 1 exit condition.*

BALDATA (0x83)

BALDATA is a read-accessible register that relates current summary information on the cell voltages vs. the CBUVTHR undervoltage threshold.

BIT	15	14	13	12	11	10	9	8
Field	CBACTIVE_M3[1:0]		DATARDY_M	–	–	–	–	–
Reset	0b00		0b0	–	–	–	–	–
Access Type	Read Only		Write, Read, Ext	–	–	–	–	–

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	CBSCAN
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Write, Read, Pulse

BITFIELD	BITS	DESCRIPTION
CBACTIVE_M3	15:14	Cell-Balancing Timer Active Indicator (Mirror) 00 = Cell Balancing is Disabled (default) 01 = Cell-Balancing Operations are Active 10 = Cell Balancing Completed Normally due to Reaching CBUVTHR or CBEXP Exit Conditions 11 = Cell Balancing Halted Unexpectedly due to Thermal Exit (ALRTCBTEMP), Timeout (ALRTCBTIMEOUT), or Calibration Fault (ALRTCBCAL) Conditions Read only.
DATARDY_M	13	Data Ready Indicator Bit (Mirror) Indicates the measurement data from the acquisition has been transferred to the data registers and may now be read. Data for all measurement registers and MIN/MAX/TOTAL is transferred at the same time. Cleared by writing to logic 0 to allow detection of the next data transfer. Writing to logic 1 has no internal effect. This is a mirror of the DATARDY bit in SCANCFG, provided to support readback of measurement results taken during Automated and Discharge Cell-Balancing modes.
CBSCAN	0	Manually Transfer Measurement Results from IIR to Data registers 0 = No transfer requested 1 = Measurement transferred from the IIR (regardless of RDFILT setting) to data registers; once transfer is complete, DATARDY bit is set. Acts as a strobe bit and therefore does not need to be cleared (self-clearing). This bit has no effect in Cell-Balancing Manual or Disable mode, or when CBMEASEN = 0x. Always reads logic 0.

I2CPNTR (0x84)

I2CPTNR is a read- and write-accessible register that contains two pointer bytes (register addresses) available for I^2C master transactions.

Once I2CSEND initiates a read or write transaction, attempts to write I2CPNTR during the transaction will be ignored and will cause an I2CRJCT fault to be issued.

BIT	15	14	13	12	11	10	9	8
Field	I2CPBYTE1[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	I2CPBYTE0[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
I2CPBYTE1	15:8	I^2C Pointer Address Byte 1 This is the Pointer (Register) Address Byte 1 available for I^2C master transactions.
I2CPBYTE0	7:0	I^2C Pointer Address Byte 0 This is the Pointer (Register) Address Byte 0 available for I^2C master transactions.

I2CWDATA1 (0x85)

I2CWDATA1 is a read- and write-accessible register that contains the upper data bytes available for I^2C master Write mode transactions.

Once I2CSEND initiates an I^2C read or write transaction, attempts to write I2CWDATA1 during the transaction will be ignored and will cause an I2CRJCT fault to be issued.

BIT	15	14	13	12	11	10	9	8
Field	I2CWBYTE3[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	I2CWBYTE2[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
I2CWBYTE3	15:8	I^2C Write Data Byte 3 This is the 3rd (MS) byte available for I^2C Master Write mode transactions.
I2CWBYTE2	7:0	I^2C Write Data Byte 2 This is the 2nd byte available for I^2C Master Write mode transactions.

I2CWDATA2 (0x86)

I2CWDATA2 is a read- and write-accessible register that contains the lower data bytes available for I^2C master Write mode transactions.

Once I2CSEND initiates an I^2C read or write transaction, attempts to write I2CWDATA2 during the transaction will be ignored and will cause an I2CRJCT fault to be issued.

BIT	15	14	13	12	11	10	9	8
Field	I2CWBYTE1[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	I2CWBYTE0[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
I2CWBYTE1	15:8	I^2C Write Data Byte 1 This is the 1st byte available for I^2C Master Write mode transactions.
I2CWBYTE0	7:0	I^2C Write Data Byte 0 This is the 0th (LS) byte available for I^2C Master Write mode transactions.

I2CRDATA1 (0x87)

I2CRDATA1 is a read-accessible register that contains the upper data bytes received for I^2C master Read mode transactions.

Note: During I^2C read transactions, data is updated as each byte is received/acknowledged, so reading back this register during active I^2C read transactions will cause an I2CRJCT fault to be issued.

BIT	15	14	13	12	11	10	9	8
Field	I2CRBYTE3[7:0]							
Reset	0xFF							
Access Type	Read Only							

BIT	7	6	5	4	3	2	1	0
Field	I2CRBYTE2[7:0]							
Reset	0xFF							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
I2CRBYTE3	15:8	I^2C Read Data Byte 3 This is the 3rd (MS) byte space available for use by I^2C Master Read mode transactions.
I2CRBYTE2	7:0	I^2C Read Data Byte 2 This is the 2nd byte space available for use by I^2C Master Read mode transactions.

I2CRDATA2 (0x88)

I2CRDATA2 is a read-accessible register that contains the lower data bytes received for I^2C master Read mode transactions.

Note: During I^2C read transactions, data is updated as each byte is received/acknowledged, so reading back this register during active I^2C read transactions will cause an I2CRJCT fault to be issued.

BIT	15	14	13	12	11	10	9	8
Field	I2CRBYTE1[7:0]							
Reset	0xFF							
Access Type	Read Only							

BIT	7	6	5	4	3	2	1	0
Field	I2CRBYTE0[7:0]							
Reset	0xFF							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
I2CRBYTE1	15:8	I^2C Read Data Byte 1 This is the 1st byte space available for use by I^2C Master Read mode transactions.
I2CRBYTE0	7:0	I^2C Read Data Byte 0 This is the 0th (LS) byte space available for use by I^2C Master Read mode transactions.

I2CCFG (0x89)

I2CCFG is a read- and write-accessible register that configures I^2C master modes and transaction formats.

Once I2CSEND initiates a read or write transaction, attempts to write I2CCFG during the transaction will be ignored and will cause an I2CRJCT fault to be issued.

BIT	15	14	13	12	11	10	9	8
Field	I2CFSCL	I2CWALT	I2CRFMT	I2C10BIT	I2CPNTRLNGTH	I2CALRTEN	–	–
Reset	0b1	0b0	0b1	0b0	0b0	0b0	–	–
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	–	–

BIT	7	6	5	4	3	2	1	0
Field	–	–	I2CANACONTEN	I2CCONTEN	I2CGLITCHEN	I2CNOISEEN	I2CRDTREN	I2CTOEN
Reset	–	–	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	–	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
I2CFSCL	15	I^2C Master SCL Speed Selection 0 = f_{SCL} = 100kHz 1 = f_{SCL} = 400kHz (default) This bit determines f_{SCL} used for the transaction initiated by the I^2C master in respose to a write to I2CSEND.
I2CWALT	14	I^2C Master Alternate Write Mode Selection 0 = Normal Mode (1, 2, 3, or 4 Byte Data) 1 = Alternate Mode (1, 2, 0, or 4 Byte Data) This bit determines the data lengths available in Write mode using I2CDATALNGTH selection bits.

BITFIELD	BITS	DESCRIPTION
I2CRFMT	13	I2C Master Read Format Selection 0 = Normal Format 1 = Combined Format (default) This bit determines the format used for Read mode transactions initiated by the I2C master in respose to a write to I2CSEND (does not impact Write mode transactions).
I2C10BIT	12	I2C Master Address Mode Selection 0 = 7-Bit Addressing (default) 1 = 10-Bit Addressing This bit determines the address format used for the transaction initiated by the I2C master in respose to a write to I2CSEND.
I2CPNTRLNGTH	11	I2C Transaction Pointer Length Selection 0 - 1-Byte Pointer (default) 1 - 2-Byte Pointer This is the pointer length used for the requested I2C master transactions. If 1-Byte Pointer mode is used (default, standard), both pointer bytes are available for use in I2C master transactions using I2CPNTRSEL (minimizing configuration time).
I2CALRTEN	10	I2C Alert Enable 0 = ALRTI2C Reporting Disabled (default) 1 = ALRTI2C Reporting Enabled If enabled, STATUS2:ALRTI2C reflects the bitwise OR of enabled/unmasked I2C fault indicators I2CSTAT[8:0]. The alert can be masked by setting I2CALRTEN = 0. The alert will be cleared when I2CSTAT is cleared and no new faults have been reported.
I2CANACONTEN	5	I2C Bus Analog Contention Report Enable 0 = Bus Contention Monitoring Masked (default) 1 = Bus Contention Monitoring Reported See the data sheet for a detailed explanations of bus monitoring operations and limitations (such as setup and hold timing violations, glitch detection, and noise handling). A zero selection will still allow the monitor circuitry to run and report results in I2CSTAT:I2CCONT, but the monitored condition will not trigger an ALRTI2C issuance or an I2CSTAT:I2CSTATUS Transaction Error (10).
I2CCONTEN	4	I2C Bus Digital Contention Report Enable 0 = Bus Contention Monitoring Masked (default) 1 = Bus Contention Monitoring Reported See the data sheet for a detailed explanations of bus monitoring operations and limitations (such as setup and hold timing violations, glitch detection, and noise handling). A zero selection will still allow the monitor circuitry to run and report results in I2CSTAT:I2CCONT, but the monitored condition will not trigger an ALRTI2C issuance or an I2CSTAT:I2CSTATUS Transaction Error (10).

BITFIELD	BITS	DESCRIPTION
I2CGLITCHEN	3	I²C Bus Glitch Report Enable 0 = Bus Glitch Monitoring Masked (default) 1 = Bus Glitch Monitoring Reported See the data sheet for a detailed explanations of bus monitoring operations and limitations (such as setup and hold timing violations, glitch detection, and noise handling). A zero selection will still allow the monitor circuitry to run and report results in I2CSTAT:I2CGLITCH, but the monitored condition will not trigger an ALRTI2C issuance or an I2CSTAT:I2CSTATUS Transaction Error (10).
I2CNOISEEN	2	I²C Bus Noise Report Enable 0 = Bus Noise Monitoring Masked (default) 1 = Bus Noise Monitoring Reported See the data sheet for a detailed explanations of bus monitoring operations and limitations (such as setup and hold timing violations, glitch detection, and noise handling). A zero selection will still allow the monitor circuitry to run and report results in I2CSTAT:I2CNOISE, but the monitored condition will not trigger an ALRTI2C issuance or an I2CSTAT:I2CSTATUS Transaction Error (10).
I2CRDTREN	1	I²C Redundant Read Check Enable 0 = Redundant Read Check Disabled (default) 1 = Redundant Read Check Enabled See the data sheet for a detailed explanation of redundant read check operations and limitations. This bit enables both Redundant Read transactions as well as discrepancy reporting.
I2CTOEN	0	I²C Timeout Enable 0 = DIsable I²C Transaction Watchdog (default) 1 = Enable I²C Transaction Watchdog

I2CSTAT (0x8A)

I2CSTAT is a read- and write-accessible register that shows the current status of the I²C master.

The I2CSTATUS bits are updated in real time, indicating the current state of the I²C master and any requested transaction. This status content can be cleared by write operations and modified by transaction progress or subsequent transaction requests.

The second byte contains I²C fault bits, indicating a fault was observed during an I²C transaction. These bits are updated as they occur and are only cleared by writing to 0. Several faults may occur during a corrupted transaction, so it is best to wait until I2CSTATUS reads 10 (Transaction Error) to ensure all errors have been reported.

While not advisable, if further I²C transactions are requested before the I²C fault bits from previous transactions are read back and cleared, a cumulative history of faults will be listed, even if subsequent transactions are successful.

BIT	15	14	13	12	11	10	9	8
Field	I2CSTATUS[1:0]		–	–	–	–	–	I2CRJCT
Reset	0b00		–	–	–	–	–	0b0
Access Type	Write, Read, Ext		–	–	–	–	–	Write, Read, Ext

BIT	7	6	5	4	3	2	1	0
Field	I2CDEVNACK	I2CDATANACK	I2CANACONT	I2CCONT	I2CGLITCH	I2CNOISE	I2CRDTRERR	I2CTIMEOUT
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write 0 to Clear, Read	Write 0 to Clear, Read	Write 0 to Clear, Read	Write 0 to Clear, Read	Write 0 to Clear, Read	Write 0 to Clear, Read	Write 0 to Clear, Read	Write 0 to Clear, Read

BITFIELD	BITS	DESCRIPTION
I2CSTATUS	15:14	I^2C Status Indicator 00 - No Transaction Requested (default) 01 - Transaction in Progress 10 - Transaction Error 11 - Transaction Complete I2CSTATUS indicates the current status of the I^2C master. These status bits will be cleared when written to 0 or when a new transaction is begun using I2CSEND. Writing to a logic 1 has no effect. Note specific clear/update behavior.
I2CRJCT	8	I^2C Transaction Reject Error Inidcator 0 = No Error Reported (default) 1 = I^2C Operation Rejected Indicates one or more I^2C master operations were rejected because 1) a user Write to I2CSEND requested a new I^2C transaction during an active I^2C transaction, 2) a user Write to a protected I^2C master register was attempted during an active I^2C transaction, or 3) a user Read from an I2CRDATA register was requested during an active I^2C Read transaction. See I^2C master register descriptions for complete details. Cleared only by writing to a logic 0. Writing to a logic 1 has no effect.
I2CDEVNACK	7	I^2C Device ID Not Acknowledged Inidcator 0 = No Error Reported (default) 1 = Slave Address Not Acknowledged Indicates the I^2C transaction Device ID byte(s) were not acknowledged by a slave. This may indicate the slave is malfunctioning or not present on the bus. For Combined Format Read transactions, both slave address acknowledge pulses are required to avoid an error. Cleared only by writing to a logic 0. Writing to a logic 1 has no effect.
I2CDATANACK	6	I^2C Data Not Acknowledged Inidcator 0 = No Error Reported (default) 1 = Data Byte Not Acknowledged Indicates one or more I^2C transaction data byte(s) written were not acknowledged by a slave. This may indicate the slave is malfunctioning, not present on the bus, is busy, or has rejected an unsupported transaction. Cleared only by writing to a logic 0. Writing to a logic 1 has no effect.

BITFIELD	BITS	DESCRIPTION
I2CANACONT	5	I²C Bus Analog Contention Error 0 = No Error Reported (default) 1 = I²C Bus Contention Error Reported Indicates an analog bus contention condition was observed. Analog contention is reported when the sampled SDA value does not match the value driven by the I²C master. This monitor observes the analog-filtered SDA port sampled by the analog-filtered SCL port when driven by the I²C master, emulating the filter circuitry typically used in I²C slave devices. Note that incoming SDA data from slaves in Read mode is latched using the analog-filtered versions of SDA and SCL. Cleared only by writing to a logic 0. Writing to a logic 1 has no effect.
I2CCONT	4	I²C Bus Digital Contention Error 0 = No Error Reported (default) 1 = I²C Bus Contention Error Reported Indicates a bus contention condition was observed. Digital contention is reported when a digital oversampled port result does not match the value driven by the I²C master. This monitor observes the unfiltered SCL port and the SDA port when driven by the I²C master during periods when the signals should be settled. Digitally oversampled contention is more sensitive than analog contention (which employs analog filters). Cleared only by writing to a logic 0. Writing to a logic 1 has no effect.
I2CGLITCH	3	I²C Bus Glitch Error 0 = No Error Reported (default) 1 = I²C Bus Glitch Error Reported Indicates a bus glitch condition was observed. A glitch is reported when a digitally oversampled port monitor reports two or more consecutive samples that disagree with the digitally evaluated filter value. This condition may also be reported if slow transition times, setup time, or hold time violations occur (outside I²C specifications). This monitor observes the unfiltered SCL port and the SDA port outside specified transition intervals. Cleared only by writing to a logic 0. Writing to a logic 1 has no effect.
I2CNOISE	2	I²C Bus Noise Error 0 = No Error Reported (default) 1 = I²C Bus Noise Error Reported Indicates a noisy bus condition was observed. A noise condition is reported when a digitally oversampled port monitor reports a large amount of samples (>25%) that disagree with the evaluated filter value. This condition may also be reported if slow transition times, setup time, or hold time violations occur (outside I²C specifications). This monitor observes the unfiltered SCL port and the SDA port outside specified transition intervals. Cleared only by writing to a logic 0. Writing to a logic 1 has no effect.

BITFIELD	BITS	DESCRIPTION
I2CRDTRERR	1	I2C Redundant Read Error Inidcator 0 = No Error Reported (default) 1 = I2C Redundant Read Error Reported Indicates the results of an I2C Redundant Read Transaction Check failed. This means the data read back in the first read transaction did not match the data in the second read transaction. This function is only enabled if I2CRDTREN = 1. Cleared only by writing to a logic 0. Writing to a logic 1 has no effect.
I2CTIMEOUT	0	I2C Time Out Error Inidcator 0 = No Error Reported (default) 1 = I2C Transaction Timed Out Indicates the transaction did not complete in the expected period of time. This function is only enabled if I2CTOEN = 1. Cleared only by writing to a logic 0. Writing to a logic 1 has no effect.

I2CSEND (0x8B)

I2CSEND is a read- and write-accessible register that configures and initiates an I2C master transaction.

A write to this register will initiate an I2C master transaction. Only one transaction is supported at any given time. If a write to I2CSEND occurs during an active I2C transaction already in progress, the latest transaction request will be ignored and the I2CSEND contents will not be updated. If this occurs, an I2CRJCT fault will be issued.

A read from this register will readback the current contents. This will represent the last transaction request accepted by the I2C master.

BIT	15	14	13	12	11	10	9	8
Field	I2CPNTRSEL	I2CDATALNGTH[1:0]		I2CDATASEL[1:0]		I2CDEVIDEXT[2:0]		
Reset	0b0	0b01		0b01		0b000		
Access Type	Write, Read	Write, Read		Write, Read		Write, Read		

BIT	7	6	5	4	3	2	1	0
Field	I2CDEVID[6:0]							I2CRWB
Reset	0x00							0b0
Access Type	Write, Read							Write, Read, Ext

BITFIELD	BITS	DESCRIPTION
I2CPNTRSEL	15	I2C Transaction Pointer Selection 0 - Use I2CPBYTE0 1 - Use I2CPBYTE1 Selects the Pointer byte used for the requested I2C Master Write mode or Combined Format Read mode transaction. If I2CPNTRLNGTH = 1 (2-byte pointer mode), this bit is ignored and both bytes are sent.

BITFIELD	BITS	DESCRIPTION
I2CDATALNGTH	14:13	I²C Transaction Data Length 00 - 1-Byte Read and Write 01 - 2-Byte Read and Write (default) 10 - 3-Byte Read, 3- or 0-Byte Write 11 - 4-Byte Read and Write This is the data length used for the requested I²C master transaction. When I2CWALT mode is engaged, the 3-Byte Data Length option is replaced by a 0-Byte Data option for Write mode only.
I2CDATASEL	12:11	I²C Data Location Selection 00 - Byte 0 01 - Byte 1 (default) 10 - Byte 2 11 - Byte 3 Selects the location of the data bytes(s) to be transferred during Write transactions and the target location for data byte(s) used for storage during Read transactions. The selection indicates the location of the MSB of the data space used during the transaction; the number of bytes used is set by I2CDATALNGTH. Some limitations do apply; see the data sheet for details.
I2CDEVIDEXT	10:8	I²C Device ID Extension This is the 3-Bit Device ID Extension (Slave Address[9:7]) available for I²C master transactions in 10-Bit Address mode. This content is ignored in 7-Bit Address mode.
I2CDEVID	7:1	I²C Device ID This is the Device ID (Slave Address[6:0]) used for the requested I²C master transaction.
I2CRWB	0	I²C R/WB Master Transaction Type 0 = Write Mode Transaction (default) 1 = Read Mode Transaction This bit determines transaction type initiated by the I²C master in response to a write to I2CSEND.

ID1 (0x8C)

ID1 is a read-accessible register that contains the 2 LSBs of the unique device ID stored in ROM, and is subject to ROMCRC validation.

BIT	15	14	13	12	11	10	9	8
Field	DEVID[15:8]							
Reset								
Access Type	Read Only							

BIT	7	6	5	4	3	2	1	0
Field	DEVID[7:0]							
Reset								
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
DEVID	15:0	Device ID (partial) The 1 LSB of the 40-bit factory-programmed device ID. ID1[0] always reads logic 1. A valid device ID has two or more bits set to logic 1. Read only.

ID2 (0x8D)

ID2 is a read-accessible register that contains the 2 MSBs of the unique device ID stored in ROM, and is subject to ROMCRC validation.

BIT	15	14	13	12	11	10	9	8
Field	DEVID[31:24]							
Reset								
Access Type	Read Only							

BIT	7	6	5	4	3	2	1	0
Field	DEVID[23:16]							
Reset								
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
DEVID	15:0	Device ID (partial) Two bytes of the 40-bit factory-programmed device ID. A valid device ID has two or more bits set to logic 1. Read only.

ID3 (0x8E)

ID3 is a read-accessible register that contains the MSB of the unique device ID and factory calibration data stored in ROM, and is subject to ROMCRC validation.

BIT	15	14	13	12	11	10	9	8
Field	OTP2[7:0]							
Reset								
Access Type	Read Only							

BIT	7	6	5	4	3	2	1	0
Field	DEVID[39:32]							
Reset								
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
OTP2	15:8	Factory Calibration Data Read only.
DEVID	7:0	Device ID (partial) The MSB of the 40-bit factory-programmed device ID. A valid device ID has two or more bits set to logic 1. Read only.

OTP3REG (0x8F)

Factory Calibration Data ROM and subject to ROMCRC validation.

BIT	15	14	13	12	11	10	9	8
Field	OTP3[15:8]							
Reset								
Access Type	Read Only							

BIT	7	6	5	4	3	2	1	0
Field	OTP3[7:0]							
Reset								
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
OTP3	15:0	Factory Calibration Data Read only.

OTP4REG (0x90)

Factory Calibration Data ROM and subject to ROMCRC validation.

BIT	15	14	13	12	11	10	9	8
Field	OTP4[1:0]		ALTREF_OTP[13:8]					
Reset								
Access Type	Read Only		Read Only					

BIT	7	6	5	4	3	2	1	0
Field	ALTREF_OTP[7:0]							
Reset								
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
OTP4	15:14	Factory Calibration Data Read only.
ALTREF_OTP	13:0	Factory Calibration Data Read only.

OTP5REG (0x91)

Factory Calibration Data ROM and subject to ROMCRC validation.

BIT	15	14	13	12	11	10	9	8
Field	OTP5[15:8]							
Reset								
Access Type	Read Only							

BIT	7	6	5	4	3	2	1	0
Field	OTP5[7:0]							
Reset								
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
OTP5	15:0	Factory Calibration Data Read only.

OTP6REG (0x92)

Factory Calibration Data ROM and subject to ROMCRC validation.

BIT	15	14	13	12	11	10	9	8
Field	OTP6[15:8]							
Reset								
Access Type	Read Only							

BIT	7	6	5	4	3	2	1	0
Field	OTP6[7:0]							
Reset								
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
OTP6	15:0	Factory Calibration Data Read only.

OTP7REG (0x93)

Factory Calibration Data ROM and subject to ROMCRC validation.

BIT	15	14	13	12	11	10	9	8
Field	OTP7[15:8]							
Reset								
Access Type	Read Only							

BIT	7	6	5	4	3	2	1	0
Field	OTP7[7:0]							
Reset								
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
OTP7	15:0	Factory Calibration Data Read Only.

OTP8REG (0x94)

Factory Calibration Data ROM and subject to ROMCRC validation.

BIT	15	14	13	12	11	10	9	8
Field	OTP8[15:8]							
Reset								
Access Type	Read Only							

BIT	7	6	5	4	3	2	1	0
Field	OTP8[7:0]							
Reset								
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
OTP8	15:0	Factory Calibration Data Read only.

OTP9REG (0x95)

Factory Calibration Data ROM and subject to ROMCRC validation.

BIT	15	14	13	12	11	10	9	8
Field	OTP9[15:8]							
Reset								
Access Type	Read Only							

BIT	7	6	5	4	3	2	1	0
Field	OTP9[7:0]							
Reset								
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
OTP9	15:0	Factory Calibration Data Read only.

OTP10REG (0x96)

Factory Calibration Data ROM and subject to ROMCRC validation.

BIT	15	14	13	12	11	10	9	8
Field	OTP10[15:8]							
Reset								
Access Type	Read Only							

BIT	7	6	5	4	3	2	1	0
Field	OTP10[7:0]							
Reset								
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
OTP10	15:0	Factory Calibration Data Read Only.

OTP11REG (0x97)

Factory Calibration Data ROM and subject to ROMCRC validation.

BIT	15	14	13	12	11	10	9	8
Field	OTP11[15:8]							
Reset								
Access Type	Read Only							

BIT	7	6	5	4	3	2	1	0
Field	OTP11[7:0]							
Reset								
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
OTP11	15:0	Factory Calibration Data Read Only.

OTP12REG (0x98)

Factory Calibration Data ROM and subject to ROMCRC validation.

BIT	15	14	13	12	11	10	9	8
Field	ROMCRC[7:0]							
Reset								
Access Type	Read Only							

BIT	7	6	5	4	3	2	1	0
Field	OTP12[7:0]							
Reset								
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
ROMCRC	15:8	ROM CRC Value 8-bit CRC value computed from the onboard read-only memory content. ID and OTP ROM output data content is protected by a 8-bit CRC with polynomial 0xA6 ($x^8+x^6+x^3+x^2+1$). Read only.
OTP12	7:0	Factory Calibration Data Read Only.

Applications Information

Vehicle Applications

Battery cells can use various chemistries such as NiMH, Li+ (NMC, LFP, LTO), supercap, or lead-acid. Supercap cells are used in fast-charge applications such as energy storage for regenerative braking. An electric vehicle system may require a high-voltage battery pack voltage from 400V to 800V, which translates from 100 to 200 Li+ cells or up to 500 NiMH cells.

A battery module is a number of cells connected in series that can be connected with other modules to build a high-voltage battery pack as shown in Figure 95. The modularity allows for economy, configurability, quick assembly, and serviceability. The minimum number of cells connected to any one device is limited by the device's minimum operating voltage. The 9V minimum for V_{DCIN} usually requires at least 2 Li+, 6 NiMH, or 6 supercap cells per module.

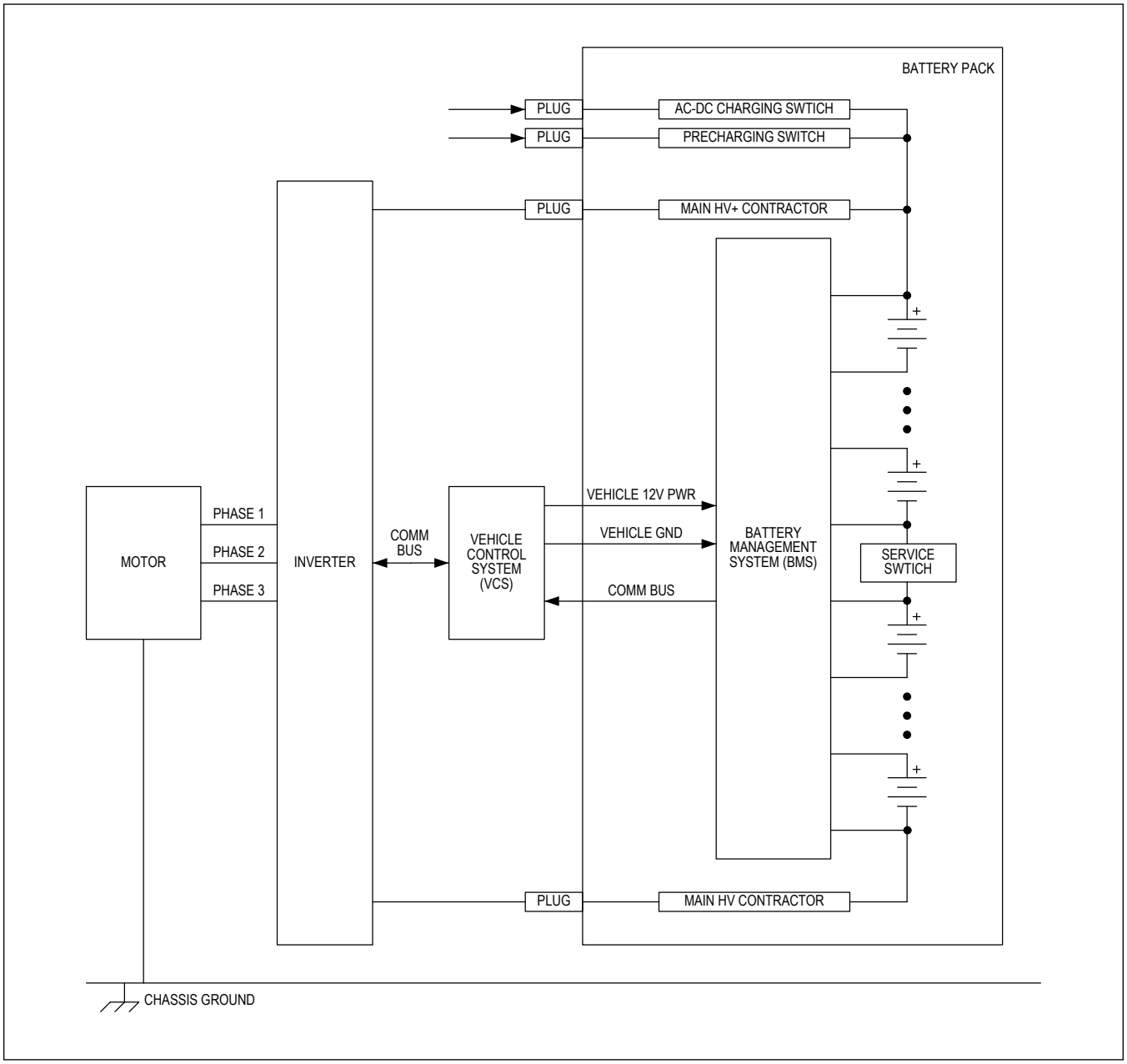


Figure 95. Electric Vehicle System

Battery-Management Systems

Daisy-Chain System

A daisy-chain system employs a communication link between the host microcontroller and all of the battery modules. The daisy-chain method reduces overall system cost as it requires only a single microcontroller, CAN PHY, and transformers between the lowest module and the host whereas all components would require redundant implementation in a non-daisy-chain (distributed CAN system). See the *Distributed CAN Systems* section for further information regarding its

implementation.

Daisy-Chain System Diagram

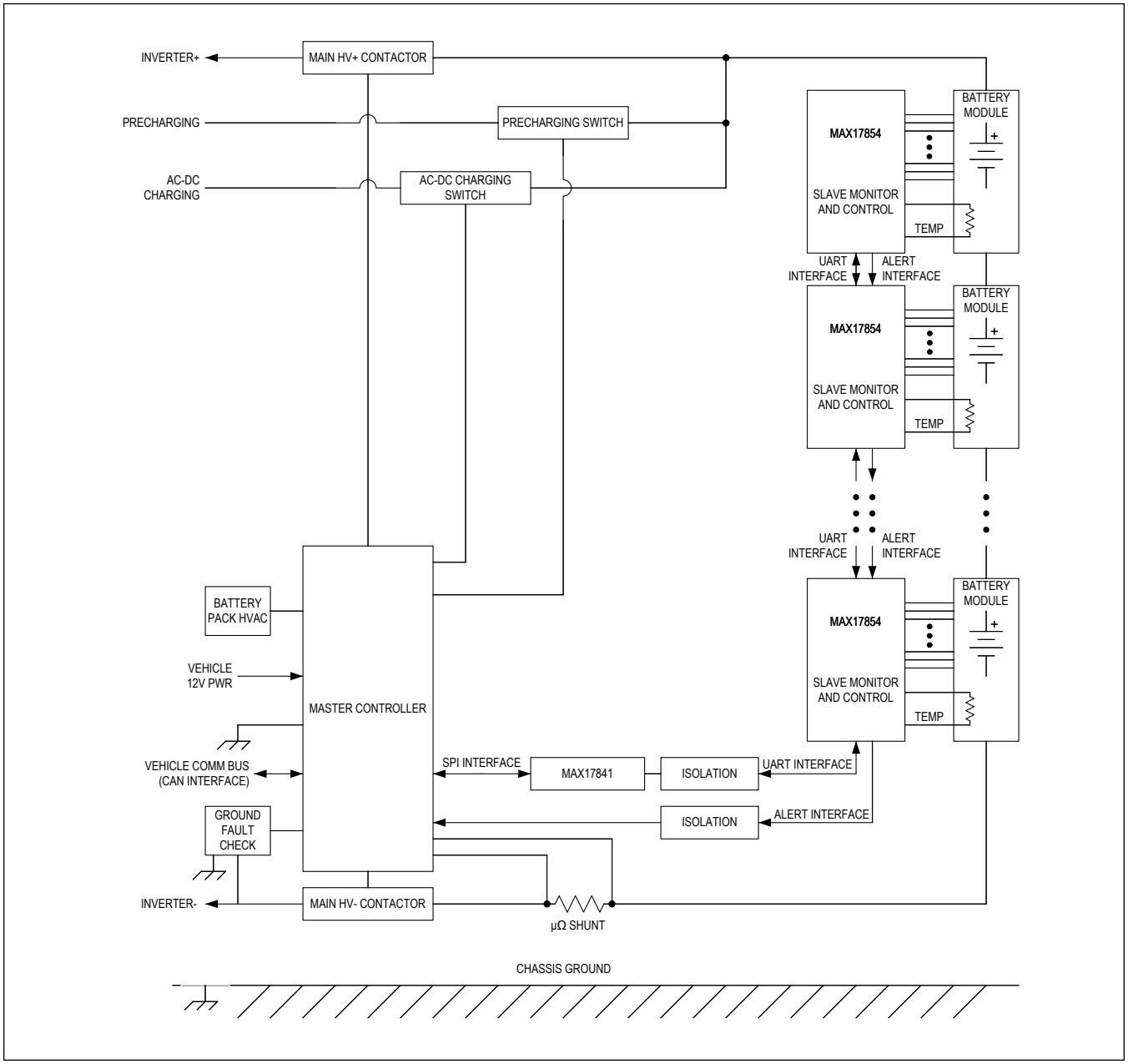


Figure 96. Daisy-Chain System

Distributed CAN Systems

A distributed CAN system as shown below in Figure 97 employs an individual CAN communication interface, battery-management microcontroller, and transformer isolation between each battery module and master controller/ECU. This system architecture, although realizable, yields increased system cost.

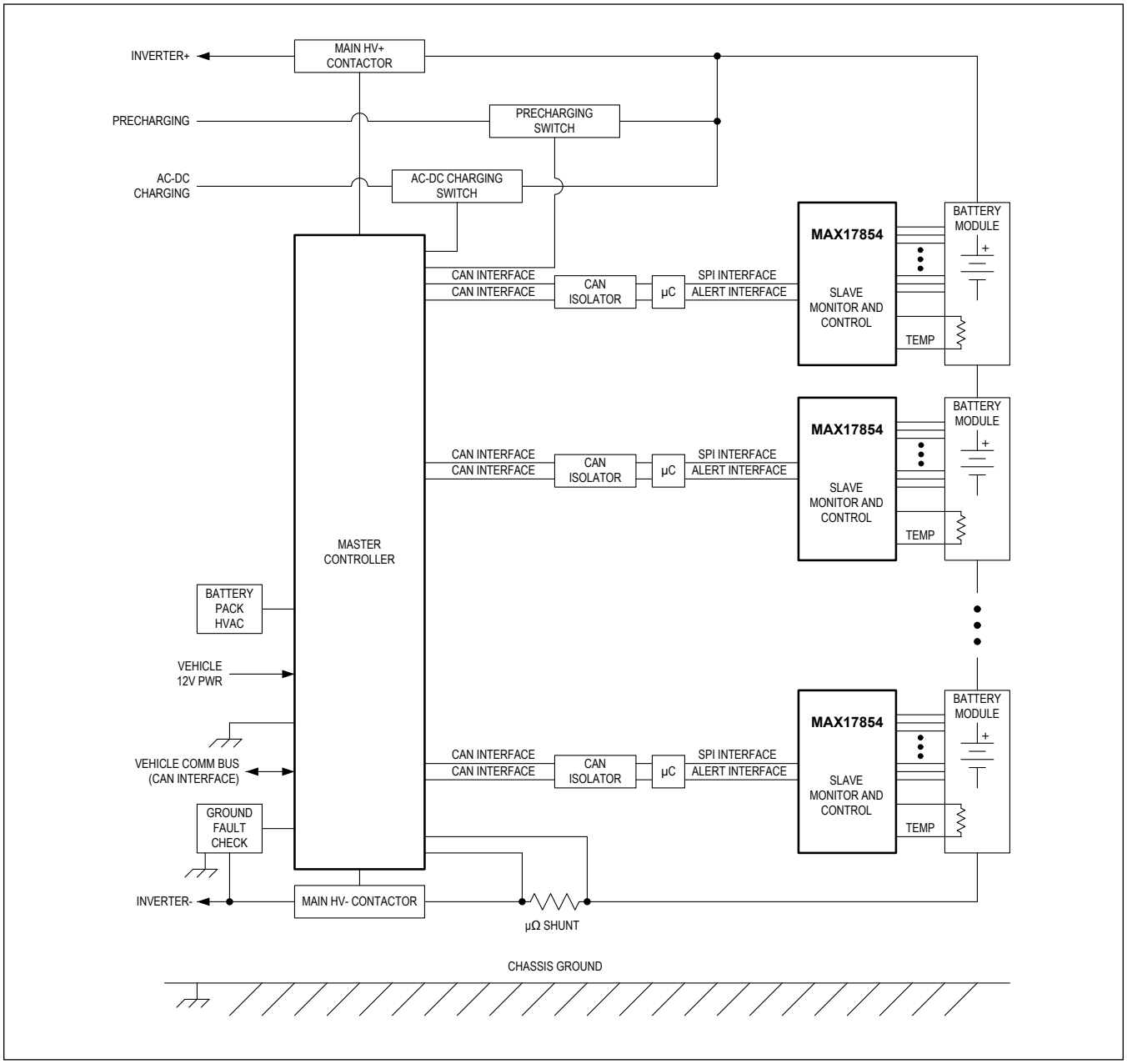


Figure 97. Distributed System

Standard Module Configuration

Power Supply Connection

In a standard module configuration, both internal and external protection circuits permit the MAX17854 to derive its supply directly from the battery module voltage using a filter network connecting the DCIN input to the top cell of the battery pack. These protection circuits protect against transients such as those that may occur when the battery voltage is first connected to the device, when the vehicle inverter is connected to the battery stack, or during charge/

discharge transitions such as regenerative braking. The internal circuits include 72V-tolerant battery inputs and a high noise rejection ratio (PSRR) for the internal low-voltage regulator.

The external protection circuit shown below in Figure 98 filters and clamps the DCIN input. During negative voltage transients, the filter capacitor maintains power the device through the transient.

For maximum measurement accuracy, dedicated wires separate from the cell sense-wires should be used for the power supply connection (Kelvin sense). This is to eliminate voltage drops in the sense-wires induced by supply current. If the application can tolerate the induced error, the supply wires can serve as the sense-wires to reduce the wire count.

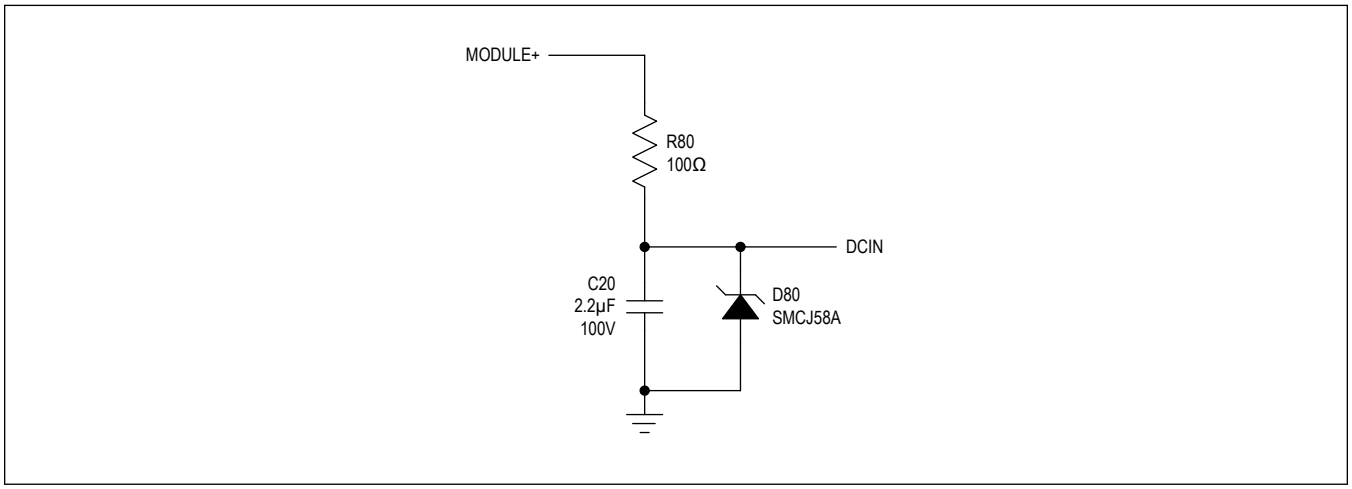


Figure 98. Power Supply Connection

Connecting Cell Inputs

As mentioned in the previous section, the DCIN input should be connected to the battery module's top cell to prevent charge imbalance between cells. If the battery module contains less than 14 cells, the lowest-order inputs (e.g., C1 and C0) should be utilized first and connected to the lowest common-mode signals. Any unused cell inputs should be shorted together and unused switch inputs should be shorted together. The TOPCELL1/2 bits must also be configured for stacks with less than 14 cells to mask out any false alerts corresponding to the unused channels.

Flexible-Pack Configuration

Power Supply, Cell Input Configuration

The Flexible-Pack (Flex-Pack) Configuration provides system flexibility such that a single MAX17854 can meet the requirements of: varying battery module configuration(s) used across multiple mild EV, HEV, and BEV distributed daisy-chain systems, as well as distributed daisy-chain systems which employ unequal module sizes within a standard battery pack.

This flexibility is allowed through internal supply routing of the top battery cell, as well as internal signal routing of the block voltage where these connection were otherwise required by a discrete external traces. Due to this internal routing, the BOM cost may be reduced through the elimination of the DCIN filter resistor as well as the block voltage measurement filter. Unused channels are left unconnected allowing for any battery wiring harness to connect to a standard battery module. See the *Flexible Battery-Pack Configuration* for further details on implementation.

For nondistributed daisy-chain systems (centralized systems), the Flex-Pack eliminates the need to route external sense wires as the voltage drop from the cell cabling can be significantly reduced using the FLXPCKSCAN, resulting a total BOM cost reduction as well as eliminating system cost and constraints for calibration.

External Cell Balancing

The cell-balancing current can be switched by external transistors if more power dissipation is required. The internal switches can be used to switch the external transistors and the power is limited by external current-limiting resistors.

External Cell Balancing Using FET Switches

An application circuit for cell balancing that employs FET switches is shown in Figure 99. $Q_{BALANCE}$ is selected for low V_T that meets the minimum V_{CELLn} requirements of the application during balancing. D_{GATE} protects $Q_{BALANCE}$ from reverse V_{GS} voltage during a hot-plug event. R_{GATE} protects the device by limiting the hot-plug inrush current. C_{GATE} may be added to attenuate transient noise coupled from the drain to the gate to maintain the transistor bias. The cell-balancing current is limited by $R_{BALANCE}$. The various external cell-balancing summary components are as shown in Table 79.

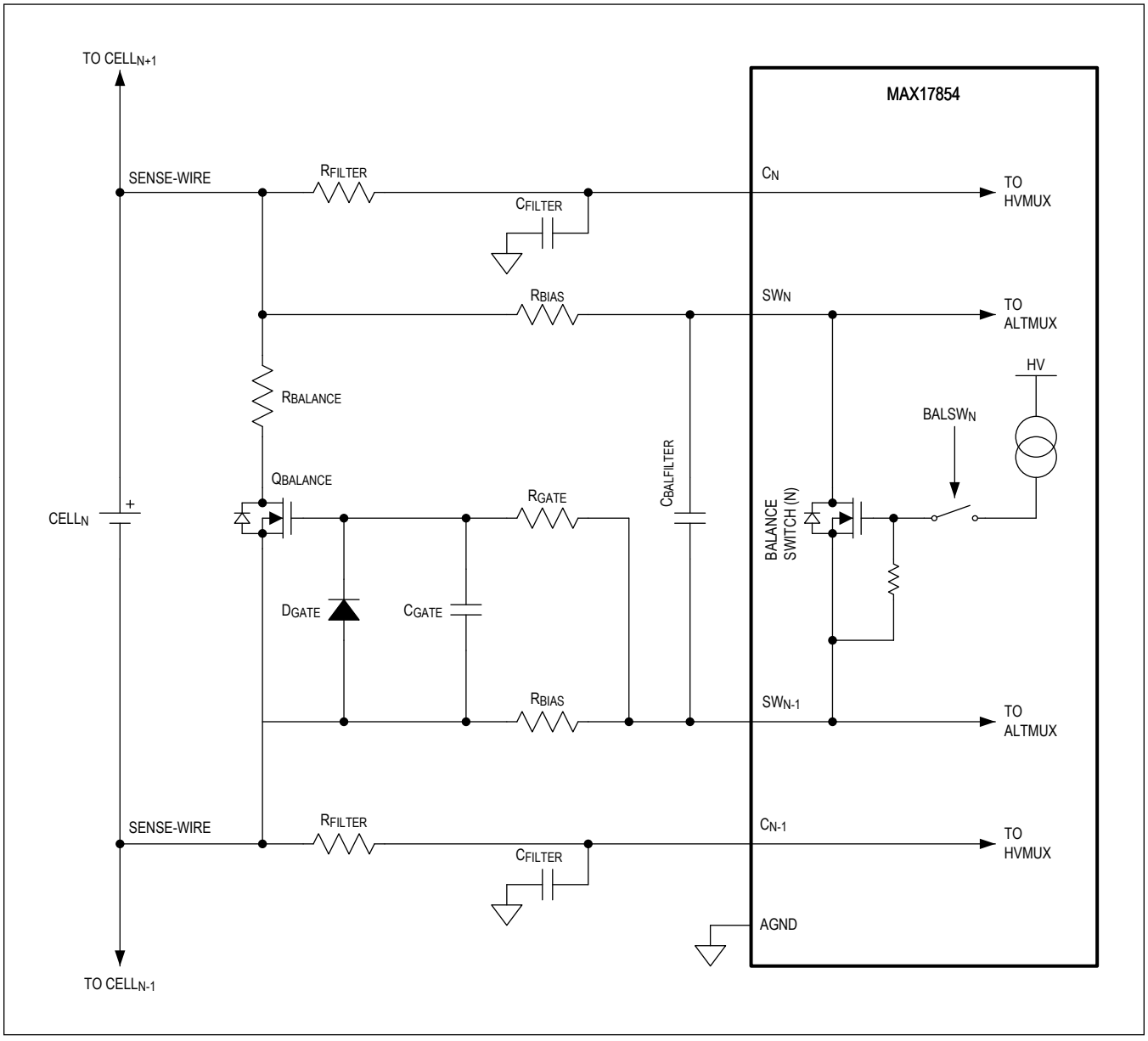


Figure 99. External Balancing FET

Table 79. FET-Balancing Components

COMPONENT NAME	TYPICAL VALUE OR PART	FUNCTION
R_{BIAS}	1kΩ	Voltage-divider for transistor bias
R_{GATE}	100Ω	Hot-plug current-limiting resistor
D_{GATE}	S1B	Reverse-voltage gate protection
C_{GATE}	1nF	Transient V_{GS} suppression
$R_{BALANCE}$	Per application	Balancing current-limiting resistor

Table 79. FET-Balancing Components (continued)

$Q_{BALANCE}$	SQ2310ES	External switch

External Cell Balancing Using BJT Switches

An application circuit for cell balancing that employs BJT switches is shown in Figure 100. $Q_{BALANCE}$ is selected for power dissipation based on the IB drive current available and the cell-balancing current. D_{BASE} protects $Q_{BALANCE}$ from negative V_{GS} during hot-plug events. R_{BASE} protects the device by limiting the hot-plug inrush current. The cell-balancing current is limited by $R_{BALANCE}$. The various external cell-balancing summary components are as shown in Table 80.

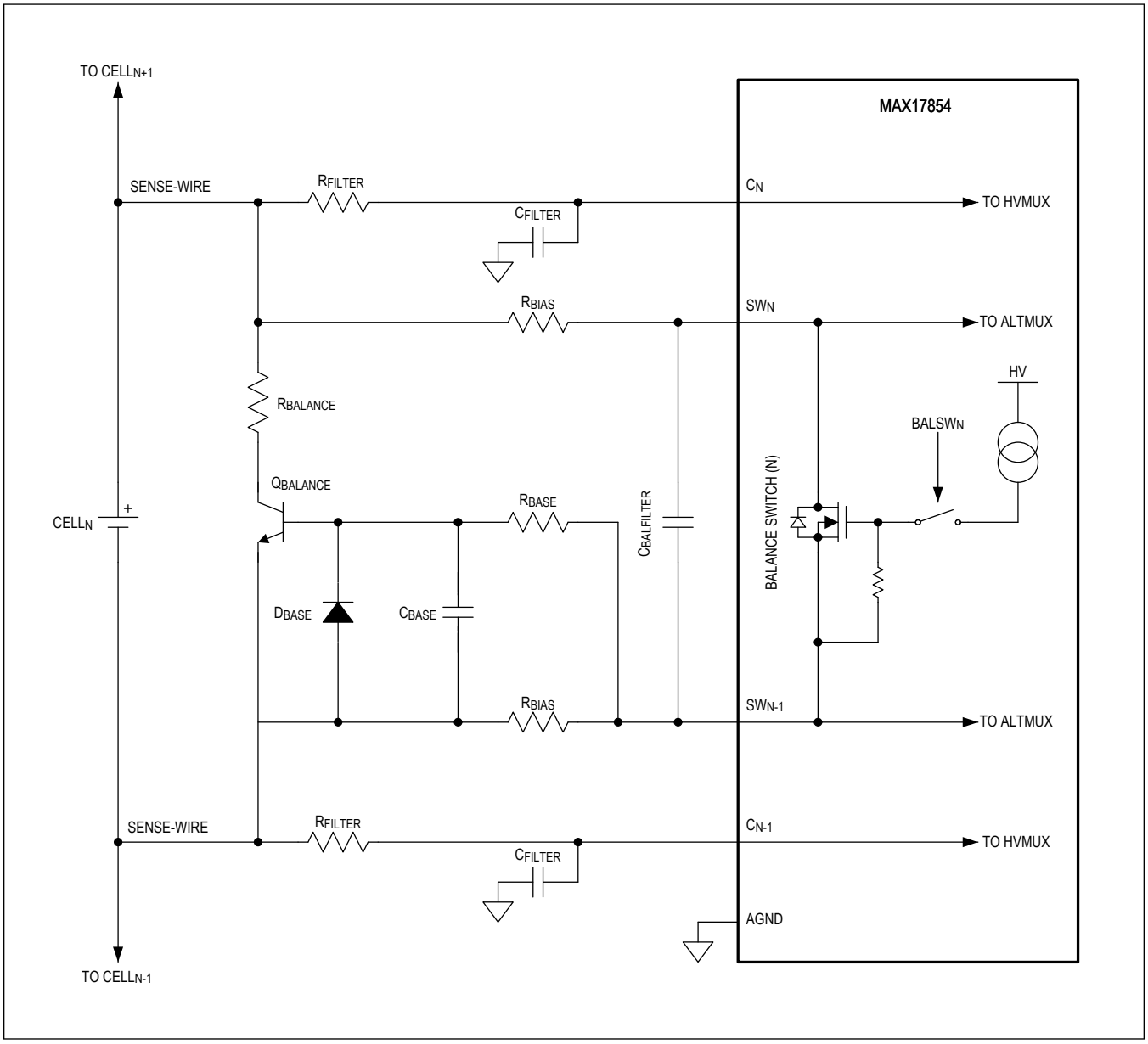


Figure 100. External Cell-Balancing BJT

Table 80. BJT Balancing Components

COMPONENT NAME	TYPICAL VALUE OR PART	FUNCTION
R_{BIAS}	22Ω	Voltage divider for transistor bias
R_{BASE}	15Ω	Hot-plug current-limiting resistor
D_{BASE}	S1B	Reverse emitter-base voltage protection
C_{BASE}	1nF	Transient VBE suppression
$R_{BALANCE}$	Per balancing current requirements	Balancing current-limiting resistor

Table 80. BJT Balancing Components (continued)

$Q_{BALANCE}$	NST489AMT1	External switch

External Cell Balancing Short-Circuit Detection

A short-circuit fault in the external balancing path results in continuous current flow through $R_{BALANCE}$ and $Q_{BALANCE}$. To detect this fault, the voltage drop across the sense-wire parasitic resistance must be measurable. A very small series resistor may added for this purpose.

UART Interface

The UART pins employ both internal and external circuits to protect against noise. The recommended external filters are shown in Figure 101. ESD protection is shown in Figure 103 and Figure 104.

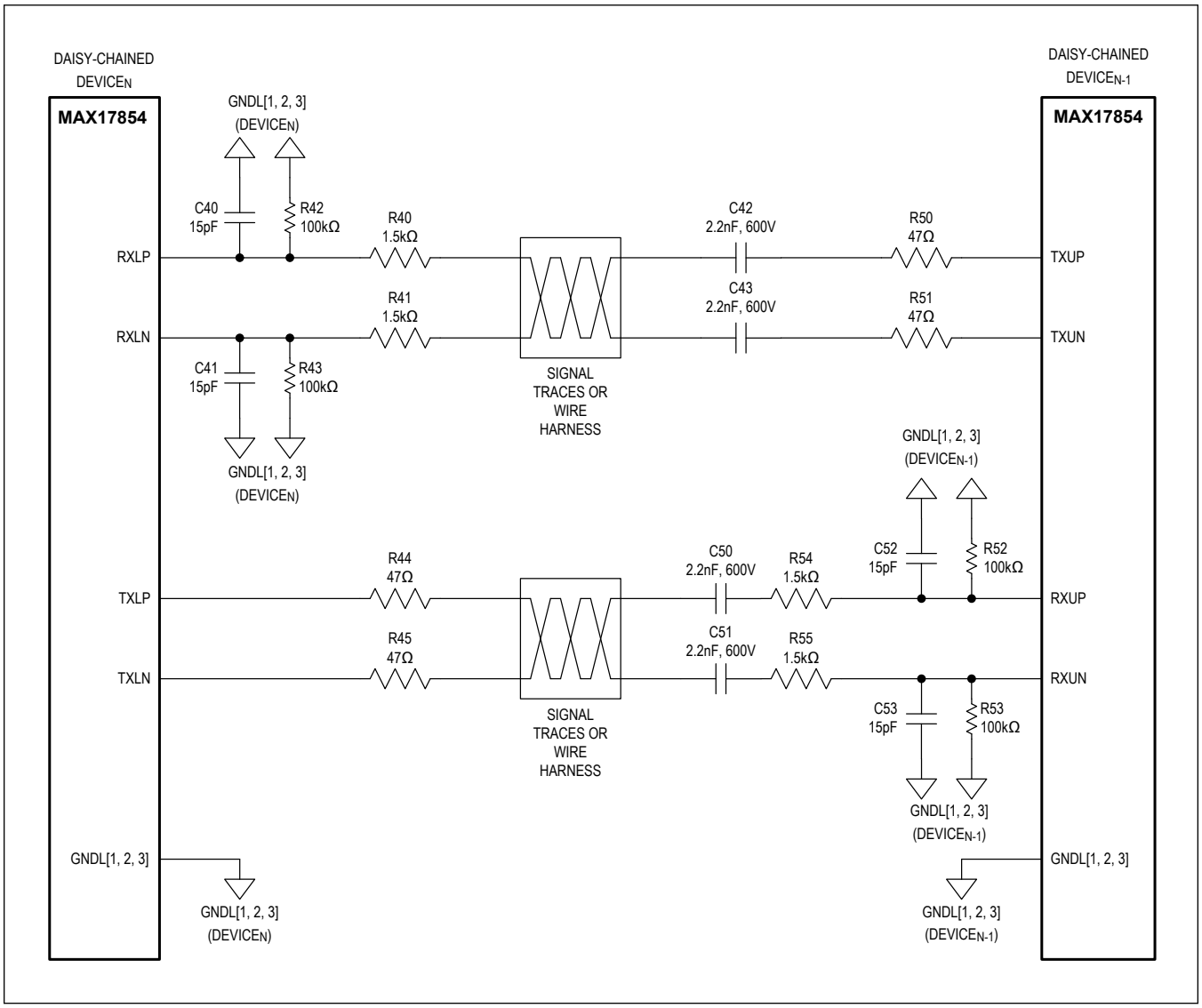


Figure 101. UART Connection

High-Z Idle Mode

The high-Z idle mode reduces radiated emissions from wire harnesses by minimizing the charging and discharging of the AC-coupling capacitors when entering and exiting the idle mode. The application circuit shown in Figure 102 uses a weak resistor-divider to bias the Tx lines to V_{DDL} during the high-Z idle period and PNP transistor clamps to limit the maximum voltage at the Tx pins during high noise injection. The resistor-divider and PNP clamps are not needed for applications utilizing only the low-Z mode. The low-Z and high-Z idle modes both exhibit a similar immunity to noise injection. Low-Z mode may be preferred for ports driving inductive loads to minimize ringing.

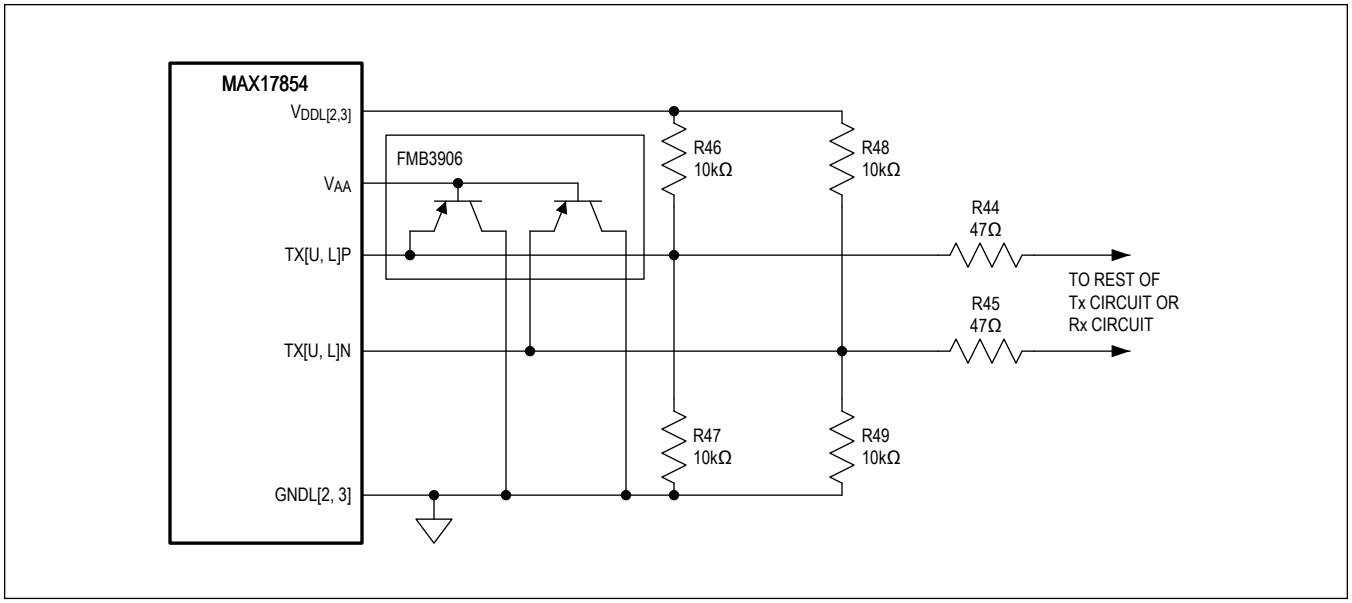


Figure 102. High-Z Idle Mode Application Circuit

UART Supplemental ESD Protection

The UART ports may require supplemental protection to meet IEC61000-4-2 requirements for Contact Discharge. The recommended circuits to meet ±8kV protection levels are shown in Figure 103 and Figure 104. The protection components should be placed as near as possible to the signal's entry point on the PCB.

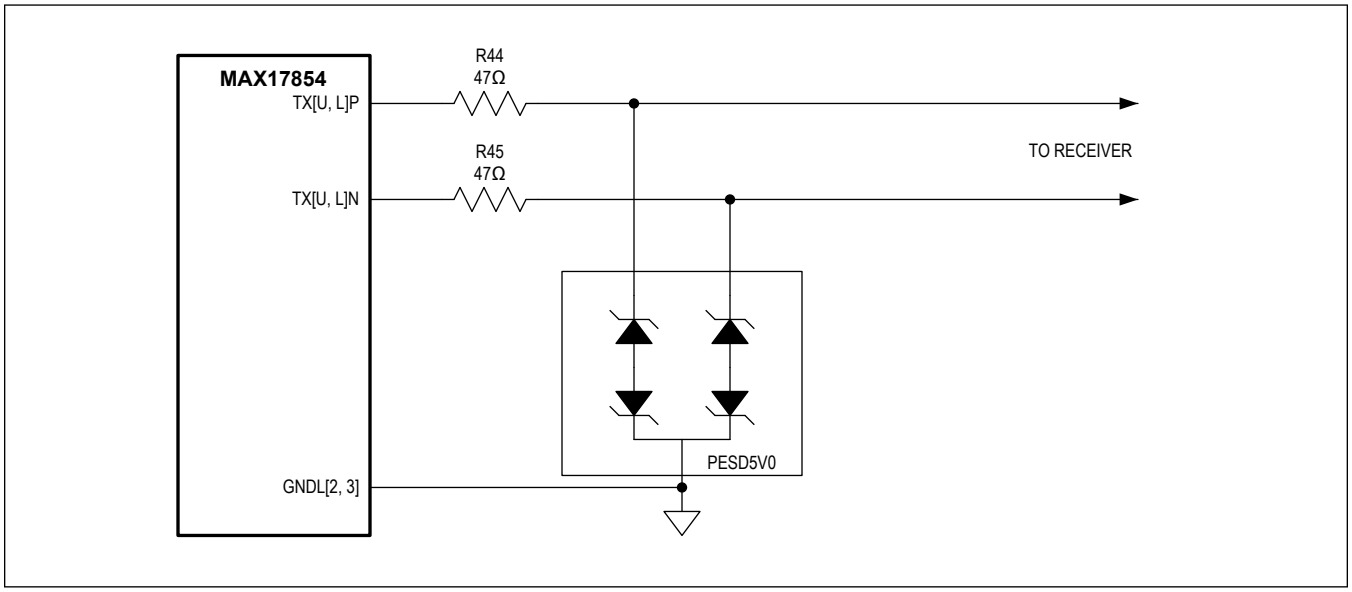


Figure 103. External ESD Protection for UART Tx Ports

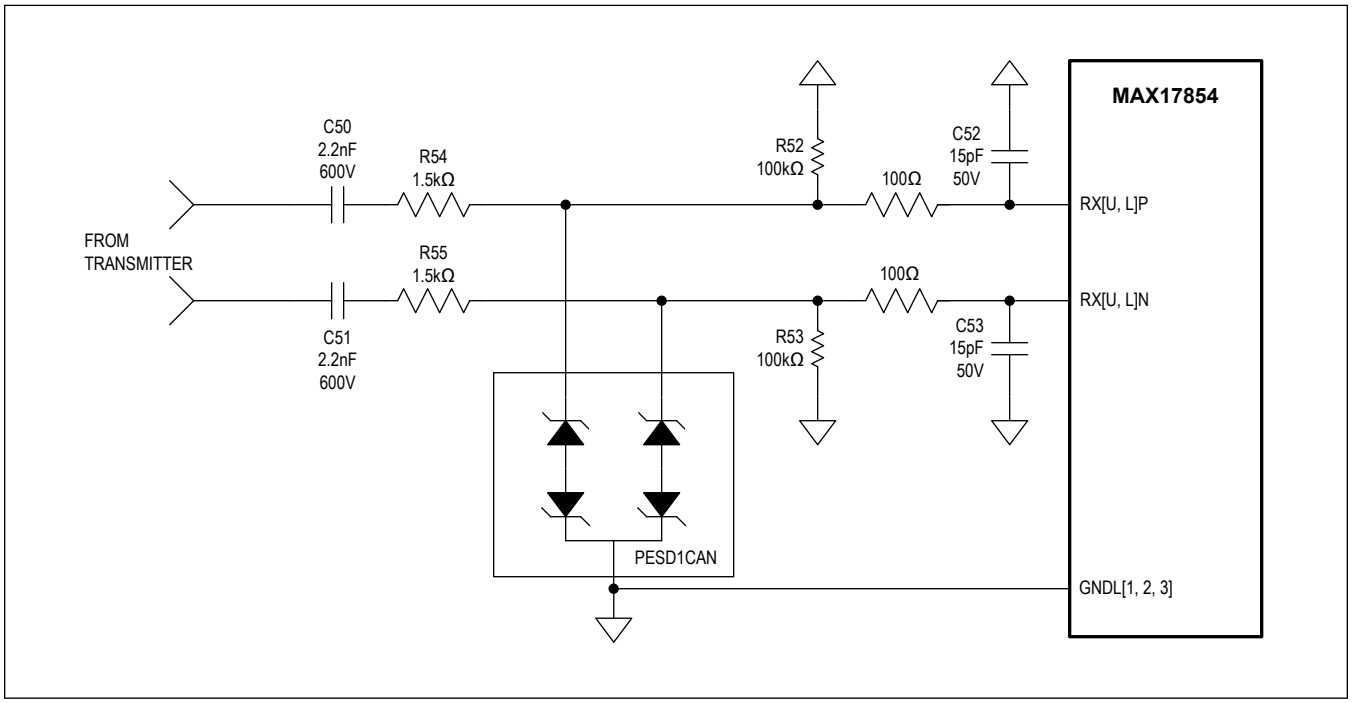


Figure 104. External ESD Protection for UART Rx Ports

Single-Ended Rx Mode

To configure the lower port for single-ended Rx mode, the RXLP input is connected to digital ground and the RXLN input receives the inverted signal, just as it does for differential mode. If the host cannot transmit inverted data, then the signal

must be inverted as shown in Figure 105. Transmitter operation is not affected. If the up-stack device is single-ended, then only the TXUN signal is required.

Note: In single-ended mode, SHDNL must be driven externally.

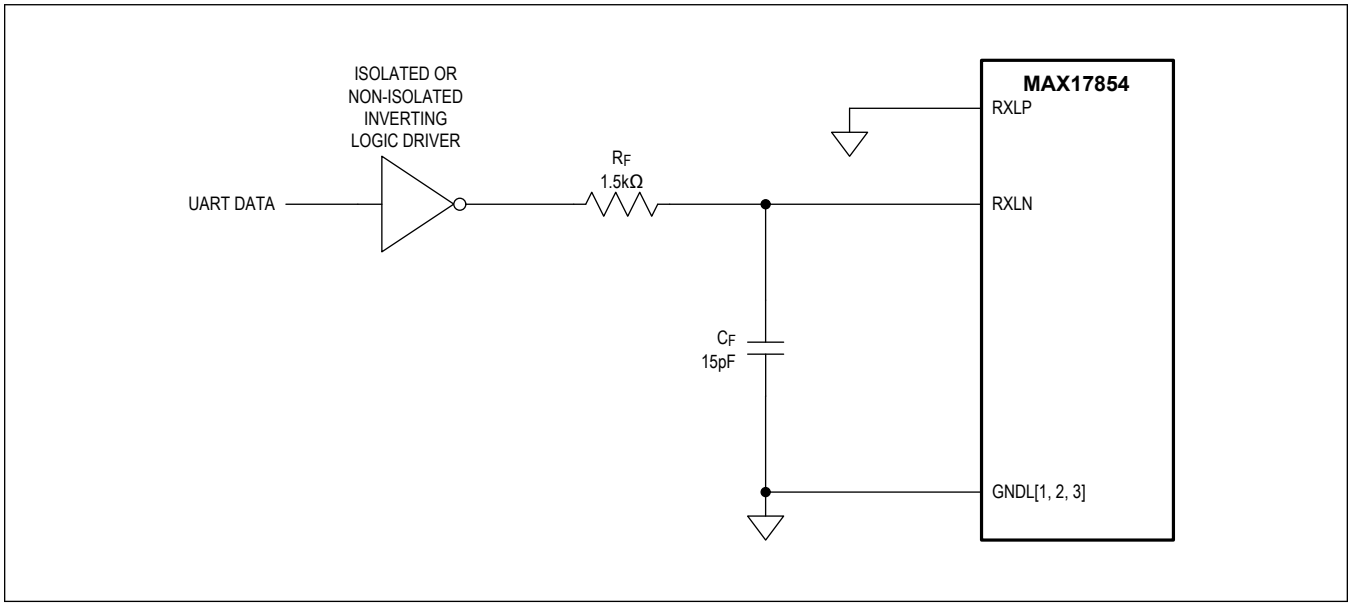


Figure 105. Application Circuit for Single-Ended UART Mode

UART Isolation

The UART is expected to communicate reliably in noisy high-power battery environments where both high dV/dt supply noise and common-mode current injection induced by electromagnetic fields are prevalent. Common-mode currents may also be induced by parasitic coupling of the system to a reference node such as a battery or vehicle chassis. The daisy-chain physical layer is designed for maximum noise immunity.

The AC-coupled differential communication architecture has a ±30V common-mode range and +6V differential swing. This range is in addition to the static common-mode voltage across the AC-coupling capacitors between modules. Transmitter drivers have low internal impedance and are source-terminated by the application circuit so that impedances are well-matched in the high and low driver states. This architecture minimizes differential noise induced by common-mode current injection. The receiver inputs are filtered above the fundamental communication frequency to prevent high-frequency noise from entering the device. The system is designed for use with isolation transformers or optocouplers to provide an even higher degree of common-mode noise rejection in circuit locations where extremely large common-mode noise is present, such as between the vehicle chassis and high-voltage battery pack terminals.

Since a mid-pack service disconnect safety switch is present in many battery packs, the device is designed to communicate with the entire daisy-chain whether the service-disconnect switch is engaged or open. This is possible with daisy-chains that employ capacitor isolation.

UART Transformer Isolation

The UART ports may be transformer-coupled because of their DC-balanced differential design. Transformer coupling between the MAX17841 interface and the MAX17854 provides excellent isolation and common-mode noise rejection. The center-tap of a signal transformer may be used to enhance common-mode rejection by AC-coupling the node to local ground. Common-mode currents that are able to pass through the parasitic coupling of the primary and secondary are shunted to ground to make a very effective common-mode noise filter.

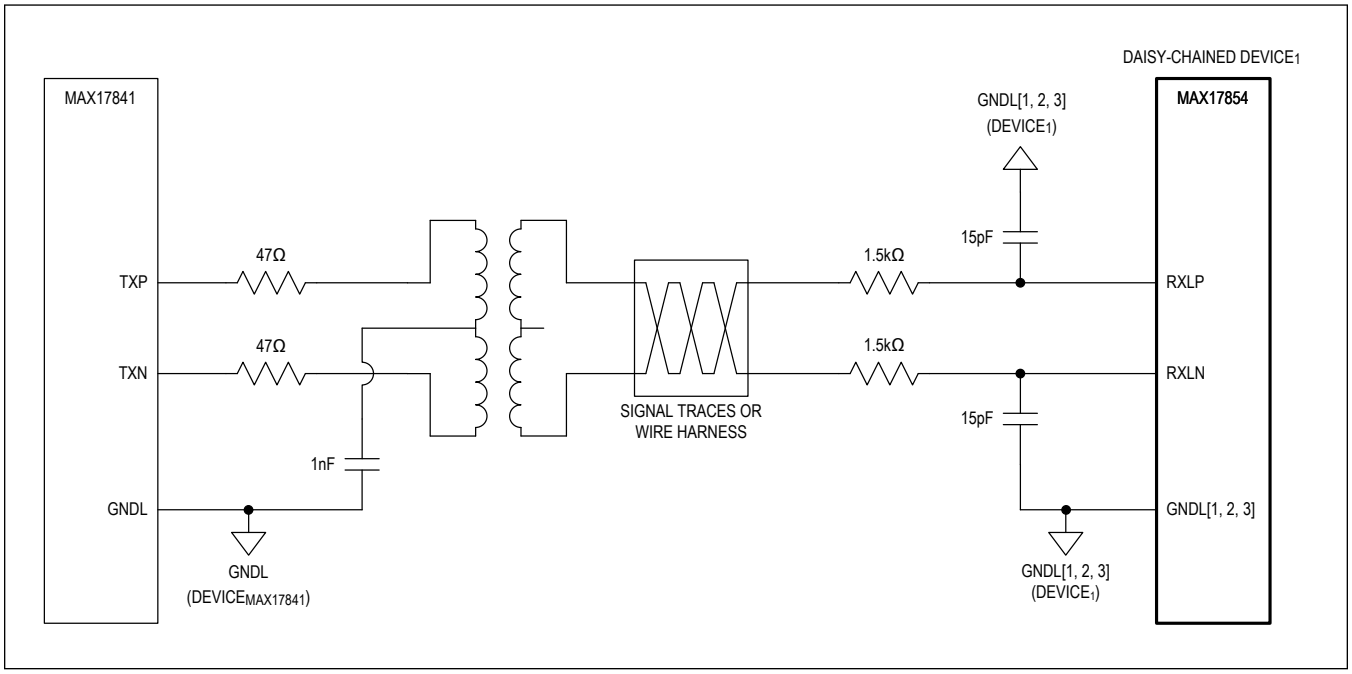


Figure 106. UART Transformer Isolation

UART Optical Isolation

The daisy-chain may use optical isolation instead of transformer or capacitor isolation, as shown in Figure 107.

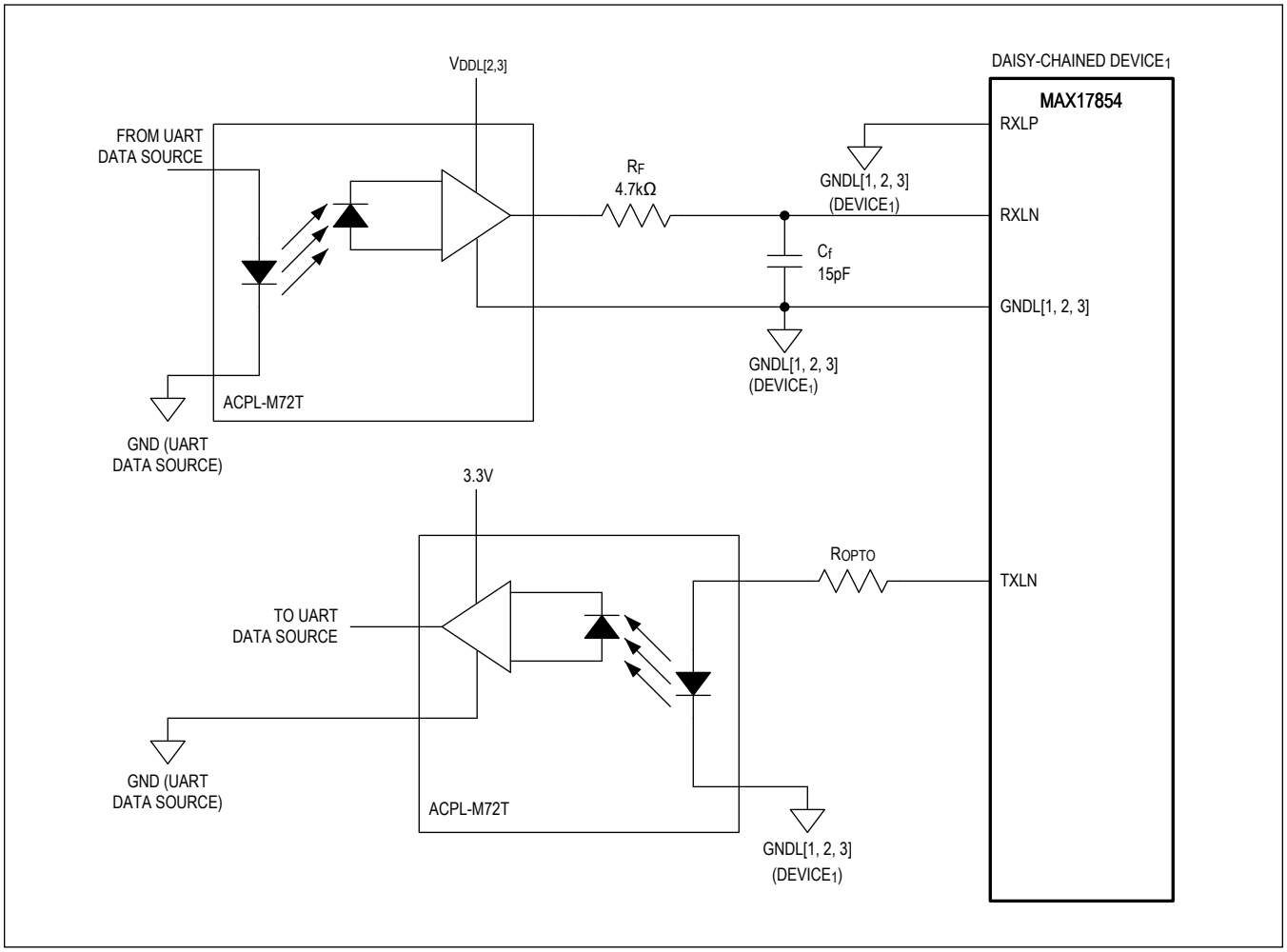


Figure 107. UART Optical Isolation

Alert Interface

V_{DDL2} and V_{DDL3} are the supply pins for the Alert Interface. The recommended external filters and ESD protection are the same as on the UART Interface. When using the single-ended Alert Interface (ALERTIN and ALERTOUT pins) in the UART daisy-chain, optical isolation is used as shown in Figure 108.

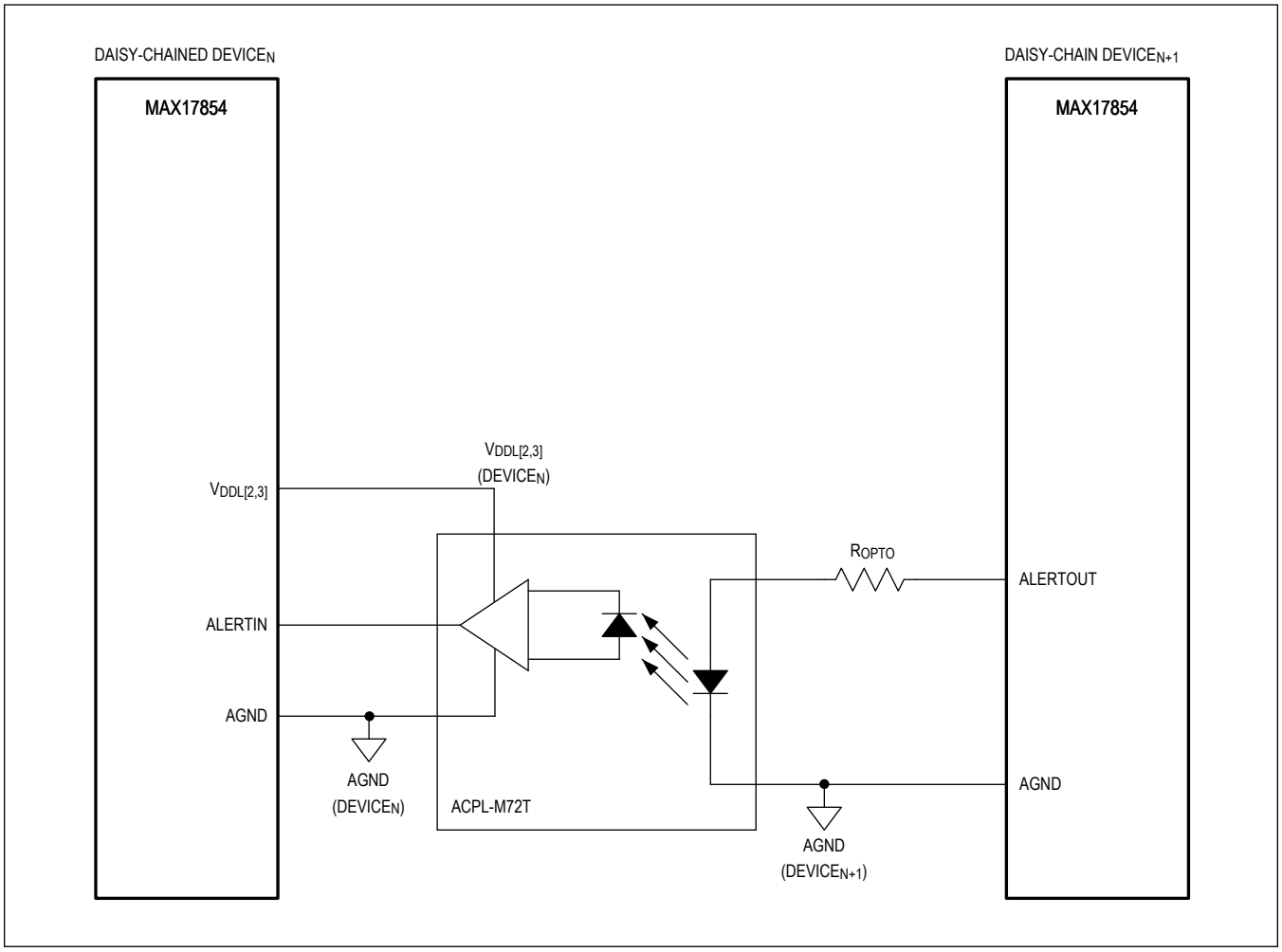


Figure 108. Single-Ended Alert Interface with UART

Device Initialization Sequence

Immediately after reset, all device addresses are set to 0x00 and the UART baud rate and receive modes have not been autodetected. Therefore the following initialization sequence is recommended after every reset or after any change to the hardware configuration:

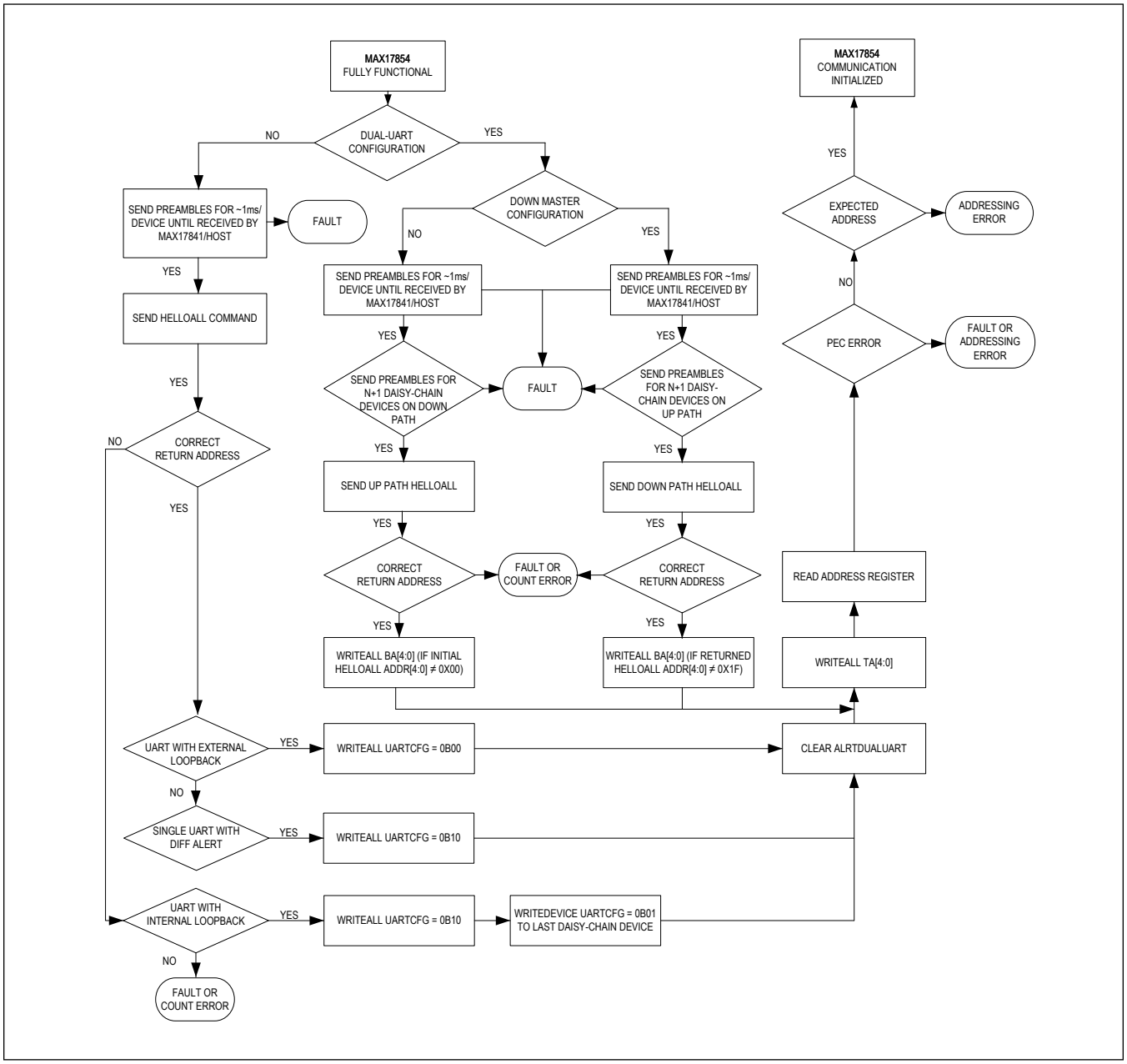


Figure 109. Device Initialization Sequence

Error Checking

Data integrity is provided by Manchester encoding, parity, character framing, and packet error checking (PEC). The combination of these features verify stage-to-stage communication both in the write and read directions with a Hamming distance (HD) value of 6 for commands with a length up to 247 bits (counted prior to Manchester encoding and character framing. This is equivalent to the longest possible command packet for a daisy-chain of up to 13 devices. The data-check byte is present in the READALL and READDEVICE commands to verify that the entire command propagated without errors. Using the data-check and PEC bytes, complete transaction integrity for READALL and READDEVICE command

packets can be verified.

PEC Errors

If the MAX17854 receives an invalid PEC byte, the corresponding ALRTPECUP, or ALRTPECDN bit in the STATUS2 register, and the summary ALRTPEC bit in the STATUS1 register are set. All single-UART configurations will set ALRTPECUP bit, since the Up Path is used for received transactions. In a dual-UART configuration, a PEC error in the Up Path will set ALRTPECUP, and a PEC error in the DOWN path will set the ALRTPECDN. The MAX17854 does not execute/accept any written command unless the received PEC byte matches the calculated CRC remainder, confirming the validity of the received command and data stream. To confirm the command was accepted, the host should perform an appropriate read transaction to verify the contents of the written register(s).

PEC Calculations

When directly communicating with the MAX17854 through the UART interface, the host must compute and send the PEC byte protecting the data sent to the device. Likewise, for returned read packets, the host should store the received data, perform the CRC calculation, and compare the results to the received PEC byte provided by the MAX17854 before accepting the data received as valid. To support PEC byte computation and checking, the host must implement a CRC-8 (8-bit cyclic redundancy check) encoding and decoding algorithm based on the following polynomial (0xA6):

$$P(x) = x^8 + x^6 + x^3 + x^2 + 1$$

This polynomial is capable of protecting a data stream of up to 247 bits with an HD of 3, meaning that any data stream 247 bits or less in length with any combination of 3 bits of error or less is guaranteed to be identified. If more than 3 bits of error are encountered, the PEC operation will very likely identify the problem, though this cannot be mathematically guaranteed.

A hardware implementation of the CRC calculation is shown in Figure 110. The CRC engine shown is implemented internally within the MAX17854; a similar implementation would be required in the host to support direct UART communication, for purposes of generating the PEC bytes sent to the MAX17854 or for checking PEC bytes received from the MAX17854. The incoming UART data stream is fed into the CRC engine, LSB first. Once the data stream has been completely shifted into the engine, the CRC remainder is known; this becomes the PEC byte for both incoming and outgoing data, PEC[7:0] = BIT[7:0] as shown - be sure to note the ordering of the bits within the remainder. Note that all UART transactions supply the command and data stream LSB first.

For incoming UART data streams, the MAX17854 will first clear the CRC engine and then input the incoming data stream into the the CRC engine, LSB first. After the final bit of data is processed (in this case, the MSB of the incoming data stream is applied to the engine), the engine is stopped and the CRC remainder is known. The incoming PEC byte, as calculated by the host using its copy of the CRC engine, then follows within the UART transaction (also LSB first), and is internally compared against the CRC remainder as calculated by the MAX17854. If the PEC byte received matches the CRC remainder calculated for the incoming data stream, the PEC operation is successful, and the transaction is accepted and executed by the MAX17854. If there is a mismatch, the MAX17854 will reject the transaction and issue the ALRTPEC status bit, notifying the host of the issue, so the transaction can be resent.

For outgoing UART data streams, the MAX17854 will first clear the CRC engine and then provide the outgoing data stream to the the CRC engine, LSB first. After the final bit of data is processed (in this case, the MSB of the outgoing data stream is applied to the engine), the engine is stopped and the CRC remainder is known—this becomes the outgoing PEC byte. The outgoing PEC byte, as calculated by the MAX17854 using its copy of the CRC engine, then follows within the UART transaction (also LSB first). As the host receives the data stream from the MAX17854, it should apply the data to its copy of the CRC engine (LSB first, in the order it arrives in the UART transaction, until the MSB of the data stream is applied to the engine). At this point, there are two equivalent ways the host can complete the PEC operation to establish the validity of the received data:

- Direct Comparison Method: The host stops the CRC engine once the data stream MSB is applied and compares the resulting CRC remainder to the PEC byte supplied by the MAX17854 (again, LSB first). If the 2 bytes match, the data is accepted as valid, otherwise it should be rejected. This is the method employed by the MAX17854 internally, as described above.
- Zero Remainder Method: The host continues CRC engine computations after the data MSB is applied by appending the received PEC byte to the end of the data stream, LSB first (i.e., in the order received during the UART transaction). Once the MSB of the PEC byte arrives at the input of the CRC engine, if the resulting CRC remainder = 00h, the data

is accepted as valid, otherwise it should be rejected.

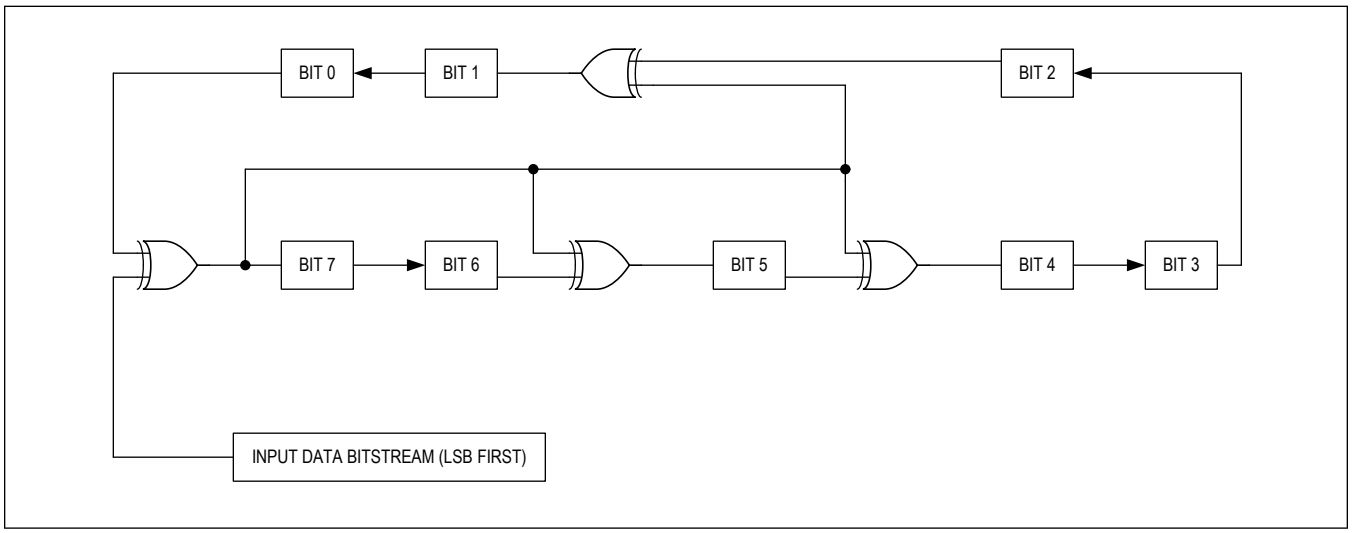


Figure 110. PEC CRC Calculation

PEC Calculation Psuedocode

The host uses the algorithm to process all bytes received in the command packet prior to the PEC byte itself. Neither the PEC nor the Alive-Counter bytes are part of the calculation. The bits are processed in the order they are received, LSB first. A bytewise pseudocode algorithm is shown below, but lookup table solutions are also possible to reduce host calculation time.

For commonly issued command packets, the host can precalculate (hard-code) the PEC byte. For commonly used partial packets, the CRC value of a partial calculation may be used as the initial value for a subsequent runtime calculation.

```
Function PEC_Calculation(ByteList(), NumberOfBytes, CRCByte)
{
// CRCByte is initialized to 0 for each ByteList in this implementation, where
// ByteList contains all bytes of a single command. It is passed into the
// function in case a partial ByteList calculation is needed.
// Data is transmitted and calculated in LSb first format
// Polynomial = x^8+x^6+x^3+x^2+1 = 1010_0110_1 = 0xA6
POLY = 8'hB2 // 10110010b – Polynomial binary representation is from left to right for LSB first (0xA6 -> 0xB2)
//Loop once for each byte in the ByteList
For ByteCounter = 0 to (NumberOfBytes – 1)
(
//Bitwise XOR the current CRC value with the ByteList byte
CRCByte = CRCByte XOR ByteList(ByteCounter)
//Process each of the 8 CRCByte remainder bits
For BitCounter = 1 to 8
(
// The LSb should be shifted toward the highest order polynomial
```

```
// coefficient. This is a right shift for data stored LSb to the right
// and POLY having high order coefficients stored to the right.
// Determine if LSb = 1 prior to right shift
If CRCByte[1] = 1 Then
// When LSb = 1, right shift and XOR CRCByte value with 8 LSbs
// of the polynomial coefficient constant. “/ 2” must be a true right
// shift in the target CPU to avoid rounding problems.
CRCByte = ((CRCByte / 2) XOR POLY)
Else
//When LSb = 0, right shift by 1 bit. “/ 2” must be a true right
// shift in the target CPU to avoid rounding problems.
CRCByte = (CRCByte / 2)
End If
//Truncate the CRC value to 8 bits if necessary
CRCByte = CRCByte AND 8'hFF
//Proceed to the next bit
Next BitCounter
)
//Operate on the next data byte in the ByteList
Next ByteCounter
)
// All calculations done; CRCByte value is the CRC byte for ByteList() and
// the initial CRCByte value
Return CRCByte
}
```

ROMCRC Calculation

For safety purposes, the factory-trimmed ROM (OTP) content can be read back by the user and checked for errors using an 8-bit CRC. ROMCRC is an 8-bit CRC remainder computed using the ID/OTP content and stored in OTP12[15:8] at the factory. Both the ID and OTP output data content (excluding OTP12[15:8], which is ROMCRC[7:0]) protected by the ROMCRC operation. To support ROMCRC computation and checking, the host must implement a CRC-8 encoding and decoding algorithm based on the following polynomial (0xA6):

$$P(x) = x^8 + x^6 + x^3 + x^2 + 1$$

This polynomial is capable of protecting the 200-bit ID/OTP content with a HD of 3, meaning any combination of 3 bits of error or less is guaranteed to be identified. If more than 3 bits of error are encountered, the ROMCRC operation will very likely identify the problem, though this cannot be mathematically guaranteed.

A hardware implementation of the CRC calculation is shown in Figure 111. The CRC engine shown would be implemented within the host. The same engine is used in the production trim software to compute and store the ROMCRC byte at the factory, using the computation method outlined below. Be sure to note the ordering of the bits within the remainder, as shown in the figure (i.e., BIT[7:0] = ROMCRC [7:0]). Note this is also the same CRC engine used for PEC byte CRC operations in UART mode.

To complete the ROMCRC operation, the host would first clear the CRC engine and then apply the entire 200-bit content of the ID/OTP data received from the MAX17854 concatenated in the following order: ID1[0:15], ID2[0:15], OTP2[0:15], OTP3[0:15], OTP4[0:15], OTP5[0:15], OTP6[0:15], OTP7[0:15], OTP8[0:15], OTP9[0:15], OTP10[0:15], OTP11[0:15],

OTP12[0:7]. Note this is essentially the entire ID/OTP content provided LSB first - ID1[0] is the first bit applied to the CRC Engine and OTP12[7] is the last, and all 200 bits must be applied. At this point, there are two equivalent ways the host can complete the ROMCRC operation to establish the validity of the received ID/OTP data:

- Direct Comparison Method: The host stops the CRC engine once the ID/OTP MSB is applied and compares the resulting CRC remainder to the ROMCRC byte supplied by the MAX17854 as ROMCRC[7:0] (OTP12[15:8]). If the 2 bytes match, the data is accepted as valid, otherwise it should be rejected and retried in case of a communication fault. If the failure persists, this may indicate a problem within the MAX17854 ROM.
- Zero Remainder Method: The host continues CRC engine computations after the data stream is applied by appending the received ROMCRC byte to the end of the data stream, LSB first (i.e., continuing the concatenation pattern shown above with OTP12[8:15], with OTP12[15] now being the last bit applied). Once the MSB of the ROMCRC byte arrives at the input of the CRC engine, if the resulting CRC remainder = 00h, the data is accepted as valid, otherwise it should be rejected and retried in case of a communication fault. If the failure persists, this may indicate a problem within the MAX17854 ROM.

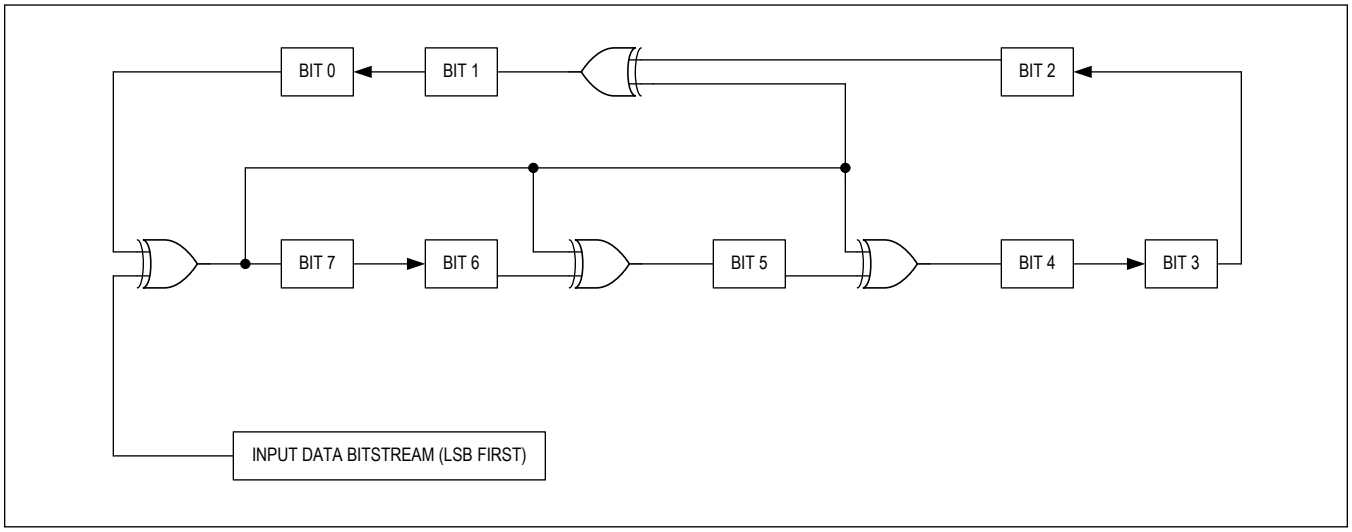


Figure 111. ROMCRC Calculation

Bus Bar Design

Some applications require that the bus bar be electrically separated from the battery cell voltage to allow for increased cell accuracy through eliminating the voltage created by the pack current interacting with the resistance of the bus bar itself. Alternatively, other applications allow for the bus bar resistivity to be included in the cell measurement while the system compensated for this error through other methods. Lastly, other designs are constructed such that the bus bar be placed between the high-voltage data acquisition devices such that the cell measurement inputs are not used and the measurement accuracy is unaffected.

The MAX17854 supports any system design evolving of the bus bar and is equally capable of making bus bar measurements for advance prediction of a bus bar connection failure. The bus bar design will utilize the same filter structure as the traditional balancing network if the SW pin current is less than the Maximum Continuous Current into Any Pin in the *Absolute Maximum Ratings*. If the SW pin current specification is exceeded, then an external Schottky diode is recommended to be placed in parallel to the filter capacitance as seen in Figure 113. The Schottky should be chosen such that the forward voltage is <0.7V at the SW pin current rating at +25°C.

The SW pin current can be calculated by:

$$I_{SW} = (V_{BUSBAR} - 0.7V) / (2 * R_{BALANCE})$$

For many applications, the resistivity of the bus bar is very low to support peak system currents that no modification to

the external network is required.

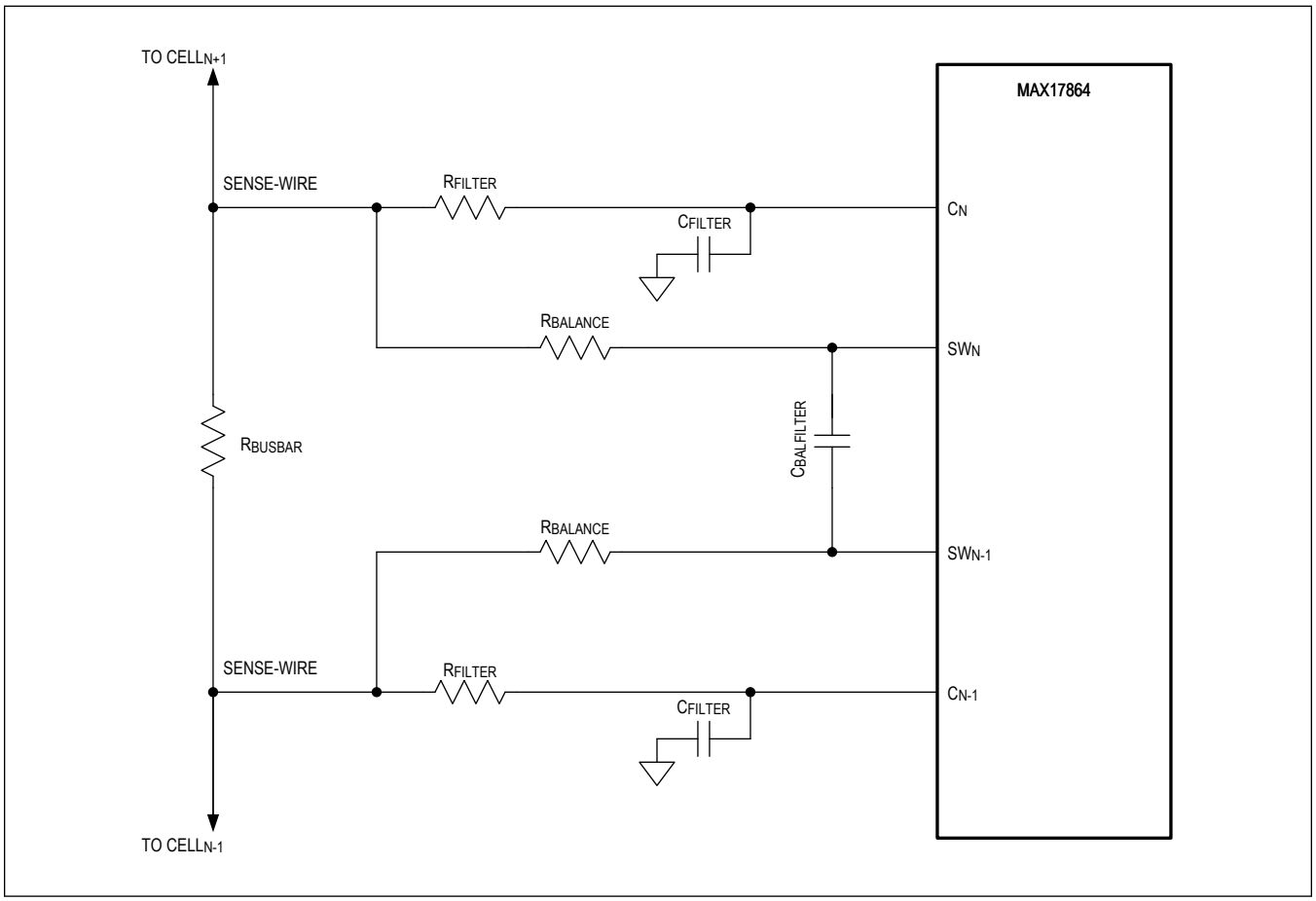


Figure 112. Bus Bar Application Circuit Less Than Continuous Current Injection

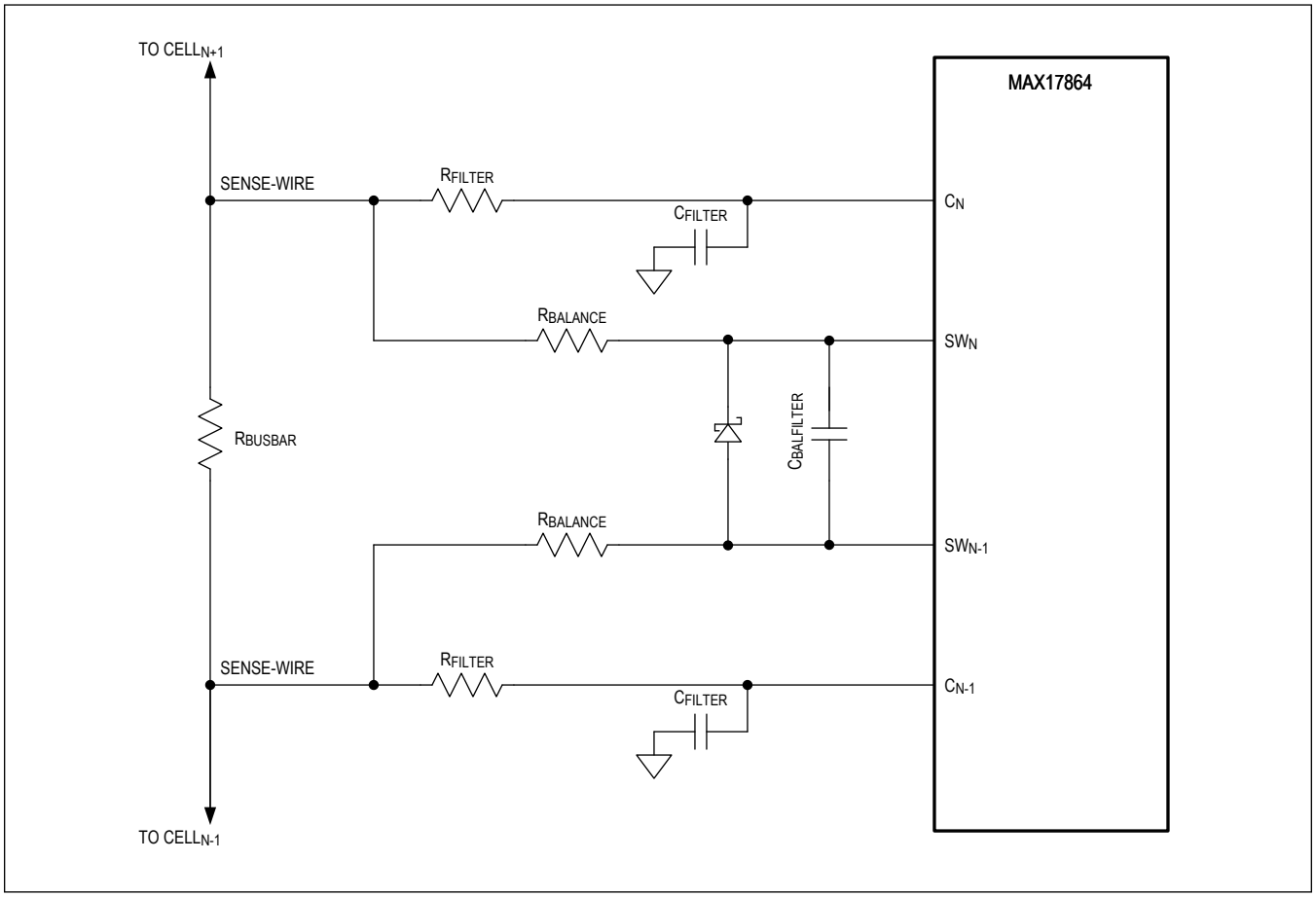


Figure 113. Bus Bar Application Circuit Greater Than Continuous Current Injection

MAX17853 to MAX17854 Migration

While migrating the solution from the MAX17853 to MAX17854, one hardware change is required. On the MAX17853 evaluation (EV) kit, the V_{AA} output is tied to V_{DDL2} and V_{DDL3} through an external resistor. Since the MAX17854 has two regulators, this connection needs to be removed, hence the external resistor needs to be depopulated on EV kit to make the hardware to be used for the MAX17854, as shown in the Figure 114. A similar change to this effect would be required for any user-defined hardware.

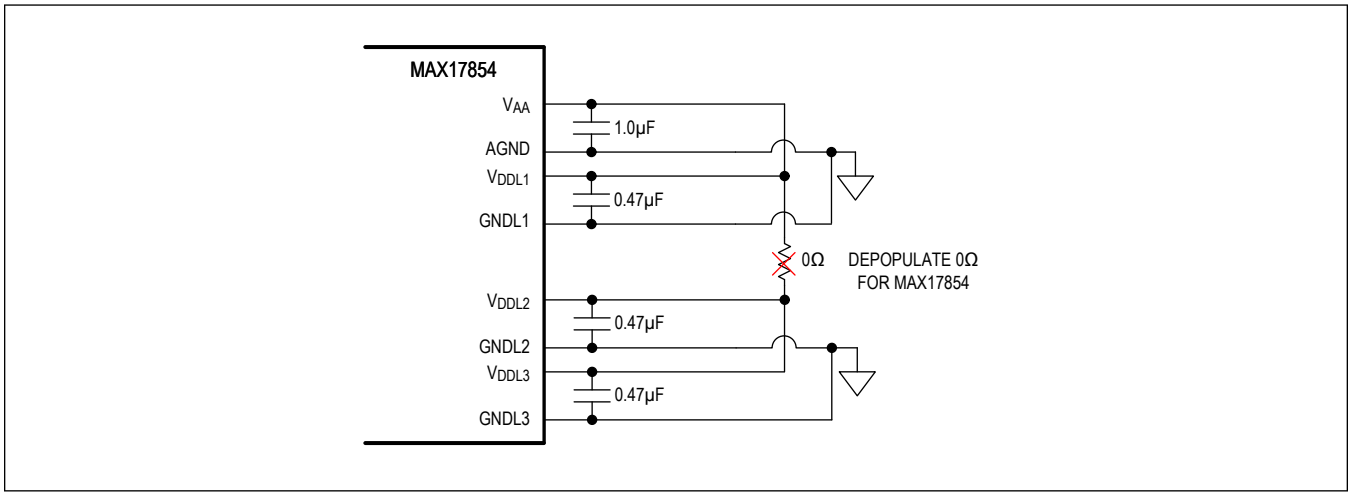


Figure 114. MAX17853 to MAX17854 Hardware Change

On MAX17854, V_{AA}/V_{DDL1} is at 1.8V due to the process update. This has an impact on AUX inputs when THERM is used as a reference. THERM is now 1.8V instead of previous 3.3V. For analog absolute measurements on AUX/GPIO, the maximum voltage is now 1.25V versus 2.3V previously.

The MAX17854 also incorporates new diagnostics to verify the 3.3V LDO. New bitfields are added in DIAGCFG register for both DIAGSEL1 and DIAGSEL2. Digital operation and timing requirements remain the same; this would only be a software update. See the *$V_{DDL2/3}$ Diagnostic* section for details.

The alternate reference (ALTREF) has been scaled to 1V. No hardware change is required as a result of this change, but a software update for adjusting the pass/fail criterion is required. See the *ALTREF Diagnostic Measurement* section for more details.

The MAX17854 also uses a 12-bit DAC to generate reference for redundant comparator path. This improves the resolution of the comparator accuracy. No hardware change is required. See the *Comparator Accuracy Diagnostic* section for more details.

The MAX17854 also introduces an I^2C master 2-wire serial interface. The data (SDA) and clock (SCL) lines are shared with AUX0/GPIO0 and AUX1/GPIO1; therefore, these pins would need to be repurposed as clock and data for this configuration. See the *I^2C Interface* section for more details.

The MAX17854 does not support an SPI interface.

Note that MAX17854 has the datacheck-byte (register 0x14) automatically disabled. To guarantee the same communication functionality as MAX17853, this register has to be written to 0x0108. This value won't have any effect on legacy MAX17853 products.

It is recommended that the user review their software implementation as the diagnostic addition and improvements would require software update.

Typical Application Circuits

MAX17854 Simplified Application Diagrams

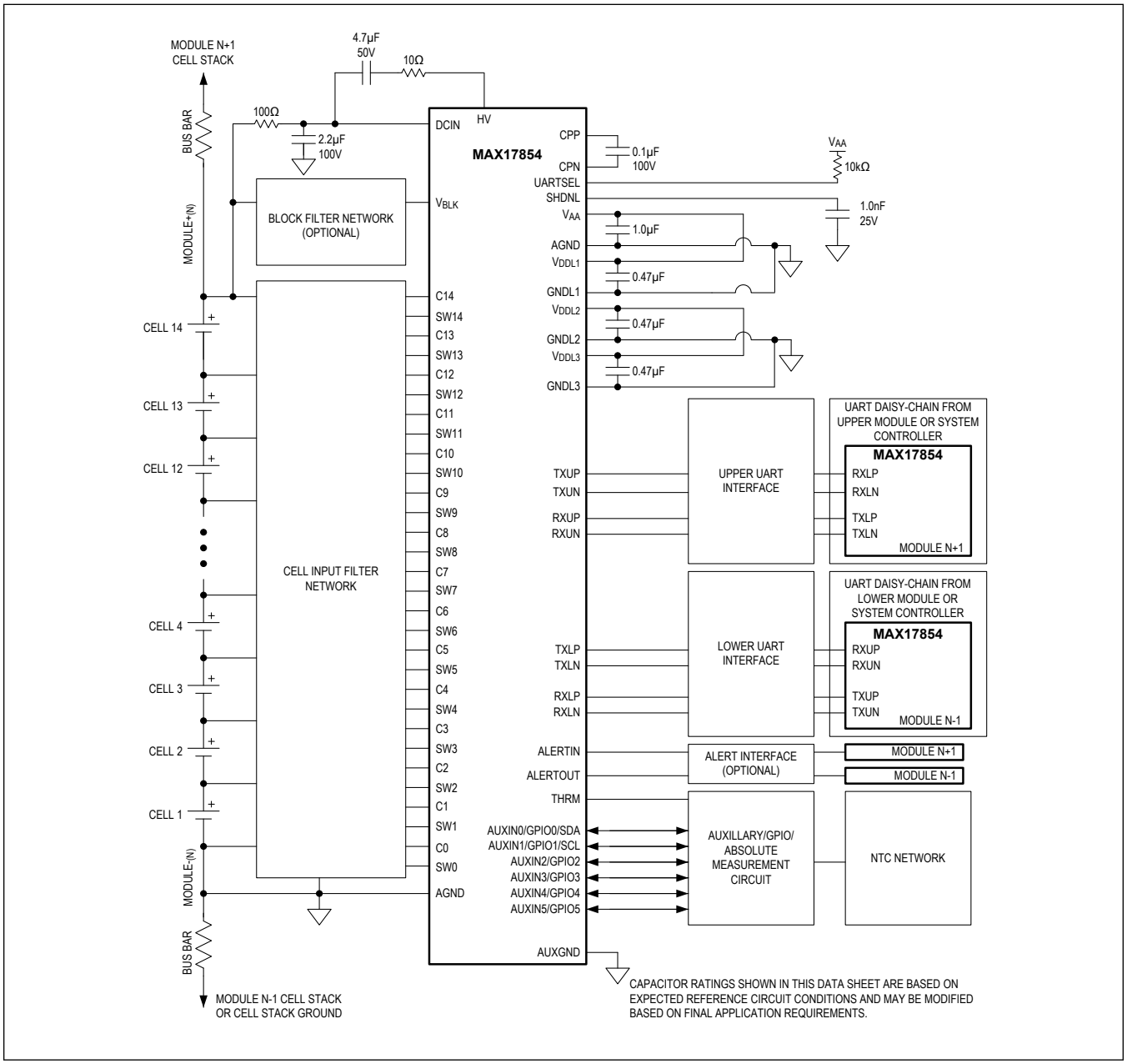


Figure 115. Simplified Application Diagram with Single-Ended Alert Interface

Typical Application Circuits (continued)

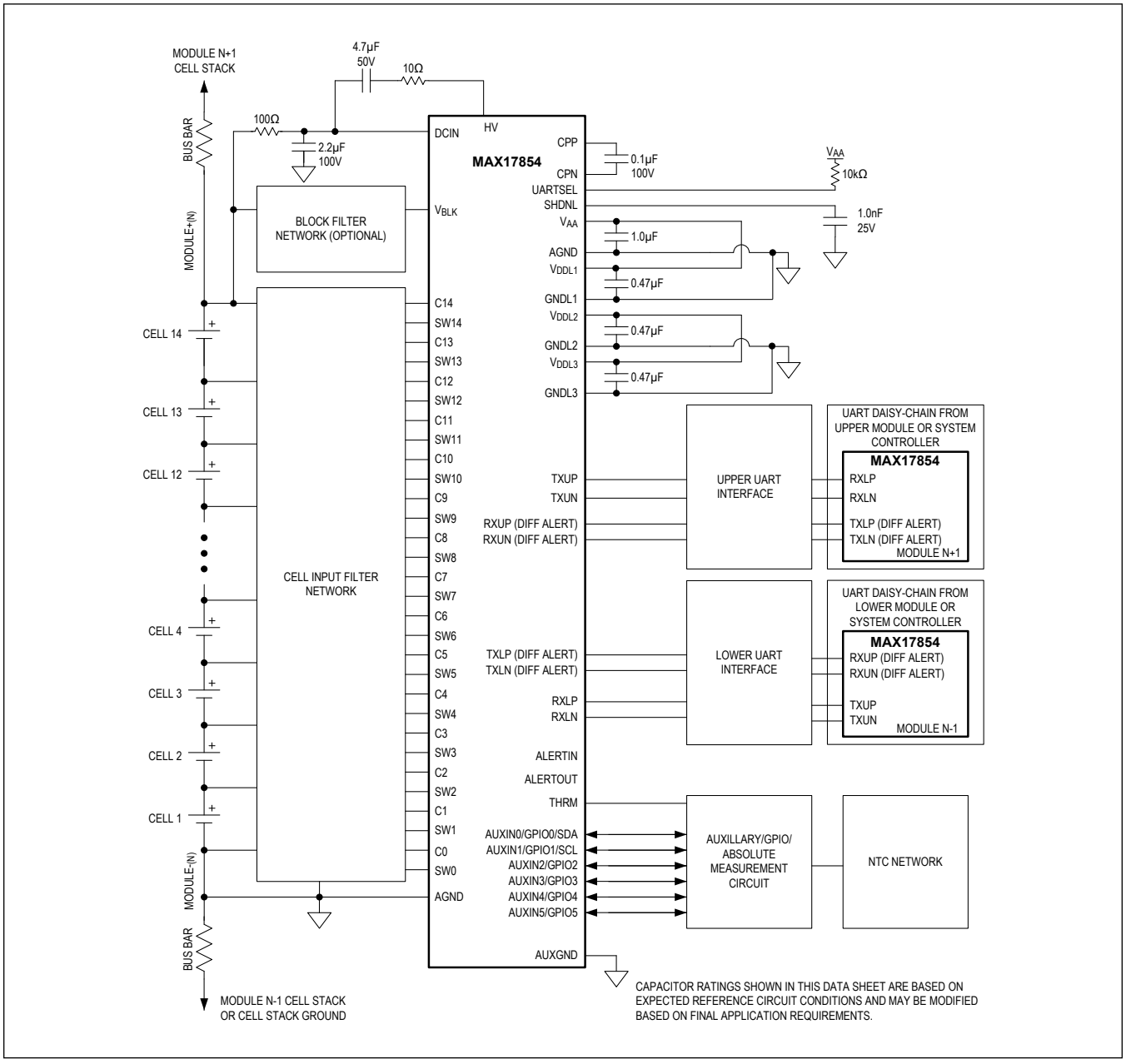


Figure 116. Simplified Application Diagram with Differential Alert Interface

PCB Layout Recommendations

Careful PCB layout is critical to achieving the best accuracy performance and robust performance against environmental conditions.

Typical Application Circuits (continued)

An example circuit and layout can be found in the EV kit data sheet.

Layout Procedure

1. Place the charge pump capacitor close to the CPP and CPN pins and on the same layer as the MAX17854. Care should be taken to avoid using vias to prevent unwanted coupling into adjacent signals and planes.
2. Place the decoupling capacitors on the V_{DCIN}, V_{AA}, and V_{DDL1} close to the respective pins and on the same layer as the MAX17854. V_{DDL2} and V_{DDL3} should be placed close to the pins and is preferred on the same layer, if possible. All capacitors should not share a ground return and each should via directly to the AGND internal layer.
3. AGND, GNDL1, GNDL2, GNDL3, and AUXGND should via directly to a solid AGND plane placed under the MAX17854. Traces and vias should not be shared within before they enter the AGND plane.
4. The DCIN input resistor must be sized depending on both device current consumption (I_{DCIN}) and board current consumption (I_{VAA_LOAD}) to prevent false ALRTHVHDRM alerts. Adjustment of the DCIN resistor due to external loading should following this equation: $R_{DCIN\_LOAD} = R_{DCIN\_NOM} \times (1 - I_{DCIN}/I_{VAA\_LOAD})$.
   - Note: In flexible-pack operation, the DCIN filter resistor is omitted.
5. The SHDNL capacitor and associated trace routing should be kept away and shielded from potential noise sources and digital signals such as those present with the communication or alert interfaces as these may effect the voltage seen by the SHDNL pin.
6. C_n traces are recommend to be routed on the same layer as the MAX17854 to avoid the potential sources for noise injection into the primary measurement path. These traces carry a negligible current and can be kept at a minimum trace widths.
7. SW_n traces should be optimized for width in the permissible layout (20mil recommended) to eliminate excessive voltage drop due to the balancing operation.
8. UART Rx and Tx ports should be routed for an 100Ω differential impedance. If the MAX17854 is used in a distributed BMS system, ESD protection is recommended to be placed as close to the UART communication connector with the ground return via'd directly to the AGND plane to clamp transient events before they can couple to other nodes that may effect device performance. For centralized BMS systems, ESD components on the UART may be omitted.

Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE
MAX17854ACB/V+T	-40°C to +125°C	64 LQFP

+ Denotes a lead(Pb)-free/RoHS-compliant package.

T Denotes tape-and-reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	11/21	Initial release	—