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APPLICATION NOTE 724

Generating Switched-Capacitor-Filter Clocks

Abstract: Some switched-capacitor-filter clocks (SCFs) are self-clocking with the addition of external components, but most applications use a CMOS-level clock signal to set the SCF's corner frequency. This application note discusses the more common methods for generating a SFC.

Recent advances in semiconductor-process technology and circuit-design techniques have brought down the prices of switched-capacitor filters (SCFs) by a factor of three. As an example, five-pole Butterworth low-pass filters sell for less than a dollar each in large quantities. Recent SCFs offer low-power single-supply operation down to 2.7V.

Implementing an SCF is easy. First, choose the kind. Fixed-response, five- and eight-pole Butterworth, Bessel, Chebyschev, and elliptic (Cauer) types are commonly available, as well as the universal SCF with user-programmable features. Follow the data-sheet recommendations on power supplies, bypassing, and signal coupling, and then select a clock frequency appropriate to the application.

Some SCFs are self-clocking with the addition of external components (for example, the MAX280), but most applications use a CMOS-level clock signal to set the SCF's corner frequency. Otherwise, many acceptable methods are available for setting the clock signal for an SCF. The more common ones are covered in the following discussion.

Proper Clock Characteristics

The first major concern in clocking an SCF is the clock's duty cycle. Deviation from the range specified by most manufacturers (40% to 60%) produces inadequate settling of the switched-capacitor element, which can cause signal distortion, inaccurate filter response, and signal attenuation. Most sources inherently produce the desired 50% duty cycle; if not, that performance can be ensured by design in nearly all cases.

Another important characteristic is the clock signal's rise and fall times. These rising and falling edges should move swiftly through the threshold of the filter's clock input. Failure to do so can produce jitter in the internal clock signals, which can cause unpredictable spurs in the filter's output spectrum. For most HCMOS devices, the output speed and symmetry are sufficient to prevent this problem.

It's also prudent to verify that the SCF's input threshold is compatible with the clock's output levels. When operated with a single supply, a filter designed for dual-supply operation can have unexpected requirements for these input levels. Be sure to consult the filter data sheet for this purpose.

Crystal Clock Oscillators

A crystal clock oscillator (XCO) offers one of the easiest ways to program the corner frequency of a filter. Expect to pay about $3.00 (US) for these devices in small quantities, with the price climbing about 50% for versions at the extreme ends of the available frequency range (usually 1MHz to 60MHz). This approach is easy if an XCO at the desired frequency is available, but the drawbacks are space, cost, and delivery. Only a limited number of frequencies are available, and custom XCOs are out of the question for all but the highest-volume requirements.

Traditional XCO packages require a PC-board footprint 0.5" by 0.75" with an installed height of 0.25", but the newer XCO packages offer dimensions comparable to that of an IC. As an alternative for µP or µC systems in which the clock requirements are somewhat arbitrary, you can save cost and real estate on the board by using the same clock for the processor and the SCF.

Digital Dividers

For many switched-capacitor filters, the required clock frequency either falls outside the available range of standard XCO values or is not available among them. A digital divider can provide a satisfactory clock in these applications. Three types are commonly available: binary ripple counters, presettable synchronous counters, and programmable timer counters.

Binary ripple counters are the easiest to apply, but they suffer from inflexibility. They progressively divide the input signal by 2, over multiple stages. The name "ripple counter" stems from the output behavior: Each stage changes state on the rising edge of the previous stage. (This action is not a problem unless you attempt to perform combinatorial logic on the outputs.) Ripple counters are appropriate when the available clock frequency is a binary multiple (2, 4, 8, 16, etc.) of the desired clock frequency.

When an application meets this binary criterion, the ripple counter is easy to implement (Figure 1). A common IC (the 74HC161) divides a 2.0MHz clock down to 125kHz. The 74HC161's output levels and symmetry are ideal for a single-supply filter operating from 5V. If you require 3V operation, substitute a MAX7405 for the filter and (if operating beyond the 74HC161 voltage or frequency range) a 74VHC4040 for the 74HC161.

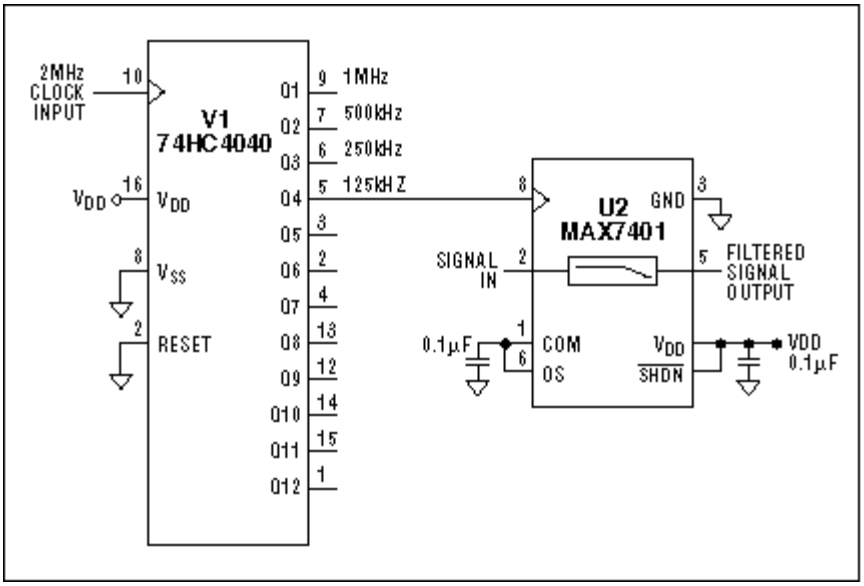

Figure 1. A binary-divider IC (U1) offers a convenient clock source, provided the available frequency is a binary multiple of the desired output.

If the desired clock frequency is an integral multiple of the available clock, but not a binary factor, you can use a presettable synchronous counter. Usually available as a 4-bit device, it counts down from a preloaded count to zero. Thus, a single device is capable of dividing by integers in the range 2 to 31. For larger integers, simply cascade the 4-bit stages. To maintain a 50% duty cycle, the last stage should perform a straight binary division. As an example (Figure 2), two 4-bit 74HC161 counters (dividing first by 6 and then by 8) divide a 16.384MHz clock down to 340.6kHz. The resulting cutoff frequency is ideal for telecom applications.

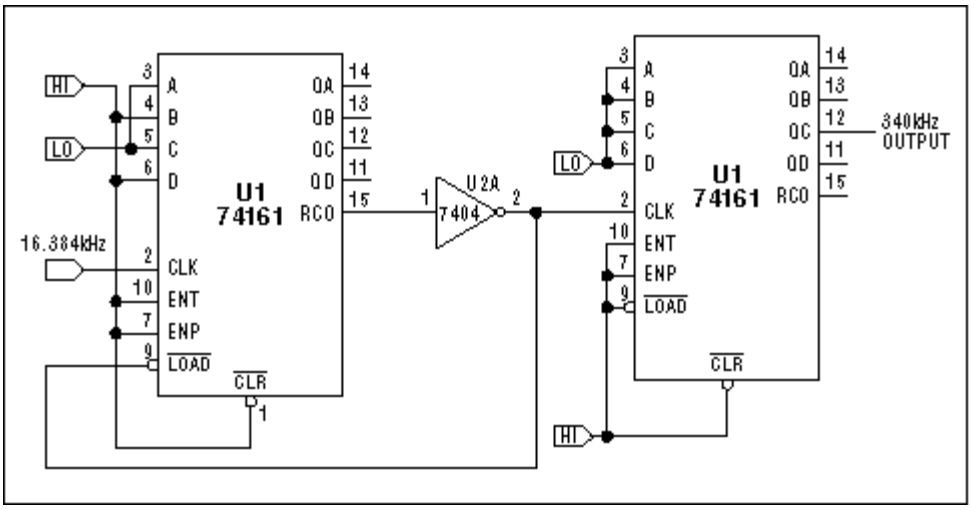

Figure 2. Synchronous counters can divide by any integral multiple of the input. Here, division by 6, then by 8, divides the input by a factor of 48.

The ultimate digital divider is a programmable timer. Initially designed as a peripheral for 8-bit microprocessors, this device is still found on many data-acquisition cards for PCs. One of the original devices, the 8053, was supersceded by the 8054 and is still multisourced as the low-power CMOS 80C54. It has three 16-bit general-purpose counters with software-programmable operation and counting intervals. You can configure these three stages to produce a staggering number of timing combinations. If an 80C54 can't provide an acceptable configuration for the clock source and counter, it probably can't be done!

A learning curve is associated with 80C54 applications. You must load counts and configurations as 8-bit words via the multiplexed address and data buses. Prudent practice dictates that you prototype the desired configuration before committing to a PC board. Because of difficulties in achieving a 50% duty cycle with the 80C54, its output should be followed by a divide-by-2 stage such as the 74HC74 D-type flip-flop.

Phase-Locked Loops

Generating an SCF clock from a lower operating frequency yields an added benefit. Because the clock and the lower frequency are synchronized, no "beat-frequency" noise is introduced in the signal path. A time-division duplex (TDD) system operating at 8kHz, for example, can easily support a 320kHz clock frequency.

SCF applications lack modulation and have predefined operating points, so the design of phase-locked loops (PLLs) for SCF clocks is easier than for other PLL applications. SCF clock frequencies also allow use of the ubiquitous 4046 divider. This venerable CMOS IC (CD4046, MC14046, 74HC4046, etc.) is easily configured for a particular operating point using external resistors and capacitors. The addition of an external divider completes the PLL.

PLL design is further simplified by the availability of free design software. In the system mentioned above, with an 8kHz clock source, the cutoff frequency is 3.2kHz. To obtain the desired 320kHz SCF clock, simply add an external divide-by-40 stage in the form of a divide-by-10 followed by a divide-by-4 (Figure 3).

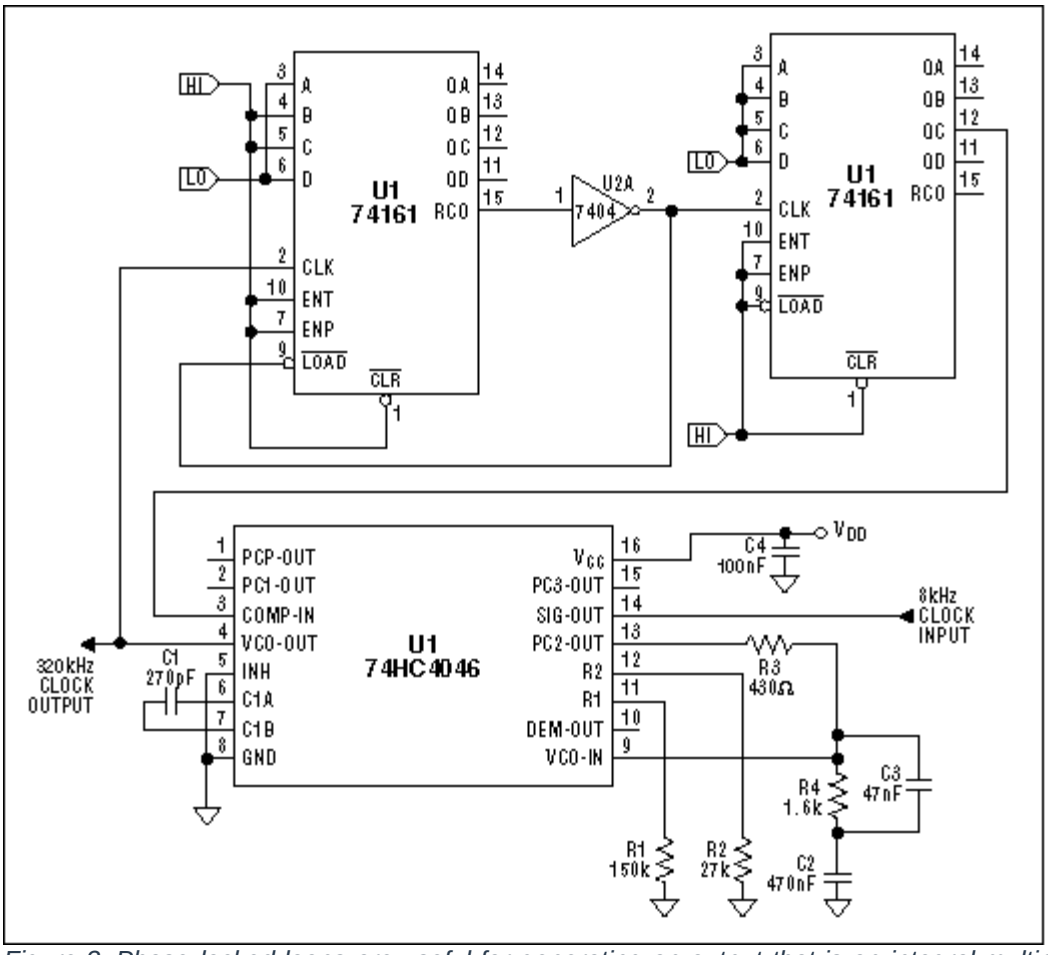

Figure 3. Phase-locked loops are useful for generating an output that is an integral multiple of the input.

RC Oscillators

If the SCF does not have a self-clocking option, an RC oscillator will usually suffice in systems for which the cutoff-frequency accuracy is not critical. Avoid the unpredictable frequency output of single-stage RC oscillators, as well as the use of digital gates with hysteresis, because they specify very loose limits for the hysteresis voltage.

Instead of a single stage, consider a ring oscillator constructed as an odd number of inverter stages separated by single-RC low-pass stages. The signal at each digital input swings from ground to VCC and crosses its switching threshold rapidly, producing a stable, low-power oscillator with predictable output (Figure 4).

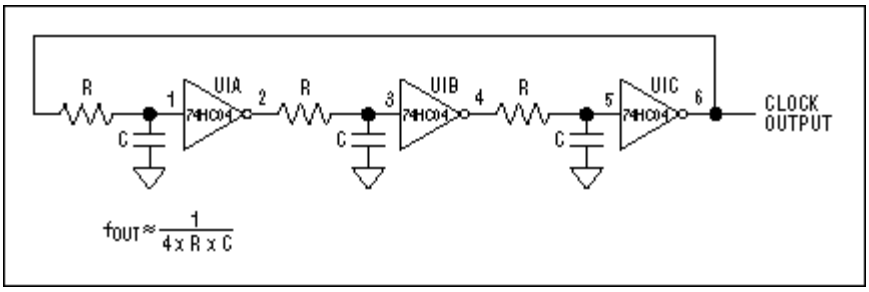

Figure 4. The ring oscillator offers stability and low-power operation.

The analog comparator offers another approach. Its high impedance and high gain, in conjunction with an external hysteresis circuit, provide a high-accuracy oscillator (Figure 5). Operation relies on a single-RC time constant, enabling ready adjustment of the output frequency with a potentiometer. Frequency is a linear function of the resistance value. Because the positive feedback is ±33%, the oscillation period is very close to 67% of the time constant formed by R1 and C1. Thus, the output frequency is closely described as $f_{OUT} = 1/(R1 \times C1)$.

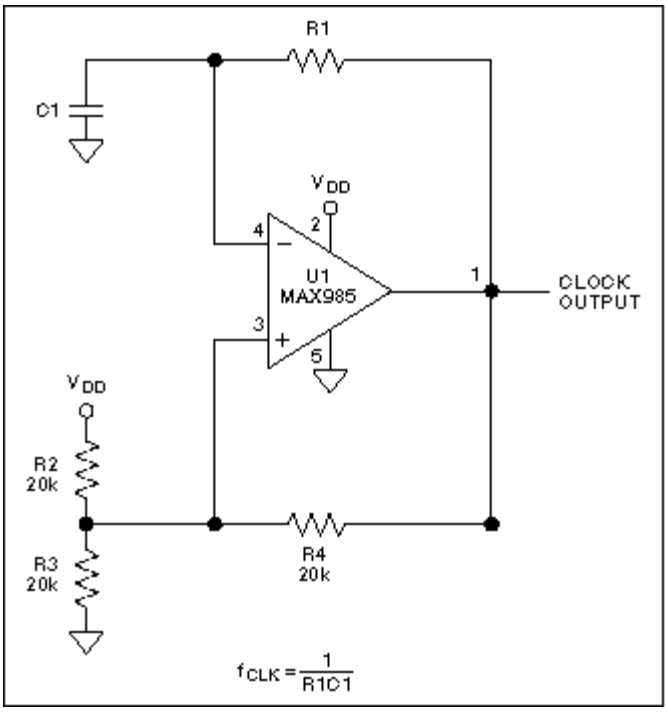

Figure 5. Analog-comparator oscillators produce an arbitrary output frequency of f_{OUT} = 1/(R1 × C1).

Appendix

Recent Developments by Maxim

Taking advantage of new design techniques and modern submicron integrated-circuit technology has enabled Maxim to develop innovative switched-capacitor filters, such as the MAX7490, that offer improved performance at lower cost. Compare the MAX7490 to the industry-standard MF10. Both are dual biquad clocked/resistor-programmable state-variable filters. The MAX7490 has 2% Q accuracy compared to 6% for the MF10, 40kHz versus 30kHz maximum center frequency, and 4mA versus 10mA supply current. Add to these improved specifications the MAX7490's 16-pin QSOP package versus the MF10's 20-pin-wide SOIC, and the progress made with these types of filters is self-evident.

Fixed transfer-function low-pass filters have also seen sweeping improvements. The MAX7426/MAX7427 5th-order elliptical filters offer a 12kHz maximum corner frequency and consume less than 1mA of supply current, whereas the MAX7408 provides a 15kHz maximum corner frequency and consumes only 1.2mA of supply current. Both devices are available in an 8-pin µMAX® package, offering significant space savings.

Maxim's latest SCFs have the further advantage of single-supply operation. Previous single-supply designs allowed a minimum supply voltage of 4.75V, making them unsuitable for most single-supply applications. However, as most of the newer SCFs include versions specified for operation down to 2.7V, they are compatible with a variety of power-supply configurations.

Application Note 724: http://www.maxim-ic.com/an724
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