

Notification Number:	20190605001	Notification Date:	06/07/2019						
Title:	DLPC34XX and DLPC150 Data Sheet Change								
Customer Contact:	Dlp-pcn-team@list.ti.com	Dept:	Quality Services						
Change Type:									
<input type="checkbox"/>	Assembly Site	<input type="checkbox"/>	Design						
<input type="checkbox"/>	Assembly Process	<input checked="" type="checkbox"/>	Data Sheet						
<input type="checkbox"/>	Assembly Materials	<input type="checkbox"/>	Part number change						
<input type="checkbox"/>	Mechanical Specification	<input type="checkbox"/>	Test Site						
<input type="checkbox"/>	Packing/Shipping/Labeling	<input type="checkbox"/>	Test Process						
<input type="checkbox"/>		<input type="checkbox"/>	Wafer Bump Site						
<input type="checkbox"/>		<input type="checkbox"/>	Wafer Bump Material						
<input type="checkbox"/>		<input type="checkbox"/>	Wafer Bump Process						
<input type="checkbox"/>		<input type="checkbox"/>	Wafer Fab Site						
<input type="checkbox"/>		<input type="checkbox"/>	Wafer Fab Materials						
<input type="checkbox"/>		<input type="checkbox"/>	Wafer Fab Process						
Notification Details									
Description of Change:									
Texas Instruments Incorporated is announcing an information only notification for the below data sheet change.									
<table border="1"> <thead> <tr> <th></th> <th>Change from</th> <th>Change to</th> </tr> </thead> <tbody> <tr> <td>Pin Functions / System Power-Up and Power-Down Sequence</td> <td>Longer mirror parking time of up to 500 μs</td> <td>Longer mirror parking time of up to 20 ms</td> </tr> </tbody> </table>					Change from	Change to	Pin Functions / System Power-Up and Power-Down Sequence	Longer mirror parking time of up to 500 μ s	Longer mirror parking time of up to 20 ms
	Change from	Change to							
Pin Functions / System Power-Up and Power-Down Sequence	Longer mirror parking time of up to 500 μ s	Longer mirror parking time of up to 20 ms							
Refer to DLP® Pico™ DMD Chipset Parking Technical Advisory for more details. Data sheets will be updated by July 1, 2019 to reflect this change.									
Reason for Change:									
Clarify chipset power-down requirements for Normal Park operation.									
Anticipated impact on Fit, Form, Function, Quality or Reliability (positive / negative):									
Within the system power-down sequence, the maximum Normal Park time will be increased from 500 μ s to 20 ms.									
Changes to product identification resulting from this notification:									
None									
Product Affected:									
DLPC3430CZVBR, DLPC3432CZVB, DLPC3433CZVB, DLPC3434CZVB, DLPC3435ZEZ, DLPC3435CZEZ, DLPC3436CZVB, DLPC3437CZEZ, DLPC3438CZEZ, DLPC3439CZEZ, DLPC3440CZEZ, DLPC150ZEZ, DLPC3479CZEZ, DLPC3478CZEZ, DLPC3470CZEZ									

For questions regarding this notice, e-mails can be sent to the contacts shown below or your local Field Sales Representative.

Location	E-Mail
DLP® Products	Dlp-pcn-team@list.ti.com
USA	PCNAmericasContact@list.ti.com
Europe	PCNEuropeContact@list.ti.com
Asia Pacific	PCNAsiaContact@list.ti.com
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