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ON Semiconductor®

# FSA3051 —High Performance SPDT Analog Switch with Over-Voltage Tolerance

## Features

- Low On Capacitance: 7.7 pF Typical
- Low On Resistance: 6 Ω Typical
- Low Power Consumption: 1 μA Maximum
  - 15 μA Maximum I<sub>CC</sub>T over an Expanded Voltage Range (V<sub>IN</sub>=1.8 V, V<sub>CC</sub>=5.5 V)
- Wide -3 db Bandwidth: 1.0 GHz
- Packaged in Ultra Small 6-Lead TMLP
- Broad V<sub>CC</sub> Operating Range: 1.6 V to 5.5 V
- Over-Voltage Tolerance (OVT) on all Data Ports up to 6 V without External Components

## Applications

- Cell Phone, PDA, Digital Camera, and Notebook
- LCD Monitor, TV, and Set-Top Box

## Description

The FSA3051 is a 6 Ω, bi-directional, low-power, two-port, high-speed, Single Pole / Double Throw (SPDT) analog switch. It features an extremely low on capacitance (C<sub>ON</sub>) of 7.7 pF and wide bandwidth of 1.0 GHz.

The FSA3051 contains special circuitry on the switch I/O pins for applications where the V<sub>CC</sub> supply is powered-off (V<sub>CC</sub>=0 V), which allows the device to withstand an over-voltage condition. This device is designed to minimize current consumption even when the control voltage applied to the select (S) pin is lower than the supply voltage (V<sub>CC</sub>). This feature is especially valuable to ultra-portable applications, such as cell phones, allowing for direct interface with the general-purpose I/Os of the baseband processor. Other applications include switching in portable cell phones, PDAs, digital cameras, printers, and notebook computers.

## Ordering Information

Part Number	Top Mark	Operating Temperature Range	Package
FSA3051TMX	NT	-40 to +85°C	6-Lead, Dual, Ultra-ultrathin Molded Leadless Package (TMLP), 1.0 x 1.0 mm. Top left unit orientation in carrier tape.
FSA3051TMX-F147	NT	-40 to +85°C	6-Lead, Dual, Ultra-ultrathin Molded Leadless Package (TMLP), 1.0 x 1.0 mm. Bottom left unit orientation in carrier tape.

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### Analog Symbols

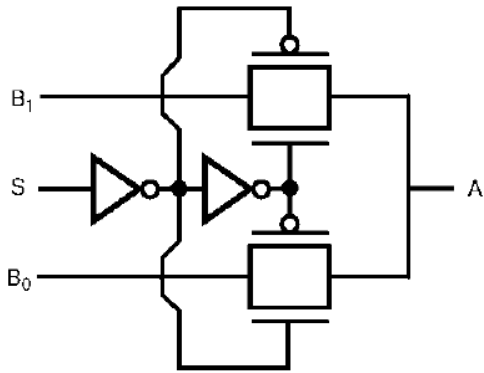


Figure 1. Logic Symbol

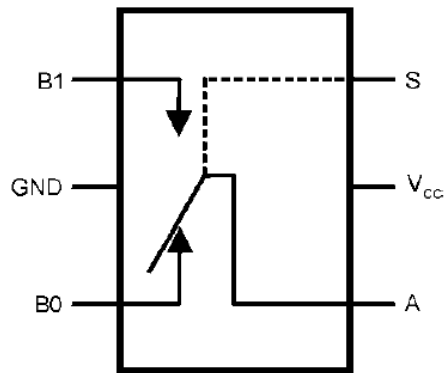


Figure 2. Analog Symbol

### Pin Assignments

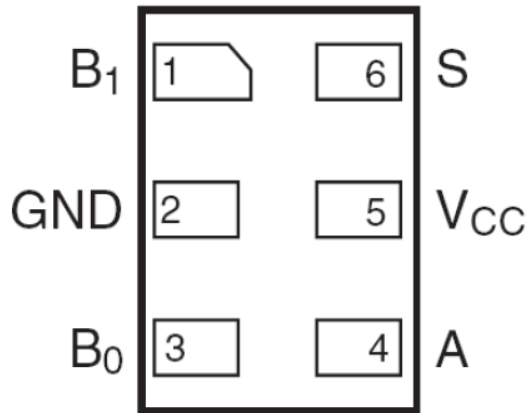


Figure 3. 6-Lead TMLP (Top-Through View)

### Pin Definitions

UMLP Pin#	Name	Description
1	B <sub>1</sub>	Data Port
2	GND	Ground
3	B <sub>0</sub>	Data Port
4	A	Data Port
5	V <sub>CC</sub>	Supply Voltage
6	S	Switch Select

### Truth Table

S	Function
LOW	B <sub>0</sub> connected to A
HIGH	B <sub>1</sub> connected to A

**Notes:**

1. LOW  $\leq V_{IL}$ .
2. HIGH  $\geq V_{IH}$ .

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
V <sub>CC</sub>	Supply Voltage	-0.5	6.0	V
V <sub>CNTRL</sub>	DC Input Voltage <sup>(3)</sup>	-0.5	V <sub>CC</sub>	V
V <sub>SW</sub>	DC Switch I/O Voltage <sup>(3)</sup>	-0.50	6.00	V
I <sub>IK</sub>	DC Input Diode Current	-50		mA
I <sub>OUT</sub>	DC Output Current		50	mA
T <sub>STG</sub>	Storage Temperature	-65	+150	°C
MSL	Moisture Sensitivity Level (JEDEC J-STD-020A)		1	Level
ESD	Human Body Model, ANSI/ESDA/JEDEC JS-001-2012	All Pins	2	kV
		I/O to GND	2	
		Power to GND	2	
	Charged Device Model, JEDEC: JESD22-C101	1		

**Note:**

- The input and output negative ratings may be exceeded if the input and output diode current ratings are observed.

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. ON Semiconductor does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
V <sub>CC</sub>	Supply Voltage	1.6	5.5	V
V <sub>CNTRL</sub>	Control Input Voltage (S) <sup>(4)</sup>	0	V <sub>CC</sub>	V
V <sub>SW</sub>	Switch I/O Voltage	-0.5	5.5	V
T <sub>A</sub>	Operating Temperature	-40	+85	°C

**Note:**

- The control input must be held HIGH or LOW and it must not float.

## DC Electrical Characteristics

All typical value are at  $T_A=25^\circ\text{C}$  unless otherw ise specified.

Symbol	Parameter	Condition	$V_{CC}$ (V)	$T_A=-40^\circ\text{C}$ to $+85^\circ\text{C}$			Unit
				Min.	Typ.	Max.	
$V_{IK}$	Clamp Diode Voltage	$I_{IN}=-18$ mA	3.0			-1.2	V
$V_{IH}$	Input Voltage High		1.8 to 4.3	1.3			V
			4.3 to 5.5	1.7			
$V_{IL}$	Input Voltage Low		1.8 to 4.3			0.5	V
			4.3 to 5.5			0.7	
$I_{IN}$	Control Input Leakage	$V_{CNTRL}=0$ to $V_{CC}$	1.8	-1		1	$\mu\text{A}$
			5.5	-1		1	
$I_{OZ}$	Off State Leakage	$V_{SW}=0$ V to $V_{CC}$	1.8	-2		2	$\mu\text{A}$
		$V_{SW}=0$ V to 3.6 V	5.5	-2		2	
$I_{OFF}$	Power-Off Leakage Current (All I/O Ports)	$V_{SW}=0$ V to 4.3 V, $V_{CC}=0$ V Figure 5	0	-2		2	$\mu\text{A}$
$R_{ON}$	Switch On Resistance <sup>(5)</sup>	$V_{SW}=0.4$ V, $I_{ON}=-8$ mA Figure 4	3.0		4	10	$\Omega$
		$V_{SW}=1.8$ V, $I_{ON}=-8$ mA Figure 4	3.0		6	10	
$R_{ON}$	Switch On Resistance <sup>(5)</sup>	$V_{SW}=0.4$ V, $I_{ON}=-8$ mA Figure 4	1.8		6	10	$\Omega$
		$V_{SW}=1.8$ V, $I_{ON}=-8$ mA Figure 4	1.8		14	25	
$\Delta R_{ON}$	On Resistance Match Between Channels <sup>(5,6)</sup>	$V_{SW}=0.4$ V, $I_{ON} = -8$ mA	3.0		35		m $\Omega$
			1.8		40		
$I_{CC}$	Quiescent Supply Current	$V_{CNTRL}=0$ or $V_{CC}$ , $I_{OUT}=0$	5.5			1	$\mu\text{A}$
$I_{CCT}$	Increase in $I_{CC}$ Current per Control Voltage and $V_{CC}$	$V_{CNTRL}=1.8$ V	3.0			10	$\mu\text{A}$
		$V_{CNTRL}=2.6$ V	5.5			10	
		$V_{CNTRL}=1.8$ V	5.5			15	

### Notes:

5. Measured by the voltage drop between A and Bn pins at the indicated current through the switch. On resistance is determined by the lower of the voltage on the two (A or Bn ports).
6.  $\Delta R_{ON} = R_{ON}$  maximum -  $R_{ON}$  minimum measured at identical  $V_{CC}$ , temperature, and voltage levels.
7. Guaranteed by characterization.

### AC Electrical Characteristics<sup>(8)</sup>

All typical value are for  $V_{CC}=3.3$  V at  $T_A=25^\circ\text{C}$  unless otherwise specified.

Symbol	Parameter	Condition	$V_{CC}$ (V)	$T_A=-40^\circ\text{C}$ to $+85^\circ\text{C}$			Unit
				Min.	Typ.	Max.	
$t_{ON}$	Turn-On Time S to Output	$R_L=50\ \Omega$ , $C_L=5\ \text{pF}$ , $V_{SW}=0.8\ \text{V}$ , Figure 6, Figure 7	3.0 to 3.6		34		ns
			1.8		110		
$t_{OFF}$	Turn-Off Time S to Output	$R_L=50\ \Omega$ , $C_L=5\ \text{pF}$ , $V_{SW}=0.8\ \text{V}$ , Figure 6, Figure 7	3.0 to 3.6		23		ns
			1.8		50		
$t_{PD}$	Propagation Delay	$C_L=5\ \text{pF}$ , $R_L=50\ \Omega$ , Figure 6, Figure 8	3.3		0.2		ns
			1.8		0.3		
$t_{BBM}$	Break-Before-Make	$R_L=50\ \Omega$ , $C_L=5\ \text{pF}$ , $V_{SW1}=V_{SW2}=0.8\ \text{V}$ , Figure 9	3.0 to 3.6	15		50	ns
			1.8			100	
$O_{IRR}$	Off Isolation	$R_L=50\ \Omega$ , $f=240\ \text{MHz}$ , Figure 11	1.8		-20		dB
			3.0 to 3.6		-23		
Xtalk	Crosstalk	$R_L=50\ \Omega$ , $f=240\ \text{MHz}$ , Figure 12	1.8		-18		dB
			3.0 to 3.6		-23		
BW	-3 db Bandwidth	$R_L=50\ \Omega$ , $C_L=0\ \text{pF}$ , $V_{SW}=0.4\ \text{V}$	1.8		810		MHz
		$R_L=50\ \Omega$ , $C_L=0\ \text{pF}$ , Figure 10	3.0 to 3.6		1		GHz
		$R_L=50\ \Omega$ , $C_L=5\ \text{pF}$ , Figure 10			750		MHz

**Note:**

8. Guaranteed by characterization. Not production tested.

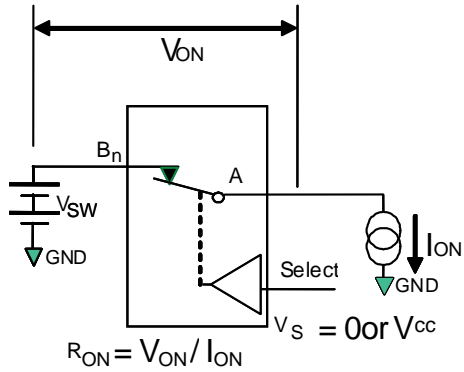
### Capacitance<sup>(9)</sup>

Symbol	Parameter	Condition	$V_{CC}$ (V)	$T_A=-40^\circ\text{C}$ to $+85^\circ\text{C}$			Unit
				Min.	Typ.	Max.	
$C_{IN}$	Control Pin Input Capacitance		0		1.5		pF
$C_{ON}$	A Port On Capacitance	$f=1\ \text{MHz}$ ,	3.0		7.7		
		$f=240\ \text{MHz}$ , Figure 14	3.3		7.7		
		$f=1\ \text{MHz}$ ,	1.8		10.0		
		$f=240\ \text{MHz}$ , Figure 14	1.8		5.0		
$C_{OFF}$	Bn Port Off Capacitance	$f=1\ \text{MHz}$	3.0		3.3		
		$f=240\ \text{MHz}$ , Figure 13	3.3		3.3		
		$f=1\ \text{MHz}$	1.8		5.0		
		$f=240\ \text{MHz}$ , Figure 13	1.8		4.0		

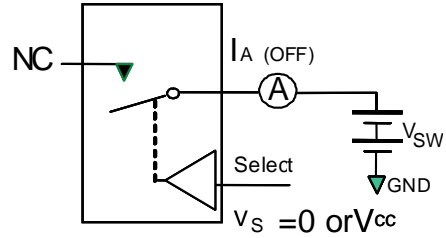
**Note:**

9. Not production tested.

### Test Diagrams

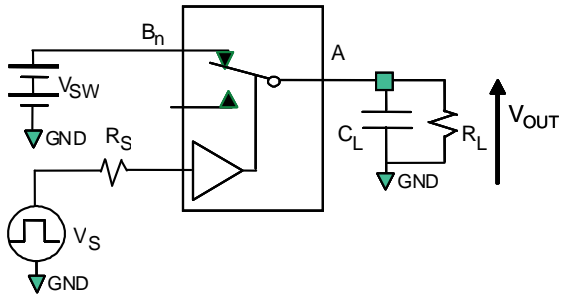


**Figure 4. On Resistance**



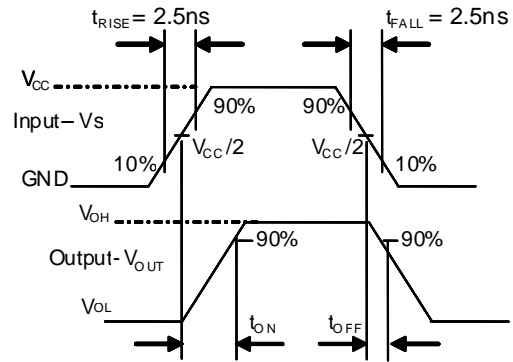
\*\*Each switch port is tested separately

**Figure 5. Off Leakage**

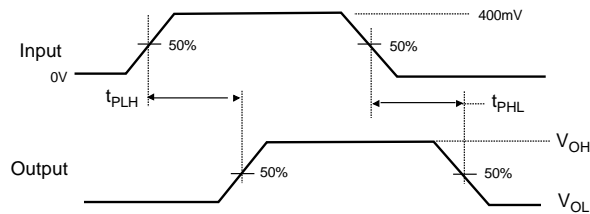


$R_L$ ,  $R_S$ , and  $C_L$  are functions of the application environment (see AC Tables for specific values)  
 $C_L$  includes test fixture and stray capacitance.

**Figure 6. AC Test Circuit Load**

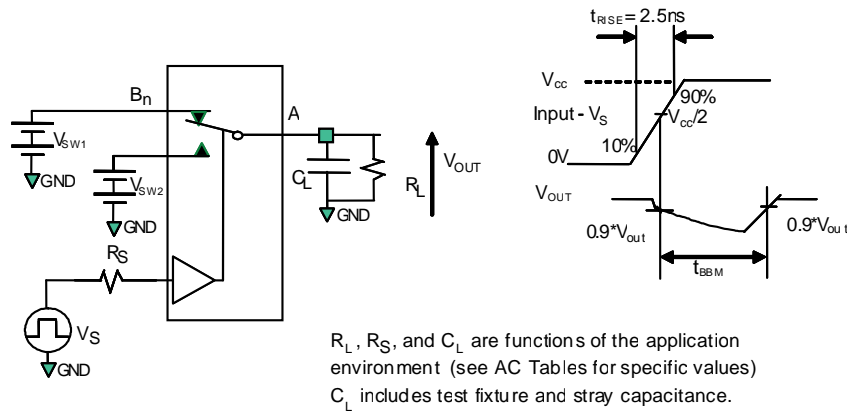


**Figure 7. Turn-On / Turn-Off Waveforms**

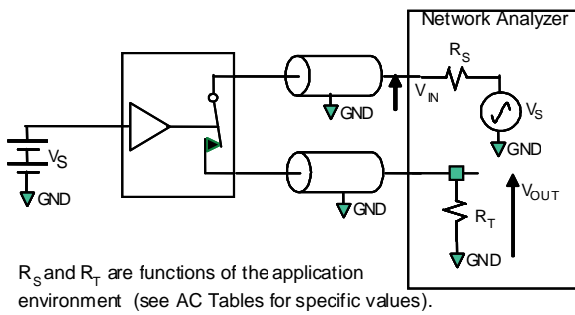


**Figure 8. Propagation Delay ( $t_{rTF} - 500$  ps)**

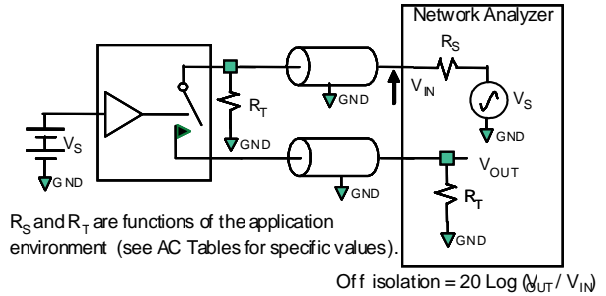
**Test Diagrams** (Continued)



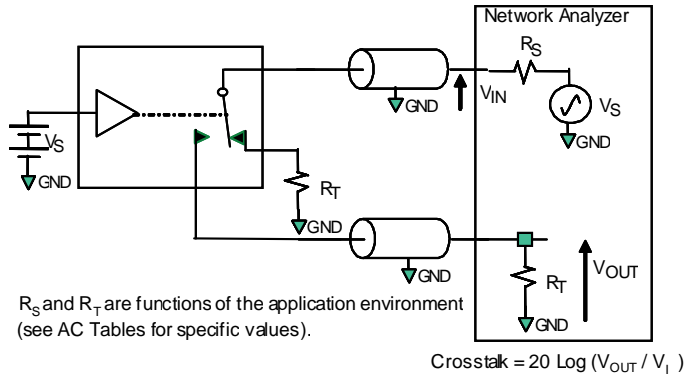
**Figure 9. Break-Before-Make Interval Timing**



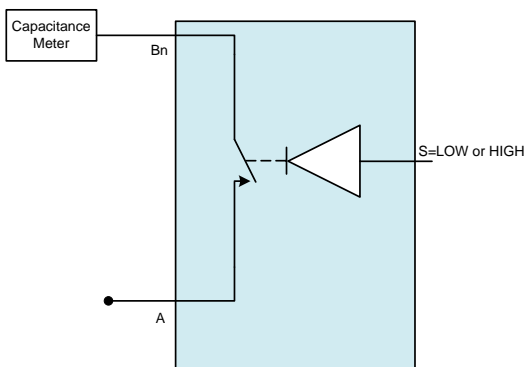
**Figure 10. Bandwidth**



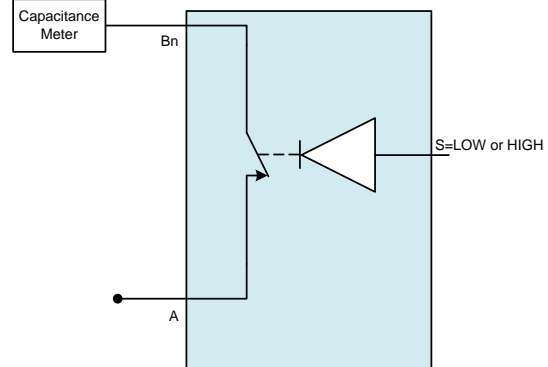
**Figure 11. Channel Off Isolation**



**Figure 12. Channel-to-Channel Crosstalk**



**Figure 13. Channel Off Capacitance**

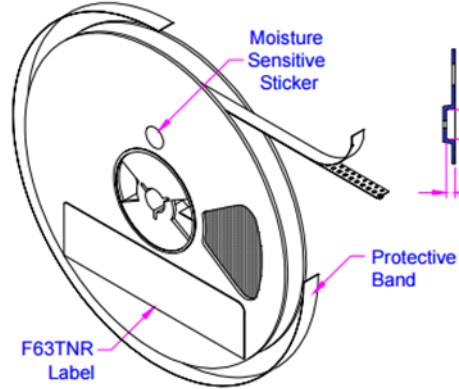


**Figure 14. Channel On Capacitance**

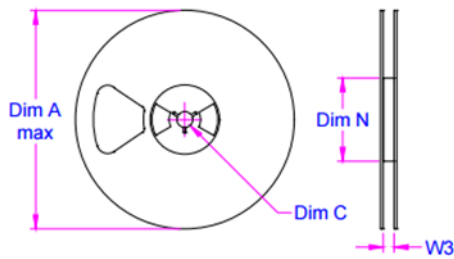


## Carrier Tape Orientation

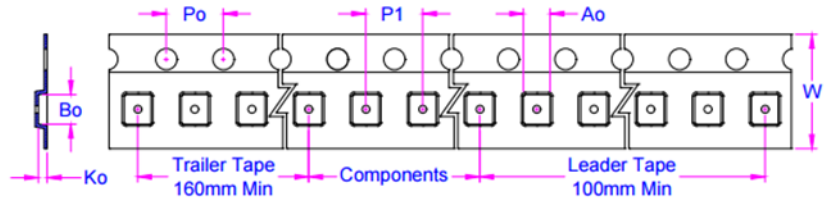
### TMLP TNR CONFIGURATION



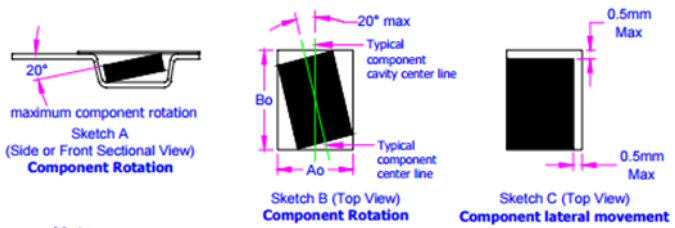
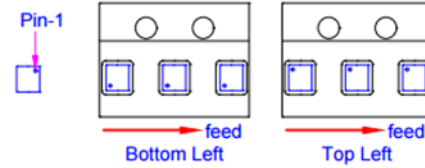
### Plastic Reel



### Embossed Carrier Tape



### Unit Orientation - refer to below table per MOD orientation



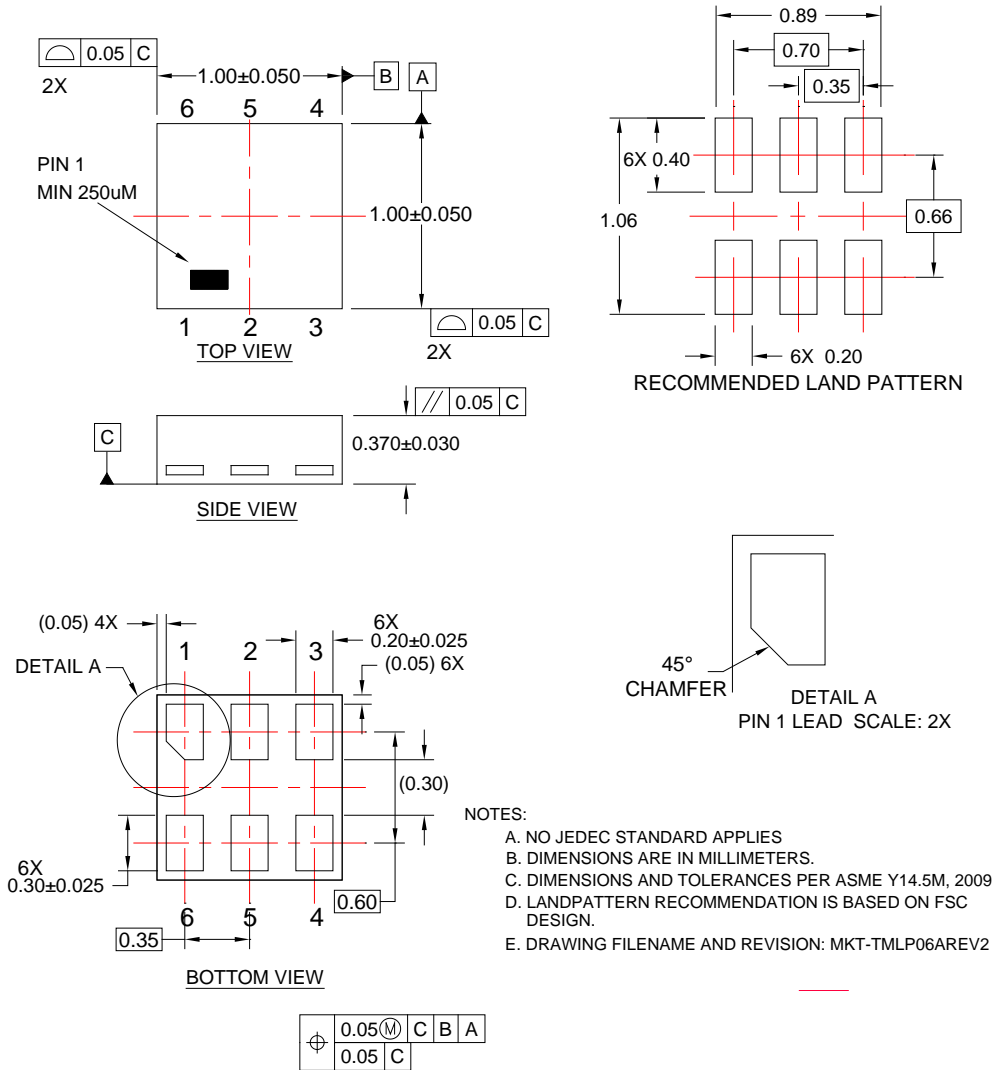
#### Notes:

Ao, Bo, and Ko dimensions are determined with respect to the EIA-481 rotational and lateral movement requirements (see sketches A, B, & C). Camber requirement also compliant to above mentioned standards.

Figure 15. TMLP Carrier Tape Packing

Part Number	Unit Orientation
FSA3051TMX	Top Left
FSA3051TMX-F147	Bottom Left

## Physical Dimensions



**6-Lead, Dual, Ultra-ultrathin Molded Leadless Package (TMLP), 1.0 x 1.0 mm**

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