

MOSFET – P-Channel, Logic Level, POWERTRENCH®

-40 V, -50 A, 13.5 mΩ

FDWS9510L-F085

Features

- Typ $R_{DS(on)}$ = 11 mΩ at $V_{GS} = -10$ V; $I_D = -50$ A
- Typ $Q_{g(tot)}$ = 28 nC at $V_{GS} = -10$ V; $I_D = -50$ A
- UIS Capability
- Wettable Flanks for Automatic Optical Inspection (AOI)
- AEC-Q101 Qualified
- These Devices are Pb-Free and are RoHS Compliant

Applications

- Automotive Engine Control
- Powertrain Management
- Solenoid and Motor Drivers
- Electronic Steering
- Integrated Starter/Alternator
- Distributed Power Architectures and VRM
- Primary Switch for 12 V Systems

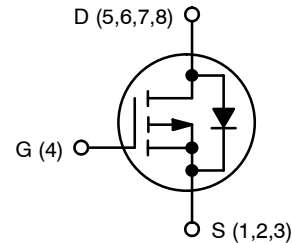
MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter		Symbol	Value	Unit
Drain-to-Source Voltage		V_{DSS}	-40	V
Gate-to-Source Voltage		V_{GS}	±16	V
Continuous Drain Current (V _{GS} = 10 V) (Note 1)	T _C = 25°C	I_D	-50	A
Pulsed Drain Current	T _C = 25°C		See Figure 4	
Single Pulse Avalanche Energy (Note 2)		E_{AS}	32	mJ
Power Dissipation		P_D	75	W
Derate above 25°C			0.5	W/°C
Operating and Storage Temperature		T _J , T _{STG}	-55 to +175	°C
Thermal Resistance (Junction-to-Case)		$R_{\theta JC}$	2	°C/W
Maximum Thermal Resistance (Junction-to-Ambient) (Note 3)		$R_{\theta JA}$	50	°C/W

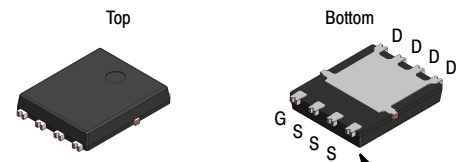
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Current is limited by wirebond configuration
2. Starting T_J = 25°C, L = 40 μH, I_{AS} = -40 A, V_{DD} = -40 V during inductor charging and V_{DD} = 0 V during time in avalanche
3. R_{θJA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{θJC} is guaranteed by design while R_{θJA} is determined by the user's board design. The maximum rating presented here is based on mounting on a 1 in² pad of 2 oz copper.

V_{DSS}	$R_{DS(ON)}$ MAX	I_D MAX
-40 V	13.5 mΩ @ -10 V	-50 A

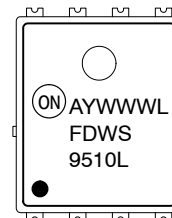


P-Channel MOSFET



DFNW8
CASE 507AU

MARKING DIAGRAM



- A = Assembly Location
- Y = Year
- WW = Work Week
- WL = Assembly Lot
- FDWS = Device Code
- 9510L = Device Code

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
FDWS9510L-F085	DFNW8 (Power56) (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

FDWS9510L-F085

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

B_{VDSS}	Drain-to-Source Breakdown Voltage	$I_D = -250 \mu\text{A}, V_{GS} = 0 \text{ V}$	-40	-	-	V	
I_{DSS}	Drain-to-Source Leakage Current	$V_{DS} = -40 \text{ V}, V_{GS} = 0 \text{ V}$	$T_J = 25^\circ\text{C}$	-	-	1	μA
			$T_J = 175^\circ\text{C}$ (Note 4)	-	-	1	mA
I_{GSS}	Gate-to-Source Leakage Current	$V_{GS} = \pm 16 \text{ V}$	-	-	± 100	nA	

ON CHARACTERISTICS

$V_{GS(th)}$	Gate-to-Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = -250 \mu\text{A}$	-1	-1.8	-3	V	
$R_{DS(on)}$	Drain-to-Source On-Resistance	$I_D = -25 \text{ A}, V_{GS} = -4.5 \text{ V}$	$T_J = 25^\circ\text{C}$	-	18	23	$\text{m}\Omega$
			$T_J = 175^\circ\text{C}$ (Note 4)	-	18.8	23	
		$I_D = -50 \text{ A}, V_{GS} = -10 \text{ V}$	-	11	13.5	$\text{m}\Omega$	

DYNAMIC CHARACTERISTICS

C_{iss}	Input Capacitance	$V_{DS} = -20 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	-	2320	-	pF	
	Output Capacitance		-	811	-		
	Reverse Transfer Capacitance		-	38	-		
R_g	Gate Resistance	$V_{GS} = 0.5 \text{ V}, f = 1 \text{ MHz}$	-	23	-	Ω	
$Q_{g(tot)}$	Total Gate Charge	$V_{GS} = 0 \text{ to } -10 \text{ V}$ $V_{DD} = -20 \text{ V}, I_D = -50 \text{ A}$	-	28	37	nC	
$Q_{g(th)}$	Threshold Gate Charge		$V_{GS} = 0 \text{ to } -1 \text{ V}$	-	4		-
Q_{gs}	Gate-to-Source Gate Charge		-	-	7		-
Q_{gd}	Gate-to-Drain "Miller" Charge		-	-	4		-

SWITCHING CHARACTERISTICS

t_{on}	Turn-On Time	$V_{DD} = -20 \text{ V}, I_D = -50 \text{ A}, V_{GS} = -10 \text{ V}, R_{GEN} = 6 \Omega$	-	-	20	ns
$t_{d(on)}$	Turn-On Delay Time		-	10	-	
t_r	Turn-On Rise Time		-	4	-	
$t_{d(off)}$	Turn-Off Delay Time		-	110	-	
t_f	Turn-Off Fall Time		-	37	-	
t_{off}	Turn-Off Time		-	-	222	

DRAIN-SOURCE DIODE CHARACTERISTICS

V_{SD}	Source-to-Drain Diode Voltage	$I_{SD} = -50 \text{ A}, V_{GS} = 0 \text{ V}$	-	-1	-1.25	V
		$I_{SD} = -25 \text{ A}, V_{GS} = 0 \text{ V}$	-	-0.9	-1.2	
T_{rr}	Reverse Recovery Time	$I_F = -50 \text{ A}, di_{SD}/dt = 100 \text{ A}/\mu\text{s}$	-	44	62	ns
Q_{rr}	Reverse Recovery Charge		-	31	47	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. The maximum value is specified by design at $T_J = 175^\circ\text{C}$. Product is not tested to this condition in production

TYPICAL CHARACTERISTICS

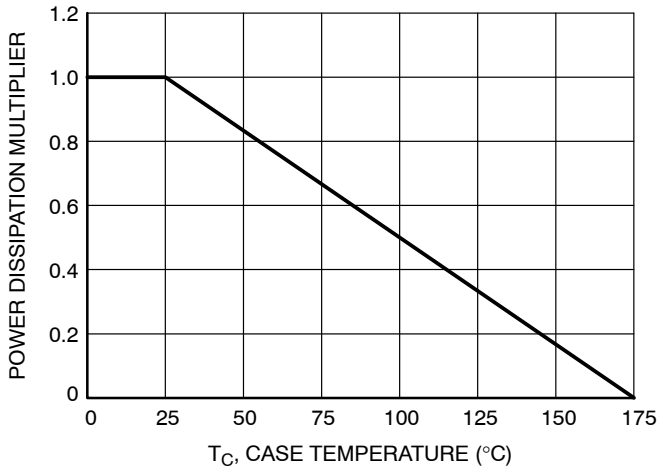


Figure 1. Normalized Power Dissipation vs. Case Temperature

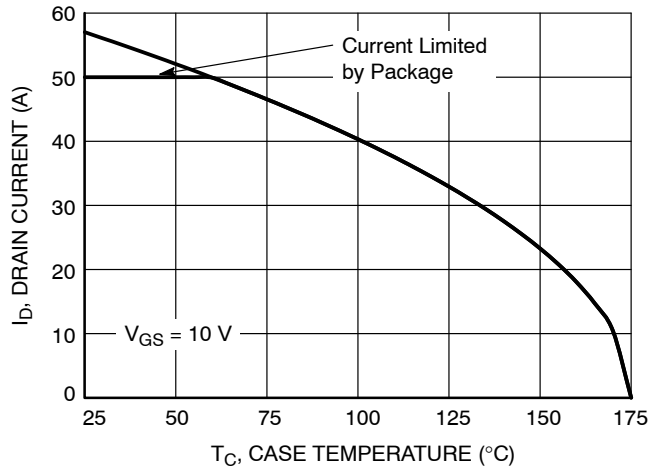


Figure 2. Maximum Continuous Drain Current vs. Case Temperature

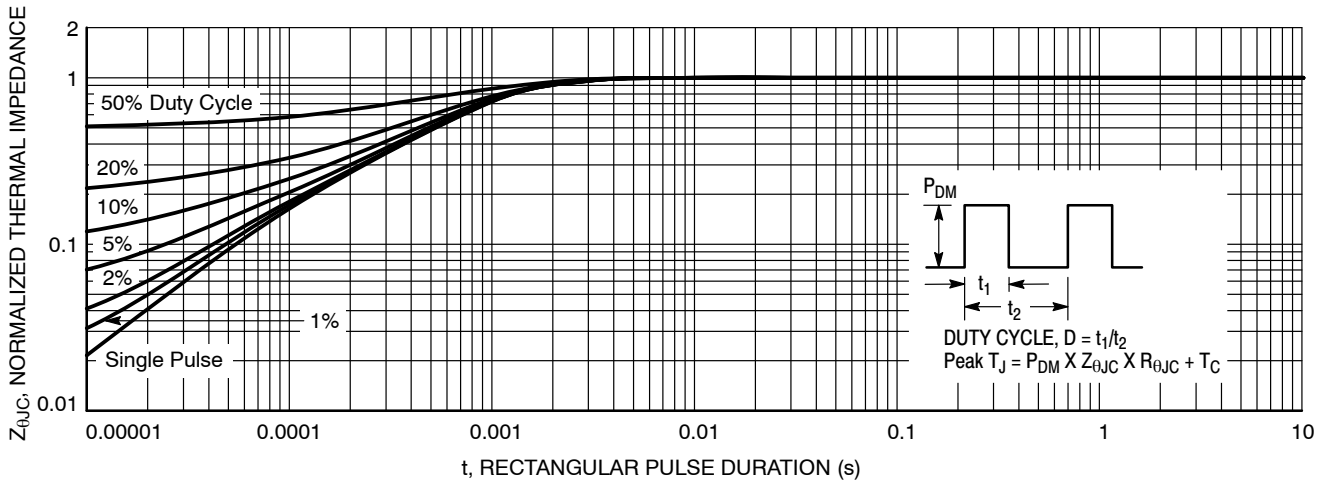


Figure 3. Normalized Maximum Transient Thermal Impedance

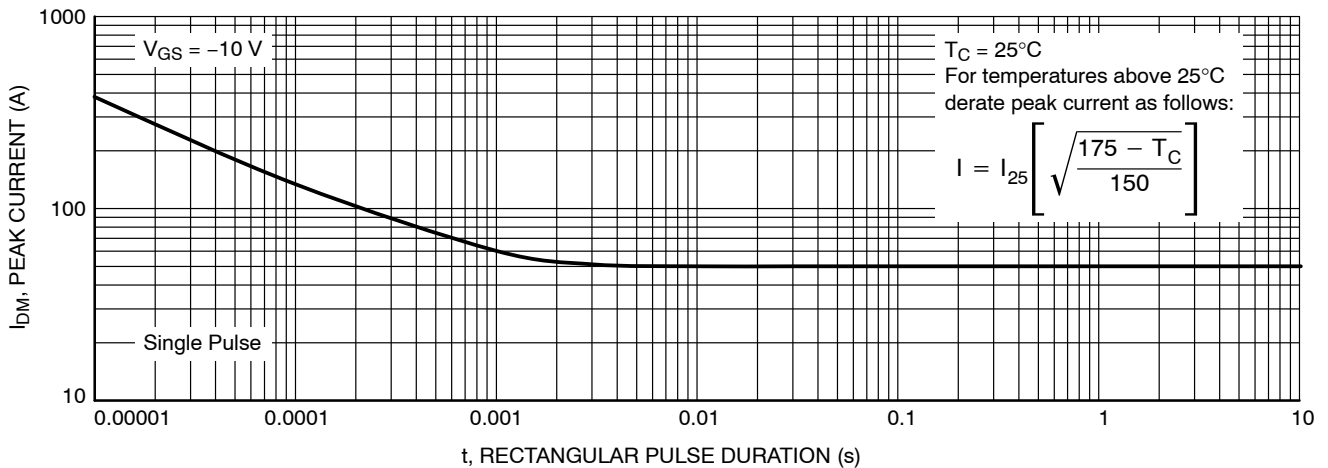


Figure 4. Peak Current Capability

TYPICAL CHARACTERISTICS

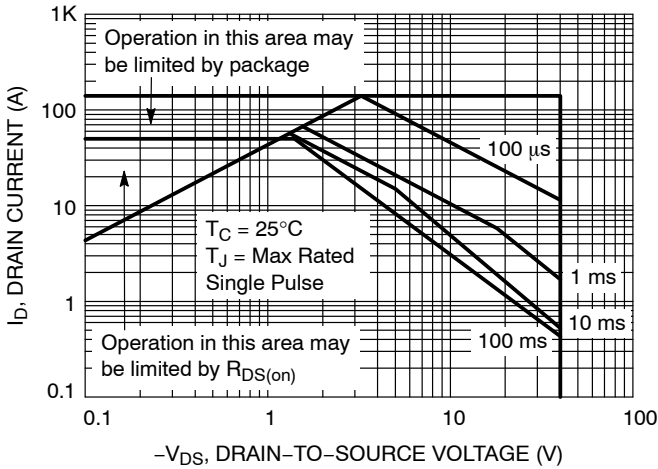


Figure 5. Forward Bias Safe Operating Area

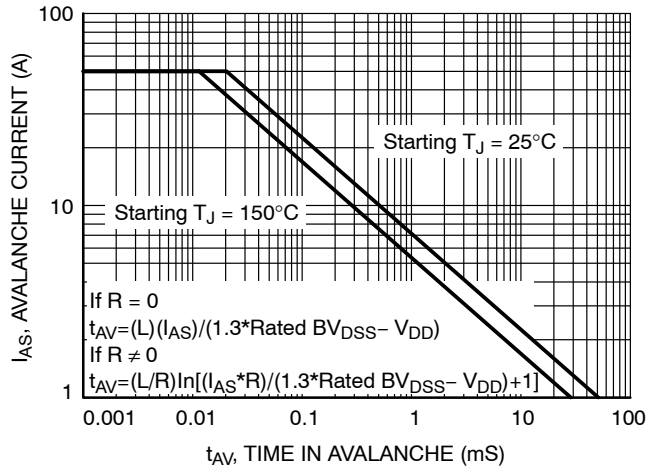


Figure 6. Unclamped Inductive Switching Capability

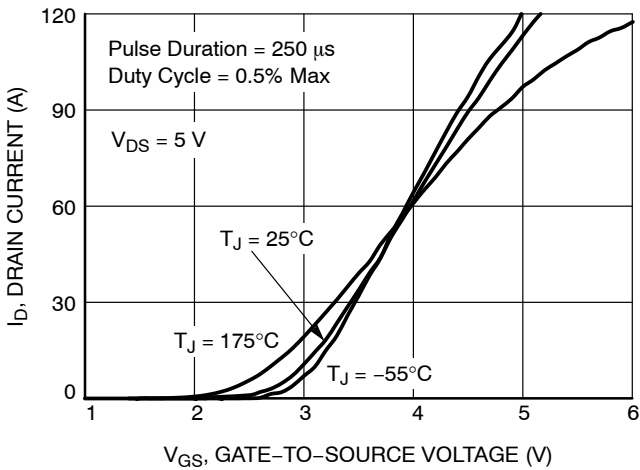


Figure 7. Transfer Characteristics

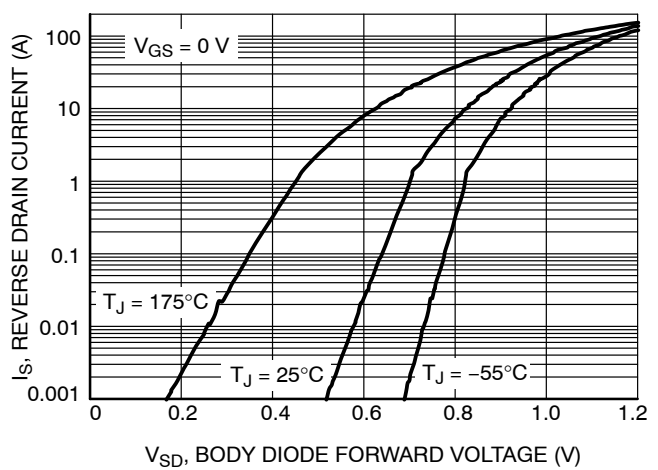


Figure 8. Forward Diode Characteristics

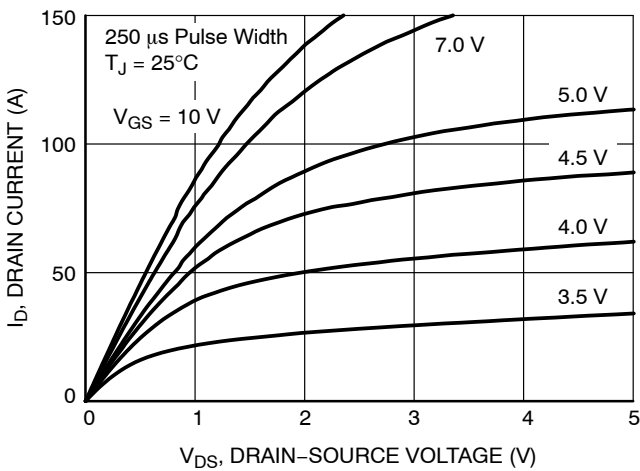


Figure 9. Saturation Characteristics

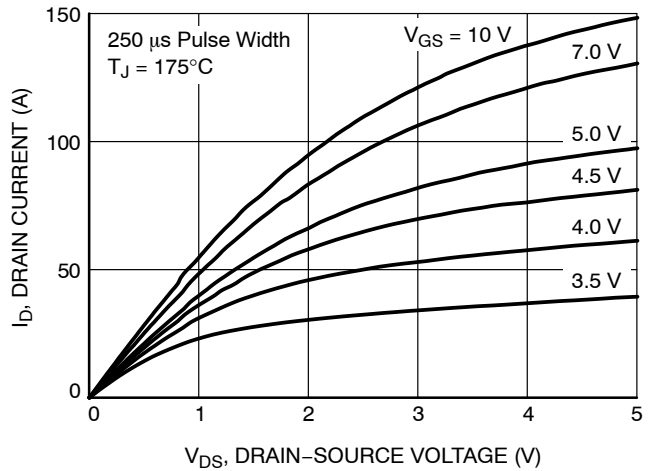


Figure 10. Saturation Characteristics

TYPICAL CHARACTERISTICS

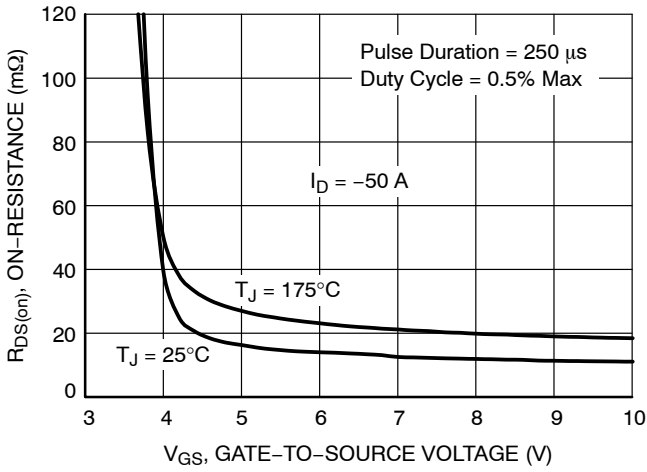


Figure 11. $R_{DS(on)}$ vs. Gate Voltage

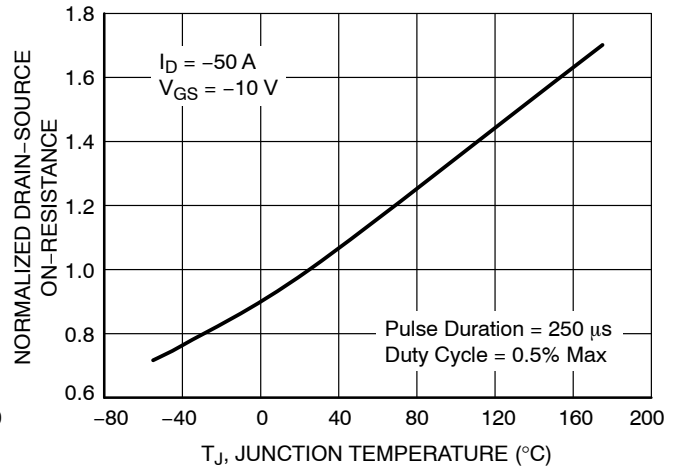


Figure 12. Normalized $R_{DS(on)}$ vs. Junction Temperature

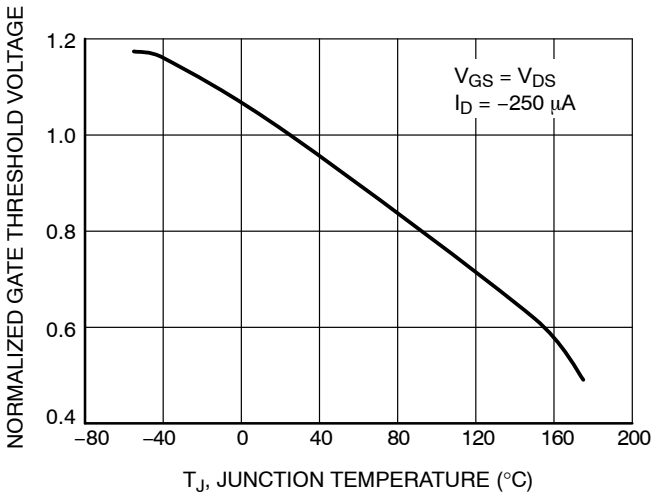


Figure 13. Normalized Gate Threshold Voltage vs. Temperature

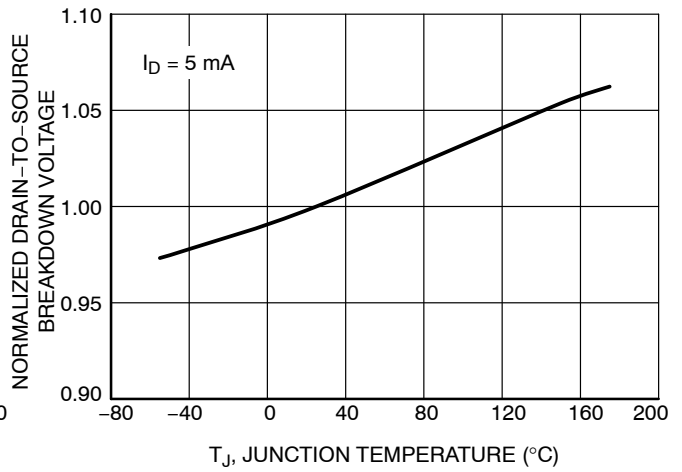


Figure 14. Normalized Drain-to-Source Breakdown Voltage vs. Junction Temperature

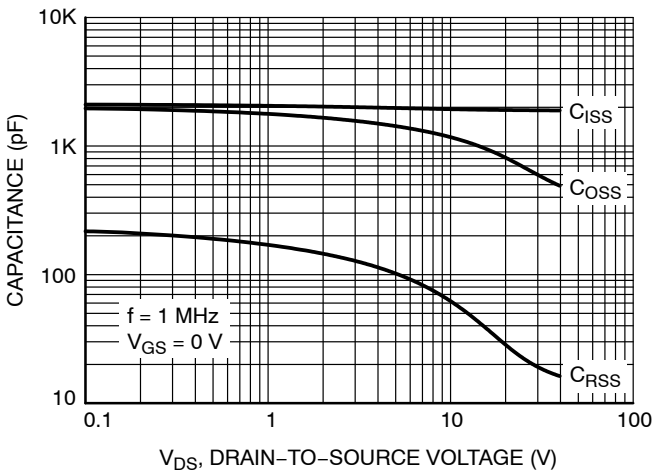


Figure 15. Capacitance vs. Drain-to-Source Voltage

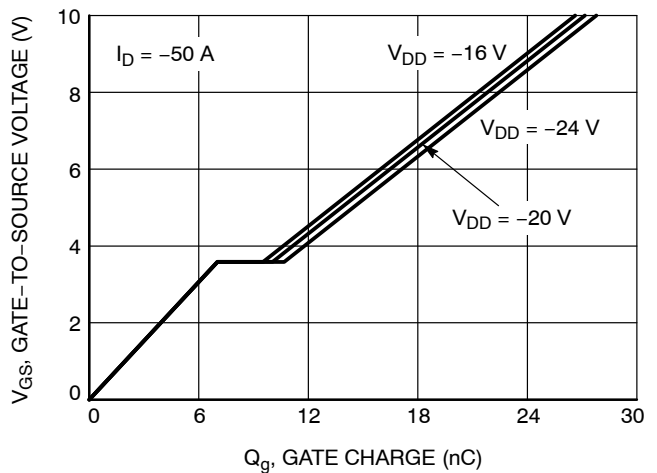
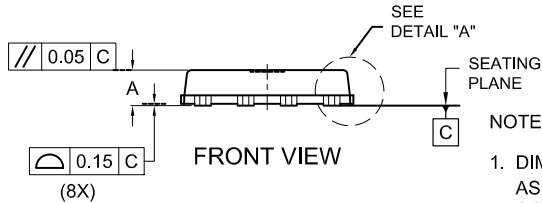
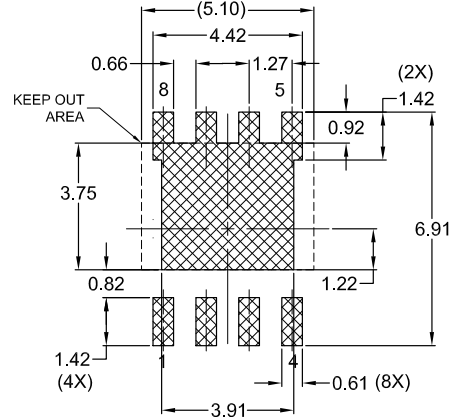
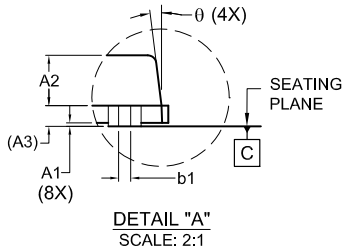
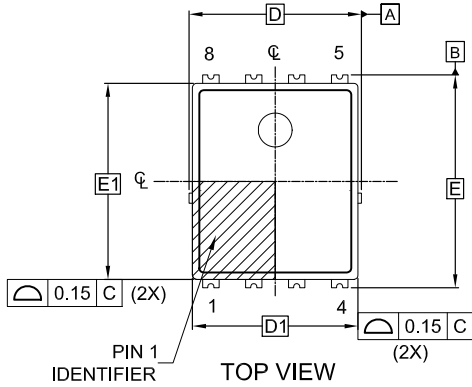


Figure 16. Gate Charge vs. Gate-to-Source Voltage

FDWS9510L-F085

PACKAGE DIMENSIONS

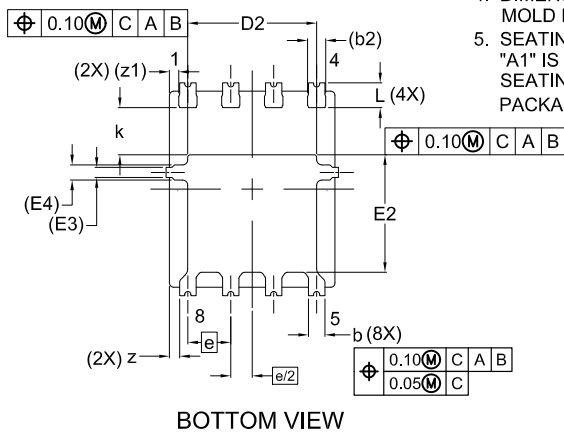
DFNW8 5.2x6.3, 1.27P
CASE 507AU
ISSUE A



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.



DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	-	-	0.05
A2	0.65	0.75	0.85
A3	0.30 REF		
b	0.47	0.52	0.57
b1	0.13	0.18	0.23
b2	(0.54)		
D	5.00	5.10	5.20
D1	4.80	4.90	5.00
D2	3.72	3.82	3.92
E	6.20	6.30	6.40
E1	5.70	5.80	5.90
E2	3.38	3.48	3.58
E3	0.30 REF		
E4	0.45 REF		
e	1.27 BSC		
e/2	0.635BSC		
k	1.30	1.40	1.50
L	0.64	0.74	0.84
z	0.24	0.29	0.34
z1	(0.28)		
θ	0°	---	12°

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