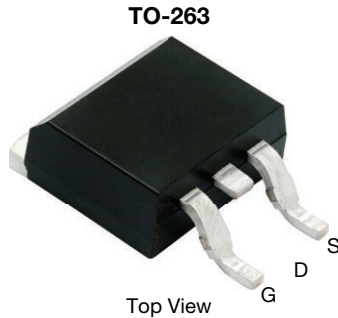


## P-Channel 100 V (D-S) 175 °C MOSFET



### FEATURES

- TrenchFET® power MOSFET
- Package with low thermal resistance
- Maximum 175 °C junction temperature
- Low  $R_{DS(on)}$  minimizes power loss from conduction
- Compatible with logic-level gate driving
- 100 %  $R_g$  and UIS tested
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)

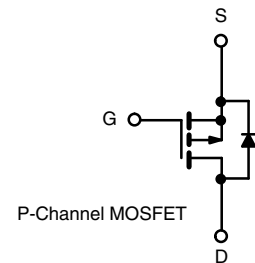


**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**

PRODUCT SUMMARY	
$V_{DS}$ (V)	-100
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = -10$ V	0.0101
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = -4.5$ V	0.0150
$Q_g$ typ. (nC)	125
$I_D$ (A)	-120
Configuration	Single

### APPLICATIONS

- Battery protection
- Motor drive control
- Load switch



ORDERING INFORMATION	
Package	TO-263
Lead (Pb)-free and halogen-free	SUM70101EL-GE3

ABSOLUTE MAXIMUM RATINGS ( $T_C = 25$ °C, unless otherwise noted)				
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		$V_{DS}$	-100	V
Gate-source voltage		$V_{GS}$	$\pm 20$	
Continuous drain current <sup>d</sup> ( $T_J = 175$ °C)	$T_C = 25$ °C	$I_D$	-120	A
	$T_C = 125$ °C		-78	
Pulsed drain current (100 $\mu$ s)		$I_{DM}$	-240	
Avalanche current	L = 0.1 mH	$I_{AS}$	-75	
Single pulse avalanche energy <sup>a</sup>		$E_{AS}$	281	mJ
Power dissipation	$T_C = 25$ °C <sup>c</sup>	$P_D$	375	W
	$T_C = 125$ °C <sup>b</sup>		125	
Operating junction and storage temperature range		$T_J, T_{stg}$	-55 to +175	°C

THERMAL RESISTANCE RATINGS				
PARAMETER		SYMBOL	TYPICAL	UNIT
Junction-to-ambient	PCB mount <sup>b</sup>	$R_{thJA}$	40	°C/W
Junction-to-case		$R_{thJC}$	0.4	

#### Notes

- Duty cycle  $\leq 1$  %
- When mounted on 1" square PCB (FR4 material)
- See SOA curve for voltage derating
- Limited by package



SPECIFICATIONS (T <sub>J</sub> = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Static</b>						
Drain-source breakdown voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = -250 μA	-100	-	-	V
Gate threshold voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250 μA	-1.5	-	-2.5	
Gate-body leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 20 V	-	-	± 100	nA
Zero gate voltage drain current	I <sub>DSS</sub>	V <sub>DS</sub> = -100 V, V <sub>GS</sub> = 0 V	-	-	-1	μA
		V <sub>DS</sub> = -100 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C	-	-	-50	
		V <sub>DS</sub> = -100 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 175 °C	-	-	-250	
On-state drain current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> ≤ -5 V, V <sub>GS</sub> = -10 V	-120	-	-	A
Drain-source on-state resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = -10 V, I <sub>D</sub> = -30 A	-	0.0081	0.0101	Ω
		V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -20 A	-	0.0114	0.0150	
Forward transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = -15 V, I <sub>D</sub> = -25 A	-	60	-	S
<b>Dynamic <sup>b</sup></b>						
Input capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = -50 V, f = 1 MHz	-	7000	-	pF
Output capacitance	C <sub>oss</sub>		-	2180	-	
Reverse transfer capacitance	C <sub>rss</sub>		-	170	-	
Total gate charge <sup>c</sup>	Q <sub>g</sub>	V <sub>DS</sub> = -50 V, V <sub>GS</sub> = -10 V, I <sub>D</sub> = -110 A	-	125	190	nC
Gate-source charge <sup>c</sup>	Q <sub>gs</sub>		-	29	-	
Gate-drain charge <sup>c</sup>	Q <sub>gd</sub>		-	30	-	
Gate resistance	R <sub>g</sub>	f = 1 MHz	1.3	6.5	13	Ω
Turn-on delay time <sup>c</sup>	t <sub>d(on)</sub>	V <sub>DD</sub> = -50 V, R <sub>L</sub> = 0.71 Ω I <sub>D</sub> ≅ -70 A, V <sub>GEN</sub> = -10 V, R <sub>g</sub> = 1 Ω	-	20	30	ns
Rise time <sup>c</sup>	t <sub>r</sub>		-	40	60	
Turn-off delay time <sup>c</sup>	t <sub>d(off)</sub>		-	110	200	
Fall time <sup>c</sup>	t <sub>f</sub>		-	40	60	
<b>Drain-Source Body Diode Characteristics (T<sub>C</sub> = 25 °C <sup>b</sup>)</b>						
Continuous current	I <sub>S</sub>		-	-	-110	A
Pulsed current	I <sub>SM</sub>		-	-	-240	
Forward voltage <sup>a</sup>	V <sub>SD</sub>	I <sub>F</sub> = -85 A, V <sub>GS</sub> = 0 V	-	-1	-1.5	V
Reverse recovery time	t <sub>rr</sub>	I <sub>F</sub> = -85 A, dI/dt = 100 A/μs	-	110	170	ns
Peak reverse recovery charge	I <sub>RM(REC)</sub>		-	-7	-11	A
Reverse recovery charge	Q <sub>rr</sub>		-	0.38	0.57	μC

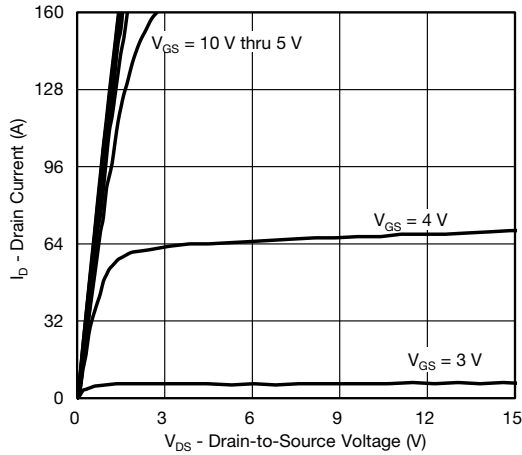
**Notes**

- Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %
- Guaranteed by design, not subject to production testing
- Independent of operating temperature

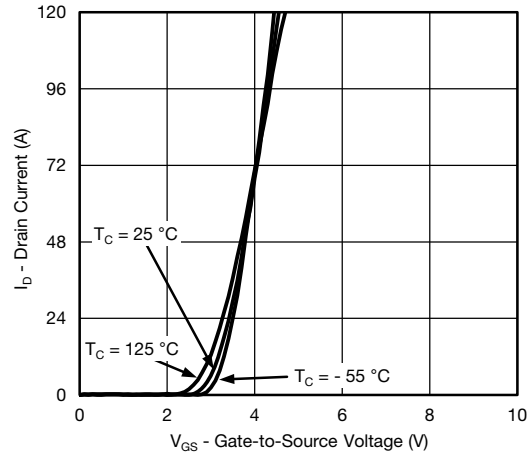
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



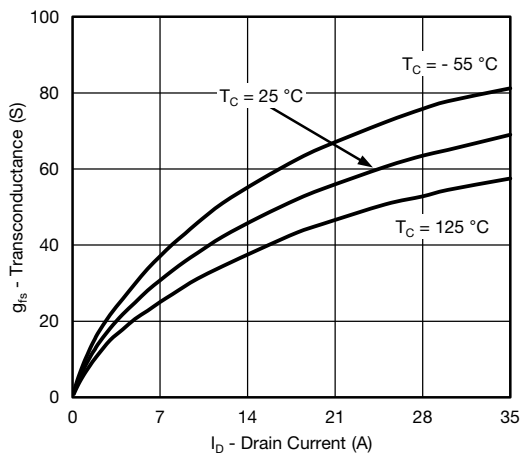
TYPICAL CHARACTERISTICS (T<sub>A</sub> = 25 °C, unless otherwise noted)



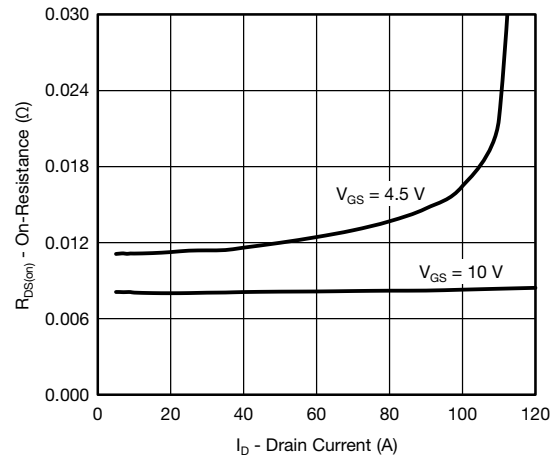
Output Characteristics



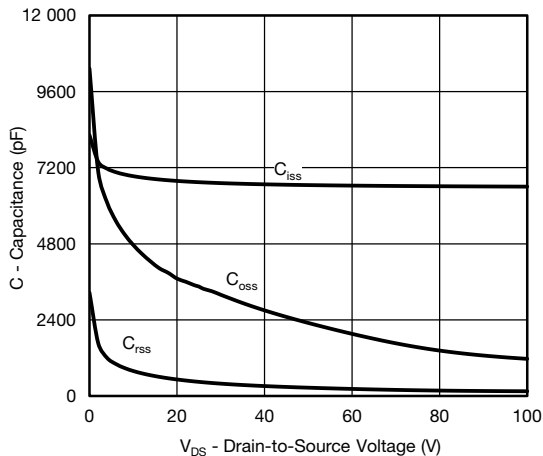
Transfer Characteristics



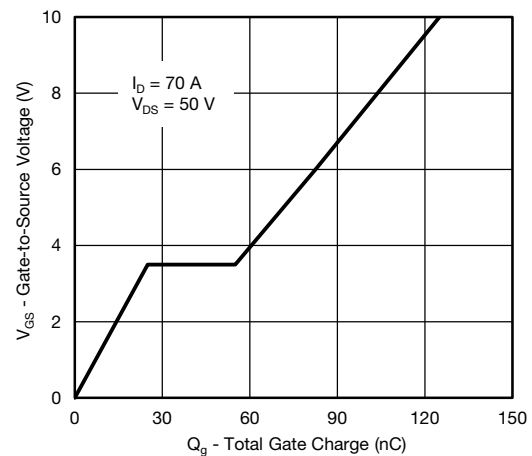
Transconductance



On-Resistance vs. Drain Current



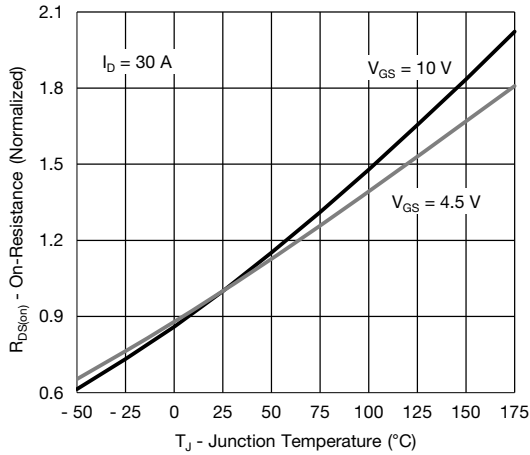
Capacitance



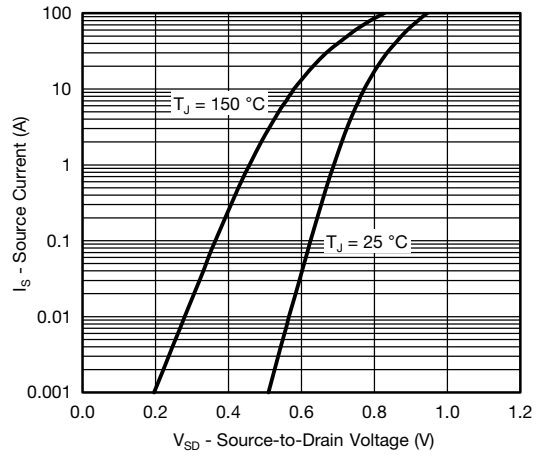
Gate Charge



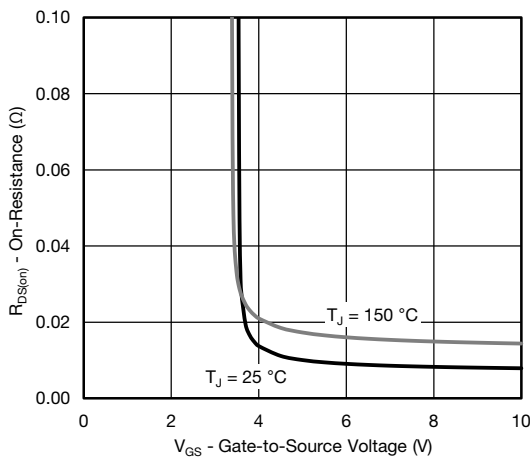
TYPICAL CHARACTERISTICS (T<sub>A</sub> = 25 °C, unless otherwise noted)



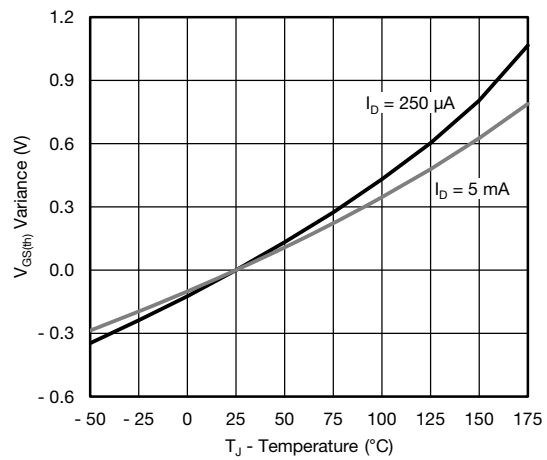
On-Resistance vs. Junction Temperature



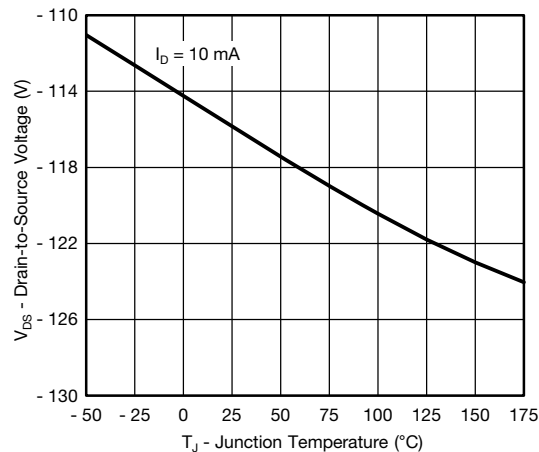
Source Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage



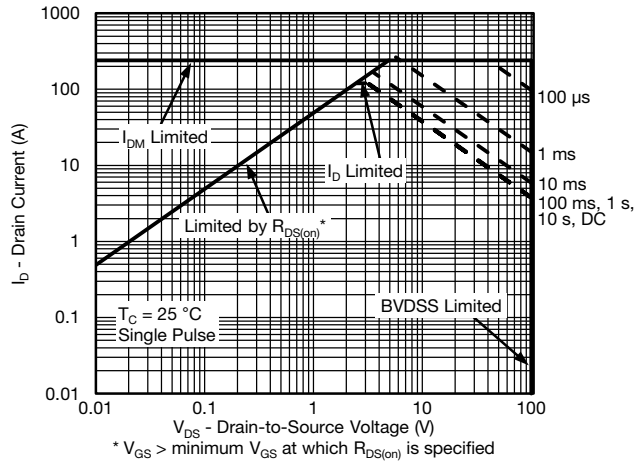
Threshold Voltage



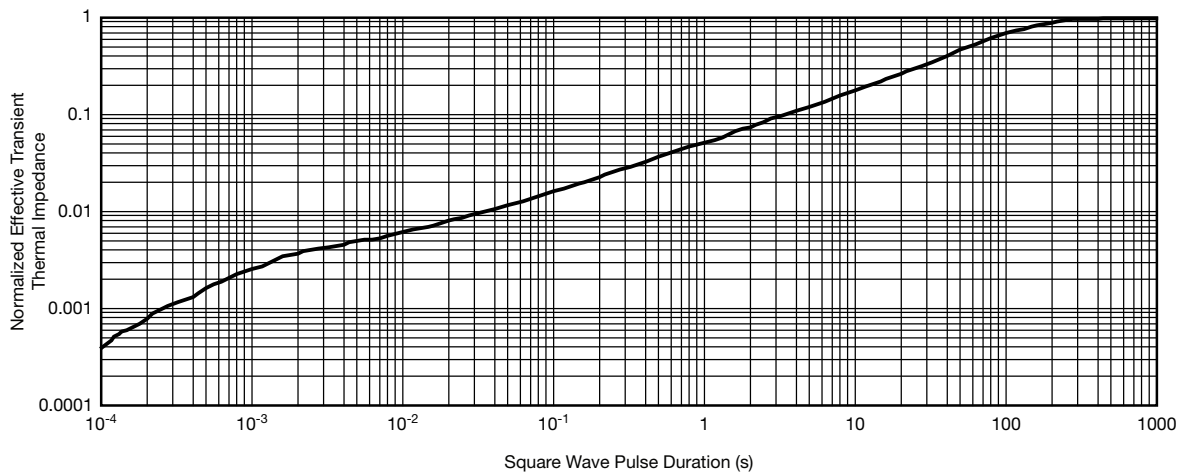
Drain Source Breakdown vs. Junction Temperature



**THERMAL RATINGS** ( $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise noted)



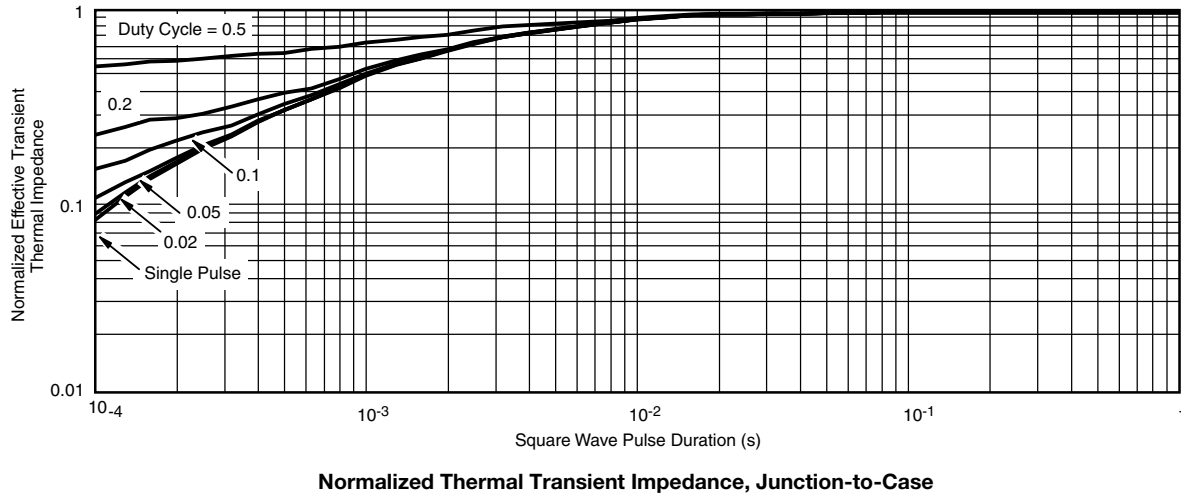
**Safe Operating Area**



**Normalized Thermal Transient Impedance, Junction-to-Ambient**



**THERMAL RATINGS** ( $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise noted)



**Note**

- The characteristics shown in the two graphs
  - Normalized Transient Thermal Impedance Junction to Ambient ( $25\text{ }^\circ\text{C}$ )
  - Normalized Transient Thermal Impedance Junction to Case ( $25\text{ }^\circ\text{C}$ )
 are given for general guidelines only to enable the user to get a “ball park” indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

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# TO-263 (D<sup>2</sup>PAK): 3-LEAD



DIM.	INCHES		MILLIMETERS		
	MIN.	MAX.	MIN.	MAX.	
A	0.160	0.190	4.064	4.826	
b	0.020	0.039	0.508	0.990	
b1	0.020	0.035	0.508	0.889	
b2	0.045	0.055	1.143	1.397	
c*	Thin lead	0.013	0.018	0.330	0.457
	Thick lead	0.023	0.028	0.584	0.711
c1	Thin lead	0.013	0.017	0.330	0.431
	Thick lead	0.023	0.027	0.584	0.685
c2	0.045	0.055	1.143	1.397	
D	0.340	0.380	8.636	9.652	
D1	0.220	0.240	5.588	6.096	
D2	0.038	0.042	0.965	1.067	
D3	0.045	0.055	1.143	1.397	
D4	0.044	0.052	1.118	1.321	
E	0.380	0.410	9.652	10.414	
E1	0.245	-	6.223	-	
E2	0.355	0.375	9.017	9.525	
E3	0.072	0.078	1.829	1.981	
e	0.100 BSC		2.54 BSC		
K	0.045	0.055	1.143	1.397	
L	0.575	0.625	14.605	15.875	
L1	0.090	0.110	2.286	2.794	
L2	0.040	0.055	1.016	1.397	
L3	0.050	0.070	1.270	1.778	
L4	0.010 BSC		0.254 BSC		
M	-	0.002	-	0.050	
ECN: T13-0707-Rev. K, 30-Sep-13					
DWG: 5843					

**Notes**

- Plane B includes maximum features of heat sink tab and plastic.
- No more than 25 % of L1 can fall above seating plane by max. 8 mils.
- Pin-to-pin coplanarity max. 4 mils.
- \*: Thin lead is for SUB, SYB.  
Thick lead is for SUM, SYM, SQM.
- Use inches as the primary measurement.
- This feature is for thick lead.

**RECOMMENDED MINIMUM PADS FOR D<sup>2</sup>PAK: 3-Lead**



Recommended Minimum Pads  
Dimensions in Inches/(mm)

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