Errata

AWR1243 DeviceSilicon Errata Silicon Revisions 1.0, 2.0, and 3.0

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1 Introduction

This document describes the known exceptions to the functional and performance specifications to TI CMOS Radar Devices (AWR1243).

2 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of Radar / mmWave sensor devices. Each of the Radar devices has one of the two prefixes: X1x or AWR1x (for example: **AWR1243**FBIGABLRQ1). These prefixes represent evolutionary stages of product development from engineering prototypes (X1x) through fully qualified production devices (AWR1x).

Device development evolutionary flow:

X1x — Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.

AWR1x — Production version of the silicon die that is fully qualified.

X1x devices are shipped with the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

Texas Instruments recommends that these devices not to be used in any production system as their expected end –use failure rate is still undefined.

3 Device Markings

Figure 3-1 shows an example of the AWR1243 Radar Device's package symbolization.

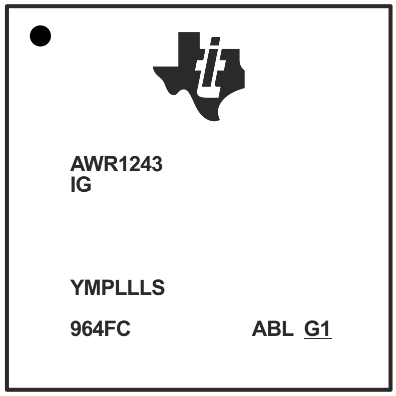

Figure 3-1. Example of Device Part Markings

This identifying number contains the following information:

- **Line 1:** Device Number
- **Line 2:** Temperature and Security Grade
- **Line 3:** Lot Trace Code
  - YM = Year/Month Code
  - PLLL = Assembly Lot
  - S = Assembly Site Code
- **Line 4:**
  - 964 = AWR1243 Identifier
  - F = ES3.0
  - D = ES2.0
  - BLANK = ES1.0
  - ABL = Package Identifier
  - G1 = "Green" Package Build (must be underlined)

4 Advisory to Silicon Variant / Revision Map

Table 4-1. Advisory to Silicon Variant / Revision Map

Advisory Number	Advisory Title	AWR1243		
		ES1.0	ES2.0	ES3.0
	Master Subsystem			
MSS#06	Internal Pulls on QSPI Data Lines not Enabled by the Device Bootloader	X	X	
MSS#18	Core Compare Module (CCM-R4F) may Cause nERROR Toggle After First Reset De-assertion Subsequent to Power Application	X	X	
MSS#44	SYNC IN input pulse wider than 4usec can cause a FRC lockstep error	X	X	X
	Analog / Millimeter Wave			
ANA#01	Noise Figure Degradation	X		
ANA#02	VCO#1 [76-77GHz] Minimum Frequency Falls Short of Target	X		
ANA#03	Spurs from LVDS Output Coupling into Synthesizer	X		
ANA#04	Receiver Gain Range Availability	X		
ANA#06	Return Loss Measurement on TX: S11 < –9dB, RX S11 < –6.5dB (Accepted Value of < –10dB)	X	X	
ANA#07	CSI2 Activity Coupling to Clock	X	X	
ANA#08A	Doppler Spur Observed at Certain RF Frequencies	X	X	X
ANA#09A	Synthesizer Frequency Nonlinearity around 76.8 GHz when Synthesizer (Chirp) Frequency Monitor Enabled	X	X	X
ANA#10A	Unreliable Readings from Synthesizer Supply Voltage Monitor	X	X	X
ANA#11A	TX, RX Gain Calibrations Sensitive to Large External Interference	X	X	X
ANA#12A	Second Harmonic (HD2) Present in the Receiver	X	X	X
ANA#13	TX1 to TX3 Phase Mismatch Variation over Temperature is Double that of TX2/TX1 and TX3/TX2 Combinations	X	X	X
ANA#15	Excessive TX-RX Coupling or Reflection can Lead to Saturated RX Output	X	X	X
ANA#17A	On-Board Supply Ringing Induced Spur	X	X	X
ANA#18B	Spurs Caused due to Digital Activity Coupling to XTAL	X	X	X
ANA#20	Occasional Failures Observed During Calibration of the Radar Subsystem	X	X	X
ANA#21A	Out of Band Radiated Spectral Emission	X	X	X
ANA#22A	Overshoot and Undershoot During Inter-Chirp Idle Time	X	X	X
ANA#23	MIPI CSI2 HS Data TX Differential Voltage Mismatch (Pulse) Marginality	X	X	X
ANA#24A	40-MHz OSC CLKOUT Causing Spurs in 2D-FFT Spectrum	X	X	X
ANA#27	Digital Temperature Sensor Having Higher Error	X	X	X

5 Known Design Exceptions to Functional Specifications

MSS#06 — *Internal Pulls on QSPI Data Lines not Enabled by the Device Bootloader*

Revision(s) Affected: AWR1243 ES1.0 and AWR1243 ES2.0

Description: Internal Pulls on the Data lines (D2 and D3) are not enabled by the device bootloader.

Workaround(s): Pulls on target board required (refer to reference schematics of TI EVM).

MSS#18 — *Core Compare Module (CCM-R4F) may Cause nERROR Toggle After First Reset De-assertion Subsequent to Power Application*

Revision(s) Affected: AWR1243 ES1.0 and AWR1243 ES2.0

Description: The CCM-R4F module compares the outputs of the two Cortex-R4F CPU cores and generates an error on any mis-compare. This ensures the lock-step operation of the two Cortex-R4F CPUs. The nERROR signal should only be set by the CCM-R4 module by a valid core mismatch. At power-on, some uninitialized circuits may cause the CCMR4-F to falsely detect a mis-compare.

Workaround(s): The anomalous nERROR toggle would need to be ignored by the external monitoring circuit (if deployed).

MSS#44 ***SYNC IN input pulse wider than 4usec can cause a FRC lockstep error***

Revision(s) Affected: AWR1243 ES1.0, AWR1243 ES2.0, and AWR1243 ES3.0

Description: In hardware based frame triggered mode of operation, external SYNC IN pulse is provided to the radar device. If the width of the pulse if > 4usec, it could cause MSS ESM group 1 fault with FRC lockstep error.

Workaround(s): The pulse width of the external SYNC IN signal should be >25nsec and < 5usec

ANA#01 *Noise Figure Degradation*

Revision(s) Affected: AWR1243 ES1.0

Description: Due to board limitation current typical Noise figure number is 18dB.

Workaround(s): None.

ANA#02 *VCO#1 [76-77GHz] Minimum Frequency Falls Short of Target*

Revision(s) Affected: AWR1243 ES1.0

Description: The supported frequency range is 77 GHz to 81 GHz (using VCO2).

Workaround(s): None.

ANA#03 *Spurs from LVDS Output Coupling into Synthesizer*

Revision(s) Affected: AWR1243 ES1.0

Description: For the characterization, the LVDS interface is used. In this mode, there is a package coupling to crystal oscillator pins causing spurs in LO (hence it comes out in IF spectrum).

Workaround(s): None.

ANA#04 ***Receiver Gain Range Availability***

Revision(s) Affected: AWR1243 ES1.0

Description: The supported receiver gain range is 18dB (versus a specification target of 24dB).

Workaround(s): None.

ANA#06 ***Return Loss Measurement on TX: S11 < –9dB, RX S11 < –6.5dB (Accepted Value of < –10dB)***

Revision(s) Affected: AWR1243 ES1.0 and AWR1243 ES2.0

Description: The return loss measurement on TX S11 is < –9dB and the return loss measurement on RX S11 is < –6.5dB. The accepted value is < –10dB.

Workaround(s): None.

ANA#07 ***CSI2 Activity Coupling to Clock***

Revision(s) Affected: AWR1243 ES1.0 and AWR1243 ES2.0

Description: The activity on the CSI lines during the state transitions at the start and at the end of CSI transfer couples into the clock leading to glitches in the TX output.

Workaround(s): Increase the idle time between chirps such that the "start of transfer" and "end of transfer" occur during the idle time between two chirps.

1. The AWR1243 sends data from ADCBuffer to High Speed Peripheral. At the start of each chirp, CSI-2 changes from Low Power Mode to Standard Mode output. At the completion of the chirp, CSI-2 goes back from Standard mode to Low Power Mode output. When CSI-2 changes mode, there is a clock contamination of the ADC subsystem. In order to not contaminate the measurement, the CSI-2 data Output must be finished before the end of the idle time chirp parameter.

   Bitrate_perChirp_perLane = (numRxch * DFEoutrate * (numDFEsamples/chirp) * (complexmode+1) *(numbits/sample[12,14,16]) / (numLanes)

   perChirp_Outperiod = Bitrate_perChirp_perLane / (DDC_Clkrate * 2)

   IdleTime = MAX(Synthesizer_IdleTime, perChirp_Outperiod)

   Note: Synthesizer_IdleTime can be calculated in the mmWave Sensing Estimator.
2. If the customer uses the LVDS High Speed output format, this ADC clock disturbance is not seen.

ANA#08A *Doppler Spur Observed at Certain RF Frequencies*

Revision(s) Affected: AWR1243 ES1.0, AWR1243 ES2.0, and AWR1243 ES3.0

Description: When the instantaneous FMCW Ramp frequency nears certain specific RF frequencies, there can be coupling between the synthesizer's reference and its output, and manifest as frequency glitches or spurs in TX output spectrum.

Implication: In FMCW radar 2D signal processing, this can lead to spurs in a fixed Doppler bin at all range bins. This situation can occur with narrow band chirps, if the FMCW ramp includes or nears 76.8-, 77.4-, 78-, 79.2-, 80.4-, 81-GHz RF frequencies. The affected Doppler bin is a function of chirp timing and RF frequency properties.

Workaround(s): Use the device's dithering features to vary idle time, RF frequency and ramp end times to spread the spurs significantly in Doppler dimension so that it does not get detected as spurious targets. Using larger chirp band widths also reduces the spur level.

ANA#09A *Synthesizer Frequency Nonlinearity around 76.8 GHz when Synthesizer (Chirp) Frequency Monitor Enabled*

Revision(s) Affected: AWR1243 ES1.0, AWR1243 ES2.0, and AWR1243 ES3.0

Description: When the synthesizer (chirp) frequency monitor is enabled and the synthesizer chirp is around 76.8 GHz, the frequency error can be as high as 500 kHz due to coupling between the monitor and the synthesizer. The RF frequencies impacted are 500Mhz around 76.8Ghz (76.8 ± 0.5 GHz).

Implication: Increased nonlinearity in the chirp can lead to up to 20 dB degradation in the noise floor surrounding large objects. This leads to potential loss of dynamic range when large and small objects are present simultaneously.

Workaround(s):

1. Disable the synthesizer frequency monitor during profiles where the LO crosses 76.8 ± 0.5 GHz.
2. Use non-functional chirps to detect nonlinearities (instead of high instantaneous frequency errors) in the synthesizer by inserting dummy chirps (where RX data is not used) after functional chirps (where RX data is consumed).

ANA#10A *Unreliable Readings from Synthesizer Supply Voltage Monitor*

Revision(s) Affected: AWR1243 ES1.0, AWR1243 ES2.0, and AWR1243 ES3.0

Description: During monitoring, the thresholds used to determine if the synthesizer supply voltage is within limits are much stricter than necessary for proper circuit operation. This can lead to occasional, erroneous reporting of supply failures even when there is no adverse impact on circuit or system behavior.

Implication: The user cannot rely on supply failure indication from the supply monitors of PM, Clock and LO subsystems. The affected field is STATUS_SUPPLY_PMCLKLO in the monitoring report message: AWR_MONITOR_PMCLKLO_INTERNAL_ANALOG_SIGNALS_REPORT_AE_SB.

Workaround(s): Ignore the field STATUS_SUPPLY_PMCLKLO in the monitoring report message: AWR_MONITOR_PMCLKLO_INTERNAL_ANALOG_SIGNALS_REPORT_AE_SB.

ANA#11A *TX, RX Calibrations Sensitive to Large External Interference*

Revision(s) Affected: AWR1243 ES1.0, AWR1243 ES2.0, and AWR1243 ES3.0

Description: External interference present on the RX or TX pins, during the period of the device calibration at RfInit, can lead to degraded accuracy or errors in the calibration results. If the interference changes its level while these calibrations are actively running, the calibration algorithm may interpret this as a change in signal power, leading to incorrect convergence. This applies to boot-time PD, Rx IQ mismatch calibration, Rx gain calibration, Tx power calibration, and phase-shifter calibration. It also impacts run-time Tx output power calibration in CLPC mode.

Workaround(s): **Workaround #1:**

The incident power detector in the TX output power detector, along with the absolute level of the PA loopback used during the PA loopback monitors, are insensitive to this, and they can be used to check that the calibrations converged correctly. Calibration can be re-run if large interference was observed.

Workaround #2:

Another workaround is to save the boot time calibrations at production (done in a clean environment without interference) and during operation, the calibrations can be restored. For the runtime Tx output power calibrations, OLPC mode can be used instead of the CLPC mode.

ANA#12A *Second Harmonic (HD2) Present in the Receiver*

Revision(s) Affected: AWR1243 ES1.0, AWR1243 ES2.0, and AWR1243 ES3.0

Description: There is a finite isolation between the RF pins/package and the FMCW synthesizer. This can create spurious tones at the synthesizer output and lead to appearance of 2nd order harmonics and inter-modulations of expected IF frequencies at RX ADC output. The amplitude of the 2nd harmonic could as high as -55 dBc , referenced to the power level of the intended tone at the LNA input.

Workaround(s): No workaround available at this time. However, in many typical radar usecases the HD2 does not affect the system performance due to two reasons:

1. Since the HD2 comes from a coupling to the LO signal, there is an inherent suppression of the HD2 level due to the self-mixing effect (that is, phase noise and phase spur suppression effect at the mixer).
2. In real-life scenarios there is often a double-bounce effect of the radar signal reflected from the target, which leads to a ghost object at twice the distance of the actual object. This effect is often indistinguishable from the effect of HD2 itself.

ANA#13 *TX1 to TX3 Phase Mismatch Variation over Temperature is Double that of TX2/TX1 and TX3/TX2 Combinations*

Revision(s) Affected: AWR1243 ES1.0, AWR1243 ES2.0, and AWR1243 ES3.0

Description: TX3/TX1 combination exhibits a phase mismatch variation of ±6° from –40°C to 140°C whereas, TX2/TX1 and TX3/TX2 combinations exhibit a lower variation of ±3°C over the same temperature range.

Workaround(s): In applications requiring high phase accuracy across TX channels, a background angle calibration or a 2-point calibration can be used to control phase variation over temperature.

ANA#15 *Excessive TX-RX Coupling or Reflection can Lead to Saturated RX Output*

Revision(s) Affected: AWR1243 ES1.0, AWR1243 ES2.0, and AWR1243 ES3.0

Description: If there is excessing TX-RX coupling or chassis reflection, it can lead to a saturated RX output. This situation can occur if the RX input is stronger than -10dBm.

Workaround(s): Improve TX-to-RX antenna isolation on PCB. Radome/chassis should give low reflection amplitude and should be as close as possible to the sensor, to reduce the IF frequency.

ANA#17A — *On-Board Supply Ringing Induced Spur*

Revision(s) Affected: AWR1243 ES1.0, AWR1243 ES2.0, and AWR1243 ES3.0

Description: Turning OFF and ON front-end modules can cause on-board supply ringing and slow the settling of the power supply. This supply ringing can manifest as a spur (~130KHz) in the FMCW synthesizer output spectrum.

Workaround(s): **Workaround #1:**

Disable inter-chirp duty cycling of the RX.

or

Workaround #2:

Design the power supply to damp out the ringing on the rails to the device.

ANA#18B ***Spurs Caused due to Digital Activity Coupling to XTAL***

Revision(s) Affected: AWR1243 ES1.0, AWR1243 ES2.0, and AWR1243 ES3.0

Description: Digital filtering activity can potentially couple to XTAL pins and lead to spurs in the LO, which would also be seen in the Rx data. The spur in the Rx data would be seen at the spur frequency offset around a strong object. For example if the spur frequency is 500Khz and there is a strong object at 2Mhz , the Rx ADC spectrum could have a spike at 1.5Mhz or 2.5Mhz. Note that the Tx – Rx antenna coupling would also form a strong object close to DC. The spur frequency depends on the sampling rate (Fs). The strongest of these spurs have been observed when Fs is close to 10, 12.5, 18, 18.75,20, 25, Msps. In these ranges, an IF spur can appear at Fs-10 Mhz, 2Fs-40MHz, 4Fs-40 MHz, 4Fs-100 MHz, 8Fs-100 MHz , 2Fs-37.5 MHz, 2Fs-36 MHz. The spur is observable when the spur frequency falls within 1.5 MHz, beyond that it gets heavily filtered out. Please refer the device datasheet for max usable sampling rate.

Workaround(s): **Workaround #1:**

Avoid sampling rates close to these numbers (10, 12.5, 18, 18.75, 20, 25 Msps) or use exactly these numbers (spur is at 0 Hz in the latter case).

Workaround #2:

Using external TCXO, instead of XTAL, with voltage swing between 1.4-1.8 Vpp can avoid these spurs.

ANA#20 — *Occasional Failures Observed During Calibration of the Radar Subsystem*

Revision(s) Affected: AWR1243 ES1.0, AWR1243 ES2.0, and AWR1243 ES3.0

Description: Rare occurrences of failures have been observed in the Dual-Clock Comparator (DCC) module, as a result the APLL or Synthesizer may report a failure.

Workaround(s): **Workaround #1:**

Any APLL calibration failure needs to be responded with a reset cycle.

or

Workaround #2:

Any SYNTH calibration failure reported by the BSS will require an RFinit.

ANA#21A — *Out of Band Radiated Spectral Emission*

Revision(s) Affected: AWR1243 ES1.0, AWR1243 ES2.0, and AWR1243 ES3.0

Description: Out-of-band radiated spectral emissions are observed at 14.4-GHz and 28.8-GHz.

Workaround(s): A grounded metallic shield around the device (excluding the antenna region) can be used to reduce the emission levels. Microwave absorber materials could also be placed on the device to reduce the emissions.

ANA#22A — *Overshoot and Undershoot During Inter-Chirp Idle Time*

Revision(s) Affected: AWR1243 ES1.0, AWR1243 ES2.0, and AWR1243 ES3.0

Description: At the end of the chirp , when the synthesizer starts to go back to the start frequency of the next chirp, there is some overshoot and undershoot. The undershoot/overshoot is proportional to the chirp bandwidth. Negative slope chirps have a worse undershoot than positive slope chirps.

Workaround(s): To ensure the TX power amplifier is OFF during chirp idle time and not causing "on-air" emissions during the undershoot/overshoot period, keep the inter-chirp power savings ON.

ANA#23 — *MIPI CSI2 HS Data TX Differential Voltage Mismatch (Pulse) Marginality*

Revision(s) Affected: AWR1243 ES1.0, AWR1243 ES2.0, and AWR1243 ES3.0

Description: Some devices could fail the MIPI CSI2 HS TX Differential Voltage Mismatch spec [$\Delta VOD = VOD1 - |VOD0|$] by a few mV on the CSI data lanes at higher temperatures. The MIPI spec for this parameter is 14 mV.

Workaround(s): None. This failure should typically not impact the data integrity/reception.

ANA#24A — *40-MHz OSC CLKOUT Causing Spurs in 2D-FFT Spectrum*

Revision(s) Affected: AWR1243 ES1.0, AWR1243 ES2.0, and AWR1243 ES3.0

Description: Harmonics of 40 MHz from osc-clkout can be coupled onto the synthesizer and can cause low amplitude spurs in the 2D-FFT spectrum. These spurs are at fixed doppler bin, across all range bins.

Workaround(s): For single chip usecases, where OSC CLKOUT is not used , OSC CLKOUT output can be disabled.

ANA#27 — *Digital Temperature Sensor Having Higher Error*

Revision(s) Affected: AWR1243 ES1.0, AWR1243 ES2.0, and AWR1243 ES3.0

Description: Due to the single-ended nature of the digital temperature sensors, as compared to the differential design of analog temperature sensors (that is, TX, RX, and PM), it is vulnerable to noise and can have higher error than the analog temperature sensors.

Workaround(s): Use only the analog temperature sensor values (TX and RX) in the algorithm. The digital temperature sensor value can be ignored.

6 Trademarks

All trademarks are the property of their respective owners.

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from October 3, 2019 to December 31, 2020 (from Revision C (October 2019) to Revision D (December 2020)) **Page**

- ***(Advisory to Silicon Variant / Revision Map):*** Added MSS#44 advisory under Master Subsystem, all silicon revisions.......... 4
- ***(Advisory to Silicon Variant / Revision Map):*** Added ANA#15, ANA#17A, ANA#18B, ANA#20 through ANA#23, ANA24A, ANA27 advisories under Analog / Millimeter Wave, all silicon revisions.......... 4
- ***(Advisory to Silicon Variant / Revision Map):*** Updated/modified ANA#08A, ANA#09A, ANA#10A, ANA#11A and ANA#12A advisories under Analog / Millimeter Wave, all silicon revisions.......... 4