ON Semiconductor

Is Now

To learn more about onsemi™, please visit our website at
www.onsemi.com

AND9672/D

Hot-Plug Insertion Startup Time Delay for eFuse

ON Semiconductor®

www.onsemi.com

APPLICATION NOTE

Introduction

The eFuse protection devices are used for limiting the system load current in the event of an overload or a short circuit. Many applications employ ON Semiconductor eFuses at the power input stage of the system between the main power input connector and DC−DC converters or power regulators. Such applications often tend to experience a voltage spikes and transients during a hot-plug events, especially when the long cables are used at the power input.

Although ON Semiconductor eFuses are extremely immune to voltage transients and eFuses with the Overvoltage clamp feature provide a fast response when limiting the output voltage during transients, sometimes various applications require a time delay between the hot-plug input voltage application and enabling of the eFuse in order for the input voltage to be stabilized before turning on the eFuse. This application note shows a convenient and easy way to implement such a startup time delay with most of the ON Semiconductor eFuses.

Schematics and Simulation

Many ON Semiconductor eFuses provide a Tristate Enable pin which is internally pulled to 3 V when the eFuse is powered on, internally pulled to 1.4 V when the eFuse is in the thermal shutdown mode or can be externally pulled to ground to disable or restart the eFuse operation. Typical application involves connection of a small NFET to the Enable pin for pulling it to ground.

The schematics in Figure 1 shows how a startup time delay can be implemented with an addition of just one more NFET and couple passive components. The L1 inductor represents parasitic inductance of a long cable. The E1 voltage dependent voltage source represents simplified operation of an eFuse enable pin; when 12 V input voltage is applied to VCC pin the enable pin is pulled to 3 V.

When M1 is off, M2 is on because its gate is tied to the input voltage through R2 resistor. When M2 is on, the eFuse is kept in the disabled state because the Enable Pin is pulled to ground. The R4 resistor and C2 capacitor represent an RC delay network which turns on M1 only after some time starting from VCC input voltage application; that time can be tuned with the value of R4. When M1 is turned on it turns off M2 by pulling its gate to ground and leaving the Enable pin floating. Once Enable pin is floating, the eFuse can turn on and internally pull this pin to 3 V.

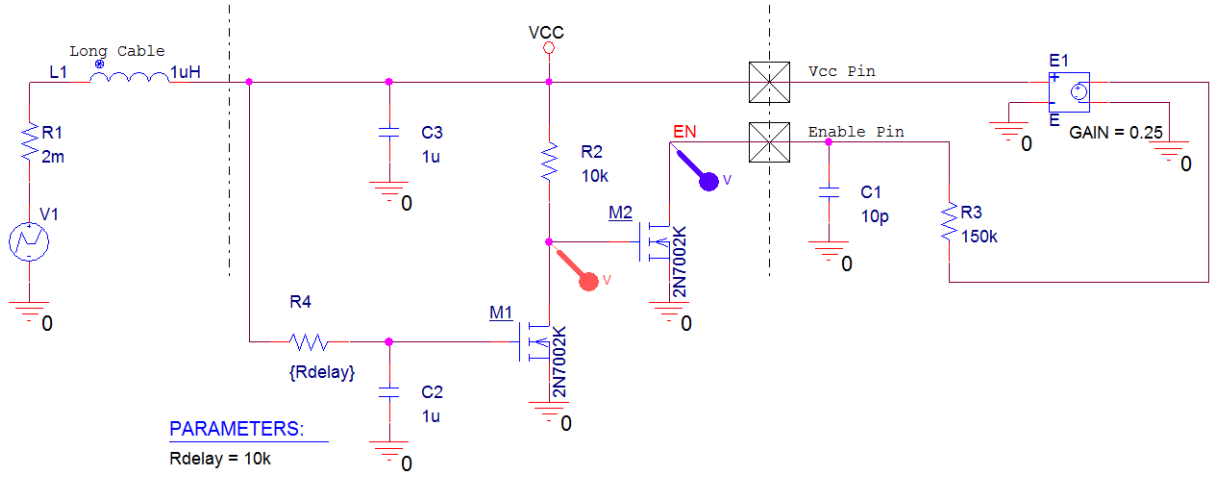

Figure 1. Circuit Implementation for Hot-Plug Insertion Time Delay

Figure 2 shows the parametric transient simulation plot with 1 μs input voltage rise time and a voltage spike due to the simulated cable parasitic inductance and input capacitance. The figure also shows the Enable Pin voltage pulling to 3 V only after startup delay time which is determined by the “Rdelay” resistance parameter of R4.

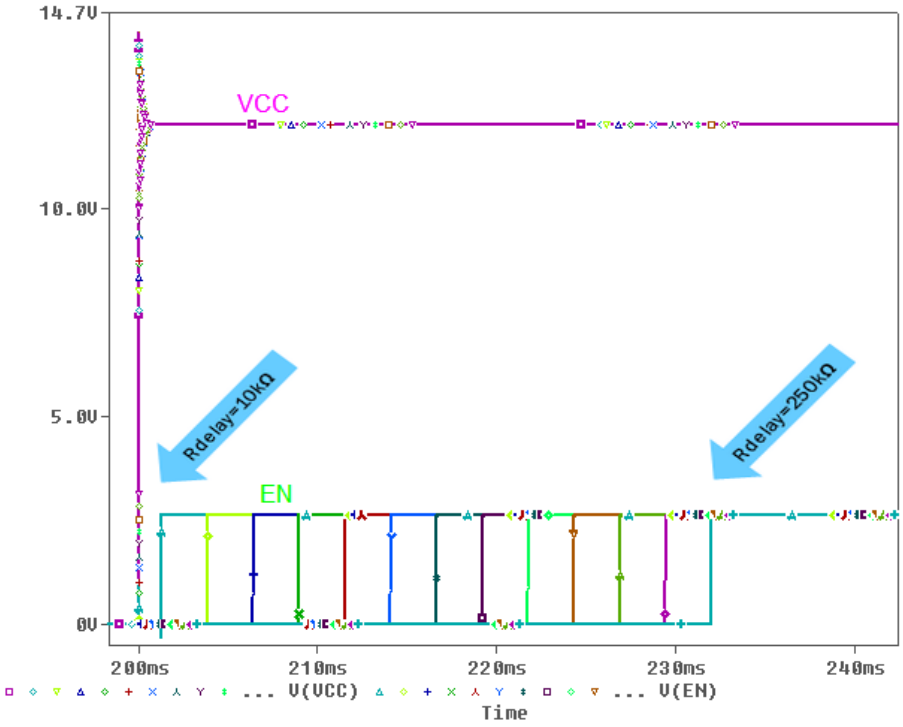

Figure 2. Transient Simulation of eFuse Startup Delay

Due to the implemented startup delay the eFuse is turned on only after the initial transient and spike condition on the VCC input rail is gone and the VCC voltage is stabilized.

Measurement and Operation

The circuit proposed in Figure 1 was constructed with one of the 12 V series ON Semiconductor eFuses. The power was instantly applied to the PCB with the eFuse through a long cable. The Figure 3 shows measured results with 10 kΩ R4 resistor. The time delay in this case was around 2 ms and the eFuse was turned on after the initial voltage spike.

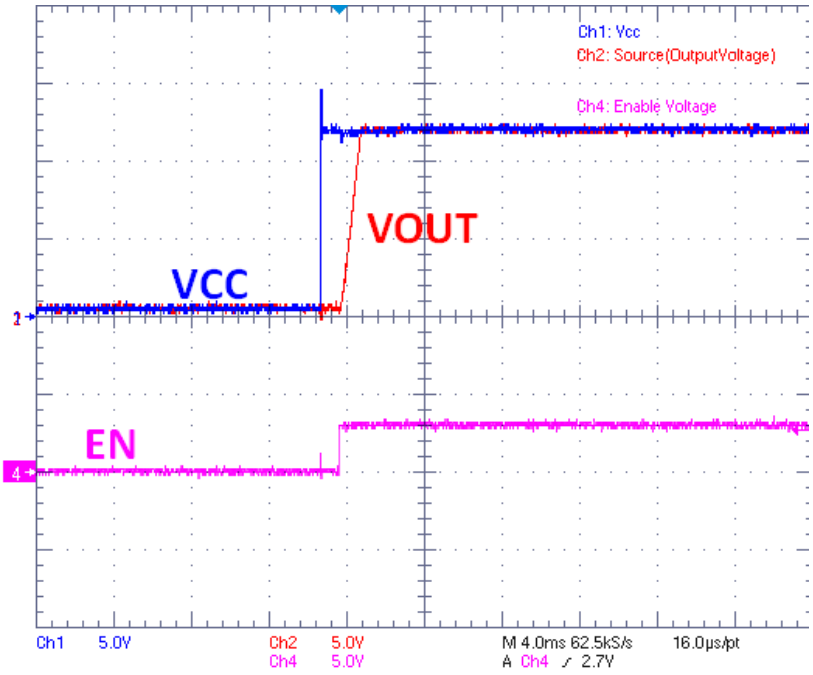

Figure 3. Insertion Startup Time Delay Measurement, R4 = 10 kΩ

The Figure 4 shows a measurement with 270 kΩ R4 resistor. In this case a longer delay of around 25 ms is inserted between the input voltage hot-plug application and enabling of the eFuse.

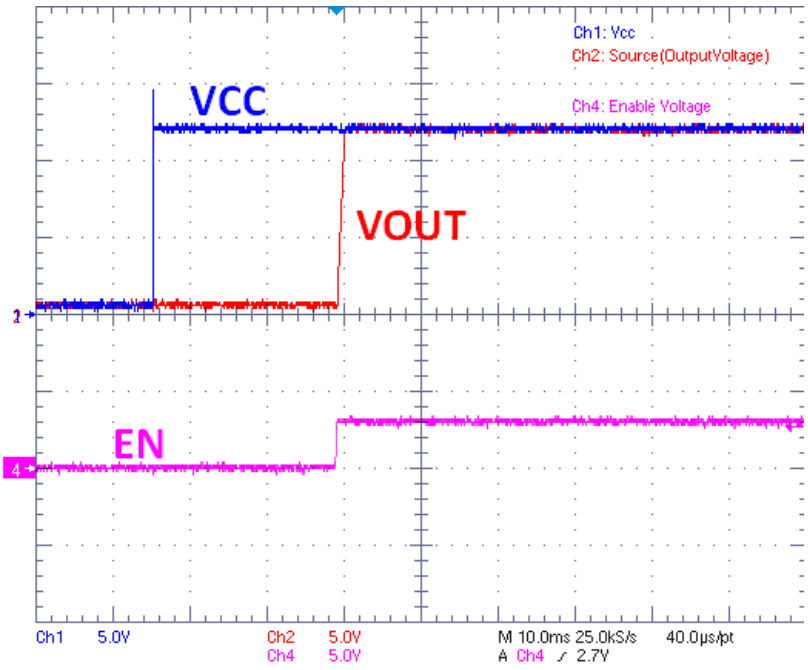

Figure 4. Insertion Startup Time Delay Measurement, R4 = 270 kΩ

Hot-Plug Insertion Startup Time Delay can be easily implemented with just a couple of passive and active components. For a more compact PCB layout, one can use a dual NFET in SOT−363 package. This way the PCB space required is almost the same as the space required by any other typical application circuit for an eFuse with similar Tristate Enable Pin functionality. Care should be taken to select FETs with maximum V_{GS} and V_{DS} ratings exceeding the potential overvoltage on the input; using the Zener diode to protect the gate of the FET may be considered as well.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5817−1050

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative