KSZ8999

Integrated 9-Port 10/100 Switch with PHY and Frame Buffer

Features

- Nine port (8+1) 10/100 Integrated Switch with Eight Physical Layer Transceivers and One MII/ SNI Interface
- Advanced Ethernet Switch with Internal Frame Buffer
  - 128K Byte of SRAM on Chip for Frame Buffering
  - 2.0 Gbps High Performance Memory Bandwidth
  - Wire Speed Reception and Transmission
  - Integrated Address Lookup Engine, Supports 1K Absolute MAC Addresses
  - Automatic Addressing Learning, Address Aging, and Address Migration
- Advanced Switch Features
  - Supports 802.1p Priority and Port-Based Priority
  - Supports Port-Based VLAN
  - Supports 1536 byte Frame for VLAN Tag
  - Supports DiffServ Priority, 802.1p Based Priority or Port-Based Priority or Broadcast Storm Protection
- Proven Transceiver Technology for UTP and Fiber Operation
  - 10BASE-T, 100BASE-TX, and 100BASE-FX Modes of Operation
  - Supports for UTP or Fiber on All Eight Ports
  - Indicators for Link, Activity, Full-/Half-Duplex, and Speed
  - Hardware-Based 10/100, Full/Half, Flow Control and Auto-Negotiation
  - Individual Port Forced Modes (Full-Duplex, 100BASE-TX) when Auto-Negotiation is Disabled
  - Full-Duplex IEEE 802.3x Flow Control
  - Half-Duplex Back Pressure Flow Control
- Supports MDI/MDI-X Auto Crossover
- External MAC Interface (MII or 7-Wire) for Router Applications
- Unmanaged Operation via Strapping or EEPROM at System Reset Time (see Reset Reference Circuit Section)
- Comprehensive LED Support
- Single 2.0V (min.), 2.1V (typ.) Power Supply with Options for 2.5V and 3.3V I/O
- 900 mA (1.80W) Including Physical Transmit Drivers
- Supports Commercial and Industrial Temperature Ranges
  - Commercial Temperature Range: 0°C to +70°C (KSZ8999)
  - Industrial Temperature Range: –40°C to +85°C (KSZ8999I)
- Available in a 208-Lead PQFP Package

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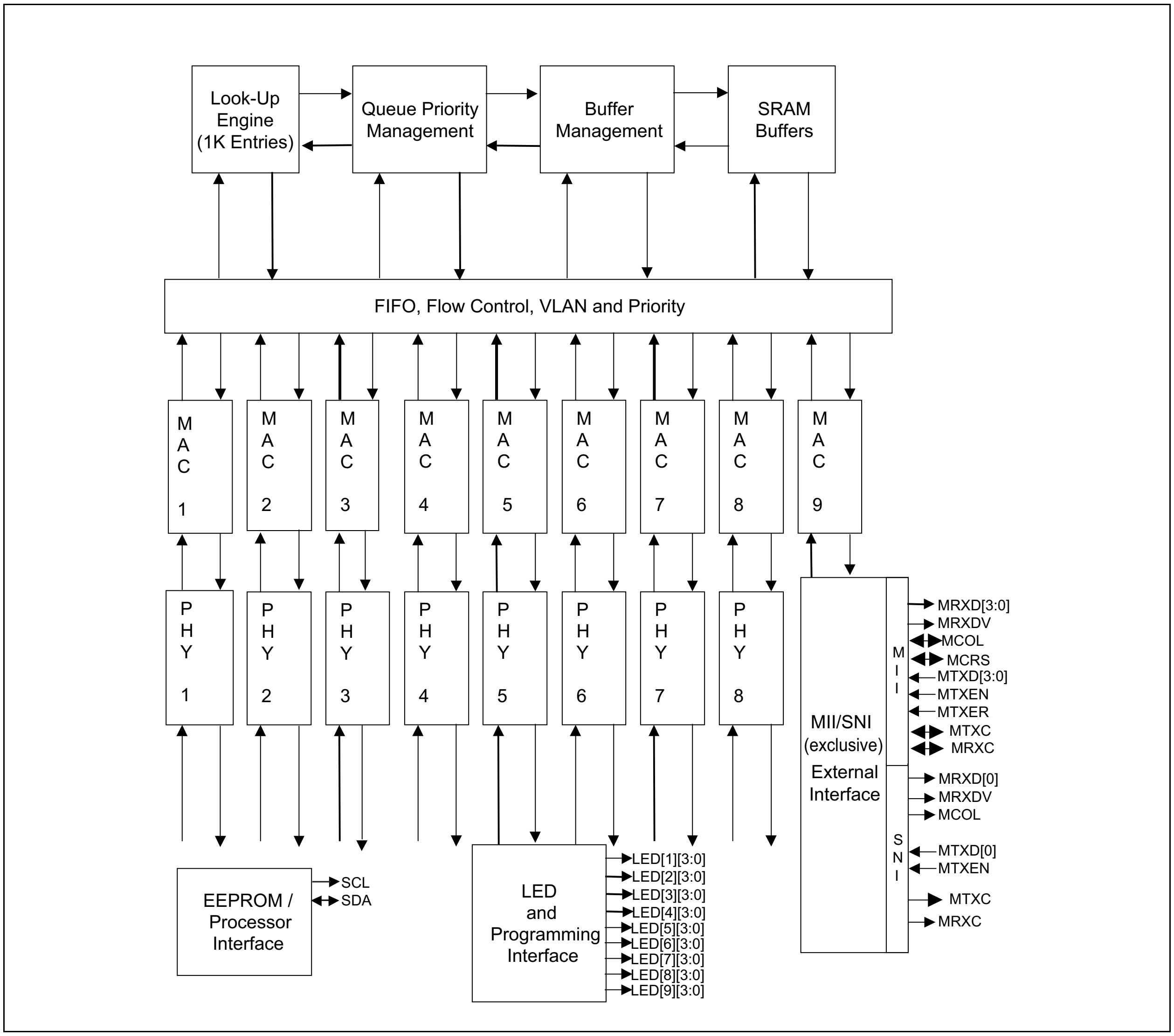
1.0 INTRODUCTION

1.1 General Description

The KSZ8999 contains eight 10/100 physical layer transceivers, nine Media Access Control (MAC) units with an integrated layer 2 switch. The device runs in two modes. The first mode is an eight-port integrated switch and the second is as a nine-port switch with the ninth port available through a Media Independent Interface (MII). Useful configurations include a stand alone eight-port switch as well as an eight-port switch with a routing element connected to the extra MII port. The additional port is also useful for a public network interfacing. The KSZ8999 is designed to reside in an unmanaged design that does not require processor intervention.

This is achieved through I/O strapping or EEPROM programming at system reset time. On the media side, the KSZ8999 supports 10BASE-T, 100BASE-TX, and 100BASE-FX, as specified by the IEEE 802.3 committee. Physical signal transmission and reception are enhanced through the use of analog circuitry that makes the design more efficient and allows for lower power consumption and smaller chip die size.

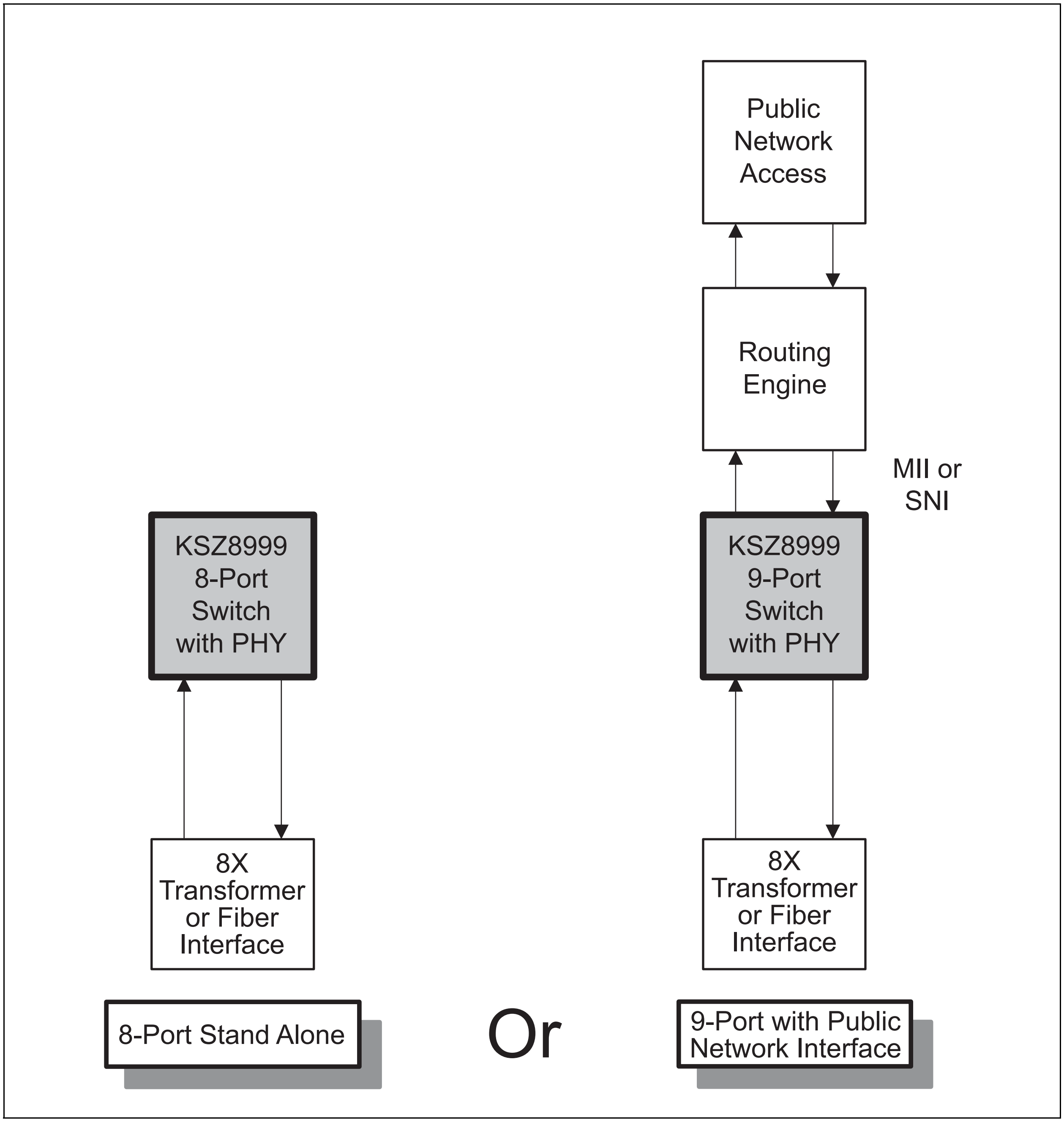
FIGURE 1-1: SYSTEM BLOCK DIAGRAM



1.2 System Level Applications

The KSZ8999 can be configured to fit either in an eight-port 10/100 application or as a nine-port 10/100 network interface with an extra MII/7-wire port. This MII/7-wire port can be connected to an external processor and used for routing purposes or public network access. The major benefits of using the KSZ8999 are the lower power consumption, unmanaged operation, flexible configuration, built-in frame buffering, VLAN abilities, and traffic priority control. Two such applications are depicted below.

FIGURE 1-2: SYSTEM APPLICATIONS



2.0 PIN DESCRIPTION AND CONFIGURATION

FIGURE 2-1: PIN CONFIGURATION FOR KSZ8999

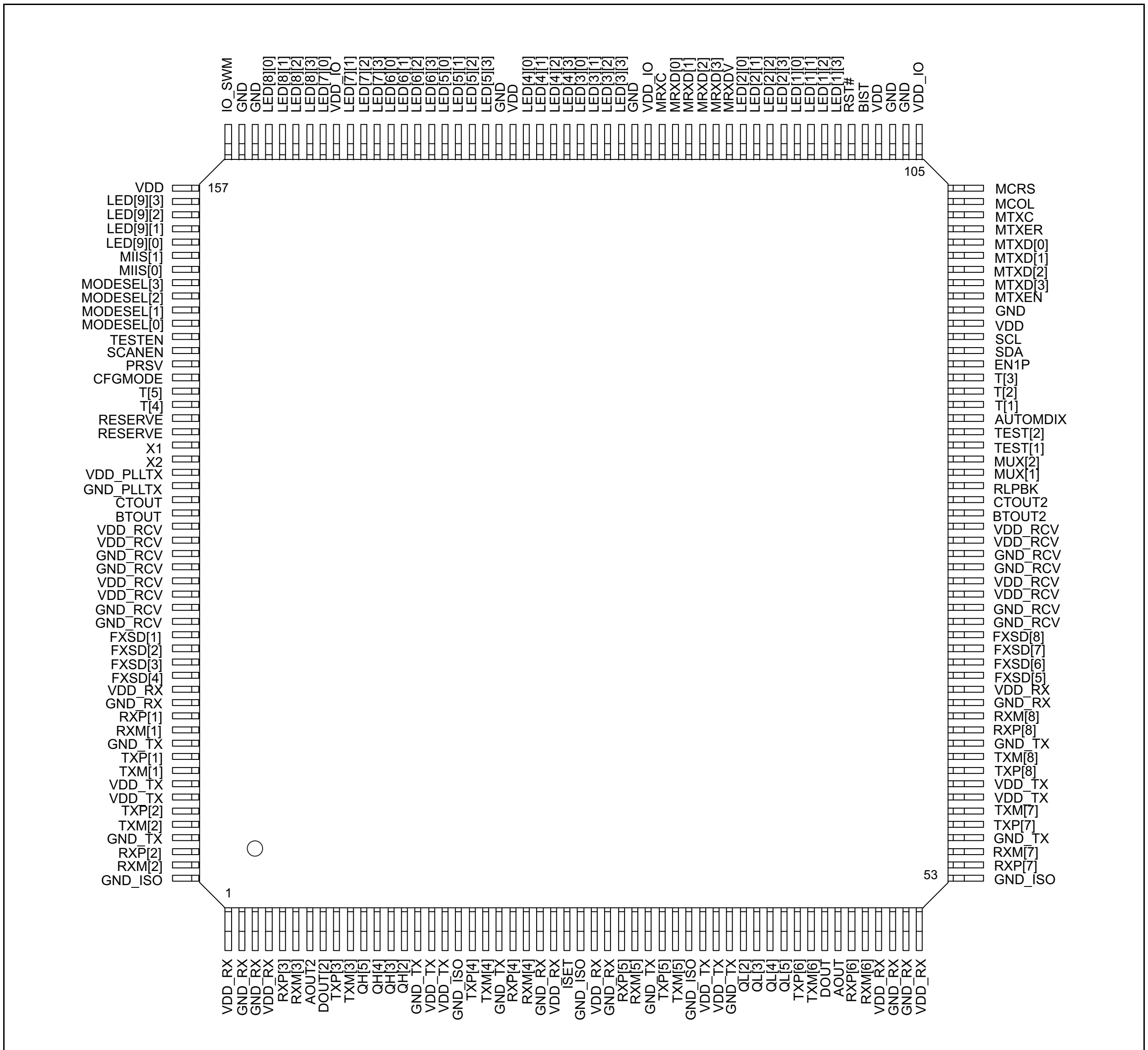


TABLE 2-1: PIN DESCRIPTION

Pin Number	Pin Name	Type (Note 2-1)	Port	Pin Function
1	VDD_RX	P	—	2.0V (min.), 2.1V (typ.) for equalizer
2	GND_RX	GND	—	Ground for equalizer
3	GND_RX	GND	—	Ground for equalizer
4	VDD_RX	P	—	2.0V (min.), 2.1V (typ.) for equalizer
5	RXP[3]	I	3	Physical receive signal + (differential)
6	RXM[3]	I	3	Physical receive signal – (differential)
7	AOUT2	O	—	Factory test output, no connection.
8	DOUT2	O	—	Factory test output, no connection.
9	TXP[3]	O	3	Physical transmit signal + (differential)
10	TXM[3]	O	3	Physical transmit signal – (differential)
11	QH[5]	OPD	—	Factory test pin. Leave open for normal operation
12	QH[4]	OPD	—	Factory test pin. Leave open for normal operation
13	QH[3]	OPD	—	Factory test pin. Leave open for normal operation
14	QH[2]	OPD	—	Factory test pin. Leave open for normal operation
15	GND_TX	GND	—	Ground for transmit circuitry
16	VDD_TX	P	—	2.0V (min.), 2.1V (typ.) for transmit circuitry
17	VDD_TX	P	—	2.0V (min.), 2.1V (typ.) for transmit circuitry
18	GND-ISO	GND	—	Analog ground
19	TXP[4]	O	4	Physical transmit signal + (differential)
20	TXM[4]	O	4	Physical transmit signal – (differential)
21	GND_TX	GND	—	Ground for transmit circuitry
22	RXP[4]	I	4	Physical receive signal + (differential)
23	RXM[4]	I	4	Physical receive signal – (differential)
24	GND_RX	GND	—	Ground for equalizer
25	VDD_RX	P	—	2.0V (min.), 2.1V (typ.) for equalizer
26	ISET	—	—	Set physical transmit output current. Pull down with a 3.01 kΩ resistor.
27	GND-ISO	GND	—	Analog ground
28	VDD_RX	P	—	2.0V (min.), 2.1V (typ.) for equalizer
29	GND_RX	GND	—	Ground for equalizer
30	RXP[5]	I	5	Physical receive signal + (differential)
31	RXM[5]	I	5	Physical receive signal – (differential)
32	GND_TX	GND	—	Ground for transmit circuitry
33	TXP[5]	O	5	Physical transmit signal + (differential)
34	TXM[5]	O	5	Physical transmit signal – (differential)
35	GND-ISO	GND	—	Analog ground
36	VDD_TX	P	—	2.0V (min.), 2.1V (typ.) for transmit circuitry
37	VDD_TX	P	—	2.0V (min.), 2.1V (typ.) for transmit circuitry
38	GND_TX	GND	—	Ground for transmit circuitry
39	QL[2]	OPD	—	Factory test pin. Leave open for normal operation
40	QL[3]	OPD	—	Factory test pin. Leave open for normal operation
41	QL[4]	OPD	—	Factory test pin. Leave open for normal operation
42	QL[5]	OPD	—	Factory test pin. Leave open for normal operation
43	TXP[6]	O	—	Physical transmit signal + (differential)

TABLE 2-1: PIN DESCRIPTION (CONTINUED)

Pin Number	Pin Name	Type (Note 2-1)	Port	Pin Function
44	TXM[6]	O	—	Physical transmit signal – (differential)
45	DOUT	O	—	Factory test pin. Leave open for normal operation
46	AOUT	O	—	Factory test pin. Leave open for normal operation
47	RXP[6]	I	6	Physical receive signal + (differential)
48	RXM[6]	I	6	Physical receive signal – (differential)
49	VDD_RX	P	—	2.0V (min.), 2.1V (typ.) for equalizer
50	GND_RX	GND	—	Ground for equalizer
51	GND_RX	GND	—	Ground for equalizer
52	VDD_RX	P	—	2.0V (min.), 2.1V (typ.) for equalizer
53	GND-ISO	GND	—	Analog ground
54	RXP[7]	I	7	Physical receive signal + (differential)
55	RXM[7]	I	7	Physical receive signal – (differential)
56	GND_TX	GND	—	Ground for transmit circuitry
57	TXP[7]	O	7	Physical transmit signal + (differential)
58	TXM[7]	O	7	Physical transmit signal – (differential)
59	VDD_TX	P	—	2.0V (min.), 2.1V (typ.) for transmit circuitry
60	VDD_TX	P	—	2.0V (min.), 2.1V (typ.) for transmit circuitry
61	TXP[8]	O	8	Physical transmit signal + (differential)
62	TXM[8]	O	8	Physical transmit signal – (differential)
63	GND_TX	GND	—	Ground for transmit circuitry
64	RXP[8]	I	8	Physical receive signal + (differential)
65	RXM[8]	I	8	Physical receive signal – (differential)
66	GND_RX	GND	—	Ground for equalizer
67	VDD_RX	P	—	2.0V (min.), 2.1V (typ.) for equalizer
68	FXSD[5]	IPD	5	Fiber signal detect
69	FXSD[6]	IPD	6	Fiber signal detect
70	FXSD[7]	IPD	7	Fiber signal detect
71	FXSD[8]	IPD	8	Fiber signal detect
72	GND_RCV	GND	—	Ground for clock recovery circuit
73	GND_RCV	GND	—	Ground for clock recovery circuit
74	VDD_RCV	P	—	2.0V (min.), 2.1V (typ.) for clock recovery circuit
75	VDD_RCV	P	—	2.0V (min.), 2.1V (typ.) for clock recovery circuit
76	GND_RCV	GND	—	Ground for clock recovery circuit
77	GND_RCV	GND	—	Ground for clock recovery circuit
78	VDD_RCV	P	—	2.0V (min.), 2.1V (typ.) for clock recovery circuit
79	VDD_RCV	P	—	2.0V (min.), 2.1V (typ.) for clock recovery circuit
80	BTOUT2	O	—	Factory test pin. Leave open for normal operation
81	CTOUT2	O	—	Factory test pin. Leave open for normal operation
82	RLPBK	I	—	Enable loop back for testing. Pull down/float for normal operation
83	MUX[1]	I	—	Factory test pin. Float for normal operation
84	MUX[2]	I	—	Factory test pin. Float for normal operation
85	TEST[1]	I	—	Factory test pin. Float for normal operation
86	TEST[2]	I	—	Factory test pin. Float for normal operation

TABLE 2-1: PIN DESCRIPTION (CONTINUED)

Pin Number	Pin Name	Type (Note 2-1)	Port	Pin Function
87	AUTOMDIX	I	—	Auto MDI/MDIX enable and disable. Pull-up/float enable; pull-down disable
88	T[1]	IPU	—	Factory test pin. Float for normal operation
89	T[2]	IPD	—	Factory test pin. Float for normal operation
90	T[3]	IPD	—	Factory test pin. Float for normal operation
91	EN1P	IPD	—	Enable 802.1p for all ports
92	SDA	IPD/O	—	Serial data from EEPROM or processor
93	SCL	IPD/O	—	Clock for EEPROM or from processor
94	VDD	P	—	2.0V (min.), 2.1V (typ.) for core digital circuitry
95	GND	GND	—	Ground for digital circuitry
96	MTXEN	IPD	9	MII transmit enable
97	MTXD[3]	IPD	9	MII transmit bit 3
98	MTXD[2]	IPD	9	MII transmit bit 2
99	MTXD[1]	IPD	9	MII transmit bit 1
100	MTXD[0]	IPD	9	MII transmit bit 0
101	MTXER	IPD	9	MII transmit error
102	MTXC	IPD/O	9	MII transmit clock
103	MCOL	IPD/O	9	MII collision detected
104	MCRS	IPD/O	9	MII carrier sense
105	VDD-IO	P	—	2.1V, 2.5V or 3.3V for I/O circuitry
106	GND	GND	—	Ground for digital circuitry
107	GND	GND	—	Ground for digital circuitry
108	VDD	P	—	2.0V (min.), 2.1V (typ.) for core digital circuitry
109	BIST	IPD	—	Built-in self test. Tie low for normal operation
110	RST#	I	—	Reset. Active-low
111	LED[1][3]	IPU/O	1	LED indicator 3
112	LED[1][2]	IPU/O	1	LED indicator 2
113	LED[1][1]	IPU/O	1	LED indicator 1
114	LED[1][0]	IPU/O	1	LED indicator 0
115	LED[2][3]	IPU/O	2	LED indicator 3
116	LED[2][2]	IPU/O	2	LED indicator 2
117	LED[2][1]	IPU/O	2	LED indicator 1
118	LED[2][0]	IPU/O	2	LED indicator 0
119	MRXDV	OPD	9	MII receive data valid
120	MRXD[3]	OPU	9	MII receive bit 3
121	MRXD[2]	OPU	9	MII receive bit 2
122	MRXD[1]	OPU	9	MII receive bit 1
123	MRXD[0]	OPU	9	MII receive bit 0
124	MRXC	IPU/O	9	MII receive clock
125	VDD-IO	P	—	2.1V, 2.5V or 3.3V for I/O circuitry
126	GND	GND	—	Ground for digital circuitry
127	LED[3][3]	IPU/O	3	LED indicator 3
128	LED[3][2]	IPU/O	3	LED indicator 2
129	LED[3][1]	IPU/O	3	LED indicator 1

TABLE 2-1: PIN DESCRIPTION (CONTINUED)

Pin Number	Pin Name	Type (Note 2-1)	Port	Pin Function
130	LED[3][0]	IPU/O	3	LED indicator 0
131	LED[4][3]	IPU/O	4	LED indicator 3
132	LED[4][2]	IPU/O	4	LED indicator 2
133	LED[4][1]	IPU/O	4	LED indicator 1
134	LED[4][0]	IPU/O	4	LED indicator 0
135	VDD	P	—	2.0V (min.), 2.1V (typ.) for core digital circuitry
136	GND	GND	—	Ground for digital circuitry
137	LED[5][3]	IPU/O	5	LED indicator 3
138	LED[5][2]	IPU/O	5	LED indicator 2
139	LED[5][1]	IPU/O	5	LED indicator 1
140	LED[5][0]	IPU/O	5	LED indicator 0
141	LED[6][3]	IPU/O	6	LED indicator 3
142	LED[6][2]	IPU/O	6	LED indicator 2
143	LED[6][1]	IPU/O	6	LED indicator 1
144	LED[6][0]	IPU/O	6	LED indicator 0
145	LED[7][3]	IPU/O	7	LED indicator 3
146	LED[7][2]	IPU/O	7	LED indicator 2
147	LED[7][1]	IPU/O	7	LED indicator 1
148	VDD-IO	P	—	2.1V, 2.5V or 3.3V for I/O circuitry
149	LED[7][0]	IPU/O	7	LED indicator 0
150	LED[8][3]	IPU/O	8	LED indicator 3
151	LED[8][2]	IPU/O	8	LED indicator 2
152	LED[8][1]	IPU/O	8	LED indicator 1
153	LED[8][0]	IPU/O	8	LED indicator 0
154	GND	GND	—	Ground for digital circuitry
155	GND	GND	—	Ground for digital circuitry
156	IO_SWM	IPU	—	Factory test pin. Tie high for normal operation
157	VDD	P	—	2.0V (min.), 2.1V (typ.) for core digital circuitry
158	LED[9][3]	IPU/O	9	LED indicator 3
159	LED[9][2]	IPU/O	9	LED indicator 2
160	LED[9][1]	IPU/O	9	LED indicator 1
161	LED[9][0]	IPU/O	9	LED indicator 0
162	MIIS[1]	IPD	9	MII mode select bit 1
163	MIIS[0]	IPD	9	MII mode select bit 0
164	MODESEL[3]	IPD	—	Selects LED and test modes
165	MODESEL[2]	IPD	—	Selects LED and test modes
166	MODESEL[1]	IPD	—	Selects LED and test modes
167	MODESEL[0]	IPD	—	Selects LED and test modes
168	TESTEN	IPD	—	Factory test pin. Tie low for normal operation
169	SCANEN	IPD	—	Factory test pin. Tie low for normal operation
170	PRSV	IPD	—	Reserve 6 KB buffer for priority frames
171	CFGMODE	IPU	—	Configures programming interface for EEPROM or processor
172	T[5]	I	—	Factory test pin. Float for normal operation
173	T[4]	IPD	—	F/D = normal operation (default) U = disable FEF

TABLE 2-1: PIN DESCRIPTION (CONTINUED)

Pin Number	Pin Name	Type (Note 2-1)	Port	Pin Function
174	Reserved	I	—	Reserved. Float for normal operation
175	Reserved	I	—	Reserved. Float for normal operation
176	X1	I	—	Crystal or clock input
177	X2	O	—	Connect to crystal
178	VDD_PLLTX	P	—	2.0V (min.), 2.1V (typ.) for phase locked loop circuit
179	GND_PLLTX	GND	—	Ground for phase locked loop circuit
180	CTOUT	O	—	Factory test pin. Leave open for normal operation
181	BTOUT	O	—	Factory test pin. Leave open for normal operation
182	VDD_RCV	P	—	2.0V (min.), 2.1V (typ.) for clock recovery circuit
183	VDD_RCV	P	—	2.0V (min.), 2.1V (typ.) for clock recovery circuit
184	GND_RCV	GND	—	Ground for clock recovery circuit
185	GND_RCV	GND	—	Ground for clock recovery circuit
186	VDD_RCV	P	—	2.0V (min.), 2.1V (typ.) for clock recovery circuit
187	VDD_RCV	P	—	2.0V (min.), 2.1V (typ.) for clock recovery circuit
188	GND_RCV	GND	—	Ground for clock recovery circuit
189	GND_RCV	GND	—	Ground for clock recovery circuit
190	FXSD[1]	IPD	1	Fiber signal detect
191	FXSD[2]	IPD	2	Fiber signal detect
192	FXSD[3]	IPD	3	Fiber signal detect
193	FXSD[4]	IPD	4	Fiber signal detect
194	VDD_RX	P	—	2.0V (min.), 2.1V (typ.) for equalizer
195	GND_RX	GND	—	Ground for equalizer
196	RXP[1]	I	1	Physical receive signal + (differential)
197	RXM[1]	I	1	Physical receive signal – (differential)
198	GND_TX	GND	—	Ground for transmit circuitry
199	TXP[1]	O	1	Physical transmit signal + (differential)
200	TXM[1]	O	1	Physical transmit signal – (differential)
201	VDD_TX	P	—	2.0V (min.), 2.1V (typ.) for transmit circuitry
202	VDD_TX	P	—	2.0V (min.), 2.1V (typ.) for transmit circuitry
203	TXP[2]	O	2	Physical transmit signal + (differential)
204	TXM[2]	O	2	Physical transmit signal – (differential)
205	GND_TX	GND	—	Ground for transmit circuitry
206	RXP[2]	I	2	Physical receive signal + (differential)
207	RXM[2]	I	2	Physical receive signal – (differential)
208	GND-ISO	GND	—	Analog ground

Note 2-1 P = power supply; GND = ground; I = input; O = output
I/O = bi-directional; IPU/O = Input with internal pull-up during reset; output pin otherwise.
IPU = Input with internal pull-up; IPD = Input with internal pull-down.
OPU = Output with internal pull-up; OPD = Output with internal pull-down.

TABLE 2-2: I/O GROUPING

Group Name	Description
PHY	Physical Interface
MII	Media Independent Interface
SNI	Serial Network Interface
IND	LED Indicators
UP	Unmanaged Programmable
CTRL	Control and Miscellaneous
TEST	Test (Factory)
PWR	Power and Ground

TABLE 2-3: I/O DESCRIPTIONS

Group	I/O Names	Active Status	Description
PHY	RXP[1:8] RXM[1:8]	Analog	Differential inputs (receive) for connection to media (transformer or fiber module)
	TXP[1:8] TXM[1:8]	Analog	Differential outputs (transmit) for connection to media (transformer or fiber module)
	FXSD[1:8]	H	Fiber signal detect. Connect to fiber signal detect output on fiber module with appropriate voltage divider if needed. Tie low for copper mode.
	ISET	Analog	Transmit Current Set. Connecting an external reference resistor to set transmitter output current. This pin connects to a 3 kΩ 1% resistor to ground if a transformer with 1:1 turn ratio is used.
MII	MRXD[0:3]	H	Four bit wide data bus for receiving MAC frames
	MRXDV	H	Receive data valid
	MCOL	H	Receive collision detection
	MCRS	H	Carrier sense
	MTXD[0:3]	H	Four bit wide data bus for transmitting MAC frames
	MTXEN	H	Transmit enable
	MTXER	H	Transmit error
	MRXC	Clock	MII receive clock
	MTXC	Clock	MII transmit clock
SNI	MTXD[0]	H	Serial transmit data
	MTXEN	H	Transmit enable
	MRXD[0]	H	Serial receive data
	MRXDV	H	Receive carrier sense/data valid
	MCOL	H	Collision detection
	MRXC	Clock	SNI receive clock
	MTXC	Clock	SNI transmit clock

TABLE 2-3: I/O DESCRIPTIONS (CONTINUED)

<table>
<tr><th>Group</th><th>I/O Names</th><th>Active Status</th><th colspan="2">Description</th></tr>
<tr><td rowspan="4">IND</td><td>LED[1:9][0]</td><td>L</td><td colspan="2">Output (after reset)
Mode 0: Speed (on = 100/off = 10)
Mode 1: 10/100 + link + activity
10 Mb link activity = slow blink (non-periodic blinking)
100 Mb link activity = fast blink (non-periodic blinking)
Mode 2: Collision (on = collision/off = no collision)
Mode 3: Speed (on = 100/off = 10)</td></tr>
<tr><td>LED[1:9][1]</td><td>L</td><td colspan="2">Output (after reset)
Mode 0: Full-Duplex (on = full/off = half)
Mode 1: Full-Duplex (on = full/off = half)
Mode 2: Full-Duplex (on = full/off = half)
Mode 3: Reserved</td></tr>
<tr><td>LED[1:9][2]</td><td>L</td><td colspan="2">Output (after reset)
Mode 0: Collision (on = collision/off = no collision)
Mode 1: Transmit Activity (on during transmission)
Mode 2: Link activity (10 Mb mode)
Mode 3: Full-Duplex + Collision
(constant on = full-duplex; intermittent on = collision; off = half-duplex with no collision)</td></tr>
<tr><td>LED[1:9][3]</td><td>L</td><td colspan="2">Output (after reset)
Mode 0: Link + Activity
When LED is solid “on”, it indicates the link is on for both 10 or 100BASE-TX, but no data is transmitting or receiving.
When LED is solid “off”, it indicates the link is off.
When LED is blinking, it indicates data is transmitting or receiving for either 10 or 100BASE-TX
Mode 1: Receive Activity (on = receiving/off = not receiving)
Mode 2: Link activity (100 Mb mode)
Mode 3: Link + Activity (see description above)

Note: Mode is set by MODESEL[3:0]. Please see description in UP (unmanaged programming) section.</td></tr>
<tr><td rowspan="14">UP</td><td rowspan="14">MODE-SEL[3:0]</td><td rowspan="14">H</td><td colspan="2">Mode select at reset time. LED mode is selected by using the table below. Note that under normal operation MODESEL[3:2] must be tied low.</td></tr>
<tr><td>MODESEL</td><td>Mode select at reset time. LED mode is selected by using the table below. Note that under normal operation MODE-SEL[3:2] must be tied low.</td></tr>
<tr><td>3 2 1 0</td><td>Operation</td></tr>
<tr><td>0 0 0 0</td><td>LED mode 0</td></tr>
<tr><td>0 0 0 1</td><td>LED mode 1</td></tr>
<tr><td>0 0 1 0</td><td>LED mode 2</td></tr>
<tr><td>0 0 1 1</td><td>LED mode 3</td></tr>
<tr><td>0 1 0 0</td><td>Used for factory testing</td></tr>
<tr><td>0 1 0 1</td><td>Used for factory testing</td></tr>
<tr><td>0 1 1 0</td><td>Used for factory testing</td></tr>
<tr><td>0 1 1 1</td><td>Used for factory testing</td></tr>
<tr><td>1 0 0 0</td><td>Used for factory testing</td></tr>
<tr><td>1 0 0 1</td><td>Used for factory testing</td></tr>
<tr><td>1 0 1 0</td><td>Used for factory testing</td></tr>
</table>

TABLE 2-3: I/O DESCRIPTIONS (CONTINUED)

Group	I/O Names	Active Status	Description	
UP	MODE-SEL[3:0]	H	1 0 1 1	Used for factory testing
			1 1 0 0	Used for factory testing
			1 1 0 1	Used for factory testing
			1 1 1 0	Used for factory testing
	LED[1][3]		Programs auto-negotiation on port 1 D = Disable auto-negotiation, F/U = Enable auto-negotiation (default)	
	LED[1][2]		Programs auto-negotiation on port 2 D = Disable auto-negotiation, F/U = Enable auto-negotiation (default)	
	LED[1][1]		Programs auto-negotiation on port 3 D = Disable auto-negotiation, F/U = Enable auto-negotiation (default)	
	LED[1][0]		Programs auto-negotiation on port 4 D = Disable auto-negotiation, F/U = Enable auto-negotiation (default)	
	LED[2][3]		Programs auto-negotiation on port 5 D = Disable auto-negotiation, F/U = Enable auto-negotiation (default)	
	LED[2][2]		Programs auto-negotiation on port 6 D = Disable auto-negotiation, F/U = Enable auto-negotiation (default)	
	LED[2][1]		Programs auto-negotiation on port 7 D = Disable auto-negotiation, F/U = Enable auto-negotiation (default)	
	LED[2][0]		Programs auto-negotiation on port 8 D = Disable auto-negotiation, F/U = Enable auto-negotiation (default)	
	LED[3][3]		Programs port speed on port 1. This is only effective if auto-negotiation is disabled. D = 10 Mbps, F/U = 100 Mbps (default)	
	LED[3][2]		Programs port speed on port 2. This is only effective if auto-negotiation is disabled. D = 10 Mbps, F/U = 100 Mbps (default)	
	LED[3][1]		Programs port speed on port 3. This is only effective if auto-negotiation is disabled. D = 10 Mbps, F/U = 100 Mbps (default)	
	LED[3][0]		Programs port speed on port 4. This is only effective if auto-negotiation is disabled. D = 10 Mbps, F/U = 100 Mbps (default)	
	LED[4][3]		Programs port speed on port 5. This is only effective if auto-negotiation is disabled. D = 10 Mbps, F/U = 100 Mbps (default)	
	LED[4][2]		Programs port speed on port 6. This is only effective if auto-negotiation is disabled. D = 10 Mbps, F/U = 100 Mbps (default)	
	LED[4][1]		Programs port speed on port 7. This is only effective if auto-negotiation is disabled. D = 10 Mbps, F/U = 100 Mbps (default)	
	LED[4][0]		Programs port speed on port 8. This is only effective if auto-negotiation is disabled. D = 10 Mbps, F/U = 100 Mbps (default)	
	LED[5][3]		Programs port duplex (full/ half) on port 1. This is only effective if auto-negotiation is disabled or if this end has auto- negotiation enabled and the far end has auto negotiation disabled. D = Full-duplex, F/U = Half-duplex (default)	
	LED[5][2]		Programs port duplex (full/ half) on port 2. This is only effective if auto-negotiation is disabled or if this end has auto-negotiation enabled and the far end has auto-negotiation disabled. D = Full-duplex, F/U = Half-duplex (default)	
	LED[5][1]		Programs port duplex (full/ half) on port 3. This is only effective if auto-negotiation is disabled or if this end has auto-negotiation enabled and the far end has auto-negotiation disabled. D = Full-duplex, F/U = Half-duplex (default)	

TABLE 2-3: I/O DESCRIPTIONS (CONTINUED)

Group	I/O Names	Active Status	Description
UP	LED[5][0]	H	Programs port duplex (full/ half) on port 4. This is only effective if auto-negotiation is disabled or if this end has auto-negotiation enabled and the far end has auto-negotiation disabled. D = Full-duplex, F/U = Half-duplex (default)
	LED[9][3]		Programs port duplex (full/ half) on port 5. This is only effective if auto-negotiation is disabled or if this end has auto-negotiation enabled and the far end has auto negotiation disabled. D = Full-duplex, F/U = Half-duplex (default)
	LED[9][2]		Programs port duplex (full/ half) on port 6. This is only effective if auto-negotiation is disabled or if this end has auto-negotiation enabled and the far end has auto-negotiation disabled. D = Full-duplex, F/U = Half-duplex (default)
	LED[9][1]		Programs port duplex (full / half) on port 7. This is only effective if auto-negotiation is disabled or if this end has auto-negotiation enabled and the far end has auto-negotiation disabled. D = Full-duplex, F/U = Half-duplex (default)
	LED[9][0]		Programs port duplex (full / half) on port 8. This is only effective if auto-negotiation is disabled or if this end has auto-negotiation enabled and the far end has auto-negotiation disabled. D = Full-duplex, F/U = Half-duplex (default)
	LED[6][3]		Programs back-off aggressiveness for half-duplex mode D = Less aggressive back-off, F/U = More aggressive back-off (default)
	LED[6][2]		Programs retries for frames that encounter collisions. D = Drop frame after 16 collisions, F/U = Continue sending frame regardless of the number of collisions (default)
	LED[6][1:0]		Reserved – use float configuration
	LED[7][3]		Programs flow control D = No flow control, F/U = Flow control enabled (default)
	LED[7][2]		Programs broadcast storm protection. D = 5% broadcast frames allowed, F/U = Unlimited broadcast frames (default)
	LED[7][1]		Programs buffer sharing feature. D = Equal amount of buffers per port (113 buffers), F/U = Share buffers up to 512 buffers on a single port (default)
	LED[7][0]		Reserved – use float configuration
	LED[8][3]		Programs address aging. D = Aging disabled, F/U = Enable 5 minute aging (default)
	LED[8][2]		Programs frame length enforcement. D = Max length for VLAN is 1522 bytes and without VLAN is 1518 bytes F/U = Max length is 1536 bytes (default)
	LED[8][1]		Reserved
	LED[8][0]		Programs half-duplex back pressure. D = No half-duplex back pressure, U = Half-duplex back pressure enabled (default)
	MRXD[3]		Programs port 9 speed D = 10 Mbps, U = 100 Mbps (default)
	MRXD[2]		Programs port 9 duplex D = Half-duplex, U = Full-duplex (default)
	MRXD[1]		Programs port 9 flow control D = Flow control, U = No flow control (default)
	MRXD[0]		D = reserved, U = normal operation (default)

TABLE 2-3: I/O DESCRIPTIONS (CONTINUED)

Group	I/O Names	Active Status	Description
CTRL	EN1P	H	Enable 802.1p for all ports –this enables QoS based on the priority field in the layer 2 header. 0 = 802.1p selected by port in EEPROM 1 = Use 802.1p priority field unless disabled in EEPROM Note: This is also controlled by the EEPROM registers (registers 4-12 bit 4). The values in the EEPROM supersede this pin. Also, if the priority selection is unaltered in the EEPROM registers (register 3 bits 0-7) then values above 3 are considered high priority and less than 4 are low priority.
	MIIS[1:0]	H	MII mode selection. Allows the MII to run in the following modes **MIIS 1 0** – **Operating mode** 0 0 – Disable MII interface 0 1 – Reverse MII (PHY Mode MII) 1 0 – Forward MII (MAC Mode MII) 1 1 – 7 wire mode (SNI)
	PRSV	H	Priority buffer reserve. Reserves 6 KB of buffer space for the priority traffic if enabled. 0 = No priority reserve 1 = Reserve 6 KB for priority traffic *Note: This is also controlled by the EEPROM registers (register 2 bit 1). The value in the EEPROM supersedes this pin.*
	CFGMODE	H	Selects between EEPROM or processor for programming interface. 0 = Processor interface 1 = EEPROM interface or not programmed on this interface (SCL/SDA not used)
	X1	Clock	External crystal or clock input
	X2	Clock	Used when other polarity of crystal is needed. This is unused for a normal clock input.
	SCL	Clock	Clock for EEPROM
	SDA	I/O	Serial data for EEPROM
	RST#	L	System reset
TEST	TESTEN	H	Factory test input. Tie low for normal operation
	SCANEN		Factory test input. Tie low for normal operation
	MUX[1:2]		Factory test input. Leave open for normal operation
	AOUT		Factory test output. Leave open for normal operation
	DOUT		Factory test output. Leave open for normal operation
	AOUT2		Factory test output. Leave open for normal operation
	DOUT2		Factory test output. Leave open for normal operation
	BTOUT		Factory test output. Leave open for normal operation
	CTOUT		Factory test output. Leave open for normal operation
	BTOUT2		Factory test output. Leave open for normal operation
	CTOUT2		Factory test output. Leave open for normal operation
	TEST[1:2]		Factory test inputs. Leave open for normal operation
	AUTOMDIX		F/U = Enable Auto MDI/MDIX (normal operation) D = Disable Auto MDI/MDIX
	T[1:3] & T[5]		Factory test inputs. Leave open (float) for normal operation
	T[4]		F/D = normal operation (default) U = Disable FEF

TABLE 2-3: I/O DESCRIPTIONS (CONTINUED)

Group	I/O Names	Active Status	Description
TEST	QH[2:5]	H	Factory test outputs. Leave open for normal operation
	QL[2:5]		Factory test outputs. Leave open for normal operation
	IO_SWM		Factory test input. Tie high for normal operation
	RLPBK		Factory test input. Tie low for normal operation
	BIST		Factory test input. Tie low for normal operation
PWR	VDD_RX	—	2.0V for equalizer
	GND_RX		Ground for equalizer
	VDD_TX		2.0V for transmit circuitry
	GND_TX		Ground for transmit circuitry
	VDD_RCV		2.0V for clock recovery circuitry
	GND_RCV		Ground for clock recovery
	VDD_PLLTX		2.0V for phase locked loop circuitry
	GND_PLLTX		Ground for phase locked loop circuitry
	GND-ISO		Analog ground
	VDD		2.0V for core digital circuitry
	VDD-IO		2.0V, 2.5V, or 3.3V for I/O circuitry
	GND		Ground for digital circuitry

Note 2-1 All unmanaged programming takes place at reset time only. For unmanaged programming: F = Float, D = Pull-down, U = Pull-up. See “Reference Circuits” section.

3.0 FUNCTIONAL DESCRIPTION

3.1 Functional Overview: Physical Layer Transceiver

3.1.1 100BASE-TX TRANSMIT

The 100BASE-TX transmit function performs parallel to serial conversion, 4B/5B coding, scrambling, NRZ to NRZI conversion, MLT3 encoding and transmission. The circuit starts with a parallel to serial conversion, which converts the data from the MAC into a 125 MHz serial bit stream. The data and control stream is then converted into 4B/5B coding followed by a scrambler. The serialized data is further converted from NRZ to NRZI format, then transmitted in MLT3 current output. The output current is set by an external 1% 3.01 kΩ resistor for the 1:1 transformer ratio. It has a typical rise/fall time of 4 ns and complies with the ANSI TP-PMD standard regarding amplitude balance, overshoot and timing jitters. The wave-shaped 10BASE-T output is also incorporated into the 100BASE-TX transmitter.

3.1.2 100BASE-TX RECEIVE

The 100BASE-TX receiver function performs adaptive equalization, DC restoration, MLT3 to NRZI conversion, data and clock recovery, NRZI to NRZ conversion, de-scrambling, 4B/5B decoding and serial to parallel conversion. The receiving side starts with the equalization filter to compensate inter-symbol interference (ISI) over the twisted pair cable. Since the amplitude loss and phase distortion is a function of the length of the cable, the equalizer has to adjust its characteristics to optimize the performance. This is an ongoing process and can self adjust to the environmental changes such as temperature variations. The equalized signal then goes through a DC restoration and data conversion block. The DC restoration circuit is used to compensate for the effect of base line wander and improve the dynamic range. The differential data conversion circuit converts the MLT3 format back to NRZI. The slicing threshold is also adaptive. The clock recovery circuit extracts the 125 MHz clock from the edges of the NRZI signal. This recovered clock is then used to convert the NRZI signal into the NRZ format. The signal is then sent through the de-scrambler followed by the 4B/5B decoder. Finally, the NRZ serial data is provided as the input data to the MAC.

3.1.3 PLL CLOCK SYNTHESIZER

The KS8999 generates 125 MHz, 62.5 MHz, 25 MHz, and 10 MHz clocks for system timing. Internal clocks are generated from an external 25 MHz crystal.

3.1.4 SCRAMBLER/DE-SCRAMBLER (100BASE-TX ONLY)

The purpose of the scrambler is to spread the power spectrum of the signal in order to reduce EMI and baseline wander. The data is scrambled by the use of an 11-bit wide linear feedback shift register (LFSR). This can generate a 2047-bit non-repetitive sequence. The receiver will then de-scramble the incoming data stream with the same sequence at the transmitter.

3.1.5 100BASE-FX OPERATION

100BASE-FX operation is very similar to 100BASE-TX operation with the differences being that the scrambler/de-scrambler and MLT3 encoder/decoder are bypassed on transmission and reception. In this mode the auto-negotiation feature is bypassed because there is no standard that supports fiber auto-negotiation.

3.1.6 100BASE-FX SIGNAL DETECTION

The physical port runs in 100BASE-FX mode if FXSDx >0.6V. FXSDx is considered 'low' when 0.6V<FXSDx<1.25V and considered 'high' when FXSDx>1.25V. If FXSDx goes into 'low' state, the link is considered lost and the link active LED will go off. For FXSDx in the high state, the link is considered active. When FXSDx is below 0.6V then 100BASE-FX mode is disabled. See application note for detailed information.

3.1.7 100BASE-FX FAR END FAULT

Far end fault occurs when the signal detection is logically false from the receive fiber module which occurs when FXSDx is below 1.2V and above 0.6V. When this occurs, the transmission side signals the other end of the link by sending 84 1's followed by a zero in the idle period between frames.

3.1.8 10BASE-T TRANSMIT

The output 10BASE-T driver is incorporated into the 100BASE-T driver to allow transmission with the same magnetics. They are internally wave-shaped and pre-emphasized into outputs with a typical 2.3V amplitude.

3.1.9 10BASE-T RECEIVE

On the receive side, input buffer and level detecting squelch circuits are employed. A differential input receiver circuit and a PLL perform the decoding function. The Manchester-encoded data stream is separated into clock signal and NRZ data. A squelch circuit rejects signals with levels less than 400 mV or with short pulse widths in order to prevent noises at the RXP or RXM input from falsely triggering the decoder. When the input exceeds the squelch limit, the PLL locks onto the incoming signal and the KS8999 decodes a data frame. The receiver clock is maintained active during idle periods in between data reception.

3.1.10 POWER MANAGEMENT

In Power Save Mode, the KSZ8999 will turn off everything except for the Energy Detect and PLL circuits when the cable is not installed on an individual port basis. In other words, the KSZ8999 will shutdown most of the internal circuits to save power if there is no link.

3.1.11 MDI/MDI-X AUTO CROSSOVER

The KSZ8999 supports MDI/MDI-X auto crossover. This facilitates the use of either a straight connection CAT-5 cable or a crossover CAT-5 cable. The auto-sense function will detect remote transmit and receive pairs, and correctly assign the transmit and receive pairs from the Microchip device. This can be highly useful when end users are unaware of cable types and can also save on an additional uplink configuration connection.

The auto MDI/MDI-X is achieved by the Microchip device listening for the far end transmission channel and assigning transmit/receive pairs accordingly. Auto MDI/MDI-X can be disabled by pulling Pin 87 (AUTOMDIX) to low.

3.1.12 AUTO-NEGOTIATION

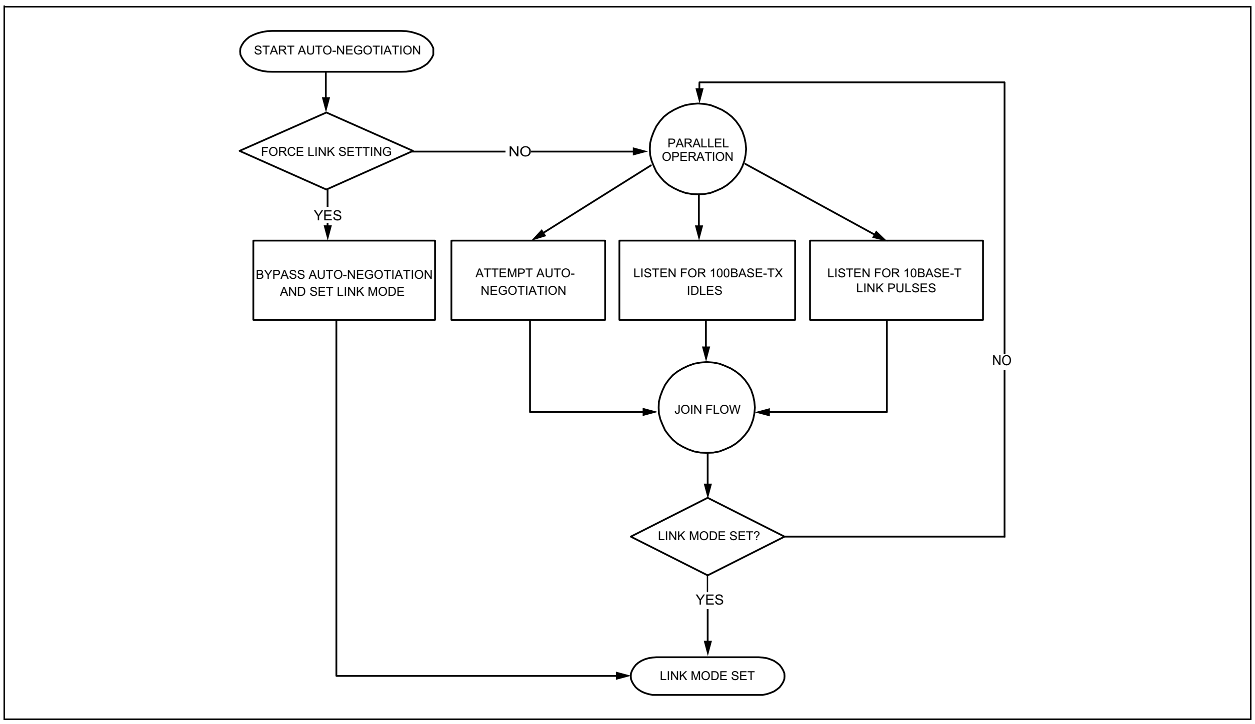
The KS8999 conforms to the auto-negotiation protocol as described by the 802.3 committee.

Auto-negotiation allows UTP (Unshielded Twisted Pair) link partners to select the best common mode of operation. In auto-negotiation the link partners advertise capabilities across the link to each other.

If auto-negotiation is not supported or the link partner to the KS8999 is forced to bypass auto-negotiation, then the mode is set by observing the signal at the receiver. This is known as parallel mode because while the transmitter is sending auto-negotiation advertisements, the receiver is listening for advertisements or a fixed signal protocol.

The flow for the link set up is depicted below.

FIGURE 3-1: AUTO-NEGOTIATION AND PARALLEL OPERATION



3.2 Functional Overview: Switch Core

3.2.1 ADDRESS LOOKUP

The internal look-up table stores MAC addresses and their associated information. It contains 1K full CAM with 48-bit address plus switching information. The KSZ8999 is guaranteed to learn 1K addresses and distinguishes itself from hash-based lookup tables which, depending on the operating environment and probabilities, may not guarantee the absolute number of addresses it can learn.

3.2.2 LEARNING

The internal lookup engine updates its table with a new entry if the following conditions are met:

- The received packet's Source Address (SA) does not exist in the lookup table.
- The received packet is good without receiving errors; the packet size is legal length.

The lookup engine inserts the qualified SA into the table, along with the port number and time stamp. If the table is full, then the last entry of the table is deleted to make room for the new entry.

3.2.3 MIGRATION

The internal look-up engine also monitors whether a station has moved. If a station has moved, it updates the table accordingly. Migration happens when the following conditions are met:

- The received packet's SA is in the table but the associated source port information is different.
- The received packet is good without receiving errors; the packet size is legal length.

The lookup engine updates the existing record in the table with the new source port information.

3.2.4 AGING

The look-up engine will update time stamp information of a record whenever the corresponding SA appears. The time stamp is used in the aging process. If a record is not updated for a period of time, the look-up engine will then remove the record from the table. The look-up engine constantly performs the aging process and will continuously remove aging records. The aging period is 300 seconds. This feature can be enabled or disabled by external pull-up or pull-down resistors.

3.2.5 FORWARDING

The KSZ8999 will forward packets as follows:

- If the DA look-up results is a “match”, the KSZ8999 will use the destination port information to determine where the packet goes.
- If the DA look-up result is a “miss”, the KSZ8999 will forward the packet to all other ports except the port that received the packet.
- All the multicast and broadcast packets will be forwarded to all other ports except the source port.

The KSZ8999 will not forward the following packets:

- Error packets. These include framing errors, FCS errors, alignment errors, and illegal size packet errors.
- 802.3x pause frames. The KSZ8999 will intercept these packets and do the appropriate actions.
- “Local” packets. Based on destination address (DA) look-up. If the destination port from the look-up table matches the port where the packet was from, the packet is defined as “local”.

3.2.6 SWITCHING ENGINE

The KSZ8999 has a very high performance switching engine to move data to and from the MAC’s, packet buffers. It operates in store and forward mode, while the efficient switching mechanism reduces overall latency.

The KSZ8999 has an internal buffer for frames that is 32Kx32 (128 KB). This resource could be shared between the nine ports and is programmed at system reset time by using the unmanaged program mode (I/O strapping).

Each buffer is sized at 128B and therefore there are a total of 1024 buffers available. Two different modes are available for buffer allocation. One mode equally allocates the buffers to all the ports (113 buffers per port). The other mode adaptively allocates buffers up to 512 to a single port based on loading. Selection is achieved by using LED[7][1] in the unmanaged programming description.

3.2.7 MAC OPERATION

The KSZ8999 strictly abides by IEEE 802.3 standard to maximize compatibility.

3.2.7.1 Inter Packet Gap (IPG)

If a frame is successfully transmitted, the 96 bit time IPG is measured between the two consecutive MTXEN. If the current packet is experiencing collision, the 96 bit time IPG is measured from MCRS and the next MTXEN.

3.2.7.2 Back-Off Algorithm

The KSZ8999 implements the IEEE standard 802.3 binary exponential back-off algorithm, and optional “aggressive mode” back off. After 16 collisions, the packet will be optionally dropped depending on the chip configuration.

3.2.7.3 Late Collision

If a transmit packet experiences collisions after 512 bit times of the transmission, the packet will be dropped.

3.2.7.4 Legal Packet Size

The KSZ8999 discards frames less than 64 bytes and can be programmed to accept frames up to 1536 bytes. Because the KSZ8999 supports VLAN tags, the maximum sizing is adjusted when these tags are present.

3.2.7.5 Flow Control

The KSZ8999 supports standard 802.3x flow control frames on both transmit and receive sides.

On the receive side, if the KSZ8999 receives a pause control frame, the KSZ8999 will not transmit the next normal frame until the timer, specified in the pause control frame, expires. If another pause frame is received before the current timer expires, the timer will be updated with the new value in the second pause frame. During this period (being flow controlled), only flow control packets from the KSZ8999 will be transmitted.

On the transmit side, the KSZ8999 has intelligent and efficient ways to determine when to invoke flow control. The flow control is based on availability of the system resources, including available buffers, available transmit queues and available receive queues.

The KSZ8999 will flow control a port, which just received a packet, if the destination port resource is being used up. The KSZ8999 will issue a flow control frame (XOFF), containing the maximum pause time defined in IEEE standard 802.3x. Once the resource is freed up, the KSZ8999 will send out the other flow control frame (XON) with zero pause time to turn off the flow control (turn on transmission to the port).

An hysteresis feature is provided to prevent flow control mechanism from being activated and deactivated too many times.

The KSZ8999 will flow control all ports if the receive queue becomes full.

3.2.7.6 Half-Duplex Back pressure

Half-duplex back pressure option (Note: not in 802.3 standards) is also provided. The activation and deactivation conditions are the same as the above in full-duplex mode. If back pressure is required, the KSZ8999 will send preambles to defer other stations’ transmission (carrier sense deference). To avoid jabber and excessive deference defined in 802.3 standard, after a certain time it will discontinue the carrier sense but it will raise the carrier sense quickly. This short silent time (no carrier sense) is to prevent other stations from sending out packets and keeps other stations in carrier sense deferred state. If the port has packets to send during a back pressure situation, the carrier sense type back pressure will be interrupted and those packets will be transmitted instead. If there are no more packets to send, carrier sense type back pressure will be active again until switch resources free up. If a collision occurs, the binary exponential back-off algorithm is skipped and carrier sense is generated immediately, reducing the chance of further colliding and maintaining carrier sense to prevent reception of packets.

3.2.8 BROADCAST STORM PROTECTION

The KSZ8999 has an intelligent option to protect the switch system from receiving too many broadcast packets. Broadcast packets will be forwarded to all ports except the source port, and thus will use too many switch resources (bandwidth and available space in transmit queues). The KSZ8999 will discard broadcast packets if the number of those packets exceeds the threshold (configured by strapping during reset and EEPROM settings) in a preset period of time. If the preset period expires it will then resume receiving broadcast packets until the threshold is reached. The options are 5% of network line rate for the maximum broadcast receiving threshold or unlimited (feature off).

3.3 MII Interface Operation

The MII (Media Independent Interface) operates in either a MAC or PHY mode. In the MAC mode, the KSZ8999 MII acts like a MAC and in the PHY mode, it acts like a PHY device. This interface is specified by the IEEE 802.3 committee and provides a common interface between physical layer and MAC layer devices. There are two distinct groups, one being for transmission and the other for receiving. The table below describes the signals used in this interface in MAC and PHY modes.

TABLE 3-1: MII SIGNALS

PHY Mode Connection		Description	MAC Mode Connection	
External MAC Controller Signals	KSZ8999 PHY Signals		External PHY Signals	KSZ8999 MAC Signals
MTXEN	MTXEN	Transmit Enable	MTXEN	MRXDV
MTXER	MTXER	Transmit Error	MTXER	Not Used
MTXD3	MTXD[3]	Transmit Data Bit 3	MTXD3	MRXD[3]
MTXD2	MTXD[2]	Transmit Data Bit 2	MTXD2	MRXD[2]
MTXD1	MTXD[1]	Transmit Data Bit 1	MTXD1	MRXD[1]
MTXD0	MTXD[0]	Transmit Data Bit 0	MTXD0	MRXD[0]
MTXC	MTXC	Transmit Clock	MTXC	MTXC
MCOL	MCOL	Collision Detection	MCOL	MCOL
MCRS	MCRS	Carrier Sense	MCRS	MCRS
MRXDV	MRXDV	Receive Data Valid	MRXDV	SMTXEN
MRXER	Not Used	Receive Error	MRXER	MTXER
MRXD3	MRXD[3]	Receive Data Bit 3	MRXD3	MTXD[3]
MRXD2	MRXD[2]	Receive Data Bit 2	MRXD2	MTXD[2]
MRXD1	MRXD[1]	Receive Data Bit 1	MRXD1	MTXD[1]
MRXD0	MRXD[0]	Receive Data Bit 0	MRXD0	MTXD[0]
MRXC	MRXC	Receive Clock	MRXC	MRXC

This interface is a nibble wide data interface and therefore runs at the network bit rate (not encoded). Additional signals on the transmit side indicate when data is valid or when an error occurs during transmission. Likewise, the receive side has indicators that convey when the data is valid and without physical layer errors.

For half-duplex operation there is a signal that indicates a collision has occurred during transmission.

Note that the signal MRXER is not provided on the MII interface for the KSZ8999 for PHY mode operation and MTXER is not represented for MAC mode. Normally this would indicate a receive/transmit error coming from the physical layer/ MAC device, but is not appropriate for this configuration. If the connecting device has a MRXER pin, this should be tied low on the other device for reverse or if it has a MTXER pin in the forward mode it should also be tied low on the other device.

The following explains the KSZ8999 in PHY mode and MAC mode of operation:

KSZ8999 PHY Mode

FIGURE 3-2: DATA SENT FROM EXTERNAL MAC CONTROLLER TO KSZ8999 PHY MODE

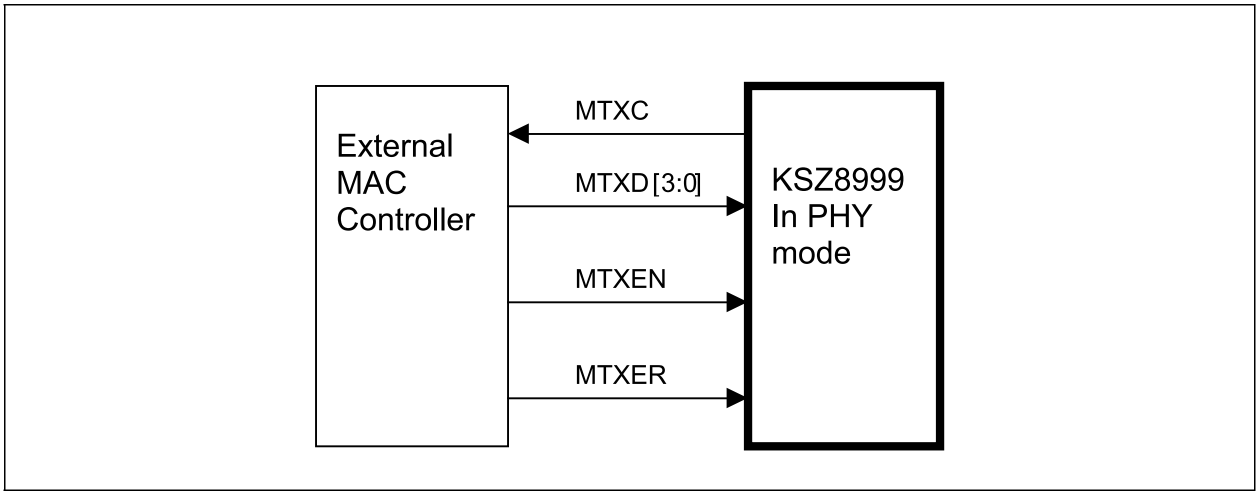
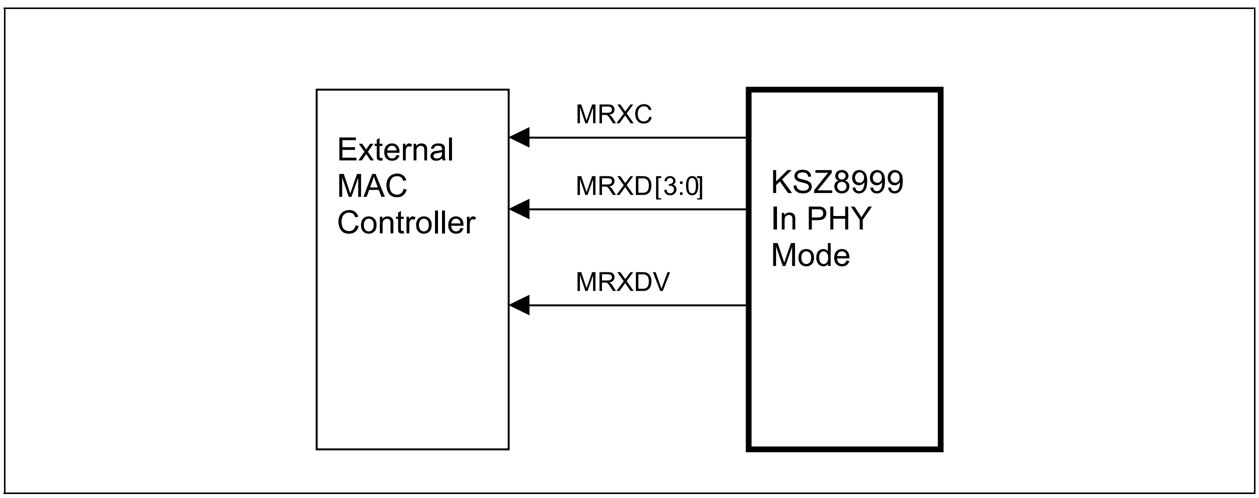


FIGURE 3-3: DATA SENT FROM PHY MODE TO EXTERNAL MAC CONTROLLER



KSZ8999 MAC Mode

FIGURE 3-4: DATA SENT FROM PHY DEVICE TO KSZ8999 MAC MODE

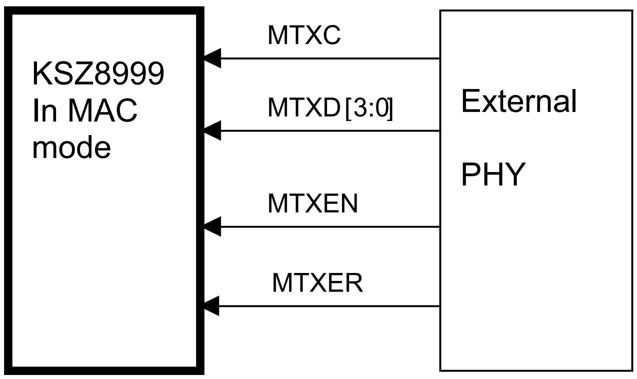
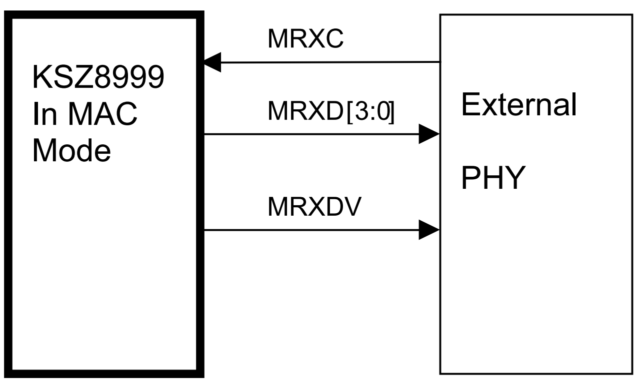


FIGURE 3-5: DATA SENT FROM KSZ8999 MAC MODE TO EXTERNAL PHY DEVICE



3.4 SNI Interface (7-wire) Operation

The SNI (Serial Network Interface) is compatible with some controllers used for network layer protocol processing. KSZ8999 acts like a PHY device to external controllers. This interface can be directly connected to these types of devices. The signals are divided into two groups, one being for transmission and the other being the receive side. The signals involved are described in the table below.

TABLE 3-2: SNI SIGNALS

SNI Signal	Description	KSZ8999 SNI Signal	KSZ8999 Input/ Output
TXEN	Transmit Enable	MTXEN	Input
TXD	Serial Transmit Data	MTXD[0]	Input
TXC	Transmit Clock	MTXC	Output
COL	Collision Detection	MCOL	Output
CRS	Carrier Sense	MRXDV	Output
RXD	Serial Receive Data	MRXD[0]	Output
RXC	Receive Clock	MRXC	Output

This interface is a bit-wide data interface and therefore runs at the network bit rate (not encoded). An additional signal on the transmit side indicates when data is valid. Likewise, the receive side has an indicator that conveys when the data is valid.

For half-duplex operation there is a signal that indicates a collision has occurred during transmission.

3.5 Programmable Features

3.5.1 PRIORITY SCHEMES

The KSZ8999 can determine priority through three different means at the ingress point. The first method is a simple per port method, the second is via the 802.1p frame tag, and the third is by viewing the DSCP (TOS) field in the IPv4 header. Of course, for the priority to be effective, the high and low priority queues must be enabled on the destination port or egress point.

3.5.2 PER PORT METHOD

General priority can be specified on a per port basis. In this type of priority all traffic from the specified input port is considered high priority in the destination queue. This can be useful in IP phone applications mixed with other data types of traffic where the IP phone connects to a specific port. The IP phone traffic would be high priority (outbound) to the wide area network. The inbound traffic to the IP phone is all of the same priority to the IP phone.

3.5.3 802.1P METHOD

This method works well when used with ports that have mixed data and media flows. The inbound port examines the priority field in the tag and determines the high or low priority. Priority profiles are setup in the Priority Classification Control in the EEPROM.

3.5.4 IPV4 DSCP METHOD

This is another per frame way of determining outbound priority. The DSCP (Differentiated Services Code Point – RFC#2474) method uses the TOS field in the IP header to determine high and low priority on a per code point basis. Each fully decoded code point can have either a high or low priority. A larger spectrum of priority flows can be defined with this larger code space.

More specific to implementation, the most significant 6 bits of the TOS field are fully decoded into 64 possibilities, and the singular code that results is compared against the corresponding bit in the DSCP register. If the register bit is a 1, the priority is high and if 0, the priority is low.

3.5.5 OTHER PRIORITY CONSIDERATIONS

When setting up the priority scheme, one should consider other available controls to regulate the traffic. One of these is Priority Control Scheme (register 2 bits 2-3) which controls the interleaving of high and low priority frames. Options allow from a 2:1 ratio up to a setting that sends all the high priority first. This setting controls all ports globally. Another global feature is Priority Buffer Reserve (register 2 bit 1). If this is set, there is a 6 KB (10%) buffer dedicated to high priority traffic, otherwise if cleared the buffer is shared between all traffic.

On an individual port basis there are controls that enable DSCP, 802.1p, port based and high/low priority queues. These are contained in registers 4-12 bits 5-3 and 0. It should be noted that there is a special pin that generally enables the 802.1p priority for all ports (Pin 91). When this pin is active (high) all ports will have the 802.1p priority enabled unless specifically disabled by EEPROM programming (bit 4 of registers 4-12). Default high priority is a value greater than 4 in the VLAN tag with low priority being 3 or less.

The table below briefly summarizes priority features. For more detailed settings see the EEPROM register description.

TABLE 3-3: PRIORITY CONTROL

Register(s)	Bit(s)	Global/Port	Description
General			
2	3-2	Global	Priority Control Scheme: Transmit buffer high/low interleave control
2	1	Global	Priority Buffer Reserve: Reserves 6 KB of the buffer for high priority traffic
4-12	0	Port	Enable Port Queue Split: Splits the transmit queue on the desired port for high and low priority traffic
DSCP Priority			
4-12	5	Port	Enable Port DSCP: Looks at DSCP field in IP header to decide high or low priority
40-47	7-0	Global	DSCP Priority Points: Fully decoded 64 bit register used to determine priority from DSCP field (6 bits) in the IP header
802.1p Priority			
4-12	4	Port	Enable Port 802.1p Priority: Uses the 802.1p priority tag (3 bits) to determine frame priority
3	7-0	Global	Priority Classification: Determines which tag values have high priority
Per Port Priority			
4-12	3	Port	Enable Port Priority: Determines which ports have high or low priority traffic

3.6 Port VLAN Operation

The VLANs are setup by programming the VLAN Mask Registers in the EEPROM. The perspective of the VLAN is from the input port and which output ports it sees directly through the switch. For example if port 1 only participated in a VLAN with ports 2 and 9 then one would set bits 0 and 7 in register 13 (Port 1 VLAN Mask Register). Note that different ports can be setup independently. An example of this would be where a router is connected to port 9 and each of the other ports would work autonomously. In this configuration ports 1 through 8 would only set the mask for port 9 and port 9 would set the mask for ports1 through 8. In this way, the router could see all ports and each of the other individual ports would only communicate with the router.

All multicast and broadcast frames adhere to the VLAN configuration. Unicast frame treatment is a function of register 2 bit 0. If this bit is set then unicast frames only see ports within their VLAN. If this bit is cleared unicast frames can traverse VLANs.

VLAN tags can be added or removed on a per port basis. Further, there are provisions to specify the tag value to be inserted on a per port basis.

The table below briefly summarizes VLAN features. For more detailed settings see the EEPROM register description.

TABLE 3-4: VLAN CONTROL

Register(s)	Bit(s)	Global/ Port	Description
4-12	2	Port	Insert VLAN Tags: If specified, will add VLAN tags to frames without existing tags
4-12	1	Port	Strip VLAN Tags: If specified, will remove VLAN tags from frames if they exist
2	0	Global	VLAN Enforcement: Allows unicast frames to adhere or ignore the VLAN configuration
13-21	7-0	Port	VLAN Mask Registers: Allows configuration of individual VLAN grouping.
22-39	7-0	Port	VLAN Tag Insertion Values: Specifies the VLAN tag to be inserted if enabled (see above)

3.7 Station MAC Address (Control Frames Only)

The MAC source address can be programmed as used in flow control frames. The table below briefly summarizes this programmable feature.

TABLE 3-5: MISCELLANEOUS CONTROL

Register(s)	Bit(s)	Global/ Port	Description
48-53	7-0	Global	Station MAC Address: Used as source address for MAC control frames as used in full-duplex flow control mechanisms.

3.8 EEPROM Operation

The EEPROM interface utilizes two pins that provide a clock and a serial data path. As part of the initialization sequence, the KSZ8999 reads the contents of the EEPROM and loads the values into the appropriate registers. Note that the first two bytes in the EEPROM must be “55” and “99” respectively for the loading to occur properly. If these first two values are not correct, all other data will be ignored.

Data start and stop conditions are signaled on the data line as a state transition during clock high time. A high to low transition indicates start of data and a low to high transition indicates a stop condition. The actual data that traverses the serial line changes during the clock low time.

The KS8999 EEPROM interface is compatible with the Microchip AT24C01A part. Address A0, A1 and A2 are fixed to 000. Further timing and data sequences can be found in the Microchip AT24C01A specification.

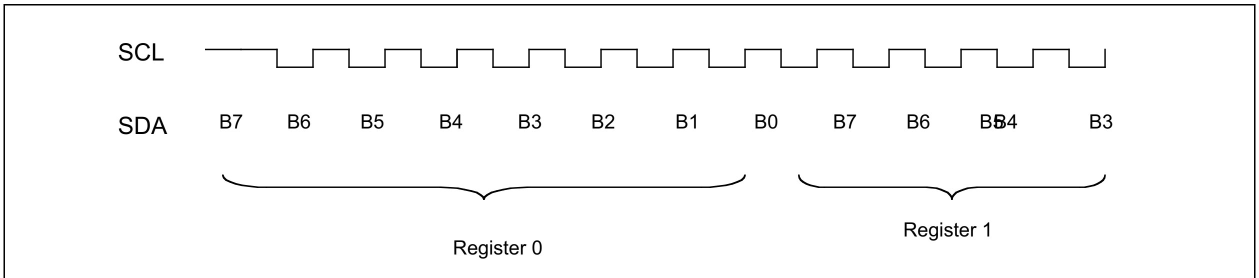
3.9 Optional CPU Interface

Instead of using an EEPROM to program the KSZ8999, one can use an external processor. To utilize this feature, the CFGMODE pin needs to pulled low. This makes the KSZ8999 serial and clock interface into a slave rather than a master. In this mode, clock and data are sourced from the processor.

Due to timing constraints, the maximum clock speed that the processor can generate is 8 MHz. Data timing is referenced to the rising edge of the clock and are 10 ns for setup and 60 ns for hold. The processor needs to supply the exact number of clock cycles and data bits to program the KSZ8999 properly. KSZ8999 won't start until all of the registers are programmed. Bits are loaded from high order (bit 7) to low order (bit 0) starting with register 0 and finishing with register 53.

Register 0: Skip clock on first bit 7	SCL clock cycle: 7
Register 1 to Register 53: provide clock on bit 7 to bit 0	SCL clock cycle: 424
	Total SCL clock cycle: 431

FIGURE 3-6: OPTIONAL CPU INTERFACE



4.0 REGISTER DESCRIPTIONS

TABLE 4-1: EEPROM MEMORY

Address	Name	Description	Default Value
0	7-0	Signature Byte 1. Value = “55”	0x55
1	7-0	Signature Byte 2. Value = “99”	0x99
General Control Register			
2	7-4	Reserved. Set to zero	0000
2	3-2	Priority control scheme (all ports) 00 = Transmit all high priority before any low priority 01 = Transmit high and low priority at a 10:1 ratio 10 = Transmit high and low priority at a 5:1 ratio 11 = Transmit high and low priority at a 2:1 ratio	00
2	1	Priority buffer reserve for high priority traffic 1 = Reserve 6 KB of buffer space for high priority 0 = None reserved	0
2	0	VLAN enforcement 1 = All unicast frames adhere to VLAN configuration 0 = Unicast frames ignore VLAN configuration	0
Priority Classification Control: 802.1p Tag Field			
3	7	1 = State “111”is high priority 0 = State “111”is low priority	1
3	6	1 = State “110”is high priority 0 = State “110”is low priority	1
3	5	1 = State “101”is high priority 0 = State “101”is low priority	1
3	4	1 = State “100”is high priority 0 = State “100”is low priority	1
3	3	1 = State “011”is high priority 0 = State “011”is low priority	0
3	2	1 = State “010”is high priority 0 = State “010”is low priority	0
3	1	1 = State “001”is high priority 0 = State “001”is low priority	0
3	0	1 = State “000”is high priority 0 = State “000”is low priority	0
Port 1 Control Register			
4	7-6	Reserved. Set to zero	00
4	5	TOS priority classification enable for port 1 1 = Enable 0 = Disable	0
4	4	802.1p priority classification enable for port 1 1 = Enable 0 = Disable	0
4	3	Port based priority classification for port 1 1 = High priority 0 = Low priority	0
4	2	Insert VLAN tags for port 1 if non-existent 1 = Enable 0 = Disable	0

TABLE 4-1: EEPROM MEMORY (CONTINUED)

Address	Name	Description	Default Value
4	1	Strip VLAN tags for port 1 if existent 1 = Enable 0 = Disable	0
4	0	Enable high and low output priority queues for port 1 1 = Enable 0 = Disable	0
Port 2 Control Register			
5	7-6	Reserved. Set to zero	00
5	5	TOS priority classification enable for port 2 1 = Enable 0 = Disable	0
5	4	802.1p priority classification enable for port 2 1 = Enable 0 = Disable	0
5	3	Port based priority classification for port 2 1 = High priority 0 = Low priority	0
5	2	Insert VLAN tags for port 2 if non-existent 1 = Enable 0 = Disable	0
5	1	Strip VLAN tags for port 2 if existent 1 = Enable 0 = Disable	0
5	0	Enable high and low output priority queues for port 2 1 = Enable 0 = Disable	0
Port 3 Control Register			
6	7-6	Reserved. Set to zero	00
6	5	TOS priority classification enable for port 3 1 = Enable 0 = Disable	0
6	4	802.1p priority classification enable for port 3 1 = Enable 0 = Disable	0
6	3	Port based priority classification for port 3 1 = High priority 0 = Low priority	0
6	2	Insert VLAN tags for port 3 if non-existent 1 = Enable 0 = Disable	0
6	1	Strip VLAN tags for port 3 if existent 1 = Enable 0 = Disable	0
6	0	Enable high and low output priority queues for port 3 1 = Enable 0 = Disable	0
Port 4 Control Register			
7	7-6	Reserved. Set to zero	00
7	5	TOS priority classification enable for port 4 1 = Enable 0 = Disable	0

TABLE 4-1: EEPROM MEMORY (CONTINUED)

Address	Name	Description	Default Value
7	4	802.1p priority classification enable for port 4 1 = Enable 0 = Disable	0
7	3	Port based priority classification for port 4 1 = High priority 0 = Low priority	0
7	2	Insert VLAN tags for port 4 if non-existent 1 = Enable 0 = Disable	0
7	1	Strip VLAN tags for port 4 if existent 1 = Enable 0 = Disable	0
7	0	Enable high and low output priority queues for port 4 1 = Enable 0 = Disable	0
Port 5 Control Register			
8	7-6	Reserved. Set to zero	00
8	5	TOS priority classification enable for port 5 1 = Enable 0 = Disable	0
8	4	802.1p priority classification enable for port 5 1 = Enable 0 = Disable	0
8	3	Port based priority classification for port 5 1 = High priority 0 = Low priority	0
8	2	Insert VLAN tags for port 5 if non-existent 1 = Enable 0 = Disable	0
8	1	Strip VLAN tags for port 5 if existent 1 = Enable 0 = Disable	0
8	0	Enable high and low output priority queues for port 5 1 = Enable 0 = Disable	0
Port 6 Control Register			
9	7-6	Reserved. Set to zero	00
9	5	TOS priority classification enable for port 6 1 = Enable 0 = Disable	0
9	4	802.1p priority classification enable for port 6 1 = Enable 0 = Disable	0
9	3	Port based priority classification for port 6 1 = High priority 0 = Low priority	0
9	2	Insert VLAN tags for port 6 if non-existent 1 = Enable 0 = Disable	0

TABLE 4-1: EEPROM MEMORY (CONTINUED)

Address	Name	Description	Default Value
9	1	Strip VLAN tags for port 6 if existent 1 = Enable 0 = Disable	0
9	0	Enable high and low output priority queues for port 6 1 = Enable 0 = Disable	0
Port 7 Control Register			
10	7-6	Reserved. Set to zero	00
10	5	TOS priority classification enable for port 7 1 = Enable 0 = Disable	0
10	4	802.1p priority classification enable for port 7 1 = Enable 0 = Disable	0
10	3	Port based priority classification for port 7 1 = High priority 0 = Low priority	0
10	2	Insert VLAN tags for port 7 if non-existent 1 = Enable 0 = Disable	0
10	1	Strip VLAN tags for port 7 if existent 1 = Enable 0 = Disable	0
10	0	Enable high and low output priority queues for port 7 1 = Enable 0 = Disable	0
Port 8 Control Register			
11	7-6	Reserved. Set to zero	00
11	5	TOS priority classification enable for port 8 1 = Enable 0 = Disable	0
11	4	802.1p priority classification enable for port 8 1 = Enable 0 = Disable	0
11	3	Port based priority classification for port 8 1 = High priority 0 = Low priority	0
11	2	Insert VLAN tags for port 8 if non-existent 1 = Enable 0 = Disable	0
11	1	Strip VLAN tags for port 8 if existent 1 = Enable 0 = Disable	0
11	0	Enable high and low output priority queues for port 8 1 = Enable 0 = Disable	0
Port 9 Control Register			
12	7-6	Reserved. Set to zero	00
12	5	TOS priority classification enable for port 9 1 = Enable 0 = Disable	0

TABLE 4-1: EEPROM MEMORY (CONTINUED)

Address	Name	Description	Default Value
12	4	802.1p priority classification enable for port 9 1 = Enable 0 = Disable	0
12	3	Port based priority classification for port 9 1 = High priority 0 = Low priority	0
12	2	Insert VLAN tags for port 9 if non-existent 1 = Enable 0 = Disable	0
12	1	Strip VLAN tags for port 9 if existent 1 = Enable 0 = Disable	0
12	0	Enable high and low output priority queues for port 9 1 = Enable 0 = Disable	0
Port 1 VLAN Mask Register			
13	7	Port 9 inclusion 1 = Port 9 in the same VLAN as port 1 0 = Port 9 not in the same VLAN as port 1	1
13	6	Port 8 inclusion 1 = Port 8 in the same VLAN as port 1 0 = Port 8 not in the same VLAN as port 1	1
13	5	Port 7 inclusion 1 = Port 7 in the same VLAN as port 1 0 = Port 7 not in the same VLAN as port 1	1
13	4	Port 6 inclusion 1 = Port 6 in the same VLAN as port 1 0 = Port 6 not in the same VLAN as port 1	1
13	3	Port 5 inclusion 1 = Port 5 in the same VLAN as port 1 0 = Port 5 not in the same VLAN as port 1	1
13	2	Port 4 inclusion 1 = Port 4 in the same VLAN as port 1 0 = Port 4 not in the same VLAN as port 1	1
13	1	Port 3 inclusion 1 = Port 3 in the same VLAN as port 1 0 = Port 3 not in the same VLAN as port 1	1
13	0	Port 2 inclusion 1 = Port 2 in the same VLAN as port 1 0 = Port 2 not in the same VLAN as port 1	1
Port 2 VLAN Mask Register			
14	7	Port 9 inclusion 1 = Port 9 in the same VLAN as port 2 0 = Port 9 not in the same VLAN as port 2	1
14	6	Port 8 inclusion 1 = Port 8 in the same VLAN as port 2 0 = Port 8 not in the same VLAN as port 2	1
14	5	Port 7 inclusion 1 = Port 7 in the same VLAN as port 2 0 = Port 7 not in the same VLAN as port 2	1

TABLE 4-1: EEPROM MEMORY (CONTINUED)

Address	Name	Description	Default Value
14	4	Port 6 inclusion 1 = Port 6 in the same VLAN as port 2 0 = Port 6 not in the same VLAN as port 2	1
14	3	Port 5 inclusion 1 = Port 5 in the same VLAN as port 2 0 = Port 5 not in the same VLAN as port 2	1
14	2	Port 4 inclusion 1 = Port 4 in the same VLAN as port 2 0 = Port 4 not in the same VLAN as port 2	1
14	1	Port 3 inclusion 1 = Port 3 in the same VLAN as port 2 0 = Port 3 not in the same VLAN as port 2	1
14	0	Port 1 inclusion 1 = Port 1 in the same VLAN as port 2 0 = Port 1 not in the same VLAN as port 2	1
Port 3 VLAN Mask Register			
15	7	Port 9 inclusion 1 = Port 9 in the same VLAN as port 3 0 = Port 9 not in the same VLAN as port 3	1
15	6	Port 8 inclusion 1 = Port 8 in the same VLAN as port 3 0 = Port 8 not in the same VLAN as port 3	1
15	5	Port 7 inclusion 1 = Port 7 in the same VLAN as port 3 0 = Port 7 not in the same VLAN as port 3	1
15	4	Port 6 inclusion 1 = Port 6 in the same VLAN as port 3 0 = Port 6 not in the same VLAN as port 3	1
15	3	Port 5 inclusion 1 = Port 5 in the same VLAN as port 3 0 = Port 5 not in the same VLAN as port 3	1
15	2	Port 4 inclusion 1 = Port 4 in the same VLAN as port 3 0 = Port 4 not in the same VLAN as port 3	1
15	1	Port 2 inclusion 1 = Port 2 in the same VLAN as port 3 0 = Port 2 not in the same VLAN as port 3	1
15	0	Port 1 inclusion 1 = Port 1 in the same VLAN as port 3 0 = Port 1 not in the same VLAN as port 3	1
Port 4 VLAN Mask Register			
16	7	Port 9 inclusion 1 = Port 9 in the same VLAN as port 4 0 = Port 9 not in the same VLAN as port 4	1
16	6	Port 8 inclusion 1 = Port 8 in the same VLAN as port 4 0 = Port 8 not in the same VLAN as port 4	1
16	5	Port 7 inclusion 1 = Port 7 in the same VLAN as port 4 0 = Port 7 not in the same VLAN as port 4	1

TABLE 4-1: EEPROM MEMORY (CONTINUED)

Address	Name	Description	Default Value
16	4	Port 6 inclusion 1 = Port 6 in the same VLAN as port 4 0 = Port 6 not in the same VLAN as port 4	1
16	3	Port 5 inclusion 1 = Port 5 in the same VLAN as port 4 0 = Port 5 not in the same VLAN as port 4	1
16	2	Port 3 inclusion 1 = Port 3 in the same VLAN as port 4 0 = Port 3 not in the same VLAN as port 4	1
16	1	Port 2 inclusion 1 = Port 2 in the same VLAN as port 4 0 = Port 2 not in the same VLAN as port 4	1
16	0	Port 1 inclusion 1 = Port 1 in the same VLAN as port 4 0 = Port 1 not in the same VLAN as port 4	1
Port 5 VLAN Mask Register			
17	7	Port 9 inclusion 1 = Port 9 in the same VLAN as port 5 0 = Port 9 not in the same VLAN as port 5	1
17	6	Port 8 inclusion 1 = Port 8 in the same VLAN as port 5 0 = Port 8 not in the same VLAN as port 5	1
17	5	Port 7 inclusion 1 = Port 7 in the same VLAN as port 5 0 = Port 7 not in the same VLAN as port 5	1
17	4	Port 6 inclusion 1 = Port 6 in the same VLAN as port 5 0 = Port 6 not in the same VLAN as port 5	1
17	3	Port 4 inclusion 1 = Port 4 in the same VLAN as port 5 0 = Port 4 not in the same VLAN as port 5	1
17	2	Port 3 inclusion 1 = Port 3 in the same VLAN as port 5 0 = Port 3 not in the same VLAN as port 5	1
17	1	Port 2 inclusion 1 = Port 2 in the same VLAN as port 5 0 = Port 2 not in the same VLAN as port 5	1
17	0	Port 1 inclusion 1 = Port 1 in the same VLAN as port 5 0 = Port 1 not in the same VLAN as port 5	1
Port 6 VLAN Mask Register			
18	7	Port 9 inclusion 1 = Port 9 in the same VLAN as port 6 0 = Port 9 not in the same VLAN as port 6	1
18	6	Port 8 inclusion 1 = Port 8 in the same VLAN as port 6 0 = Port 8 not in the same VLAN as port 6	1
18	5	Port 7 inclusion 1 = Port 7 in the same VLAN as port 6 0 = Port 7 not in the same VLAN as port 6	1

TABLE 4-1: EEPROM MEMORY (CONTINUED)

Address	Name	Description	Default Value
18	4	Port 5 inclusion 1 = Port 5 in the same VLAN as port 6 0 = Port 5 not in the same VLAN as port 6	1
18	3	Port 4 inclusion 1 = Port 4 in the same VLAN as port 6 0 = Port 4 not in the same VLAN as port 6	1
18	2	Port 3 inclusion 1 = Port 3 in the same VLAN as port 6 0 = Port 3 not in the same VLAN as port 6	1
18	1	Port 2 inclusion 1 = Port 2 in the same VLAN as port 6 0 = Port 2 not in the same VLAN as port 6	1
18	0	Port 1 inclusion 1 = Port 1 in the same VLAN as port 6 0 = Port 1 not in the same VLAN as port 6	1
Port 7 VLAN Mask Register			
19	7	Port 9 inclusion 1 = Port 9 in the same VLAN as port 7 0 = Port 9 not in the same VLAN as port 7	1
19	6	Port 8 inclusion 1 = Port 8 in the same VLAN as port 7 0 = Port 8 not in the same VLAN as port 7	1
19	5	Port 6 inclusion 1 = Port 6 in the same VLAN as port 7 0 = Port 6 not in the same VLAN as port 7	1
19	4	Port 5 inclusion 1 = Port 5 in the same VLAN as port 7 0 = Port 5 not in the same VLAN as port 7	1
19	3	Port 4 inclusion 1 = Port 4 in the same VLAN as port 7 0 = Port 4 not in the same VLAN as port 7	1
19	2	Port 3 inclusion 1 = Port 3 in the same VLAN as port 7 0 = Port 3 not in the same VLAN as port 7	1
19	1	Port 2 inclusion 1 = Port 2 in the same VLAN as port 7 0 = Port 2 not in the same VLAN as port 7	1
19	0	Port 1 inclusion 1 = Port 1 in the same VLAN as port 7 0 = Port 1 not in the same VLAN as port 7	1
Port 8 VLAN Mask Register			
20	7	Port 9 inclusion 1 = Port 9 in the same VLAN as port 8 0 = Port 9 not in the same VLAN as port 8	1
20	6	Port 7 inclusion 1 = Port 7 in the same VLAN as port 8 0 = Port 7 not in the same VLAN as port 8	1
20	5	Port 6 inclusion 1 = Port 6 in the same VLAN as port 8 0 = Port 6 not in the same VLAN as port 8	1

TABLE 4-1: EEPROM MEMORY (CONTINUED)

Address	Name	Description	Default Value
20	4	Port 5 inclusion 1 = Port 5 in the same VLAN as port 8 0 = Port 5 not in the same VLAN as port 8	1
20	3	Port 4 inclusion 1 = Port 4 in the same VLAN as port 8 0 = Port 4 not in the same VLAN as port 8	1
20	2	Port 3 inclusion 1 = Port 3 in the same VLAN as port 8 0 = Port 3 not in the same VLAN as port 8	1
20	1	Port 2 inclusion 1 = Port 2 in the same VLAN as port 8 0 = Port 2 not in the same VLAN as port 8	1
20	0	Port 1 inclusion 1 = Port 1 in the same VLAN as port 8 0 = Port 1 not in the same VLAN as port 8	1
Port 9 VLAN Mask Register			
21	7	Port 8 inclusion 1 = Port 8 in the same VLAN as port 9 0 = Port 8 not in the same VLAN as port 9	1
21	6	Port 7 inclusion 1 = Port 7 in the same VLAN as port 9 0 = Port 7 not in the same VLAN as port 9	1
21	5	Port 6 inclusion 1 = Port 6 in the same VLAN as port 9 0 = Port 6 not in the same VLAN as port 9	1
21	4	Port 5 inclusion 1 = Port 5 in the same VLAN as port 9 0 = Port 5 not in the same VLAN as port 9	1
21	3	Port 4 inclusion 1 = Port 4 in the same VLAN as port 9 0 = Port 4 not in the same VLAN as port 9	1
21	2	Port 3 inclusion 1 = Port 3 in the same VLAN as port 9 0 = Port 3 not in the same VLAN as port 9	1
21	1	Port 2 inclusion 1 = Port 2 in the same VLAN as port 9 0 = Port 2 not in the same VLAN as port 9	1
21	0	Port 1 inclusion 1 = Port 1 in the same VLAN as port 9 0 = Port 1 not in the same VLAN as port 9	1
Port 1 VLAN Tag Insertion Value Registers			
22	7-5	User priority [2:0]	000
22	4	CFI	0
22	3-0	VID [11:8]	0x0
23	7-0	VID [7:0]	0x00
Port 2 VLAN Tag Insertion Value Registers			
24	7-5	User priority [2:0]	000
24	4	CFI	0
24	3-0	VID [11:8]	0x0

TABLE 4-1: EEPROM MEMORY (CONTINUED)

Address	Name	Description	Default Value
25	7-0	VID [7:0]	0x00
Port 3 VLAN Tag Insertion Value Registers			
26	7-5	User priority [2:0]	000
26	4	CFI	0
26	3-0	VID [11:8]	0x0
27	7-0	VID [7:0]	0x00
Port 4 VLAN Tag Insertion Value Registers			
28	7-5	User priority [2:0]	000
28	4	CFI	0
28	3-0	VID [11:8]	0x0
29	7-0	VID [7:0]	0x00
Port 5 VLAN Tag Insertion Value Registers			
30	7-5	User priority [2:0]	000
30	4	CFI	0
30	3-0	VID [11:8]	0x0
31	7-0	VID [7:0]	0x00
Port 6 VLAN Tag Insertion Value Registers			
32	7-5	User priority [2:0]	000
32	4	CFI	0
32	3-0	VID [11:8]	0x0
33	7-0	VID [7:0]	0x00
Port 7 VLAN Tag Insertion Value Registers			
34	7-5	User priority [2:0]	000
34	4	CFI	0
34	3-0	VID [11:8]	0x0
35	7-0	VID [7:0]	0x00
Port 8 VLAN Tag Insertion Value Registers			
36	7-5	User priority [2:0]	000
36	4	CFI	0
36	3-0	VID [11:8]	0x0
37	7-0	VID [7:0]	0x00
Port 9 VLAN Tag Insertion Value Registers			
38	7-5	User priority [2:0]	000
38	4	CFI	0
38	3-0	VID [11:8]	0x0
39	7-0	VID [7:0]	0x00
Diff Serv Code Point Registers			
40	7-0	DSCP[63:56]	0x00
41	7-0	DSCP[55:48]	0x00
42	7-0	DSCP[47:40]	0x00
43	7-0	DSCP[39:32]	0x00
44	7-0	DSCP[31:24]	0x00

TABLE 4-1: EEPROM MEMORY (CONTINUED)

Address	Name	Description	Default Value
45	7-0	DSCP[23:16]	0x00
46	7-0	DSCP[15:8]	0x00
47	7-0	DSCP[7:0]	0x00
Station MAC Address Registers (All Ports - MAC Control Frames Only)			
48	7-0	MAC address [47:40]	0x00
49	7-0	MAC address [39:32]	0x40
50	7-0	MAC address [31:24]	0x05
51	7-0	MAC address [23:16]	0x43
52	7-0	MAC address [15:8]	0x5E
53	7-0	MAC address [7:0]	0xFE

5.0 OPERATIONAL CHARACTERISTICS

5.1 Absolute Maximum Ratings*

Supply Voltage (V_{DD_RX}, V_{DD_TX}, V_{DD_RCV}, V_{DD}, V_{DD_PLLTX}) .... –0.5V to +2.3V

Supply Voltage (V_{DDIO}) .... –0.5V to +3.8V

Input Voltage .... –0.5V to +4.0V

Output Voltage .... –0.5V to +4.0V

Storage Temperature (T_S) .... –55°C to +150°C

Lead Temperature (Soldering, 10 sec) .... +270°C

*Exceeding the absolute maximum rating may damage the device. Stresses greater than those listed in the table above may cause permanent damage to the device. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability. Unused inputs must always be tied to an appropriate logic voltage level.

5.2 Operating Ratings**

Supply Voltage (V_{DD_RX}, V_{DD_TX}, V_{DD_RCV}, V_{DD}, V_{DD_PLLTX}) .... +2.0V to +2.3V

Supply Voltage (V_{DDIO}) .... +2.0V to +2.3V or +3.0V to +3.6V

Ambient Operating Temperature for Commercial Option (T_A) .... 0°C to +70°C

Ambient Operating Temperature for Industrial Option (T_A) .... –40°C to +85°C

Thermal Resistance (Note 5-1) (Θ_{JA}) .... +39.1°C/W

**The device is not guaranteed to function outside its operating ratings. Unused inputs must always be tied to an appropriate logic voltage level (Ground to VDD).

Note 5-1 No heat spreader (HS) in this package.

Note:	Do not drive input signals without power supplied to the device.

6.0 ELECTRICAL CHARACTERISTICS

V_{DD} = 2.0V to 2.3V; T_A = 0°C to +70°; unless noted. Specification is for packaged product only.

TABLE 6-1: ELECTRICAL CHARACTERISTICS

Parameters	Symbol	Min.	Typ.	Max.	Units	Condition
Supply Voltage	V_{DD}	2.0	2.1	2.3	V	—
Supply Current (including TX output driver current)						
100BASE-TX Operation: Total		—	0.64	0.85	A	—
100BASE-TX (Transmitter)	I_{DX}	—	0.35	0.40	A	—
100BASE-TX (Analog)	I_{DA}	—	0.18	0.25	A	—
100BASE-TX (Digital)	I_{DD}	—	0.11	0.20	A	—
10BASE-T Operation: Total		—	1.04	1.32	A	—
10BASE-T (Transmitter)	I_{DX}	—	0.84	0.95	A	—
10BASE-T (Analog)	I_{DA}	—	0.11	0.17	A	—
10BASE-T (Digital)	I_{DD}	—	0.09	0.20	A	—
TTL Inputs						
Input High Voltage	V_{IH}	(1/2 V_{DDIO}) + 0.4	—	—	V	—
Input Low Voltage	V_{IL}	—	—	(1/2 V_{DDIO}) – 0.4	V	—
Input Current	I_{IN}	–10	—	10	µA	V_{IN} = GND ~ V_{DD}
TTL Outputs						
Output High Voltage	V_{OH}	V_{DDIO} – 0.4	—	—	V	I_{OH} = –4 mA
Output Low Voltage	V_{OL}	—	—	0.4	V	I_{OL} = 4 mA
Output Tri-State Leakage	$\|I_{OZ}\|$	—	—	10	µA	—
100BASE-TX Transmit (measured differentially after 1:1 transformer)						
Peak Differential Output Voltage	V_O	0.95	—	1.05	V	50Ω from each output to V_{DD}
Output Voltage Imbalance	V_{IMB}	—	—	2	%	50Ω from each output to V_{DD}
Rise/Fall Time	t_r/t_f	3	—	5	ns	—
Rise/Fall Time Imbalance		0	—	0.5	ns	—
100BASE-TX Transmit (measured differentially after 1:1 transformer)						
Duty Cycle Distortion	—	—	—	±0.5	ns	—
Overshoot	—	—	—	5	%	—
Reference Voltage of ISET	V_{SET}	—	0.75	—	V	—
Output Jitters	—	—	0.7	1.4	ns	Peak-to-peak
10BASE-TX Receive						
Squelch Threshold	V_{SQ}	—	400	—	mV	5 MHz square wave
10BASE-T Transmit (measured differentially after 1:1 transformer)						
Peak Differential Output Voltage	V_P	—	2.3	—	V	50Ω from each output to V_{DD}
Jitters Added	—	—	—	±3.5	ns	50Ω from each output to V_{DD}
Rise/Fall Times	—	—	28	—	ns	—

7.0 TIMING DIAGRAMS

FIGURE 7-1: EEPROM INPUT TIMING

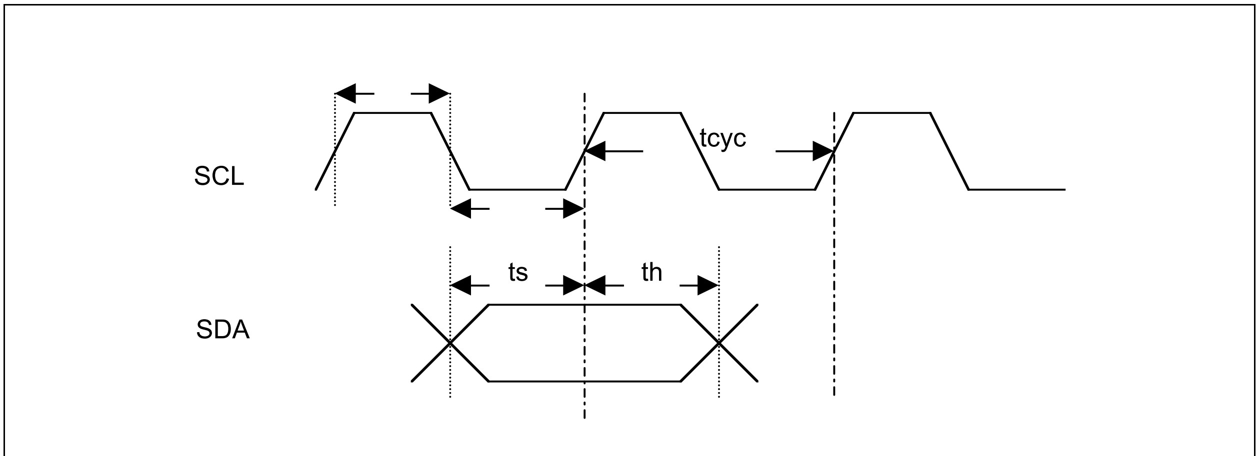


TABLE 7-1: EEPROM INPUT TIMING PARAMETERS

Symbol	Parameter	Min.	Typ.	Max.	Units
t_{cyc}	Clock cycle	—	16384	—	ns
t_S	Set-up time	20	—	—	ns
t_H	Hold time	20	—	—	ns

FIGURE 7-2: EEPROM OUTPUT TIMING

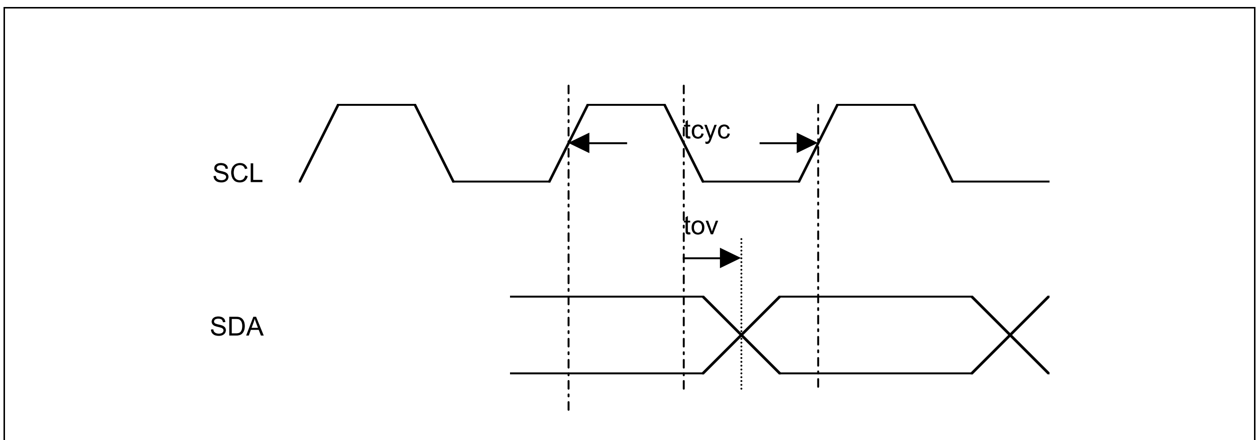


TABLE 7-2: EEPROM OUTPUT TIMING PARAMETERS

Symbol	Parameters	Min.	Typ.	Max.	Units
t_{cyc}	Clock cycle	—	16384	—	ns
t_{OV}	Output valid	4096	4112	4128	ns

FIGURE 7-3: SNI (7-WIRE) INPUT TIMING

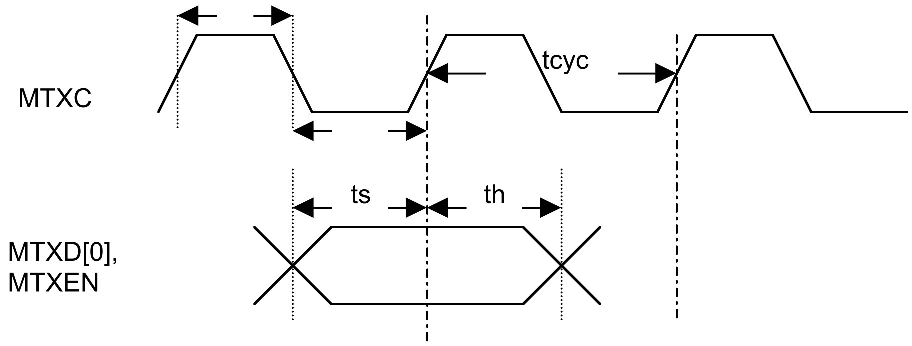


TABLE 7-3: SNI (7-WIRE) INPUT TIMING PARAMETERS

Symbol	Parameters	Min.	Typ.	Max.	Units
t_{cyc}	Clock cycle	—	100	—	ns
t_S	Set-up time	10	—	—	ns
t_H	Hold time	0	—	—	ns

FIGURE 7-4: SNI (7-WIRE) OUTPUT TIMING

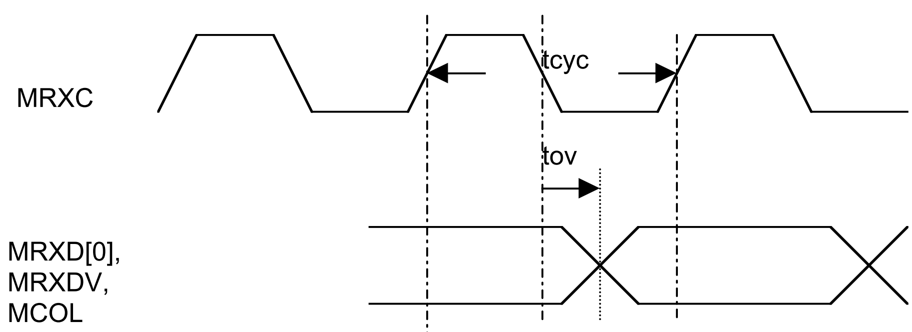


TABLE 7-4: SNI (7-WIRE) OUTPUT TIMING PARAMETERS

Symbol	Parameters	Min.	Typ.	Max.	Units
t_{cyc}	Clock cycle	—	100	—	ns
t_{OV}	Output valid	0	3	6	ns

FIGURE 7-5: KSZ8999 PHY MODE: DATA SENT FROM EXT. MAC CONTROLLER TO KSZ8999

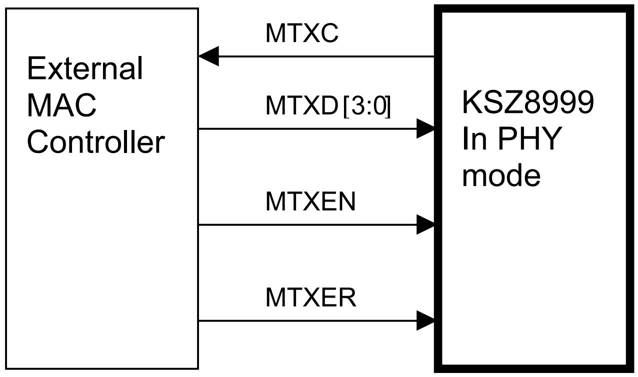


FIGURE 7-6: KSZ8999 PHY MODE RECEIVE TIMING

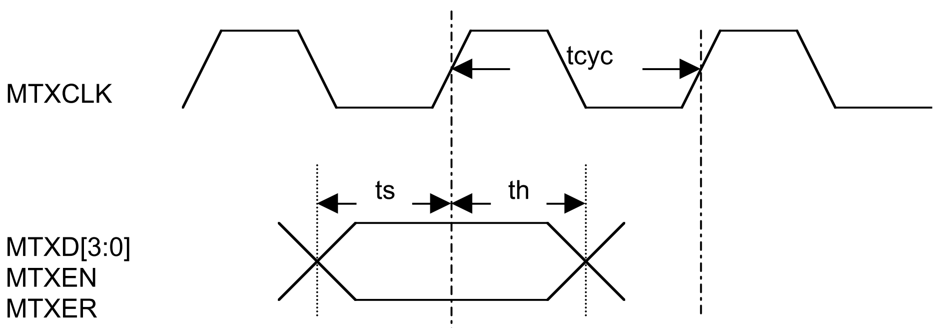


TABLE 7-5: MII TIMING IN KSZ8999 PHY AND MAC MODE TIMING PARAMETERS

Symbol	Parameters	Min.	Typ.	Max.	Units
t_{cyc}	Clock cycle (100BASE-TX)	—	40	—	ns
t_{cyc}	Clock cycle (10BASE-T)	—	400	—	ns
t_S	Set-up time	10	—	—	ns
t_H	Hold time	0	—	—	ns

FIGURE 7-7: KSZ8999 PHY MODE: DATA SENT FROM KSZ8999 PHY TO EXT. MAC CONTROLLER

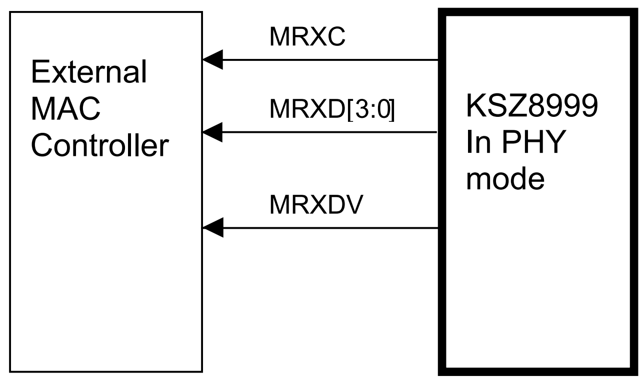


FIGURE 7-8: KSZ8999 PHY MODE TRANSMIT TIMING

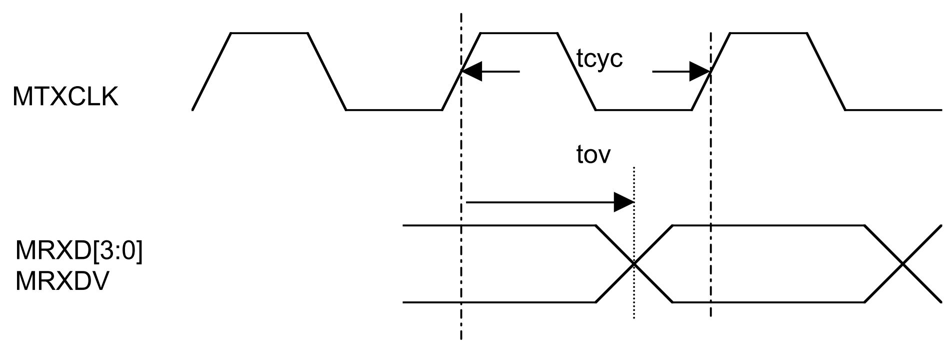


TABLE 7-6: KSZ8999 PHY MODE TRANSMIT TIMING PARAMETERS

Symbol	Parameters	Min.	Typ.	Max.	Units
t_{cyc}	Clock cycle (100BASE-TX)	—	40	—	ns
t_{cyc}	Clock cycle (10BASE-T)	—	400	—	ns
t_{OV}	Output valid	18	25	28	ns

FIGURE 7-9: KSZ8999 MAC MODE: DATA SENT FROM EXT. PHY DEVICE TO KSZ8999

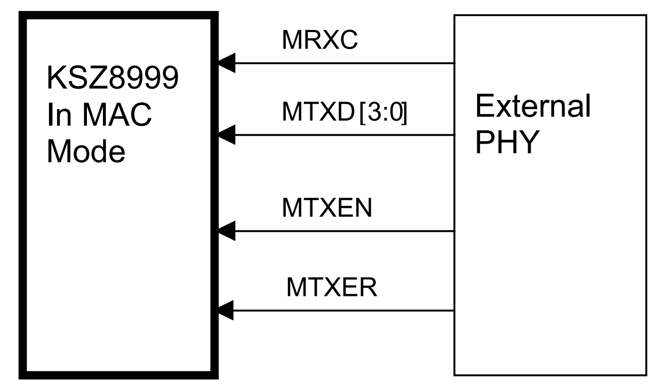


FIGURE 7-10: KSZ8999 MAC MODE RECEIVE TIMING

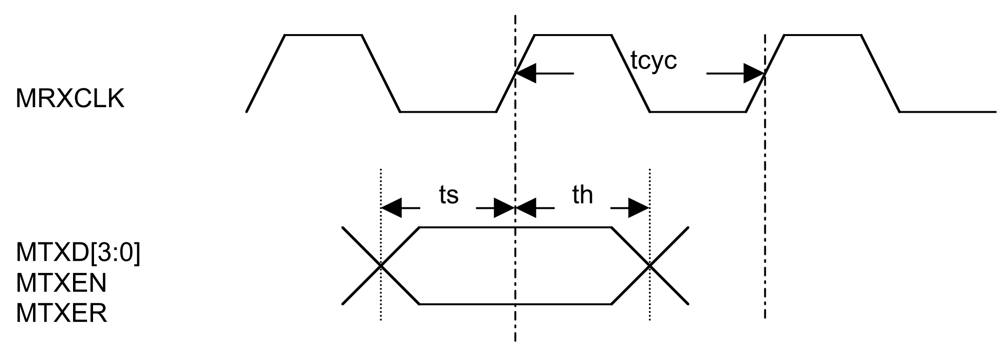


TABLE 7-7: KSZ8999 PHY MODE TRANSMIT TIMING PARAMETERS

Symbol	Parameters	Min.	Typ.	Max.	Units
t_{cyc}	Clock cycle (100BASE-TX)	—	40	—	ns
t_{cyc}	Clock cycle (10BASE-T)	—	400	—	ns
t_S	Set-up time	10	—	—	ns
t_H	Hold time	5	—	—	ns

FIGURE 7-11: KSZ8999 MAC MODE: DATA SENT FROM KSZ8999 MAC MODE TO EXT. PHY DEVICE

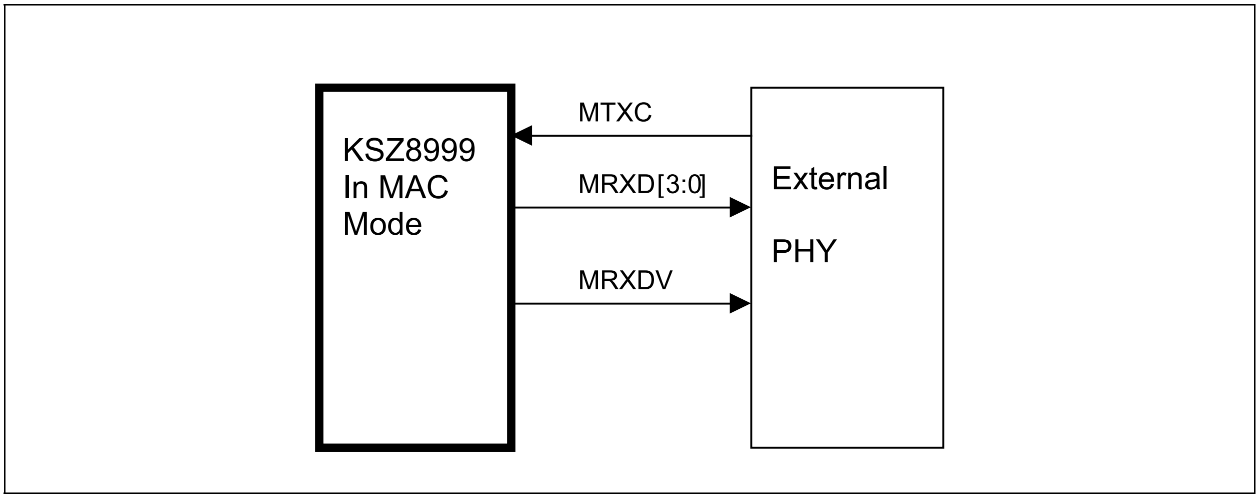


FIGURE 7-12: KSZ8999 MAC MODE TRANSMIT TIMING

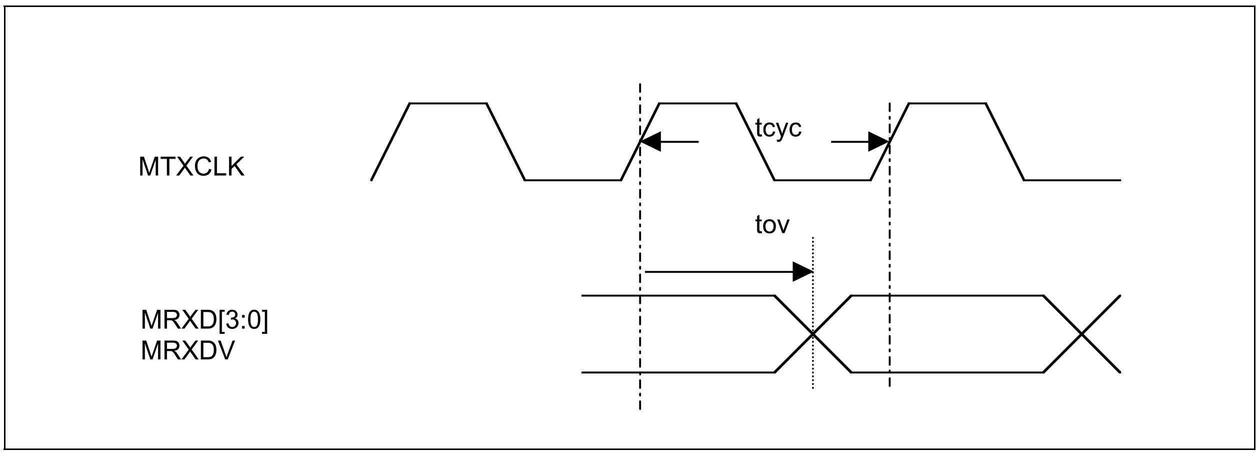


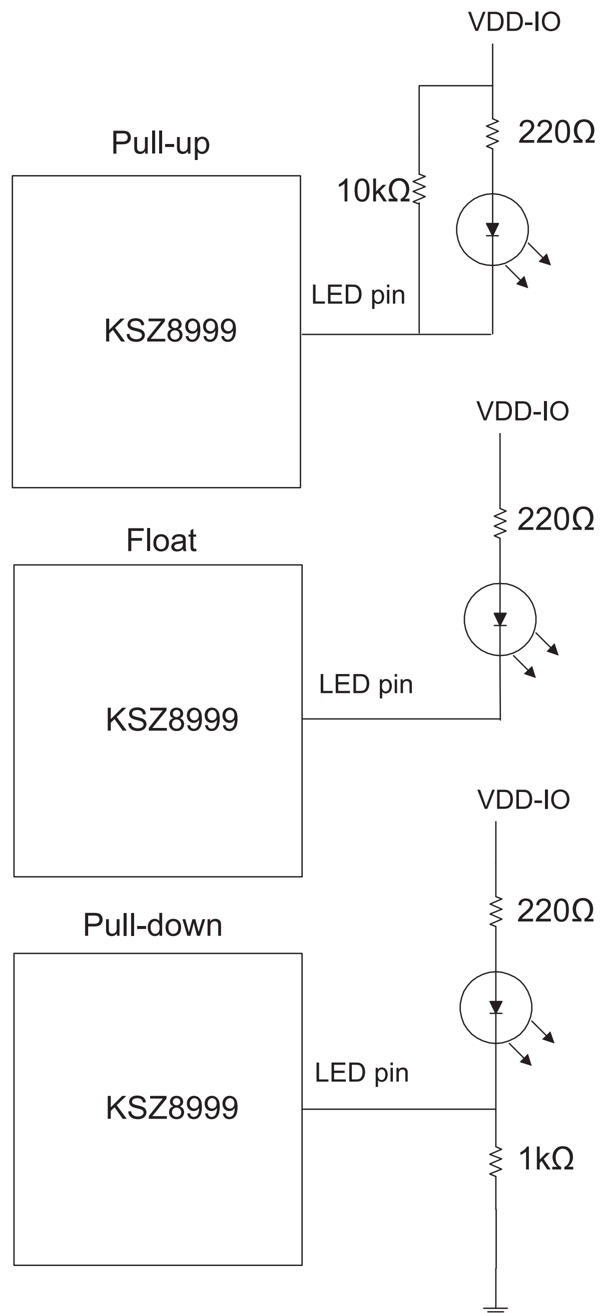
TABLE 7-8: KSZ8999 MAC MODE TRANSMIT TIMING PARAMETERS

Symbol	Parameters	Min.	Typ.	Max.	Units
t_{cyc}	Clock cycle (100BASE-TX)	—	40	—	ns
t_{cyc}	Clock cycle (10BASE-T)	—	400	—	ns
t_{OV}	Output valid	7	11	16	ns

8.0 REFERENCE CIRCUITS

See the "I/O Description" section for pull-up/pull-down and float information.

FIGURE 8-1: UNMANAGED PROGRAMMING CIRCUIT



Reference circuits for unmanaged programming through LED ports
Note: For brighter LED operation use VDD-IO = 3.3V

8.1 Reset Reference Circuit

Microchip recommended the following discrete reset circuit as shown in Figure 8-2 when powering up the KSZ8999 device. For the application where the reset circuit signal comes from another device (e.g., CPU, FPGA, etc), we recommend the reset circuit as shown in Figure 8-3.

FIGURE 8-2: RECOMMENDED RESET CIRCUIT

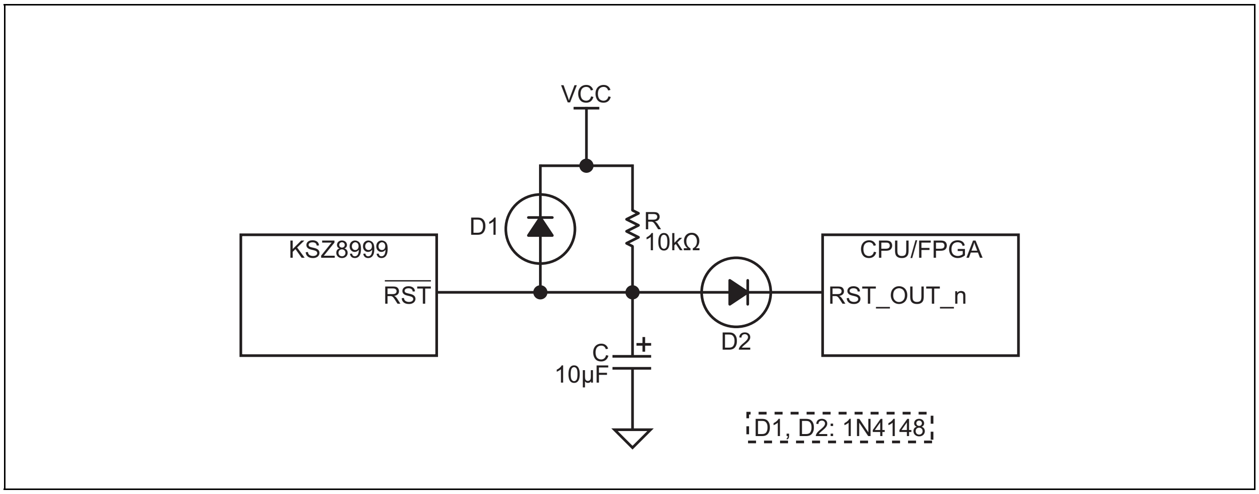
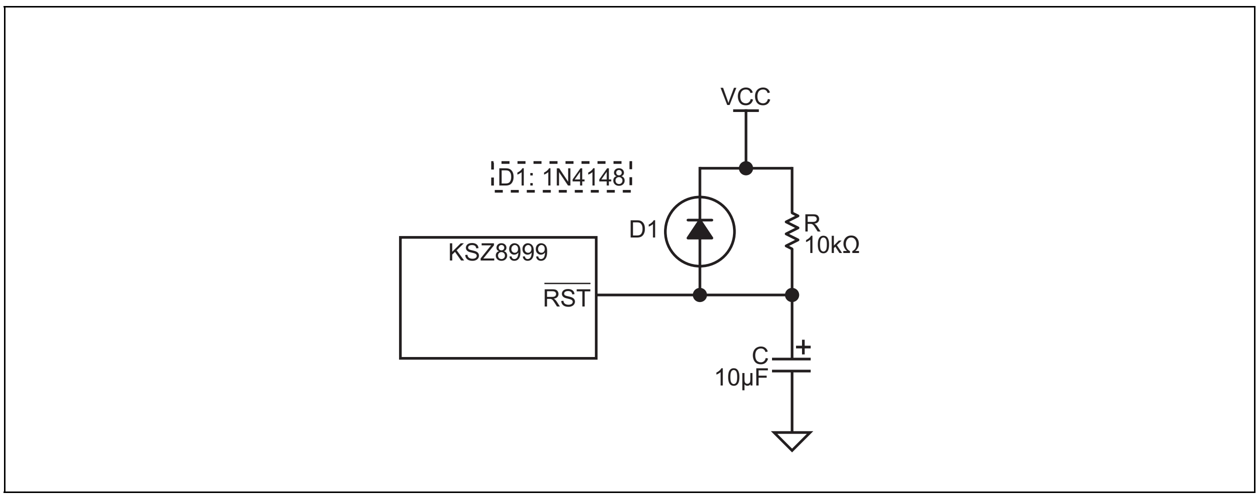


FIGURE 8-3: RECOMMENDED RESET CIRCUIT FOR INTERFACING WITH CPU/FPGA RESET



At power-on-reset, R, C, and D1 provide the necessary ramp rise time to reset the KSZ8999 device. The reset out from CPU/FPGA provides warm reset after power up. It is also recommended to power up the VDD core voltage earlier than VDDIO voltage. At worst case, the both VDD core and VDDIO voltages should come up at the same time.

9.0 CODING

9.1 4B/5B Coding

In 100BASE-TX and 100BASE-FX, the data and frame control are encoded in the transmitter (and decoded in the receiver) using a 4B/5B code. The extra code space is required to encode extra control (frame delineation) points. It is also used to reduce run length as well as supply sufficient transitions for clock recovery. The table below provides the translation for the 4B/5B coding.

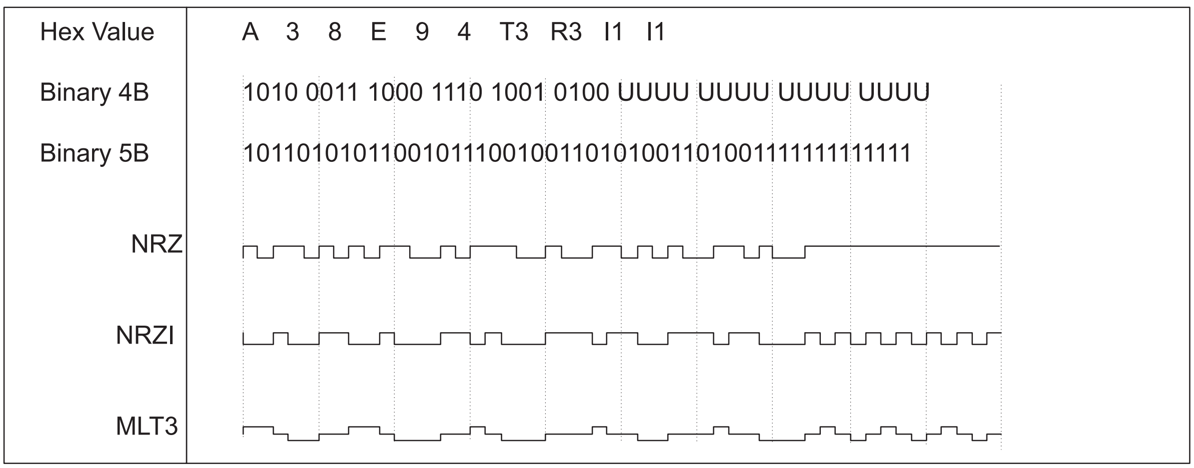
TABLE 9-1: 4B/5B CODING

Code Type	4B Code	5B Code	Value
Data	0000	11110	Data value 0
	0001	01001	Data value 1
	0010	10100	Data value 2
	0011	10101	Data value 3
	0100	01010	Data value 4
	0101	01011	Data value 5
	0110	01110	Data value 6
	0111	01111	Data value 7
	1000	10010	Data value 8
	1001	10011	Data value 9
	1010	10110	Data value A
	1011	10111	Data value B
	1100	11010	Data value C
	1101	11011	Data value D
	1110	11100	Data value E
	1111	11101	Data value F
Control	Not defined	11111	Idle
	0101	11000	Start delimiter part 1
	0101	10001	Start delimiter part 2
	Not defined	01101	End delimiter part 1
	Not defined	00111	End delimiter part 2
	Not defined	00100	Transmit error
Invalid	Not defined	00000	Invalid code
	Not defined	00001	Invalid code
	Not defined	00010	Invalid code
	Not defined	00011	Invalid code
	Not defined	00101	Invalid code
	Not defined	00110	Invalid code
	Not defined	01000	Invalid code
	Not defined	01100	Invalid code
	Not defined	10000	Invalid code
	Not defined	11001	Invalid code

9.2 MLT3 Coding

For 100BASE-TX operation, the NRZI (Non-Return to Zero Invert on ones) signal is line coded as MLT3. The net result of using MLT3 is to reduce the EMI (Electro Magnetic Interference) of the signal over twisted pair media. In NRZI coding, the level changes from high-to-low or low-to-high for every “1” bit. For a “0” bit, there is no transition. MLT3 line coding transitions through three distinct levels. For every transition of the NRZI signal, the MLT3 signal either increments or decrements depending on the current state of the signal. For instance, if the MLT3 level is at its lowest point, the next two NRZI transitions will change the MLT3 signal initially to the middle level followed by the highest level (second NRZI transition). On the next NRZI change, the MLT3 level will decrease to the middle level. On the following transition of the NRZI signal, the MLT3 level will move to the lowest level where the cycle repeats. The diagram below describes the level changes. Note that in the actual 100BASE-TX circuit there is a scrambling circuit and that scrambling is not shown in this diagram.

FIGURE 9-1: MLT3 CODING



9.3 MAC Frame

The MAC (Media Access Control) fields are described in the table below.

TABLE 9-2: MAC FRAME

Field	Octet Length	Description
Preamble/SFD	8	Preamble and Start of Frame Delimiter
DA	6	48-bit Destination MAC Address
SA	6	48-bit Source MAC Address
Length	2	Frame Length
Protocol/Data	46 to 1500	Higher Layer Protocol and Frame Data
Frame CRC	4	32-bit Cyclical Redundancy Check
ESD	1	End of Stream Delimiter
Idle	Variable	Inter Frame Idles

10.0 SELECTION OF ISOLATION TRANSFORMER

One simple 1:1 isolation transformer is needed at the line interface. An isolation transformer with integrated common-mode choke is recommended for exceeding FCC requirements. The following table gives recommended transformer characteristics.

TABLE 10-1: RECOMMENDED TRANSFORMER CHARACTERISTICS (Note 10-1)

Characteristic	Value	Test Condition
Turns Ratio	1 CT:1 CT	—
Open-Circuit Inductance (min.)	350 µH	100 mV, 100 kHz, 8 mA
Leakage Inductance (max.)	0.4 µH	1 MHz (min.)
Interwinding Capacitance (max.)	12 pF	—
DC Resistance (max.)	0.9Ω	—
Insertion Loss (max.)	1.0 dB	0 MHz to 65 MHz
HIPOT (max.)	$1500V_{RMS}$	—

Note 10-1 The IEEE 802.3u standard for 100BASE-TX assumes a transformer loss of 0.5 dB. For the transmit line transformer, insertion loss of up to 1.3 dB can be compensated by increasing the line drive current by means of reducing the ISET resistor value.

11.0 SELECTION OF REFERENCE OSCILLATOR/CRYSTAL

An oscillator or crystal with the following typical characteristics is recommended.

TABLE 11-1: TYPICAL OSCILLATOR/CRYSTAL CHARACTERISTICS

Characteristic	Value
Frequency	25 MHz
Maximum Frequency Tolerance	±50 ppm
Maximum Jitter	$150\ ps_{PP}$

The following transformer vendors provide compatible magnetic parts for Microchip’s device:

TABLE 11-2: TRANSFORMER VENDORS

4-Port Integrated		Auto MDIX	Number of Ports	Single Port		Auto MDIX	Number of Ports
Vendor	Part			Vendor	Part		
Pulse	H1164	Yes	4	Pulse	H1102	Yes	1
Bel Fuse	558-5999-Q9	Yes	4	Bel Fuse	S558-5999-U7	Yes	1
YCL	PH406466	Yes	4	YCL	PT163020	Yes	1
Transpower	HB826-2	Yes	4	Transpower	HB726	Yes	1
Delta	LF8731	Yes	4	Delta	LF8505	Yes	1

12.0 PACKAGE OUTLINE

12.1 Package Marking Information

208-Lead PQFP*	Example
XXXXXX XXXXXXX YYWWXX XXXXXXYYWWNNN WWLWXX ●	MICREL KSZ8999 2030A5 G000002030971 30L754 ●

Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	e3	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

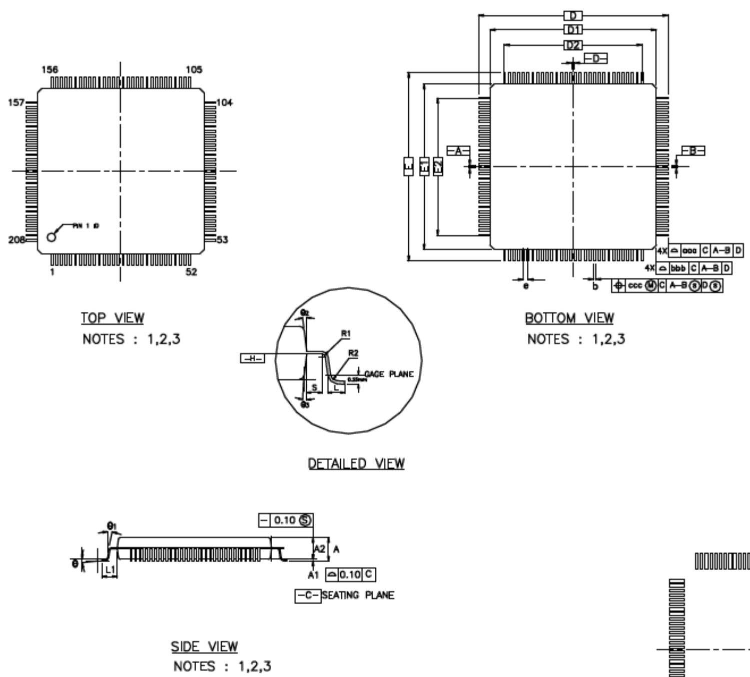
Underbar (_) and/or Overbar (‾) symbol may not be to scale.

FIGURE 12-1: 208-LEAD PQFP 28 MM X 28 MM PACKAGE OUTLINE AND RECOMMENDED LAND PATTERN

TITLE

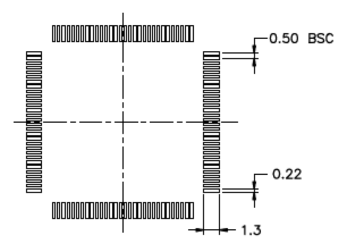
208 LEAD PQFP 28x28mm PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

DRAWING #	PQFP28x28-208LD-PL-1	**UNIT**	INCH



SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	4.10	—	—	0.161
A_1	0.25	—	—	0.010	—	—
A_2	3.20	3.32	3.60	0.126	0.131	0.142
D	31.20 BASIC			1.228 BASIC		
D_1	28.00 BASIC			1.102 BASIC		
E	31.20 BASIC			1.228 BASIC		
E_1	28.00 BASIC			1.102 BASIC		
R_2	0.13	—	0.30	0.005	—	0.012
R_1	0.13	—	—	0.005	—	—
θ	0°	—	7°	0°	—	7°
θ_1	0°	—	—	0°	—	—
θ_2	8° REF			8° REF		
θ_3	8° REF			8° REF		
c	0.11	0.15	0.23	0.004	0.006	0.009
L	0.73	0.88	1.03	0.029	0.035	0.041
L_1	1.60 REF			0.063 REF		
S	0.20	—	—	0.008	—	—
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BSC.			0.020 BSC.		
D2	25.50			1.004		
E2	25.50			1.004		
TOLERANCES OF FORM AND POSITION						
aaa	0.25			0.010		
bbb	0.20			0.008		
ccc	0.08			0.003		

COTROL DIMENSIONS ARE IN MILLIMETERS.



RECOMMENDED LAND PATTERN

NOTES : 4

NOTES :

1. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE −H− .
2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
3. THE DIAGRAMS DO NOT REPRESNET THE ACTUAL PIN COUNT.
4. LAND PATTERN UNIT IN MM. TOLERANCE +/− 0.05.

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

APPENDIX A: DATA SHEET REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision	Section/Figure/Entry	Correction
DS00003635A (09-15-20)	—	Converted Micrel data sheet KSZ8999 to Microchip DS00003635A. Minor text changes throughout.

THE MICROCHIP WEB SITE

Microchip provides online support via our WWW site at www.microchip.com. This web site is used as a means to make files and information easily available to customers. Accessible by using your favorite Internet browser, the web site contains the following information:

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- Technical Support

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Technical support is available through the web site at: http://microchip.com/support

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

Device	[X]	[-XX]
Part Number	Temperature	Media Type

Device:	KSZ8999: Integrated 9-Port 10/100 Switch with PHY and Frame Buffer
Temperature:	<blank> = 0°C to +70°C (Commercial) I = –40°C to +85°C (Industrial)
Media Type:	<blank> = 24/Tray

Examples:

a) KSZ8999: Integrated 9-Port 10/100 Switch with PHY and Frame Buffer, Commercial Temperature Range, 24/Tray

b) KSZ8999I: Integrated 9-Port 10/100 Switch with PHY and Frame Buffer, Industrial Temperature Range, 24/Tray

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods being used in attempts to breach the code protection features of the Microchip devices. We believe that these methods require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Attempts to breach these code protection features, most likely, cannot be accomplished without violating Microchip's intellectual property rights.
- Microchip is willing to work with any customer who is concerned about the integrity of its code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of its code. Code protection does not mean that we are guaranteeing the product is "unbreakable." Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

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