# PRODUCT/PROCESS CHANGE NOTIFICATION

PCN IPG-IPC/14/8789
Dated 21 Nov 2014

**VIPER16 : Metal mask change**

**Table 1. Change Implementation Schedule**

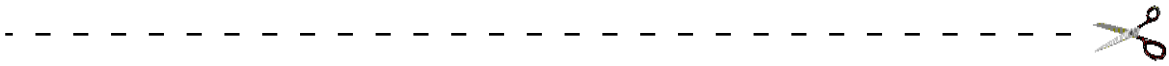
| | |
|---|---|
| Forecasted implementation date for change | 15-Feb-2015 |
| Forecasted availability date of samples for customer | 20-Dec-2014 |
| Forecasted date for **STMicroelectronics** change Qualification Plan results availability | 14-Nov-2014 |
| Estimated date of changed product first shipment | 15-Mar-2015 |

**Table 2. Change Identification**

| | |
|---|---|
| Product Identification (Product Family/Commercial Product) | See attached |
| Type of change | Product design change |
| Reason for change | To improve the device application performance |
| Description of the change | We have modified the enable logic port of the circuitry error amplifier in order to improve the ESD up to 8 kV and we have increased the UVLO value in order to enhance the performances during the repetitive test for turn-on and turn-off. |
| Change Product Identification | By a new Finished Goods code |
| Manufacturing Location(s) | |

**Table 3. List of Attachments**

| | |
|---|---|
| Customer Part numbers list | |
| Qualification Plan results | |



| Customer Acknowledgement of Receipt | **PCN IPG-IPC/14/8789** |
|---|---|
| Please sign and return to STMicroelectronics Sales Office | **Dated 21 Nov 2014** |

| | |
|---|---|
| ☐ Qualification Plan Denied | Name: |
| ☐ Qualification Plan Approved | Title: |
| | Company: |
| ☐ Change Denied | Date: |
| ☐ Change Approved | Signature: |

Remark

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# DOCUMENT APPROVAL

| Name | Function |
|---|---|
| Mercadante, Giacomo | Marketing Manager |
| Sandrini, Francesca Marta | Product Manager |
| Moretti, Paolo | Q.A. Manager |

**ATTACHMENT TO PCN IPD-IPC/14/8789**

**WHAT:**
A metal mask modification has been introduced on the controller UP40, belonging to the MV61 line of the VIPER16 products listed below.

We have modified the enable logic port of the circuitry error amplifier in order to improve the ESD up to 8 kV and we have increased the UVLO value in order to enhance the performances during the repetitive test for turn-on and turn-off.

**WHY*:***
The change has been made in order to improve the device application performance.

**HOW*:***
Please see the attached Reliability Report.

The new version of the VIPER16 will be identified by a new internal part number (Finished Goods), as follows:

| Commercial Product | Package | New Finished Goods |
|---|---|---|
| VIPER16HD (tube)<br>VIPER16HDTR (Tape & Reel)<br><br>VIPER16LD (tube)<br>VIPER16LDTR (Tape & Reel) | SO 16 | VIPER16HD-13/<br>VIPER16HDTR-13/<br><br>VIPER16LD-13/<br>VIPER16LDTR-13/ |
| VIPER16LN (tube)<br><br>VIPER16HN (tube) | PDIP 7 | VIPER16LN-39/<br><br>VIPER16HN-25/ |

**WHEN*:***
The production of the new products is planned to start middle of February 2015, depending on the material availability and customers' volumes. Phase-out and phase-in will be done accordingly.

Samples of the new version will be available from Dec 20$^{th}$ onwards.

# Reliability Report

| General Information | |
|---|---|
| **Product Line** | *MV61BE6 (VL8O6WT+UP40BE5)* |
| **Product Description** | *High Voltage Converter* |
| **Product division** | *I&PC* |
| **Package** | *PDIP7/SO16N* |
| **Silicon process technology** | *BCD6 (UP40) SUPERMESH (VL8Q)* |

| Locations | |
|---|---|
| **Wafer fab location** | *AMJ9 (VL8Q6WT) + CTM8 (UP40BE5)* |
| **Assembly plant location** | *ST-LONGGANG(CHINA) & UTAC THAI* |
| **Reliability assessment** | *Pass* |

## DOCUMENT HISTORY

| Version | Date | Pages | Author | Comment |
|---|---|---|---|---|
| 1.0 | 17-Jul-12 | 7 | G. D'Angelo | Original document |
| | | | | |
| | | | | |

Issued by

***Gianfranco D'Angelo***

Approved by

***Alceo Paratore***

# Table of Contents

# 1 APPLICABLE AND REFERENCE DOCUMENTS

| Document reference | Short description |
|---|---|
| **AEC-Q100** | : Stress test qualification for integrated circuits |
| **8161393A** | : General Specification For Product Development |

# 2 RELIABILITY EVALUATION OVERVIEW

## 2.1 Objectives

This report contains the reliability evaluation of MV61BE6 (VL8Q6WT+UP40BE5) device diffused in ANG MO KIO AMJ9 (VL8Q6WT) + CTM8 (UP40BE5) and assembled in PDIP7/SO16N in ST-LONGGANG(CHINA) & UTAC THAI.

Considering that UP40BE5 controller is a metal option of UP409BC5 controller, included in the already qualified MV61BCA (see Report RR004011CS2047) only a reduced set of trials has to be performed

According to Reliability Qualification Plan, below is the list of the trials performed:

*Die Oriented Tests*

- High Temperature Reverse Bias

## 2.2 Conclusion

Taking in account the results of the trials performed the MV61BE6 (VL8Q6WT+UP40BE5) diffused in ANG MO KIO AMJ9 (VL8Q6WT) + CTM8 (UP40BE5) and assembled in PDIP7 & SO16N in ST-LONGGANG(CHINA) & UTAC THAI can be qualified from reliability viewpoint.

## 2.3 Traceability

| Wafer fab information UP40 | |
|---|---|
| **Wafer fab manufacturing location** | *CATANIA* |
| **Wafer diameter** | *8 inches* |
| **Wafer thickness** | *375µm* |
| **Silicon process technology** | *BCD6 3M* |
| **Die finishing back side** | *RAW SILICON* |
| **Die size** | *1320x1112µm* |
| **Bond pad metallization layers** | *AlCu* |
| **Passivation** | *USG - SiN - PIX* |
| **Metal levels** | *3* |

| Wafer fab information VL8Q | |
|---|---|
| **Wafer fab manufacturing location** | *AMJ9* |
| **Wafer diameter** | *6 inches* |
| **Wafer thickness** | *280µm* |
| **Silicon process technology** | *SUPERMESH* |
| **Die finishing back side** | *Ti-Ni-Au* |
| **Die size** | *2650x1290µm* |
| **Bond pad metallization layers** | *AlSi* |
| **Passivation** | *SiN* |
| **Metal levels** | *1* |

| Assembly Information | |
|---|---|
| **Assembly plant location** | *ST-LONGGANG -CHINA* |
| **Package description** | *PDIP 7* |
| **Molding compound** | *Hysol GR360A-ST* |
| **Wires bonding materials/diameters** | *Au/1mil* |
| **Die attach material** | *Ablestik 8390S* |

| Assembly Information | |
|---|---|
| **Assembly plant location** | *UTAC Thai Limited* |
| **Package description** | *SO16N* |
| **Die pad size** | *Dual Die Pads 2.83x3.4mm – 1.8x1.8mm* |
| **Molding compound** | *Sumitomo G605* |
| **Wires bonding materials/diameters** | *Au/1mil* |
| **Die attach material** | *Ablebond 8200T* |
| **Lead solder material** | *Ni/Pd/Au PPF* |

# 3 TESTS RESULTS SUMMARY

## 3.1 Test plan and results summary

| Die Oriented Tests (on PDIP7) | | | | | | | |
|---|---|---|---|---|---|---|---|
| Test | Method | Conditions | Failure/SS | | | Duration | Note |
| | | | Lot 1(a) | Lot 2(b) | Lot 3(b) | | |
| HTRB | High Temperature Reverse Bias | | | | | | |
| | | Tj=150°C<br>Vdrain=800V, Vdd=22V | 0/77 | - | - | 168h | |

# 4 TESTS DESCRIPTION & DETAILED RESULTS

## 4.1 Die oriented tests

### 4.1.1 High Temperature Reverse Bias

This test is performed to evaluate die problems related with chip stability, layout structure, surface contamination and oxide faults.

The flow chart is the following:

- Initial testing @ Ta=25°C
- Final Testing @ 168hrs @ Ta=25°C

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