

LITIX™ Power

TLD5098EL - Multitopology LITIX™ Power DC/DC Controller IC



1 Overview

Description

The TLD5098EL is a flexibly usable DC/DC boost controller with built in diagnosis and protection features especially designed to drive LEDs.

It is designed to support fixed current and fixed voltage configurations in multiple topologies such as Boost, Buck, Buck-Boost, SEPIC and Flyback by simply adjusting the external components. The TLD5098EL drives a low side n-channel power MOSFET from an internal 5 V linear regulator. The switching frequency is adjustable in the range from 100 kHz to 500 kHz and can also be synchronized to an external clock source.

The TLD5098EL can be flexibly dimmed by means of analog and PWM dimming; an enable function reduces the shut-down current consumption to $I_{Q_OFF} < 10 \mu A$.

The current mode control scheme of this device provides a stable regulation loop maintained by small external compensation components. Additionally an integrated soft start feature limits the current peak as well as voltage overshoot at start-up. This IC is suited for use in the harsh automotive environments.

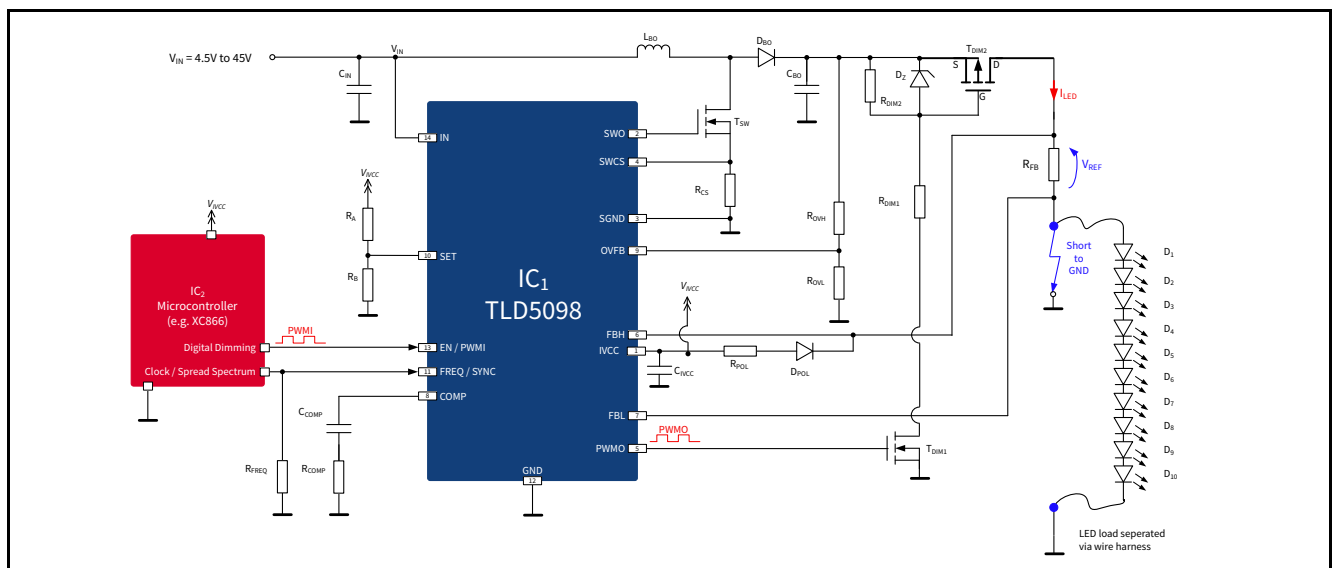
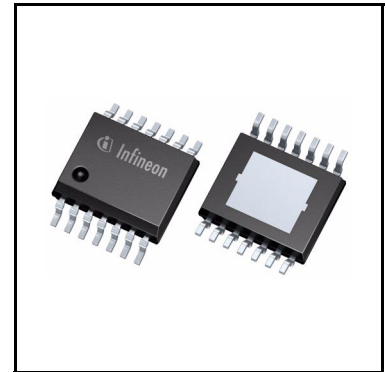


Figure 1 Typical application: Boost LED driver with short circuit protection circuitry

| Type | Package | Marking |
|-----------|--------------|---------|
| TLD5098EL | PG-SSOP-14-3 | TLD5098 |

Potential applications

Potential applications

- Automotive exterior and interior lighting
- General illumination
- General purpose current/voltage controlled DC/DC driver

Features

- Fixed current or fixed voltage configuration in Boost, Buck, Buck-Boost, SEPIC and Flyback topology
- Drives low-side external n-Channel switching MOSFET from internal 5 V voltage regulator
- Flexible switching frequency range, 100 kHz to 500 kHz or synchronization with external clock source
- Wide input voltage range from 4.5 V to 45 V
- Enable & PWM function with very low shutdown current: $I_{Q_OFF} < 10 \mu A$ and internal start-up
- Analog dimming and PWM dimming feature to adjust average LED current
- PWMO Gate driver for PWM dimming and output disconnection
- Integrated protection and diagnostic functions
- 300 mV high-side current sense
- Available in a small thermally enhanced 14-pin PG-SSOP-14-3 package (RoHS compliant)

Table 1 Product summary

| Feature | Symbol | Range |
|---|------------------|--|
| Nominal supply voltage range | V_{IN} | 8 V ... 34 V |
| Extended supply voltage range | V_{IN} | 4.5 V ... 45 V $V_{IVCC} > V_{IVCC,RTH,d}$; parameter deviations possible |
| Switching frequency range | f_{FREQ} | 100 kHz ... 500 kHz oscillator frequency adjustment range 250 kHz ... 500 kHz synchronization frequency capture range |
| Maximum duty cycle | $D_{max,fixed}$ | 91% ...95% fixed frequency mode |
| | $D_{max,synced}$ | 88% synchronization mode |
| Typical gate driver peak sourcing current | $I_{SWO,src}$ | 380 mA |
| Typical gate driver peak sinking current | $I_{SWO,snk}$ | 550 mA |

Protection and diagnostic functions

- Open circuit detection
- Output overvoltage protection
- Short to GND protection
- Overtemperature shutdown
- Electrostatic discharge (ESD) protection

Product validation

Qualified for automotive applications. Product validation according to AEC-Q100/101.

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Block diagram

2 Block diagram

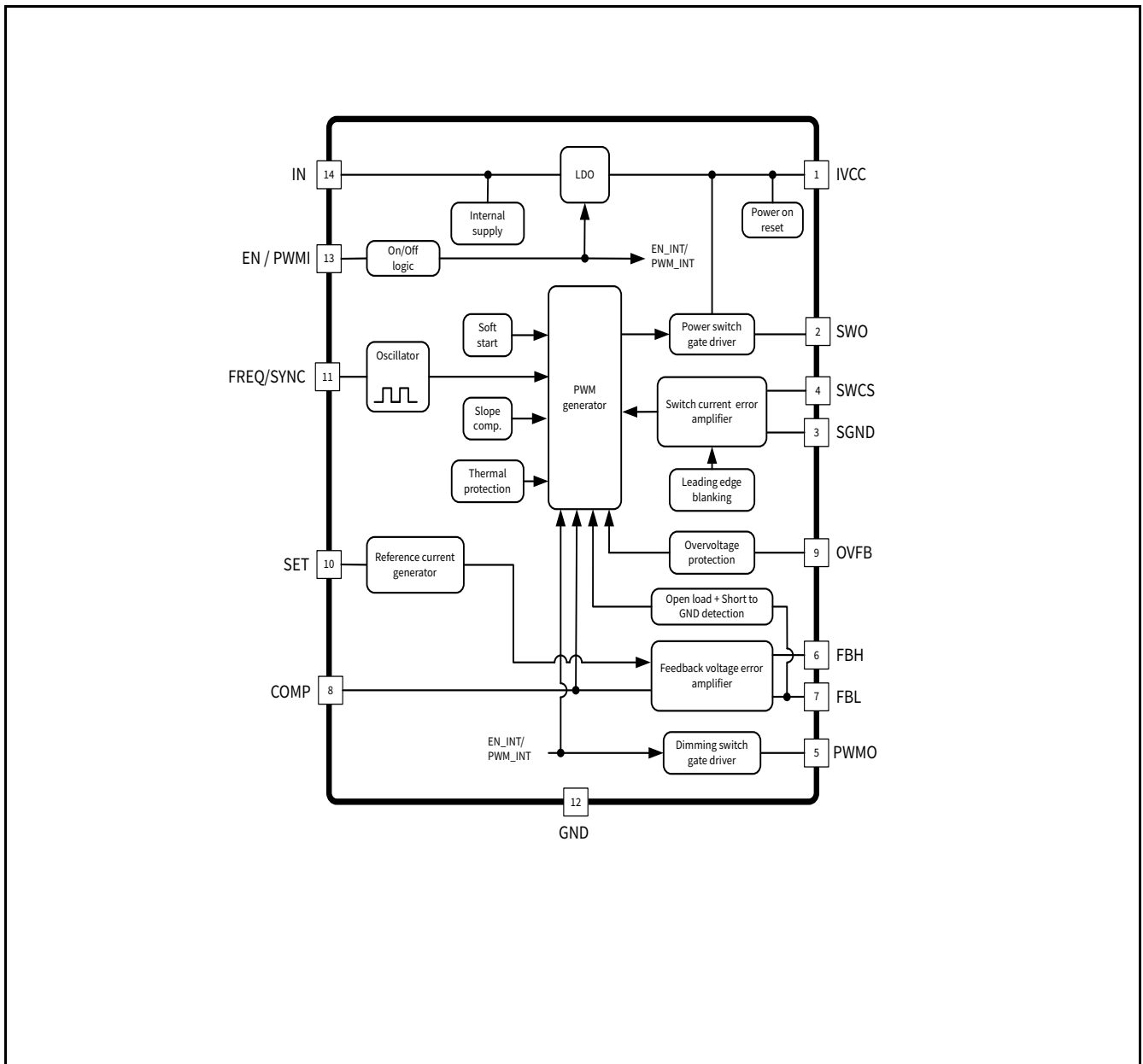


Figure 2 Block diagram TLD5098EL

Pin configuration

3 Pin configuration

3.1 Pin assignment

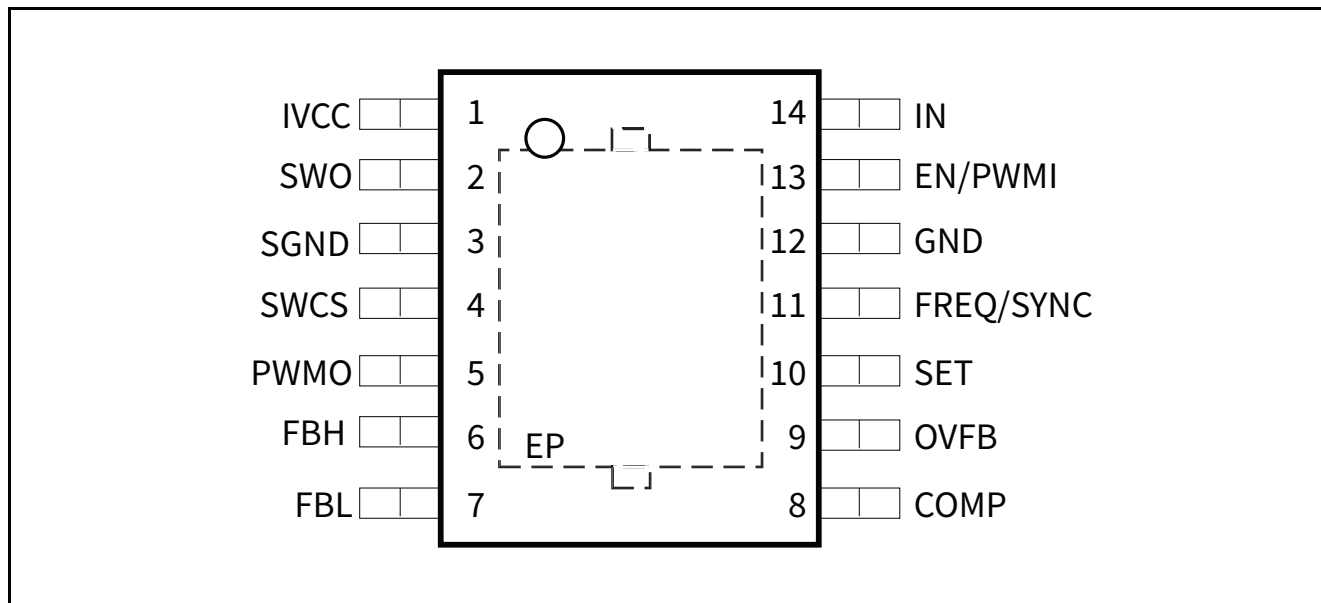


Figure 3 Pin configuration TLD5098EL

3.2 Pin definitions and functions

Table 2 Pin definition and function

| # | Symbol | Direction | Function |
|---|--------|-----------|--|
| 1 | IVCC | Output | Internal LDO Used for internal biasing and gate drive. Bypass with external capacitor. Pin must not be left open |
| 2 | SWO | Output | Switch gate driver Connect to gate of external switching MOSFET |
| 3 | SGND | - | Current Sense Ground Ground return for switch current sense |
| 4 | SWCS | Input | Current Sense Detects the peak current through switch |
| 5 | PWMO | Output | PWM Dimming Connect to gate of external MOSFET |
| 6 | FBH | Input | Voltage Feedback Positive Non inverting Input (+) |
| 7 | FBL | Input | Voltage Feedback Negative Inverting Input (-) |
| 8 | COMP | Input | Compensation Connect R and C network to pin for stability |

Pin configuration

Table 2 Pin definition and function

| # | Symbol | Direction | Function |
|----|-------------|-----------|---|
| 9 | OVFB | Input | Overvoltage Protection Feedback Connect to resistive voltage divider to set overvoltage threshold |
| 10 | SET | Input | Analog Dimming Load current adjustment Pin. Pin must not be left open. If analog dimming feature is not used connect to IVCC pin |
| 11 | FREQ / SYNC | Input | Frequency Select or Synchronization Connect external resistor to GND to set frequency. Or apply external clock signal for synchronization within frequency capture range |
| 12 | GND | – | Ground Connect to system ground |
| 13 | EN / PWMI | Input | Enable or PWM Apply logic HIGH signal to enable device or PWM signal for dimming LED |
| 14 | IN | Input | Supply Input Supply for internal biasing |
| | EP | – | Exposed Pad Connect to external heat spreading GND Cu area (e.g. inner GND layer of multilayer PCB with thermal vias) |

General product characteristics

4 General product characteristics

4.1 Absolute maximum ratings

$T_J = -40^{\circ}\text{C}$ to $+150^{\circ}\text{C}$; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Table 3 Absolute maximum ratings¹⁾

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|--|--------------------|--------|------|------|------|---|----------|
| | | Min. | Typ. | Max. | | | |
| Voltage | | | | | | | |
| IN Supply input | V_{IN} | -0.3 | | 45 | V | | P_4.1.1 |
| EN / PWMI Enable or PWM input | V_{EN} | -40 | | 45 | V | | P_4.1.2 |
| FBH-FBL; Feedback Error Amplifier Differential | $V_{FBH}-V_{FBL}$ | -40 | | 61 | V | The maximum delta must not exceed 61 V. Differential signal (not referred to GND) | P_4.1.3 |
| FBH; Feedback error amplifier positive input | V_{FBH} | -40 | | 61 | V | The difference between V_{FBH} and V_{FBL} must not exceed 61 V, refer to P_4.1.3 | P_4.1.4 |
| FBL Feedback error amplifier negative input | V_{FBL} | -40 | | 61 | V | The difference between V_{FBH} and V_{FBL} must not exceed 61 V, refer to P_4.1.3 | P_4.1.5 |
| FBH and FBL current | I_{FBL}, I_{FBH} | | 1 | | mA | $t < 100$ ms, $V_{FBH}-V_{FBL} = 0.3$ V | P_4.1.6 |
| OVFB Overvoltage feedback input | V_{OVP} | -0.3 | | 5.5 | V | | P_4.1.7 |
| OVFB Overvoltage feedback input | V_{OVP} | -0.3 | | 6.2 | V | $t < 10$ s | P_4.1.8 |
| SWCS Switch current sense input | V_{SWCS} | -0.3 | | 5.5 | V | | P_4.1.9 |
| SWCS Switch current sense input | V_{SWCS} | -0.3 | | 6.2 | V | $t < 10$ s | P_4.1.10 |
| SWO Switch gate drive output | V_{SWO} | -0.3 | | 5.5 | V | | P_4.1.11 |

General product characteristics

Table 3 Absolute maximum ratings¹⁾

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|-----------------------|--------|------|------|------|------------------------|----------|
| | | Min. | Typ. | Max. | | | |
| SWO Switch gate drive output | V_{SWO} | -0.3 | | 6.2 | V | t < 10 s | P_4.1.12 |
| SGND Current sense switch GND | V_{SGND} | -0.3 | | 0.3 | V | | P_4.1.13 |
| COMP Compensation input | V_{COMP} | -0.3 | | 5.5 | V | | P_4.1.14 |
| COMP Compensation input | V_{COMP} | -0.3 | | 6.2 | V | t < 10 s | P_4.1.15 |
| FREQ / SYNC; Frequency and synchronization input | V_{FREQ} / V_{SYNC} | -0.3 | | 5.5 | V | | P_4.1.16 |
| FREQ / SYNC; Frequency and synchronization input | V_{FREQ} / V_{SYNC} | -0.3 | | 6.2 | V | t < 10 s | P_4.1.17 |
| PWMO PWM dimming output | V_{PWMO} | -0.3 | | 5.5 | V | | P_4.1.18 |
| PWMO PWM dimming output | V_{PWMO} | -0.3 | | 6.2 | V | t < 10 s | P_4.1.19 |
| SET | V_{SET} | -0.3 | | 45 | V | | P_4.1.20 |
| IVCC Internal linear voltage regulator output | V_{IVCC} | -0.3 | | 5.5 | V | | P_4.1.21 |
| IVCC Internal linear voltage regulator output | V_{IVCC} | -0.3 | | 6.2 | V | t < 10 s | P_4.1.22 |
| Temperature | | | | | | | |
| Junction temperature | T_J | -40 | | 150 | °C | | P_4.1.23 |
| Storage temperature | T_{stg} | -55 | | 150 | °C | | P_4.1.24 |
| ESD Susceptibility | | | | | | | |
| ESD resistivity of all pins | $V_{ESD,HBM}$ | -2 | | 2 | kV | HBM ²⁾ | P_4.1.25 |
| ESD resistivity of IN, EN/PWMI, FBH, FBL and SET pin to GND | $V_{ESD,HBM}$ | -4 | | 4 | kV | HBM ²⁾³⁾ | P_4.1.26 |

1) Not subject to production test, specified by design.

2) ESD susceptibility, Human Body Model “HBM” according to ANSI/ESDA/JEDEC JS-001 (1.5 kΩ, 100 pF)

3) ESD susceptibility, Charged Device Model “CDM” EIA/JESD22-C101 or ESDA STM5.3.1

Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

General product characteristics

1. Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.

4.2 Functional range

Table 4 Functional range

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|-------------------------------|--------------------|--------|------|------|------|---|---------|
| | | Min. | Typ. | Max. | | | |
| Extended supply voltage range | V_{IN} | 4.5 | – | 45 | V | ¹⁾ $V_{IVCC} > V_{IVCC,RTH,d}$; parameter deviations possible | P_4.2.1 |
| Nominal supply voltage range | V_{IN} | 8 | – | 34 | V | – | P_4.2.2 |
| Feedback voltage input | $V_{FBH}; V_{FBL}$ | 3 | – | 60 | V | – | P_4.2.3 |
| Junction temperature | T_J | -40 | – | 150 | °C | – | P_4.2.4 |

1) Not subject to production test, specified by design

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

4.3 Thermal resistance

Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For further information visit <https://www.jedec.org>

Table 5 Thermal resistance

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---------------------|------------|--------|------|------|------|--|---------|
| | | Min. | Typ. | Max. | | | |
| Junction to Case | R_{thJC} | – | 10 | – | K/W | ¹⁾²⁾ | P_4.3.1 |
| Junction to Ambient | R_{thJA} | – | 47 | – | K/W | ¹⁾³⁾ 2s2p | P_4.3.2 |
| Junction to Ambient | R_{thJA} | – | 54 | – | K/W | ¹⁾³⁾ 1s0p + 600 mm ² | P_4.3.3 |
| Junction to Ambient | R_{thJA} | – | 64 | – | K/W | ¹⁾³⁾ 1s0p + 300 mm ² | P_4.3.4 |

1) Not subject to production test, specified by design

2) Specified R_{thJC} value is simulated at natural convection on a cold plate setup (all pins and the exposed pad are fixed to ambient temperature). $T_A = 25^\circ\text{C}$ dissipates 1 W

3) Specified R_{thJA} value is according to JEDEC 2s2p (JESD 51-7) + (JESD 51-5) and JEDEC 1s0p (JESD 51-3) + heatsink area at natural convection on FR4 board; The device was simulated on a 76.2 x 114.3 x 1.5 mm board. The 2s2p board has 2 outer copper layers (2 x 70 μm Cu) and 2 inner copper layers (2 x 35 μm Cu), A thermal via (diameter = 0.3 mm and 25 μm plating) array was applied under the exposed pad and connected the first outer layer (top) to the first inner layer and second outer layer (bottom) of the JEDEC PCB. $T_A = 25^\circ\text{C}$, IC dissipates 1W

Switching regulator

5 Switching regulator

5.1 Description

The TLD5098EL regulator is suitable for Boost, Buck, Buck-Boost, SEPIC and Flyback configurations. The constant output current is especially useful for light emitting diode (LED) applications. The switching regulator function is implemented by a pulse width modulated (PWM) current mode controller.

The PWM current mode controller uses the peak current through the external power switch and error in the output current to determine the appropriate pulse width duty cycle (on time) for constant output current. The current mode controller provides a PWM signal to an internal gate driver which then outputs to an external n-channel enhancement mode metal oxide field effect transistor (MOSFET) power switch.

The current mode controller also has built-in slope compensation to prevent sub-harmonic oscillations which is a characteristic of current mode controllers operating at high duty cycles (>50% duty).

An additional built-in feature is an integrated soft start that limits the current through the inductor and external power switch during initialization. The soft start function gradually increases the inductor and switch current over t_{SS} (P_5.2.9) to minimize potential overvoltage at the output.

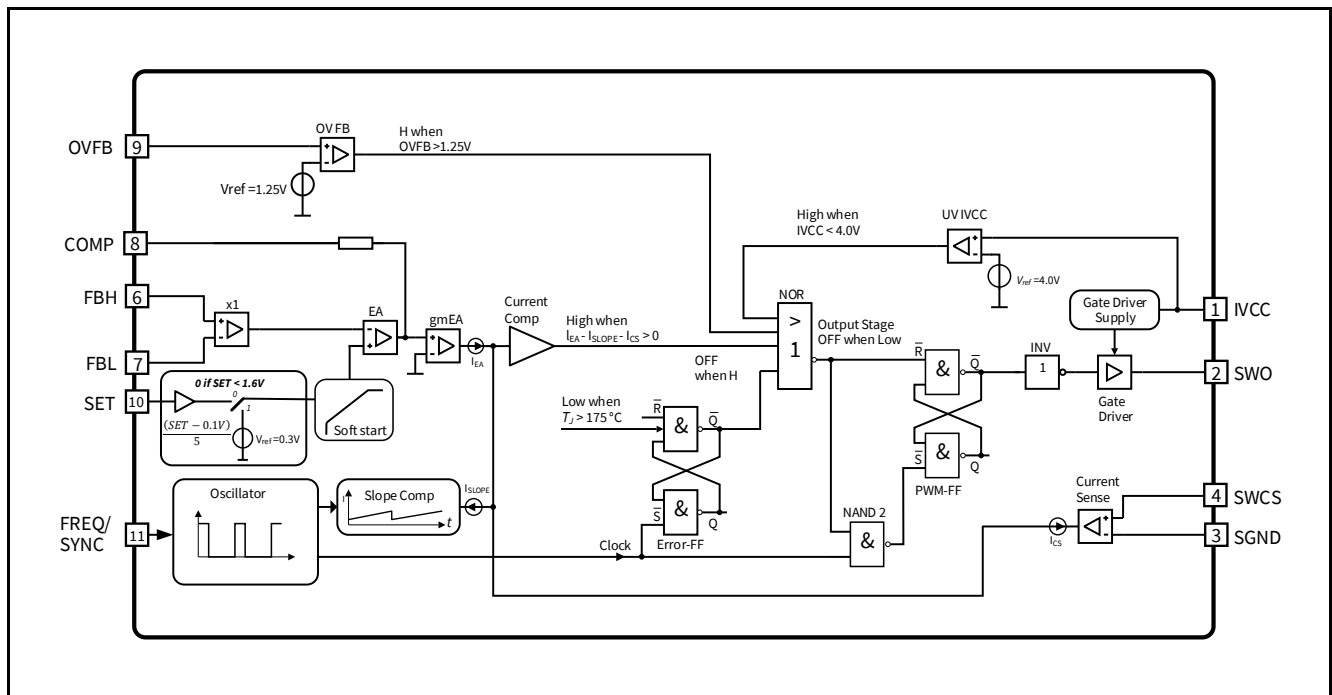


Figure 4 Switching regulator block diagram

Switching regulator

5.2 Electrical characteristics

$V_{IN} = 8\text{ V to }34\text{ V}$; $T_J = -40^\circ\text{C to }+150^\circ\text{C}$, all voltages with respect to ground, positive current flowing into pin; (unless otherwise specified)

Table 6 Electrical characteristics: Switching regulator

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|-------------------------------------|--|--------|------|-------|---------------|---|----------|
| | | Min. | Typ. | Max. | | | |
| Regulator | | | | | | | |
| Feedback reference voltage | V_{REF} | 0.29 | 0.30 | 0.31 | V | refer to Figure 30 $V_{REF} = V_{FBH} - V_{FBL}$ $V_{SET} = 5\text{ V}$ $I_{LED} = 350\text{ mA}$ | P_5.2.1 |
| Feedback reference voltage | V_{REF} | 0.057 | 0.06 | 0.063 | V | refer to Figure 30 $V_{REF} = V_{FBH} - V_{FBL}$ $V_{SET} = 0.4\text{ V}$ $I_{LED} = 70\text{ mA}$ | P_5.2.2 |
| Feedback reference voltage offset | V_{REF_offset} | – | – | 5 | mV | refer to Figure 18 and Figure 30 $V_{REF} = V_{FBH} - V_{FBL}$ $V_{SET} = 0.1\text{ V}$ $V_{OUT} > V_{IN}$ | P_5.2.3 |
| Voltage line regulation | $(\Delta V_{REF}/V_{REF}) / \Delta V_{IN}$ | – | – | 0.15 | %/V | refer to Figure 30 $V_{IN} = 8\text{ V to }19\text{ V}$; $V_{SET} = 5\text{ V}$; $I_{LED} = 350\text{ mA}$ | P_5.2.4 |
| Voltage load regulation | $(\Delta V_{REF}/V_{REF}) / \Delta I_{BO}$ | – | – | 5 | %/A | refer to Figure 30 $V_{SET} = 5\text{ V}$; $I_{LED} = 100\text{ to }500\text{ mA}$ | P_5.2.5 |
| Switch peak over-current threshold | V_{SWCS} | 130 | 150 | 170 | mV | $V_{FB} = V_{FBL} = 5\text{ V}$ $V_{COMP} = 3.5\text{ V}$ | P_5.2.6 |
| Maximum duty cycle | $D_{MAX, fixed}$ | 91 | 93 | 95 | % | Fixed frequency mode | P_5.2.7 |
| Maximum duty cycle | $D_{MAX, sync}$ | 88 | – | – | % | Synchronization mode | P_5.2.8 |
| Soft start ramp | t_{SS} | 350 | 1000 | 1500 | μs | V_{FBH} rising from 5% to 95% of V_{FB} , typ. | P_5.2.9 |
| IFBH Feedback high input current | I_{FBH} | 38 | 46 | 54 | μA | $V_{FBH} - V_{FBL} = 0.3\text{ V}$ | P_5.2.10 |
| IFBL Feedback low input current | I_{FBL} | 15 | 21 | 27 | μA | $V_{FBH} - V_{FBL} = 0.3\text{ V}$ | P_5.2.11 |
| Switch current sense input current | I_{SWCS} | 10 | 50 | 100 | μA | $V_{SWCS} = 150\text{ mV}$ | P_5.2.12 |

Switching regulator

Table 6 Electrical characteristics: Switching regulator

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|-----------------------------|--------------|--------|------|------|------|------------------------|----------|
| | | Min. | Typ. | Max. | | | |
| Input undervoltage shutdown | $V_{IN,off}$ | 3.5 | – | 4.5 | V | V_{IN} decreasing | P_5.2.13 |
| Input voltage startup | $V_{IN,on}$ | – | – | 4.85 | V | V_{IN} increasing | P_5.2.14 |

Gate driver for external switch

| | | | | | | | |
|-----------------------------------|---------------|-----|-----|-----|----|---|----------|
| Gate driver peak sourcing current | $I_{SWO,src}$ | – | 380 | – | mA | ¹⁾ $V_{SWO} = 1\text{ V to }4\text{ V}$ | P_5.2.15 |
| Gate driver peak sinking current | $I_{SWO,snk}$ | – | 550 | – | mA | ¹⁾ $V_{SWO} = 4\text{ V to }1\text{ V}$ | P_5.2.16 |
| Gate driver output rise time | $t_{R,SWO}$ | – | 30 | 60 | ns | ¹⁾ $C_{GATE} = 3.3\text{ nF};$ $V_{SWO} = 1\text{ V to }4\text{ V}$ | P_5.2.17 |
| Gate driver output fall time | $t_{F,SWO}$ | – | 20 | 40 | ns | ¹⁾ $C_{GATE} = 3.3\text{ nF};$ $V_{SWO} = 4\text{ V to }1\text{ V}$ | P_5.2.18 |
| Gate driver output voltage | V_{SWO} | 4.5 | – | 5.5 | V | ¹⁾ $C_{GATE} = 3.3\text{ nF}$ | P_5.2.19 |

1) Not subject to production test, specified by design

6 Oscillator and synchronization

6.1 Description

R_{freq} vs. switching frequency

The internal oscillator is used to determine the switching frequency of the boost regulator. The switching frequency can be selected from 100 kHz to 500 kHz with an external resistor to GND. To set the switching frequency with an external resistor the following formula can be applied.

$$R_{FREQ} = \frac{1}{(141 \cdot 10^{-12} \left[\frac{s}{\Omega} \right]) \cdot \left(f_{FREQ} \left[\frac{1}{s} \right] \right)} - (3.5 \cdot 10^3 [\Omega]) [\Omega] \tag{6.1}$$

In addition, the oscillator is capable of changing from the frequency set by the external resistor to a synchronized frequency from an external clock source. If an external clock source is provided on the pin FREQ/SYNC, then the internal oscillator synchronizes to this external clock frequency and the boost regulator switches at the synchronized frequency. The synchronization frequency capture range is 250 kHz to 500 kHz.

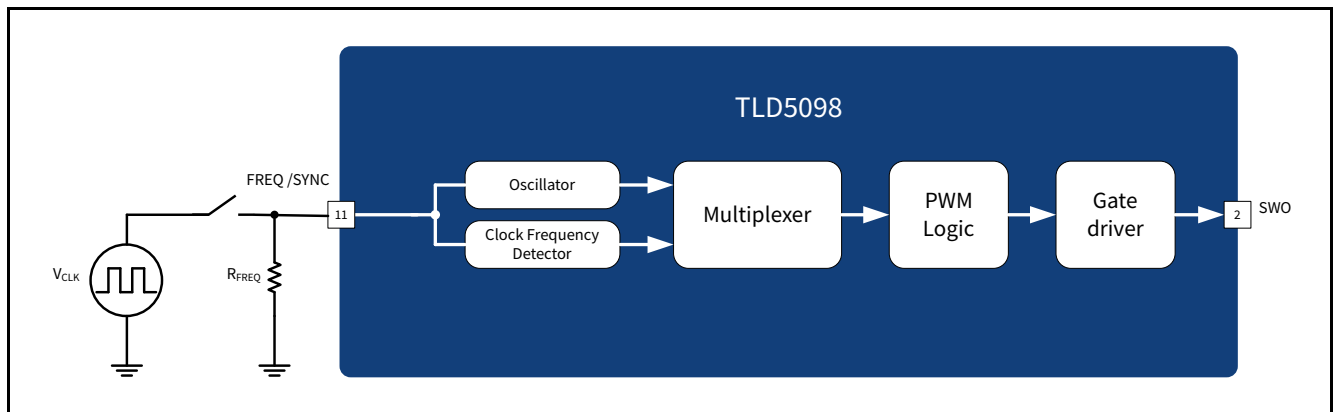


Figure 5 Oscillator and synchronization block diagram and simplified application circuit

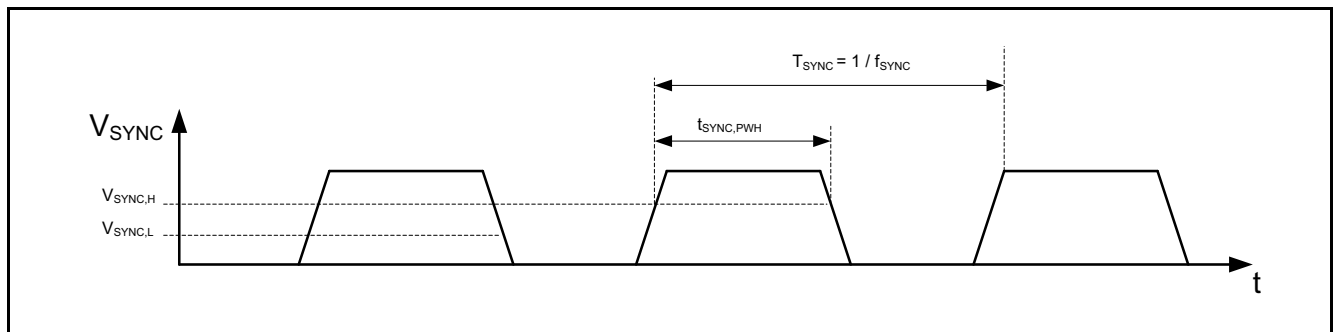


Figure 6 Synchronization timing diagram

Oscillator and synchronization

6.2 Electrical characteristics

$V_{IN} = 8\text{ V to }34\text{ V}$, $T_J = -40^\circ\text{C to }+150^\circ\text{C}$, all voltages with respect to ground, positive current flowing into pin; (unless otherwise specified)

Table 7 Electrical characteristics: Oscillator and synchronization

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|----------------|--------|------|------|---------------|--------------------------------|---------|
| | | Min. | Typ. | Max. | | | |
| Oscillator | | | | | | | |
| Oscillator frequency | f_{FREQ} | 250 | 300 | 350 | kHz | $R_{FREQ} = 20\text{ k}\Omega$ | P_6.2.1 |
| Oscillator frequency adjustment range | f_{FREQ} | 100 | – | 500 | kHz | | P_6.2.2 |
| FREQ / SYNC supply current | I_{FREQ} | – | – | -700 | μA | $V_{FREQ} = 0\text{ V}$ | P_6.2.3 |
| Frequency voltage | V_{FREQ} | 1.16 | 1.24 | 1.32 | V | $f_{FREQ} = 100\text{ kHz}$ | P_6.2.4 |
| Synchronization | | | | | | | |
| Synchronization frequency capture range | f_{SYNC} | 250 | – | 500 | kHz | | P_6.2.5 |
| Synchronization signal high logic level valid | $V_{SYNC,H}$ | 3.0 | – | – | V | ¹⁾²⁾ | P_6.2.6 |
| Synchronization signal low logic level valid | $V_{SYNC,L}$ | – | – | 0.8 | V | ¹⁾²⁾ | P_6.2.7 |
| Synchronization signal logic high pulse width | $t_{SYNC,PWH}$ | 200 | – | – | ns | ¹⁾²⁾ | P_6.2.8 |

1) Synchronization of external PWM ON signal to falling edge

2) Not subject to production test, specified by design

6.3 Typical performance characteristics of oscillator

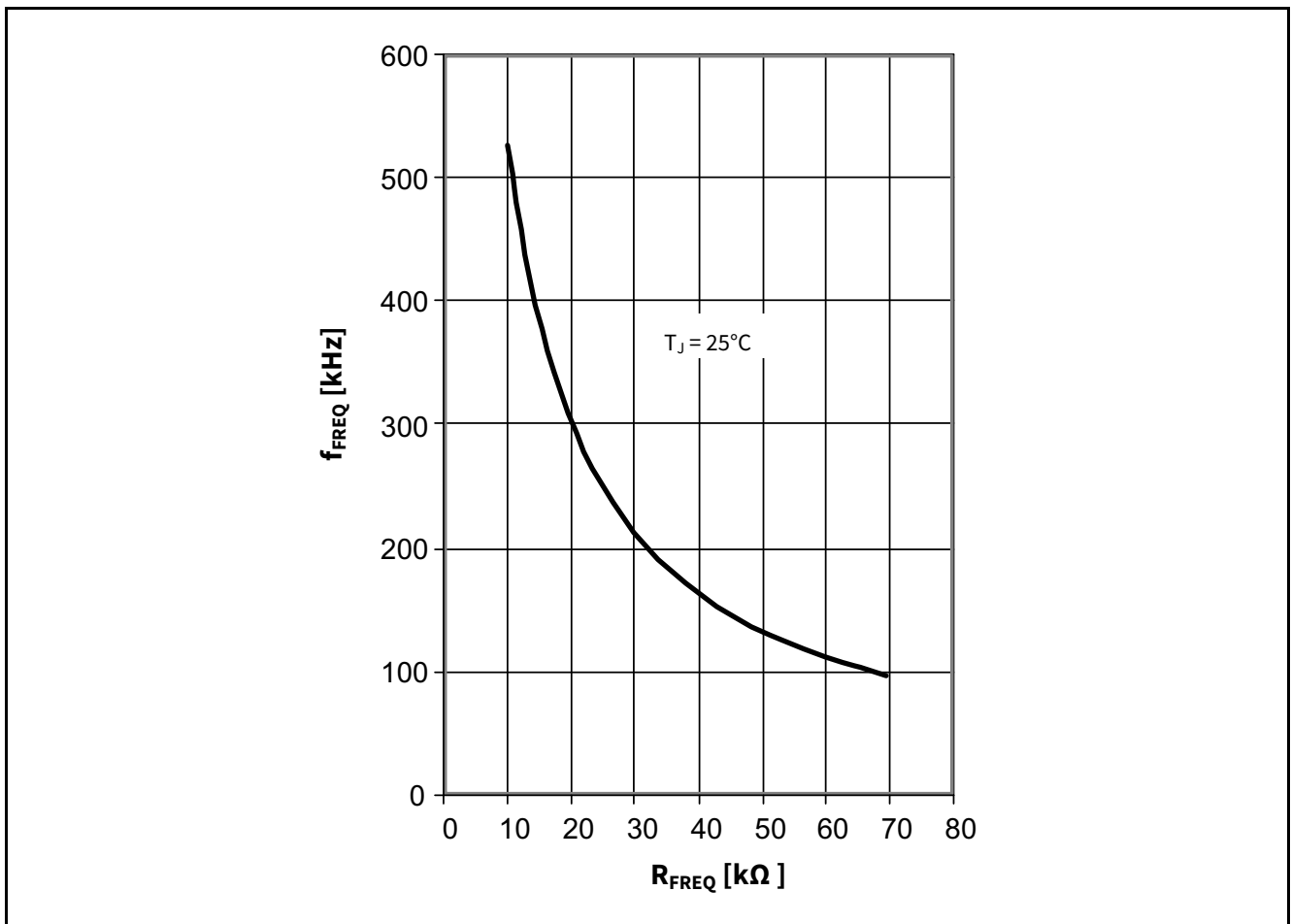


Figure 7 Switching frequency f_{SW} versus frequency select resistor to GND R_{FREQ}

7 Enable and dimming function

7.1 Description

The enable function powers the device on or off. A valid logic “low” signal on enable pin EN/PWMI powers “off” the device and current consumption is less than I_{Q_OFF} (P_7.1.14). A valid logic “high” enable signal on enable pin EN/PWMI powers on the device. The enable function features an integrated pull down resistor which ensures that the IC is shut down and the power switch is off in case the enable pin EN is left open.

In addition to the enable function described above, the EN/PWMI pin detects a pulse width modulated (PWM) input signal that is fed through to the internal gate driver. The EN/PWMI enables and disables the gate driver for the main switch during PWM operation. PWM dimming an LED is a commonly practiced dimming method and can prevent color shift in an LED light source.

The enable and PWM input function share the same pin. Therefore a valid logic “low” signal at the EN/PWMI pin needs to differentiate between an enable power “off” or a PWM dimming “low” signal. The device differentiates between enable off and PWM dimming signal by requiring the enable off at the EN/PWMI pin to stay “low” for the “**Enable turn off delay time**” ($t_{EN,OFF,DEL}$ P_7.1.6).

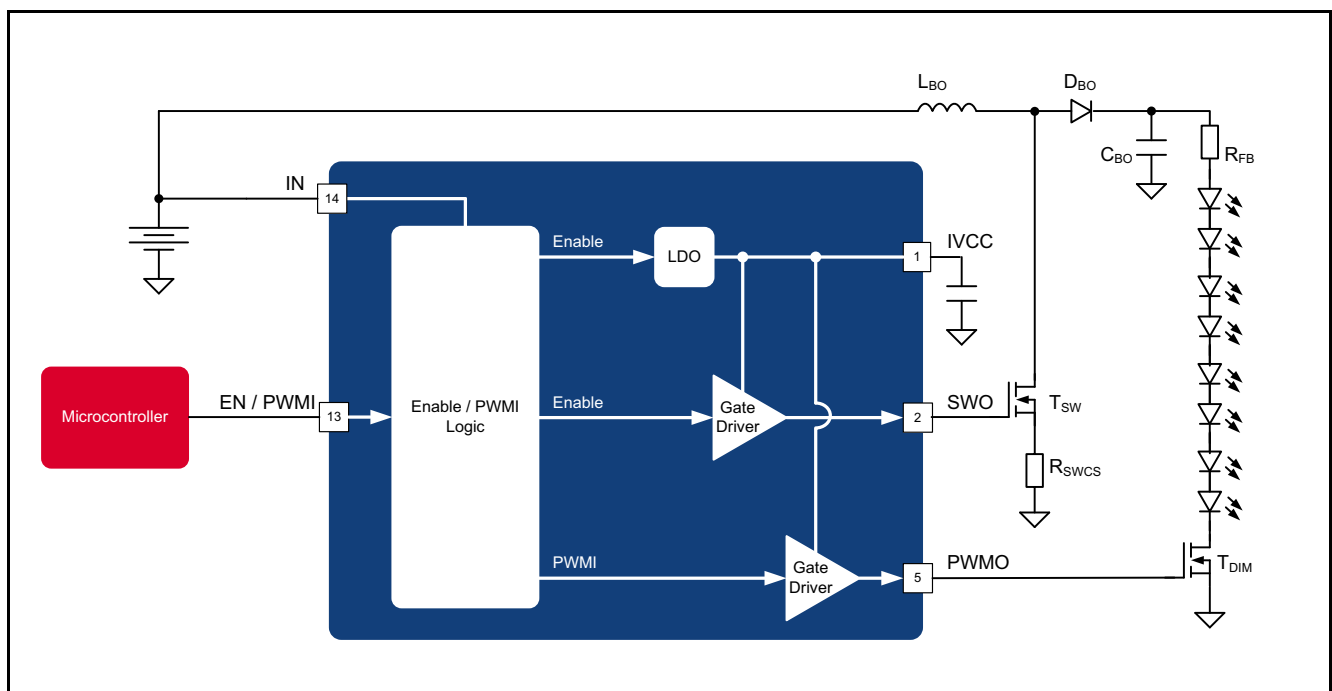


Figure 8 Block diagram and simplified application circuit enable and LED dimming

Enable and dimming function

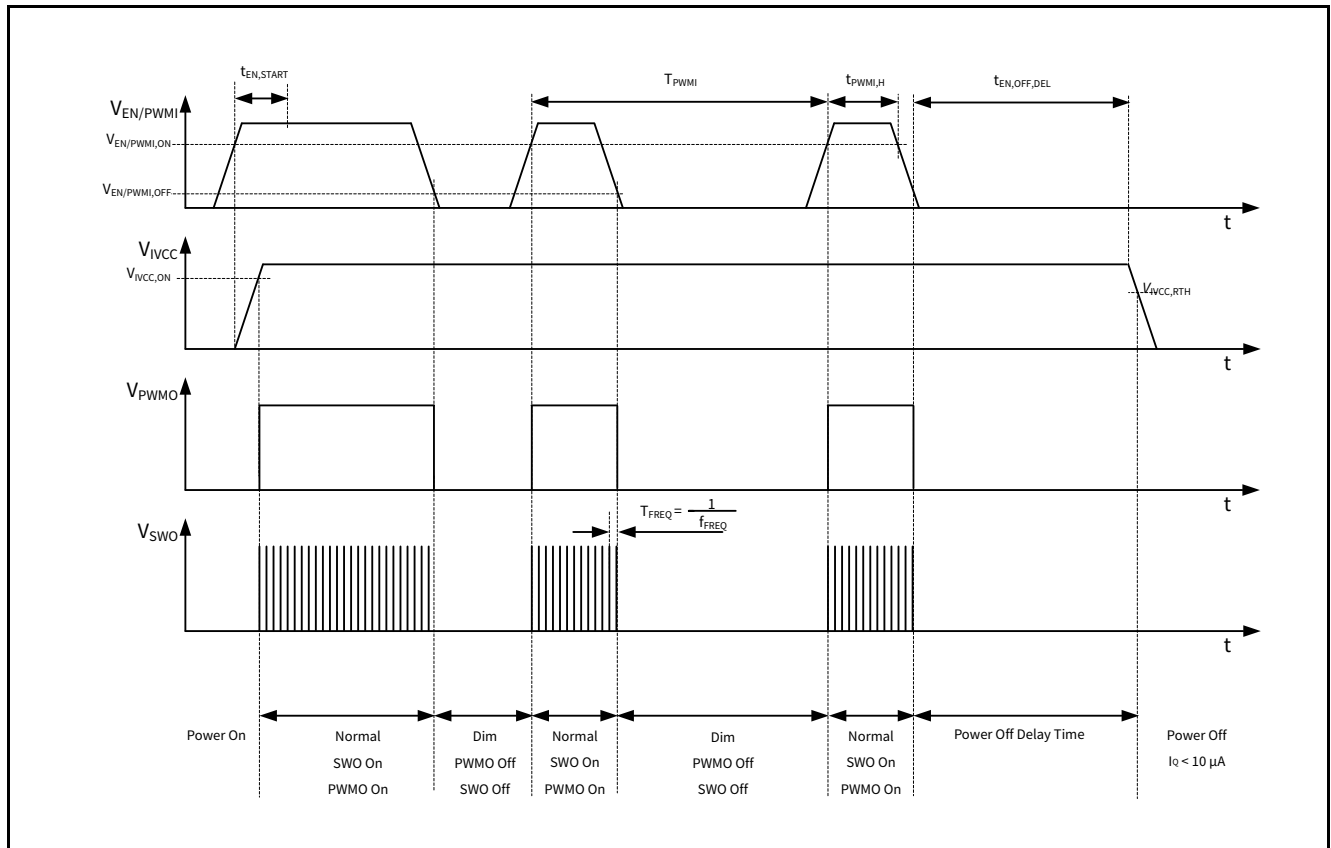


Figure 9 Timing diagram enable and LED dimming

7.2 Electrical characteristics

$V_{IN} = 8\text{ V to }34\text{ V}$, $T_J = -40^\circ\text{C to }+150^\circ\text{C}$, all voltages with respect to ground, positive current flowing into pin; (unless otherwise specified)

Table 8 Electrical characteristics: Enable and dimming

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|--------------------------------|-------------------|--------|------|------|---------------|-------------------------------|---------|
| | | Min. | Typ. | Max. | | | |
| Enable / PWM Input | | | | | | | |
| Enable/PWMI turn on threshold | $V_{EN/PWMI,ON}$ | 3.0 | – | | V | – | P_7.1.1 |
| Enable/PWMI turn off threshold | $V_{EN/PWMI,OFF}$ | – | – | 0.8 | V | – | P_7.1.2 |
| Enable/PWMI hysteresis | $V_{EN/PWMI,HYS}$ | 50 | 200 | 400 | mV | 1) | P_7.1.3 |
| Enable/PWMI high input current | $I_{EN/PWMI,H}$ | – | – | 30 | μA | $V_{EN/PWMI} = 16.0\text{ V}$ | P_7.1.4 |
| Enable/PWMI low input current | $I_{EN/PWMI,L}$ | – | 0.1 | 1 | μA | $V_{EN/PWMI} = 0.5\text{ V}$ | P_7.1.5 |
| Enable turn off delay time | $t_{EN,OFF,DEL}$ | 8 | 10 | 12 | ms | – | P_7.1.6 |
| PWMI min duty time | $t_{PWM,H}$ | 4 | – | – | μs | – | P_7.1.7 |
| Enable startup time | $t_{EN,START}$ | 100 | – | – | μs | 1) | P_7.1.8 |

Enable and dimming function

Table 8 Electrical characteristics: Enable and dimming

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|--|--------------------|--------|------|------|------|---|----------|
| | | Min. | Typ. | Max. | | | |
| Gate driver for dimming Switch | | | | | | | |
| PWMO gate driver peak sourcing current | $I_{P_{WMO, SRC}}$ | – | 230 | – | mA | ¹⁾ $V_{P_{WMO}} = 1\text{ V to }4\text{ V}$ | P_7.1.9 |
| PWMO gate driver peak sinking current | $I_{P_{WMO, SNK}}$ | – | 370 | – | mA | ¹⁾ $V_{P_{WMO}} = 4\text{ V to }1\text{ V}$ | P_7.1.10 |
| PWMO gate driver output rise time | $t_{R, P_{WMO}}$ | – | 50 | 100 | ns | ¹⁾ $C_{GATE} = 3.3\text{ nF};$ $V_{P_{WMO}} = 1\text{ V to }4\text{ V}$ | P_7.1.11 |
| PWMO gate driver output fall time | $t_{F, P_{WMO}}$ | – | 30 | 60 | ns | ¹⁾ $C_{GATE} = 3.3\text{ nF};$ $V_{P_{WMO}} = 4\text{ V to }1\text{ V}$ | P_7.1.12 |
| PWMO gate driver output voltage | $V_{P_{WMO}}$ | 4.5 | – | 5.5 | V | ¹⁾ $C_{GATE} = 3.3\text{ nF}$ | P_7.1.13 |
| Current consumption | | | | | | | |
| Current consumption, shutdown mode | I_{Q_OFF} | – | – | 10 | μA | $V_{EN/P_{WMI}} = 0.8\text{ V};$ $T_J \leq 105^\circ\text{C};$ $V_{IN} = 16\text{ V}$ | P_7.1.14 |
| Current consumption, active mode | I_{Q_ON} | – | – | 7 | mA | ²⁾ $V_{EN/P_{WMI}} \geq 4.75\text{ V};$ $I_{BO} = 0\text{ mA};$ $V_{SWO} = 0\% \text{ duty cycle}$ | P_7.1.15 |

1) Not subject to production test, specified by design

2) Dependency on switching frequency and gate charge of external switches

8 Linear regulator

8.1 Description

The internal linear voltage regulator supplies the internal gate drivers with a typical voltage of 5 V and current up to $I_{LIM,min}$ (P_8.1.2). An external output capacitor with ESR lower than $R_{IVCC,ESR}$ (P_8.1.5) is required on pin IVCC for stability and buffering transient load currents. During normal operation the external MOSFET switches will draw transient currents from the linear regulator and its output capacitor. Proper sizing of the output capacitor must be considered to supply sufficient peak current to the gate of the external MOSFET switches.

Integrated undervoltage protection for the external switching MOSFET

An integrated undervoltage reset threshold circuit monitors the linear regulator output voltage (V_{IVCC}) and resets the device in case the output voltage falls below the V_{IVCC} undervoltage reset switch OFF threshold ($V_{IVCC,RTH,d}$). The undervoltage reset threshold for the IVCC pin helps to protect the external switches from excessive power dissipation by ensuring the gate drive voltage is sufficient to enhance the gate of an external logic level n-channel MOSFET.

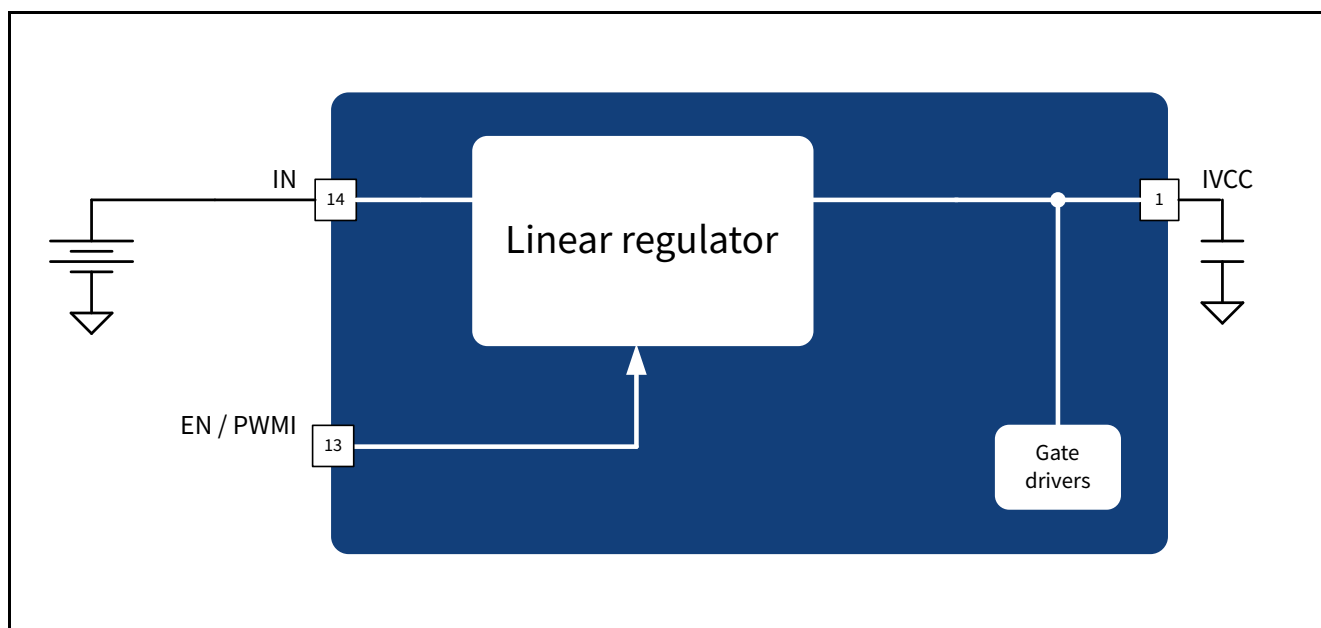


Figure 10 Voltage regulator block diagram and simplified application circuit

Linear regulator

8.2 Electrical characteristics

$V_{IN} = 8\text{ V to }34\text{ V}$, $T_J = -40^\circ\text{C to }+150^\circ\text{C}$, all voltages with respect to ground, positive current flowing into pin; (unless otherwise specified)

Table 9 Electrical characteristics: Line regulator

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|--|--------------------|--------|------|------|---------------|--|---------|
| | | Min. | Typ. | Max. | | | |
| Output voltage | V_{IVCC} | 4.85 | 5 | 5.15 | V | $6\text{ V} \leq V_{IN} \leq 45\text{ V}$ $0.1\text{ mA} \leq I_{IVCC} \leq 40\text{ mA}$ | P_8.1.1 |
| Output current limitation | I_{LIM} | 51 | – | 90 | mA | $V_{IN} = 13.5\text{ V}$ $V_{IVCC} = 4.5\text{ V}$ | P_8.1.2 |
| Drop out voltage | V_{DR} | – | – | 0.5 | V | $V_{IN} = 4.5\text{ V}$ $I_{IVCC} = 25\text{ mA}$ | P_8.1.3 |
| IVCC buffer capacitor | C_{IVCC} | 0.47 | 1 | 100 | μF | ¹⁾²⁾ | P_8.1.4 |
| IVCC buffer capacitor ESR | $R_{IVCC, ESR}$ | – | – | 0.5 | Ω | ¹⁾ | P_8.1.5 |
| Undervoltage reset headroom | $V_{IVCC, HDRM}$ | 100 | – | – | mV | V_{IVCC} decreasing $V_{IVCC} - V_{IVCC, RTH, d}$ | P_8.1.6 |
| IVCC undervoltage reset switch-off threshold | $V_{IVCC, RTH, d}$ | 3.6 | – | 4.0 | V | ³⁾ V_{IVCC} decreasing | P_8.1.7 |
| IVCC undervoltage reset switch-on threshold | $V_{IVCC, RTH, i}$ | – | – | 4.5 | V | V_{IVCC} increasing | P_8.1.8 |

- 1) Not subject to production test, specified by design
- 2) Minimum value given is needed for regulator stability; application might need higher capacitance than the minimum.
- 3) Selection of external switching MOSFET is crucial and the $V_{IVCC, RTH, d, min}$ as worst case the threshold voltage of MOSFET must be considered.

9 Protection and diagnostic functions

9.1 Description

The TLD5098EL has integrated circuits to diagnose and protect against output overvoltage, open load, open feedback and overtemperature faults. Additionally the FBH and FBL potential is monitored and in case the LED load short circuits to GND (see description [Figure 16](#)) the regulator stops the operation and protects the system. In case any of the six fault conditions occur the PWM0 and IVCC signal will change to an active logic “low” signal to communicate that a fault has occurred (detailed overview in [Figure 11](#) and [Figure 12](#) below). [Figure 12](#) illustrates the various open load and open feedback conditions. In case of an overtemperature condition the integrated thermal shutdown function turns off the gate drivers and internal linear voltage regulator. The typical junction shutdown temperature is 175°C ($T_{J,SD}$ P_9.2.2). After cooling down the IC will automatically restart. Thermal shutdown is an integrated protection function designed to prevent IC destruction and is not intended for continuous use in normal operation ([Figure 14](#)). To calculate the proper overvoltage protection resistor values an example is given in [Figure 15](#).

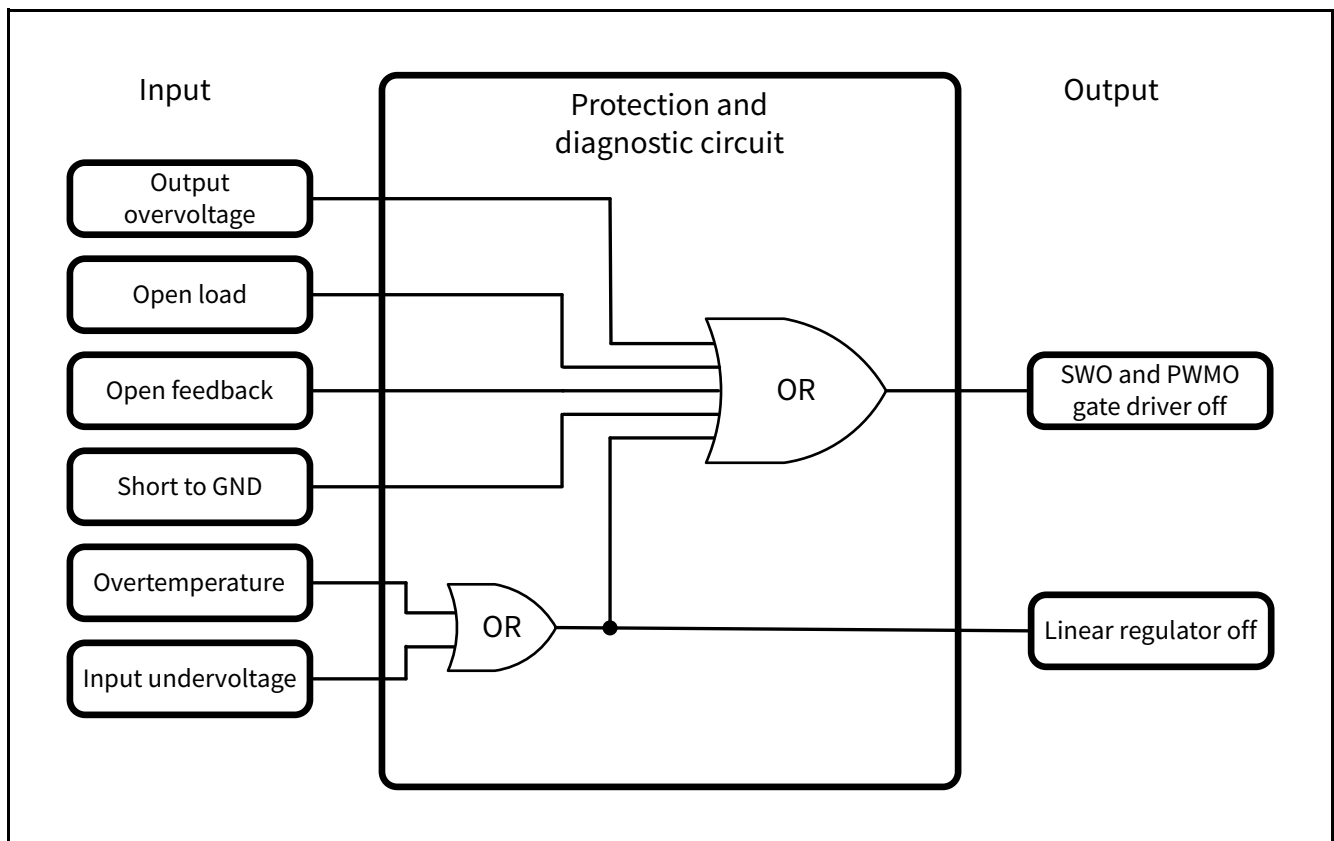


Figure 11 Protection and diagnostic function block diagram

Protection and diagnostic functions

Table 10 Diagnosis truth table¹⁾

| Input | | Output | | |
|---------------------------|-------|--------|------------|----------|
| Condition | Level | SWO | PWMO | IVCC |
| Overvoltage at output | False | Sw | High or Sw | Active |
| | True | Low | Low | Active |
| Open load | False | Sw | High or Sw | Active |
| | True | Low | Low | Active |
| Open feedback | False | Sw | High or Sw | Active |
| | True | Low | Low | Active |
| Short to GND at LED chain | False | Sw | High or Sw | Active |
| | True | Low | Low | Active |
| Overtemperature | False | Sw | High or Sw | Active |
| | True | Low | Low | Shutdown |
| Undervoltage at input | False | Sw | High or Sw | Active |
| | True | Low | Low | Shutdown |

1) Sw = Switching; False = Condition does NOT exist; True = Condition does exist

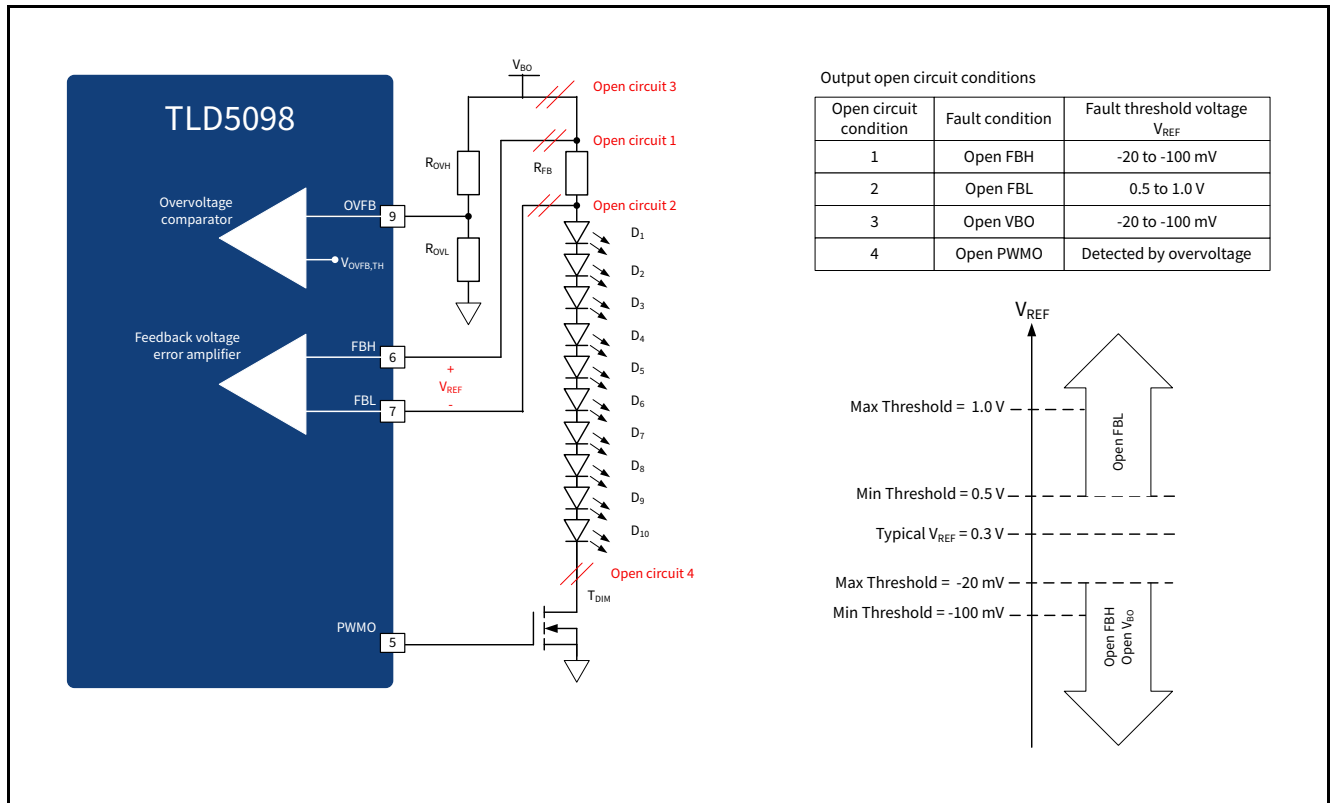


Figure 12 Open load and open feedback conditions

Protection and diagnostic functions

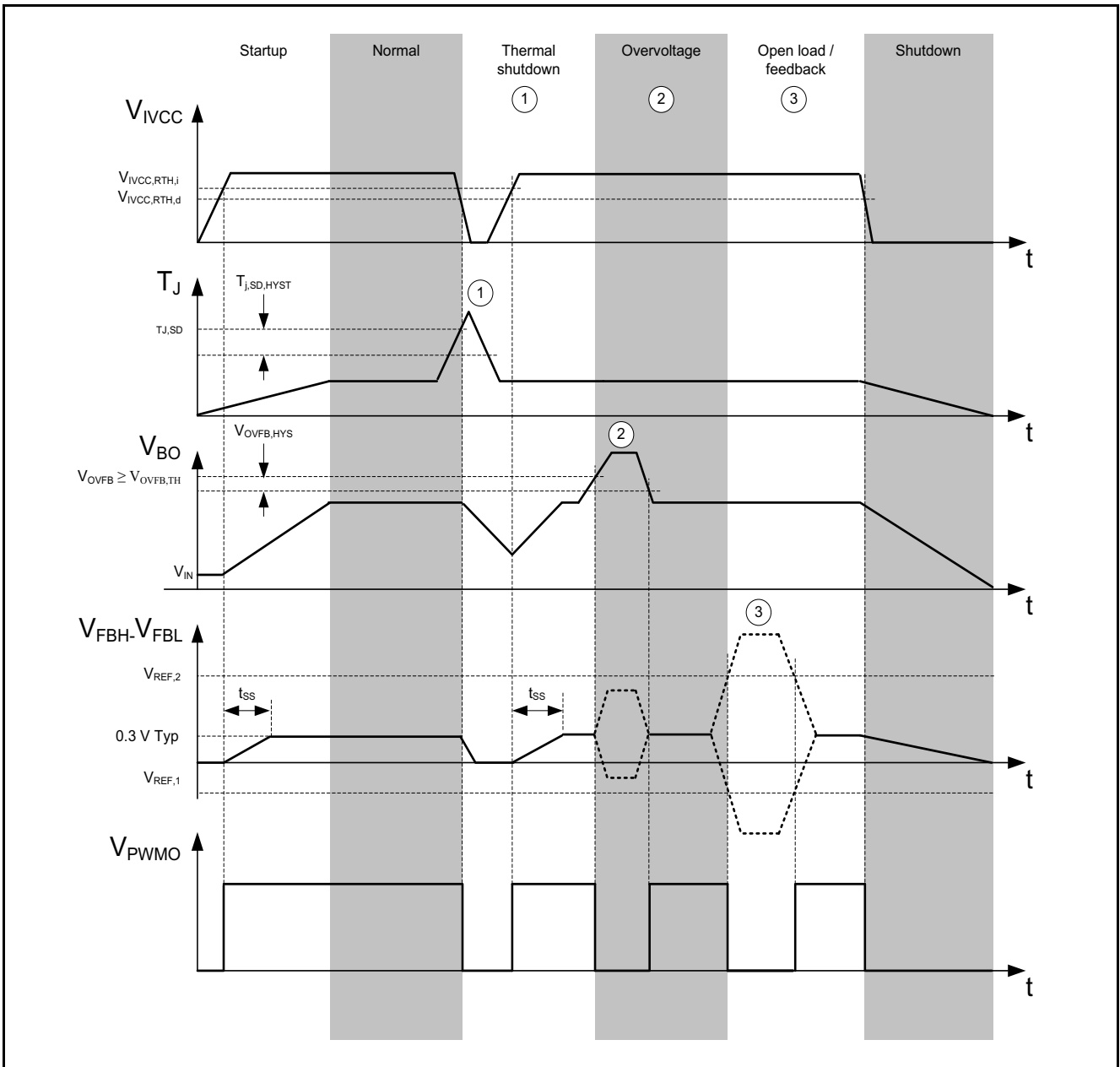


Figure 13 Open load, overvoltage and overtemperature timing diagram

Protection and diagnostic functions

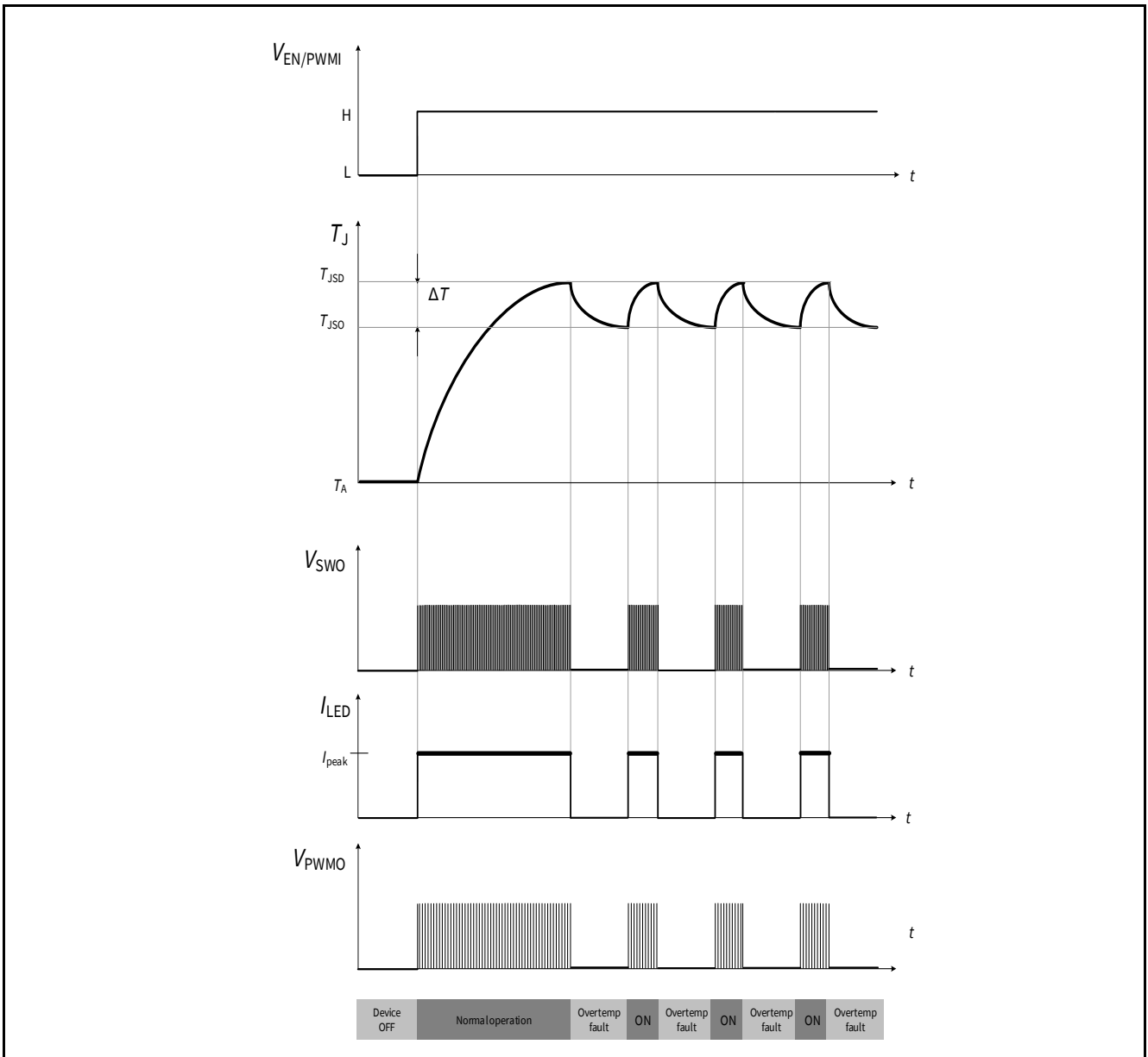


Figure 14 Device overtemperature protection behavior

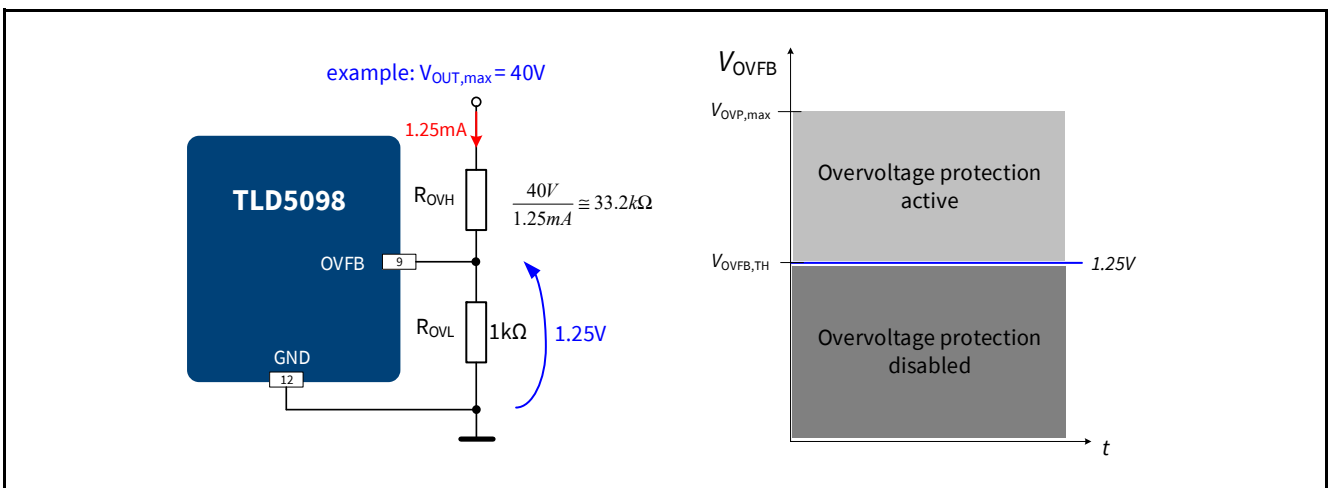


Figure 15 Overvoltage protection description

Protection and diagnostic functions

Short to GND protection for high-side return applications (B2B) from Figure 26

The FBH and FBL pins features a short to GND detection threshold ($V_{FBL, FBH}$, F_{BH_S2G}). If the potential on these pins is below this threshold the device stops its operation. This means that the PWM0 signal changes to inactive state (low potential) and the corresponding p-channel (T_{DIM2}) is switched off accordingly and protects the LED chain. For the B2B application some external components are needed to ensure a low potential during a short circuit event. D1 and D2 are low power diodes (eg. BAS16-03W) and the resistor R_{lim} (eg. 10 k Ω) is needed to limit the current through this path. The diode D3 should be a high power diode and is needed to protect the R_{FB} and the FBH and FBL pins in case of an short circuit to GND event. This short circuit detection and protection concept considers potential faults for LED chains (LED modules) which are separated from the ECU via two wires (at the beginning and at the end of the LED chain). If the short circuit condition disappears, the device will re-start with a soft start.

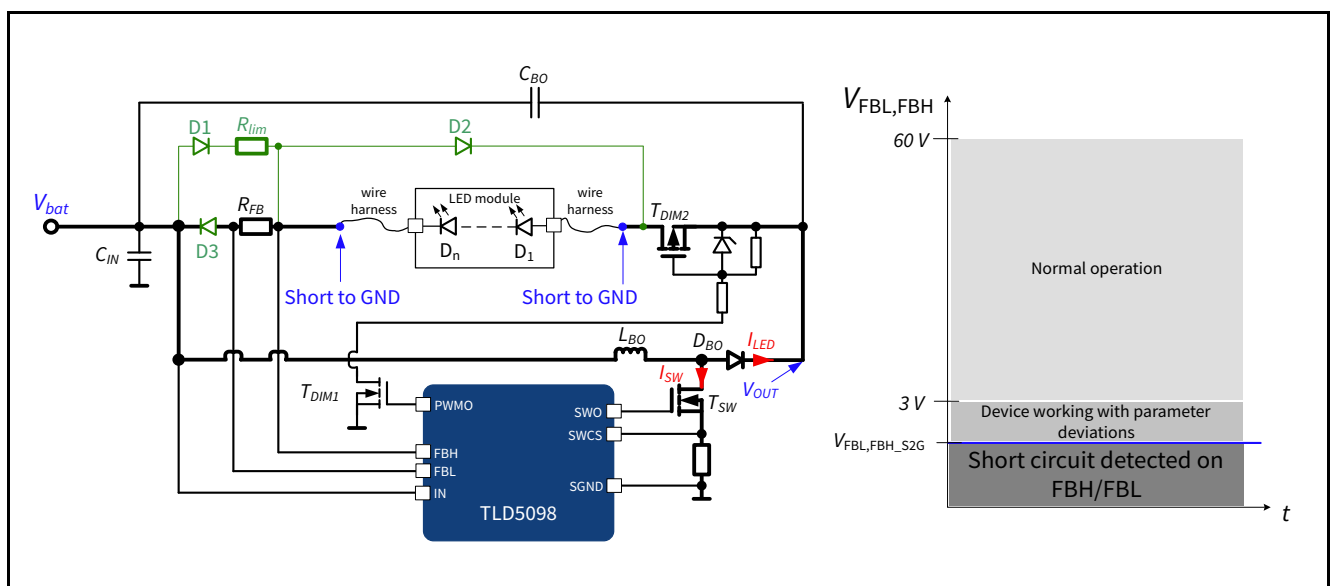


Figure 16 Short circuit to GND protection

Protection and diagnostic functions

9.2 Electrical characteristics

$V_{IN} = 8\text{ V to }34\text{ V}$, $T_J = -40^\circ\text{C to }+150^\circ\text{C}$, all voltages with respect to ground, positive current flowing into pin; (unless otherwise specified)

Table 11 Electrical characteristics: Protection and diagnosis

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|--------------------|--------|------|------|------|---|---------|
| | | Min. | Typ. | Max. | | | |
| Short circuit protection | | | | | | | |
| FBH and FBL short-circuit fault sensing common mode range | V_{FBL,FBH_S2G} | 1.5 | – | 2 | V | refer to Figure 16 $V_{FBH} = V_{FBL}$ decreasing | P_9.2.1 |
| Temperature protection | | | | | | | |
| Overtemperature shutdown | $T_{J,SD}$ | 160 | 175 | 190 | °C | ¹⁾ refer to Figure 14 | P_9.2.2 |
| Overtemperature shutdown hystereses | $T_{J,SD,HYST}$ | – | 15 | – | °C | ¹⁾ | P_9.2.3 |
| Overvoltage protection | | | | | | | |
| Output overvoltage feedback threshold increasing | $V_{OVFB,TH}$ | 1.21 | 1.25 | 1.29 | V | refer to Figure 15 | P_9.2.4 |
| Output overvoltage feedback hysteresis | $V_{OVFB,HYS}$ | 50 | – | 150 | mV | ¹⁾ Output Voltage decreasing | P_9.2.5 |
| Overvoltage reaction time | t_{OVPRR} | 2 | – | 10 | µs | Output Voltage increasing | P_9.2.6 |
| Overvoltage feedback input current | I_{OVFB} | -1 | 0.1 | 1 | µA | $V_{OVFB} = 1.25\text{ V}$ | P_9.2.7 |
| Open load and open feedback diagnostics | | | | | | | |
| Open load/feedback threshold | $V_{REF,1,3}$ | -100 | – | -20 | mV | refer to Figure 12 $V_{REF} = V_{FBH} - V_{FBL}$ Open circuit 1 or 3 | P_9.2.8 |
| Open feedback threshold | $V_{REF,2}$ | 0.5 | – | 1 | V | $V_{REF} = V_{FBH} - V_{FBL}$ Open circuit 2 | P_9.2.9 |

1) Specified by design; not subject to production test

Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.

10 Analog dimming

This pin influences the “feedback voltage error amplifier” by generating an internal current accordingly to an external reference voltage (V_{SET}). If the analog dimming feature is not needed this pin must be connected to IVCC or external > 1.6 V supply. Different application scenarios are described in [Figure 19](#). This pin can also go outside of the ECU for instance if a thermistor is connected on a separated LED module and the “Analog dimming input” is used to thermally protect the LEDs. For reverse battery protection of this pin an external series resistor should be placed to limit the current.

10.1 Purpose of analog dimming

1. It is difficult for LED manufacturers to deliver LEDs which have the same brightness, colorpoint and forward voltage class. Due to this relatively wide spread of the crucial LED parameters automotive customers order LEDs from one or maximum two different colorpoint classes. The LED manufacturer must preselect the LEDs to deliver the requested colorpoint class. These preselected LEDs are matched in terms of the colorpoint but a variation of the brightness remains. To correct the brightness deviation an analog dimming feature is needed. The mean LED current can be adjusted by applying an external voltage V_{SET} at the SET pin.
2. If the DC/DC application is separated from the LED loads the ECU manufacturers aim is to develop one hardware which should be able to handle different load current conditions (e.g. 80 mA to 400 mA) to cover different applications. To achieve this average LED current adjustment the analog dimming is a crucial feature.

10.2 Description

Application example

Desired LED current = 400 mA. For the calculation of the correct feedback resistor R_{FB} the following equation can be used: This formula is valid if the analog dimming feature is disabled and $V_{SET} > 1.6$ V.

(10.1)

$$I_{LED} = \frac{V_{REF}}{R_{FB}} \rightarrow R_{FB} = \frac{V_{REF}}{I_{LED}} \rightarrow R_{FB} = \frac{0.3V}{400mA} = 750m\Omega$$

Related electrical parameter is guaranteed with $V_{SET} = 5$ V ([P_5.2.1](#)) A decrease of the average LED current can be achieved by controlling the voltage at the SET pin (V_{SET}) between 0.1 V and 1.6 V. The mathematical relation is given in the formula below:

(10.2)

$$I_{LED} = \frac{V_{SET} - 0.1V}{5 \cdot R_{FB}}$$

Refer to the concept drawing in [Figure 18](#).

Analog dimming

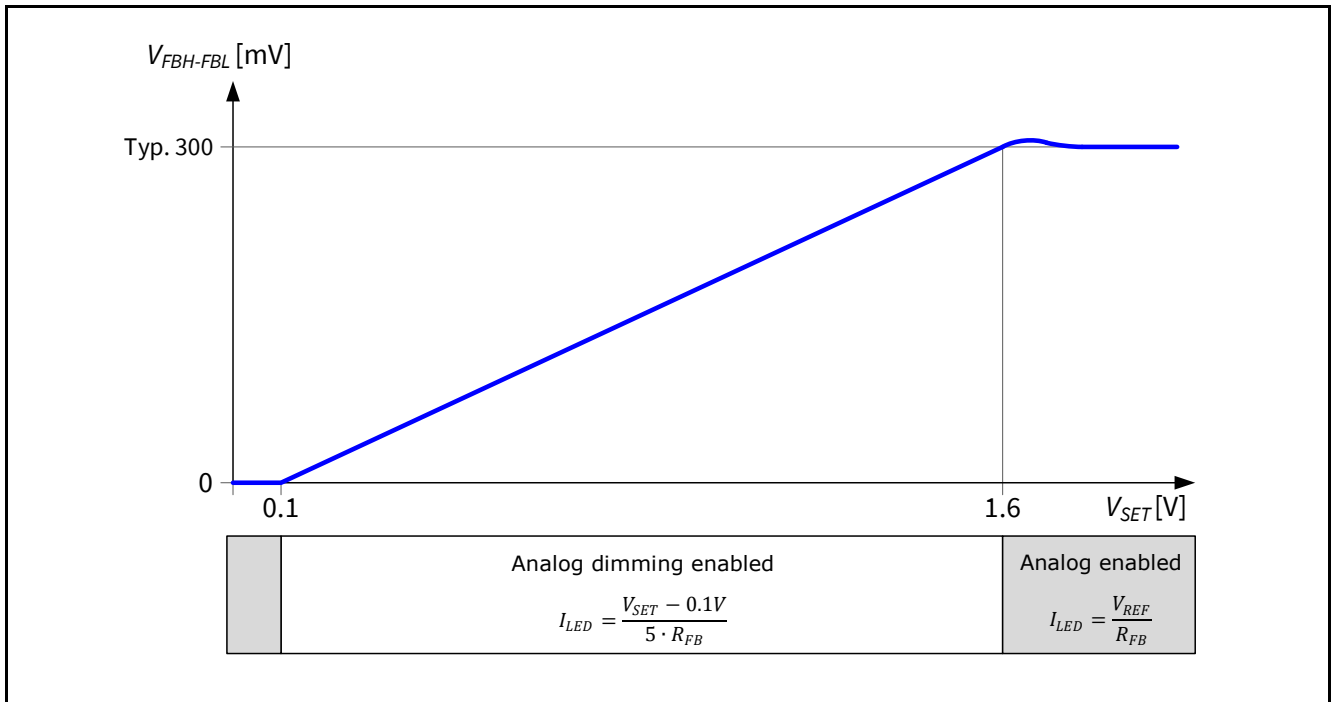


Figure 17 Basic relationship between V_{REF} and V_{SET} voltage

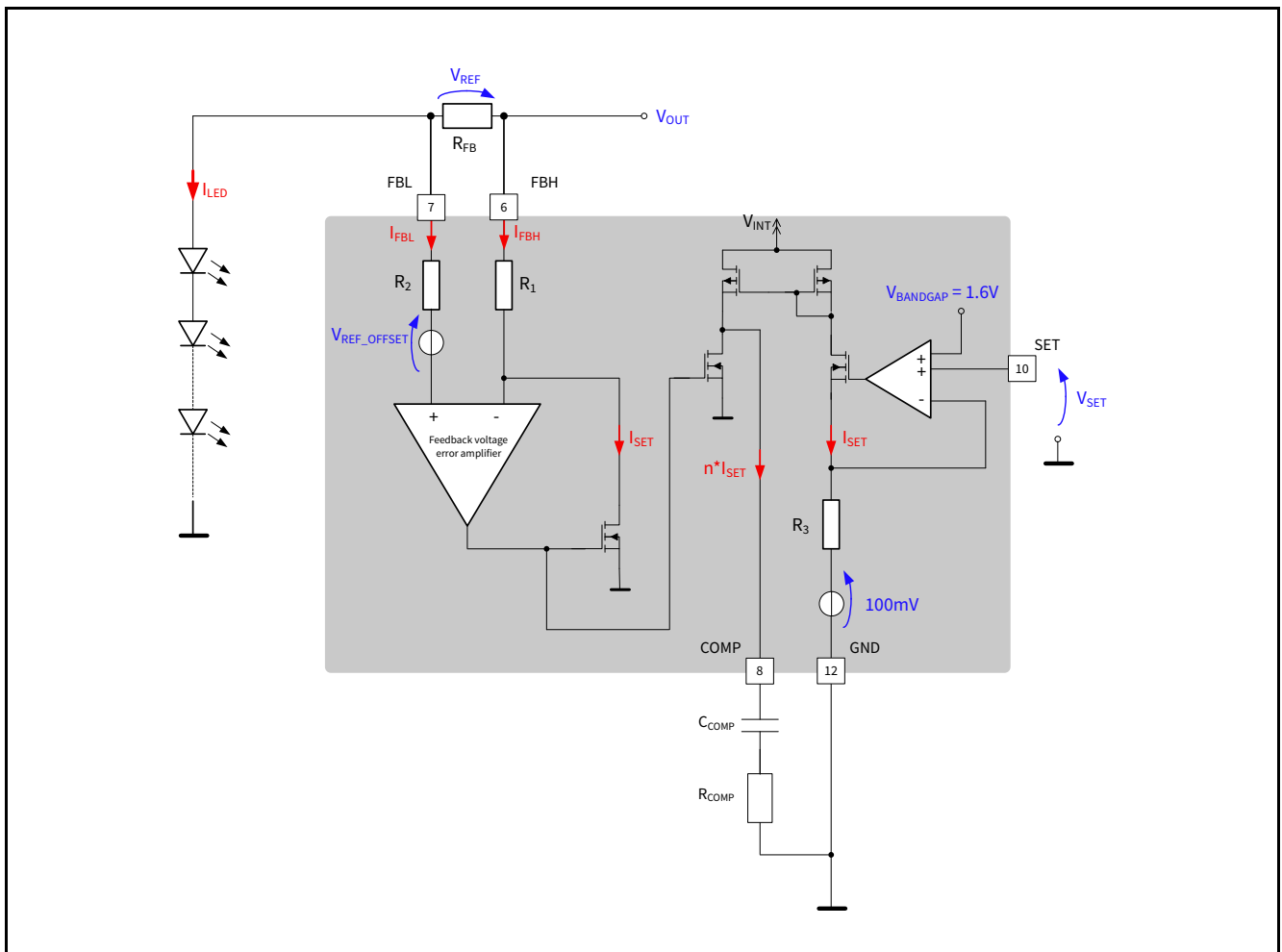


Figure 18 Concept drawing analog dimming

Analog dimming

Multi-purpose usage of the analog dimming feature

1. A μC integrated digital analog converter (DAC) output or a stand alone DAC can be used to supply the SET pin of the TLD5098EL. The integrated voltage regulator (V_{VCC}) can be used to supply the μC or external components if the current consumption does not exceed 20 mA.
2. The analog dimming feature is directly connected to the input voltage of the system. In this configuration the LED current is reduced if the input voltage V_{IN} is decreasing. The DC/DC boost converter is changing (increasing) the switching duty cycle if V_{IN} drops to a lower potential. This causes an increase of the input current consumption. If applications require a decrease of the LED current in respect to V_{IN} variations this setup can be chosen.
3. The usage of an external resistor divider connected between I_{VCC} (integrated 5 V regulator output and gate buffer pin) SET and GND can be chosen for systems without μC on board. The concept allows to control the LED current via placing cheap low power resistors. Furthermore a temperature sensitive resistor (Thermistor) to protect the LED loads from thermal destruction can be connected additionally.
4. If the analog dimming feature is not needed the SET pin must be connected directly to $> 1.6\text{ V}$ potential (e.g. I_{VCC} potential)
5. Instead of a DAC the μC can provide a PWM signal and an external R-C filter produces a constant voltage for the analog dimming. The voltage level depends on the PWM frequency (f_{PWM}) and duty cycle (DC) which can be controlled by the μC software after reading the coding resistor placed at the LED module.

Analog dimming

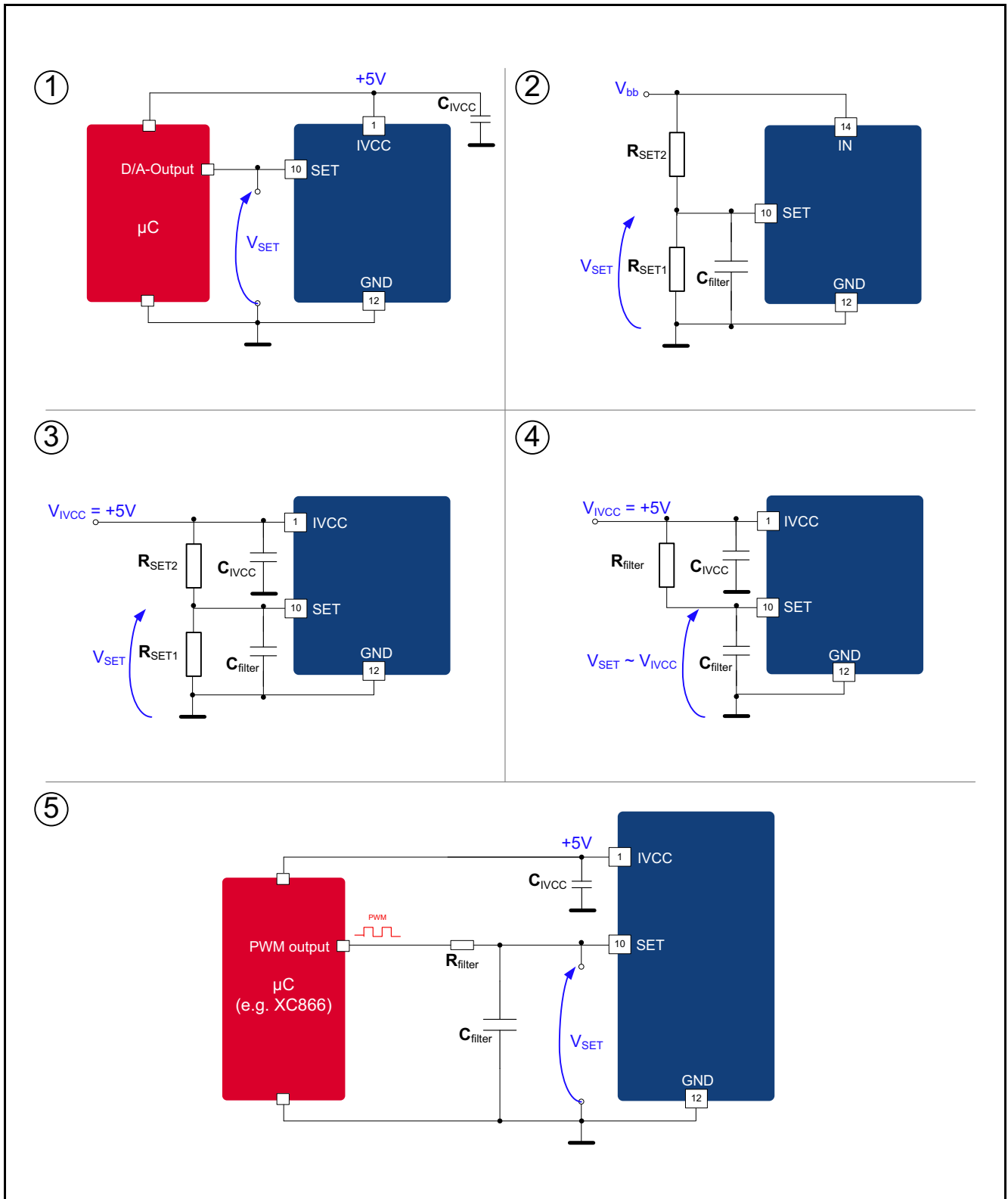


Figure 19 Analog dimming in various applications

Analog dimming

10.3 Electrical characteristics

$V_{IN} = 8\text{ V to }34\text{ V}$, $T_J = -40^\circ\text{C to }+150^\circ\text{C}$, all voltages with respect to ground, positive current flowing into pin; (unless otherwise specified)

Table 12 Electrical characteristics: Protection and diagnosis

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|-----------------------|-----------|--------|------|------|------|---|----------|
| | | Min. | Typ. | Max. | | | |
| SET programming range | V_{SET} | 0 | – | 1.6 | V | ¹⁾ refer to Figure 17 | P_10.3.1 |

1) Specified by design; not subject to production test.

Application information

11 Application information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

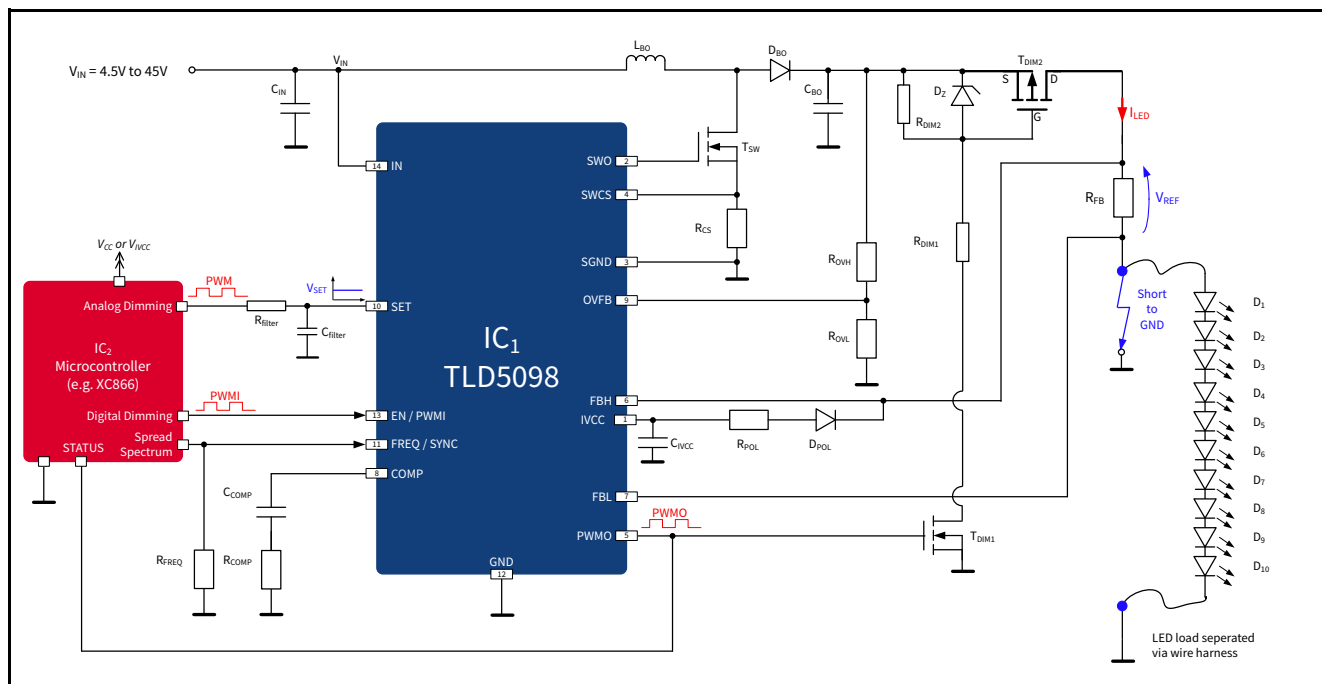


Figure 20 Boost to Ground application circuit - B2G (Boost configuration)

| Reference Designator | Value | Manufacturer | Part Number | Type | Quantity |
|--|--|--------------|-----------------------|------------|----------|
| D ₁ - 10 | White | Osram | LUW H9GP | LED | 10 |
| D _{BO} | Schottky, 3 A, 100 V _R | Vishay | SS3H10 | Diode | 1 |
| D _Z | 5V or 10V | Vishay | ZENER | Diode | 1 |
| D _{POL} | 80V Diode | Infineon | BAS1603W | Diode | 1 |
| C _{IN} , C _{BO} | 100 uF, 50V | Panasonic | EEEFK1H101GP | Capacitor | 2 |
| C _{COMP} | 10 nF | EPCOS | X7R | Capacitor | 1 |
| C _{IVCC} | 1uF, 6.3V | EPCOS | MLCC CCNPZC105KBW X7R | Capacitor | 1 |
| IC ₁ | -- | Infineon | TLD5098 | IC | 1 |
| IC ₂ | -- | Infineon | XC866 | IC | 1 |
| L _{BO} | 100 uH | Coilcraft | MSS1278T-104ML | Inductor | 1 |
| R _{DIM1+2} , R _{COMP} , R _{POL} | 10 kΩ, 1% | Panasonic | ERJ3EKF 1002V | Resistor | 4 |
| R _{FB} | 820 mΩ, 1% | Panasonic | ERJ14BQFR82U | Resistor | 1 |
| R _{FREQ} | 20 kΩ, 1% | Panasonic | ERJ3EKF2002V | Resistor | 1 |
| R _{OVH} | 33.2 kΩ, 1% | Panasonic | ERJ3EKF3322V | Resistor | 1 |
| R _{OVL} | 1 kΩ, 1% | Panasonic | ERJ3EKF 1001V | Resistor | 1 |
| R _{CS} | 50 mΩ, 1% | Panasonic | ERJB 1CFR05U | Resistor | 1 |
| T _{SW} | 100V N-ch, 35A | Infineon | IPG20N10S4L-22 | Transistor | 1 |
| T _{DIM1} , T _{DIM2} | 60V Dual N-ch (3.1A) and P-ch. enh. (2A) | Infineon | BSO615CG | Transistor | 1 |
| | alternativ: 100V N-ch (0.37A), | Infineon | BSP123 | Transistor | 1 |
| | alternativ: 60V P-ch (1.9A) | Infineon | BSP171P | Transistor | 1 |

Figure 21 Bill of Materials for B2G application circuit

Application information

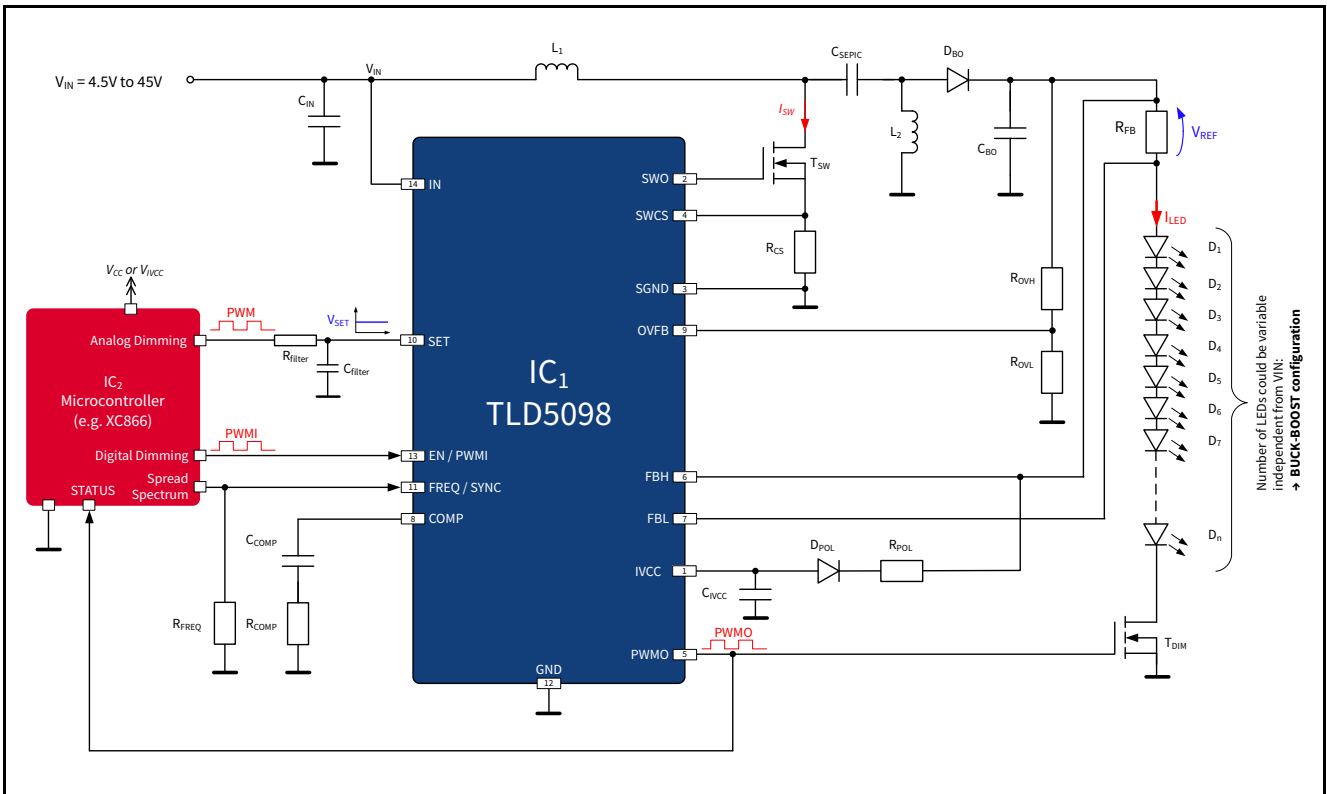


Figure 22 SEPIC application circuit (Buck - Boost configuration)

| Reference Designator | Value | Manufacturer | Part Number | Type | Quantity |
|--------------------------------------|-----------------------------------|--------------|----------------|------------|----------|
| D _{1 - n} | White | Osram | LUW H9GP | LED | variable |
| D _{BO} | Schottky, 3 A, 100 V _R | Vishay | SS3H10 | Diode | 1 |
| D _{POL} | 80V Diode | Infineon | BAS 1603W | Diode | 1 |
| C _{SEPIC} | 3.3 uF, 20V | EPCOS | X7R, Low ESR | Capacitor | 1 |
| C _{IN} , C _{BO} | 100 uF, 50V | Panasonic | EEEFK1H101GP | Capacitor | 2 |
| C _{COMP} | 10 nF | EPCOS | X7R | Capacitor | 1 |
| C _{IVCC} | 1uF, 6.3V | EPCOS | X7R | Capacitor | 1 |
| IC ₁ | -- | Infineon | TLD5098 | IC | 1 |
| IC ₂ | -- | Infineon | XC866 | IC | 1 |
| L ₁ , L ₂ | 47 uH | Coilcraft | MSS1278T-473ML | Inductor | 2 |
| | alternativ: 22uH coupled inductor | Coilcraft | MSD1278-223MLD | Inductor | 1 |
| R _{COMP} , R _{POL} | 10 kΩ, 1% | Panasonic | ERJ3EKF 1002V | Resistor | 2 |
| R _{FB} | 820 mΩ, 1% | Panasonic | ERJ14BQFR82U | Resistor | 1 |
| R _{FREQ} | 20 kΩ, 1% | Panasonic | ERJ3EKF 2002V | Resistor | 1 |
| R _{OVH} | 33.2 kΩ, 1% | Panasonic | ERJ3EKF 3322V | Resistor | 1 |
| R _{OVL} | 1 kΩ, 1% | Panasonic | ERJ3EKF 1001V | Resistor | 1 |
| R _{CS} | 50 mΩ, 1% | Panasonic | ERJB 1CFR05U | Resistor | 1 |
| T _{DIM} , T _{SW} | Dual N-ch enh. (60V, 20A) | Infineon | IPG20N06S4L-26 | Transistor | 1 |
| | alternativ: 100V N-ch, 35A | Infineon | IPD35N10S3L-26 | Transistor | 2 |
| | alternativ : 60V N-ch, 2.6A | Infineon | BSP318S | Transistor | 2 |

Figure 23 Bill of Materials for SEPIC application circuit

Application information

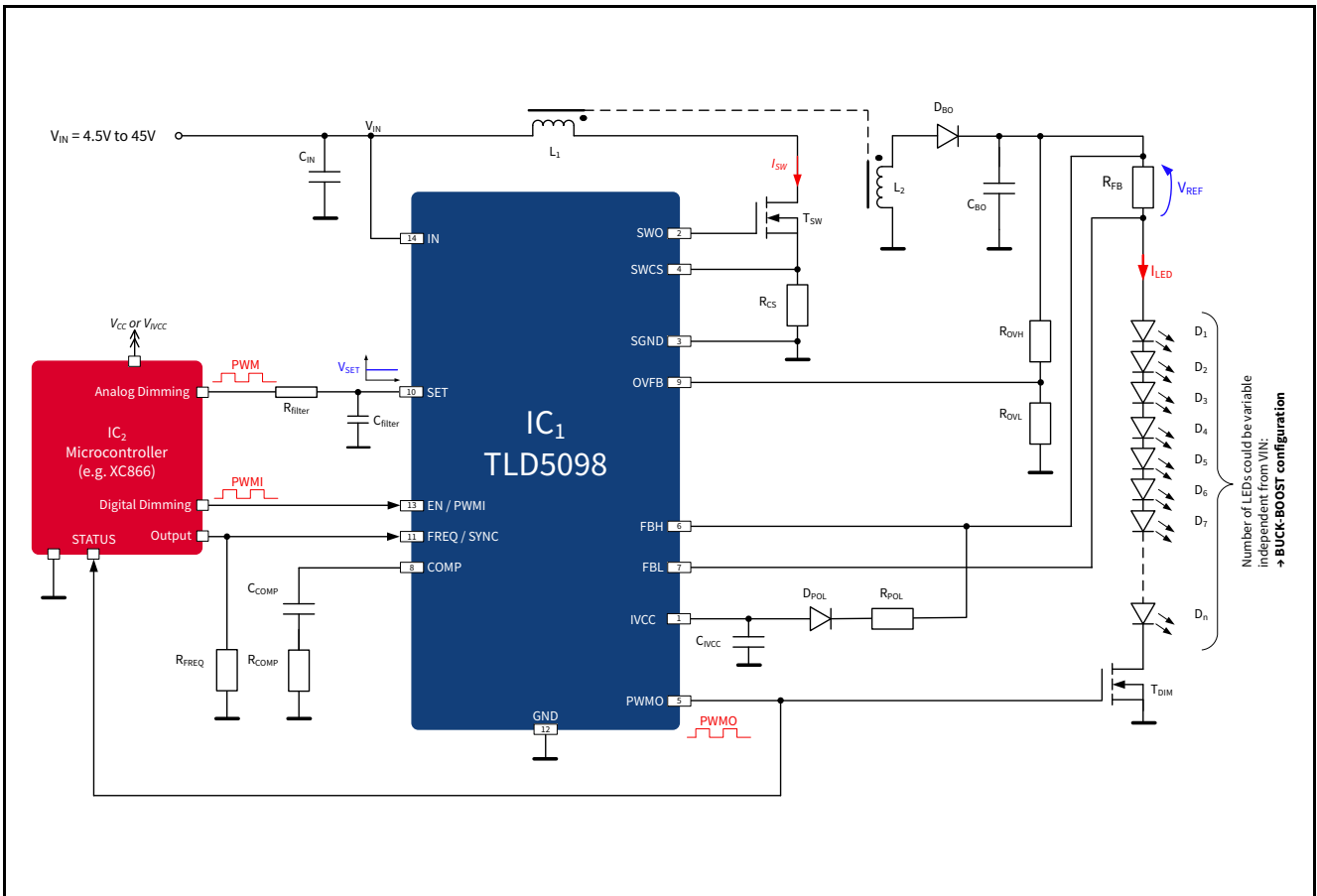


Figure 24 Flyback application circuit (Buck - Boost configuration)

| Reference Designator | Value | Manufacturer | Part Number | Type | Quantity |
|--------------------------------------|-----------------------------------|----------------|----------------------|------------|----------|
| D ₁ - n | White | Osram | LUW H9GP | LED | variable |
| D _{BO} | Schottky, 3 A, 100 V _R | Vishay | SS3H10 | Diode | 1 |
| C _{BO} | 3.3 uF, 50V (100V) | EPCOS | X7R, Low ESR | Capacitor | 1 |
| C _{IN} | 100 uF, 50V | Panasonic | EEEFK1H101GP | Capacitor | 1 |
| C _{COMP} | 47 nF | EPCOS | X7R | Capacitor | 1 |
| C _{IVCC} | 1 uF, 6.3V | EPCOS | X7R | Capacitor | 1 |
| IC ₁ | -- | Infineon | TLD5098 | IC | 1 |
| IC ₂ | -- | Infineon | XC866 | IC | 1 |
| L ₁ , L ₂ | 1 μH / 9 uH | EPCOS | Transformer EHP 16 | Inductor | 1 |
| R _{COMP} , R _{POL} | 10 kΩ, 1% | Panasonic | ERJ3EKF 1002V | Resistor | 2 |
| D _{POL} | 80 V Diode | Infineon | BAS 1603W | Diode | 1 |
| R _{FB} | 820 mΩ, 1% | Isabellenhütte | SMS – Power Resistor | Resistor | 1 |
| R _{FREQ} | 10 kΩ, 1% | Panasonic | ERJ3EKF 1002V | Resistor | 1 |
| R _{OVH} | 56.2 kΩ, 1% | Panasonic | ERJ3EKF 5622V | Resistor | 1 |
| R _{OVL} | 1.24 kΩ, 1% | Panasonic | ERJ3EKF 1241V | Resistor | 1 |
| R _{CS} | 5 mΩ, 1% | Isabellenhütte | SMS - Power Resistor | Resistor | 1 |
| T _{DIM} , T _{SW} | Dual N-ch enh. (60V, 20A) | Infineon | IPG20N06S4L-26 | Transistor | 1 |
| | alternativ: 100V N-ch, 35A | Infineon | IPG20N10S4L-22 | Transistor | 2 |
| | alternativ : 60V N-ch, 2.6A | Infineon | BSP318S | Transistor | 2 |

Figure 25 Bill of Materials for Flyback application circuit

Application information

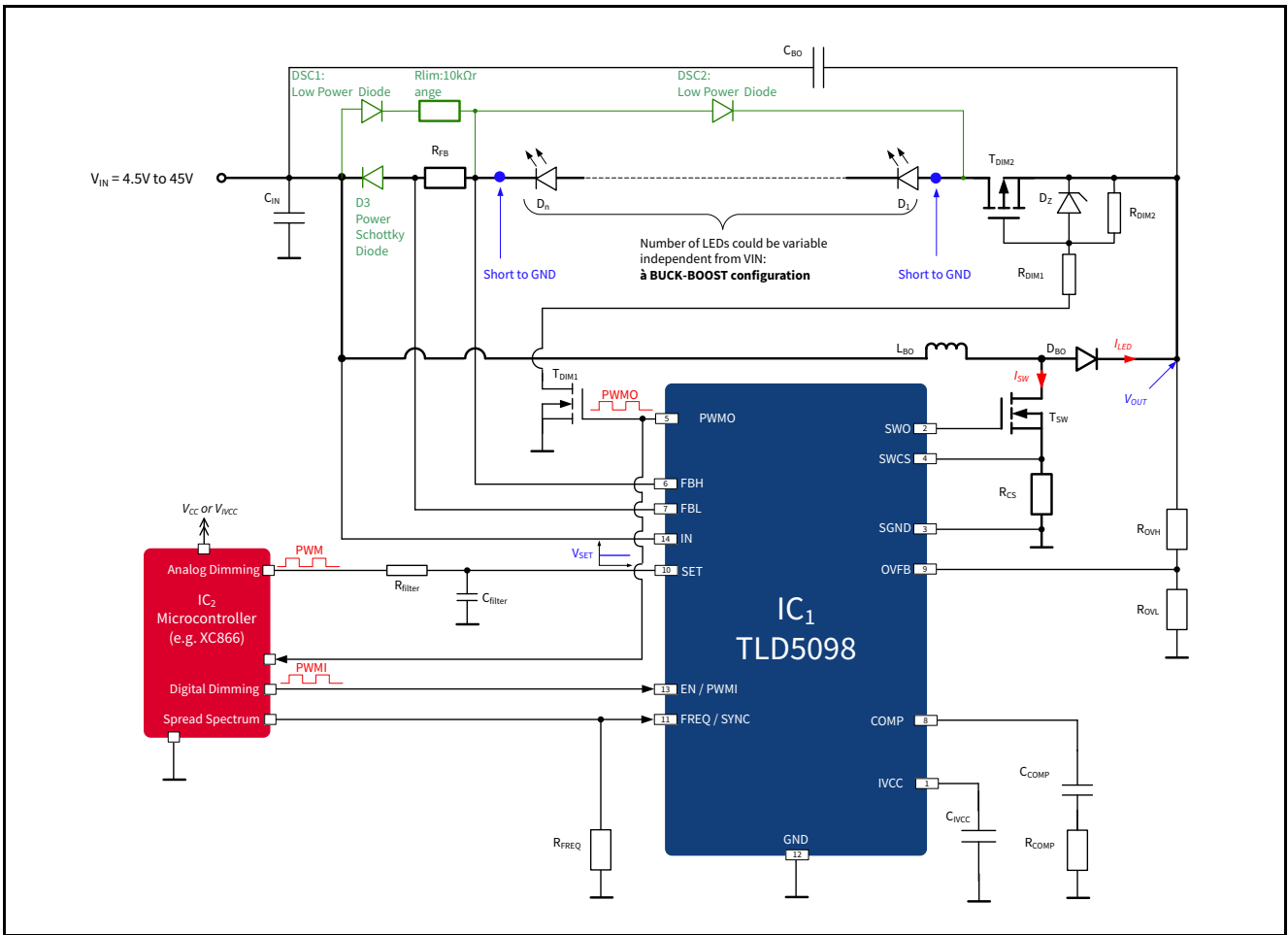


Figure 26 Boost to Battery application circuit - B2B (Buck - Boost configuration)

| Reference Designator | Value | Manufacturer | Part Number | Type | Quantity |
|---|--|--------------|-----------------------|------------|----------|
| D_{1-n} | White | Osram | LUW H9GP | Diode | variable |
| D_{BO}, D_3 | Schottky, 3 A, 100 V_R | Vishay | SS3H10 | Diode | 2 |
| D_{SC1}, D_{SC2} | Low Power Diode | Infineon | BAS16-03W | Diode | 2 |
| D_Z | Zener Diode | -- | -- | Diode | 1 |
| C_{BO} | 100 μF , 80V | Panasonic | EEVFK1K101Q | Capacitor | 1 |
| C_{IN} | 100 μF , 50V | Panasonic | EEEFK1H101GP | Capacitor | 1 |
| C_{COMP} | 10 nF | EPCOS | X7R | Capacitor | 1 |
| C_{IVCC} | 1 μF , 6.3V | EPCOS | MLCC CCNP2C105KBW X7R | Capacitor | 1 |
| IC_1 | -- | Infineon | TLD5098 | IC | 1 |
| IC_2 | -- | Infineon | XC866 | IC | 1 |
| L_{BO} | 100 μH | Coilcraft | MSS1278T-104ML_ | Inductor | 1 |
| $R_{COMP}, R_{DIM1}, R_{DIM2}, R_{lim}$ | 10 k Ω , 1% | Panasonic | ERJ3EKF1002V | Resistor | 4 |
| R_{FB} | 820 m Ω , 1% | Panasonic | ERJ14BQFR82U | Resistor | 1 |
| R_{FREQ} | 20 k Ω , 1% | Panasonic | ERJ3EKF2002V | Resistor | 1 |
| R_{OVH} | 33.2 k Ω , 1% | Panasonic | ERJP06F5102V | Resistor | 1 |
| R_{OVL} | 1 k Ω , 1% | Panasonic | ERJ3EKF1001V | Resistor | 1 |
| R_{CS} | 50 m Ω , 1% | Panasonic | ERJB1CFR05U | Resistor | 1 |
| T_{DIM1}, T_{DIM2} | 60V Dual N-ch (3.1A) and P-ch. enh. (2A) | Infineon | BSO615CG | Transistor | 1 |
| | alternativ: 100V N-ch (0.37A), | Infineon | BSP123 | Transistor | 1 |
| | alternativ: 60V P-ch (1.9A) | Infineon | BSP171P | Transistor | 1 |
| T_{SW} | N-ch, OptiMOS-T2 100V, 35A | Infineon | IPD35N10S3L-26 | Transistor | 1 |
| | alternativ: 60V N-ch, 30A | Infineon | IPD30N06S4L-23 | Transistor | 1 |
| | alternativ: 60V N-ch, 2.6A | Infineon | BSP318S | Transistor | 1 |

Figure 27 Bill of Materials for B2B application circuit

Application information

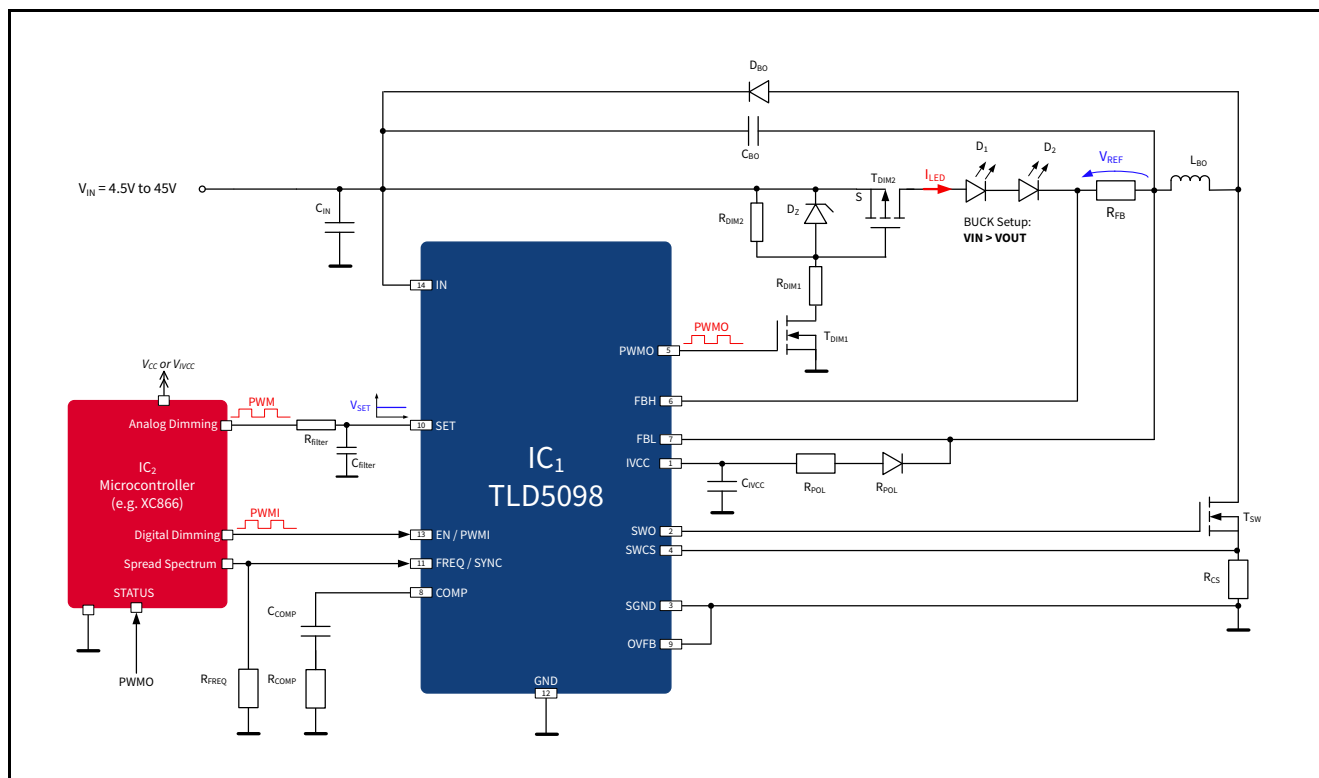


Figure 28 Buck application circuit

| Reference Designator | Value | Manufacturer | Part Number | Type | Quantity |
|--|-----------------------------------|----------------|-----------------------|------------|----------|
| D ₁₋₂ | White | Osram | LE UW Q9WP | LED | 2 |
| D _{BO} | Schottky, 3 A, 100 V _R | Vishay | SS3H10 | Diode | 1 |
| D _Z | 10V | Vishay | Zener Diode | Diode | 1 |
| D _{POL} | 80V Diode | Infineon | BAS1603W | Diode | 1 |
| C _{BO} | 4.7 uF, 50V | EPCOS | X7R | Capacitor | 1 |
| C _{IN} | 100 uF, 50V | Panasonic | EEEFK1H101GP | Capacitor | 1 |
| C _{COMP} | 47 nF | EPCOS | X7R | Capacitor | 1 |
| C _{IVCC} | 1 uF , 6.3V | EPCOS | MLCC CCNPZC105KBW X7R | Capacitor | 1 |
| IC ₁ | -- | Infineon | TLD5098 | IC | 1 |
| IC ₂ | -- | Infineon | XC866 | IC | 1 |
| L ₁ | 22 uH | Coilcraft | MSS1278T | Inductor | 1 |
| R _{DIM1+2} , R _{COMP} , R _{POL} | 10 kΩ, 1% | Panasonic | ERJ3EKF 1002V | Resistor | 4 |
| R _{FB} | 820 mΩ, 1% | Isabellenhütte | SMS – Power Resistor | Resistor | 1 |
| R _{FREQ} | 20 kΩ, 1% | Panasonic | ERJ3EKF 2002V | Resistor | 1 |
| R _{CS} | 50 mΩ, 1% | Isabellenhütte | SMS - Power Resistor | Resistor | 1 |
| T _{DIM1} | 60V, 0.28A | Infineon | BSS138 | Transistor | 1 |
| T _{DIM2} | -60V, -1.9A | Infineon | BSP171 | Transistor | 1 |
| T _{SW} | 100V N-ch, 35A | Infineon | IPG20N10S4L-22 | Transistor | 1 |
| | alternativ: 60V N-ch, 30A | Infineon | IPD30N06S4L-23 | Transistor | 1 |

Figure 29 Bill of Materials for Buck application circuit

Application information

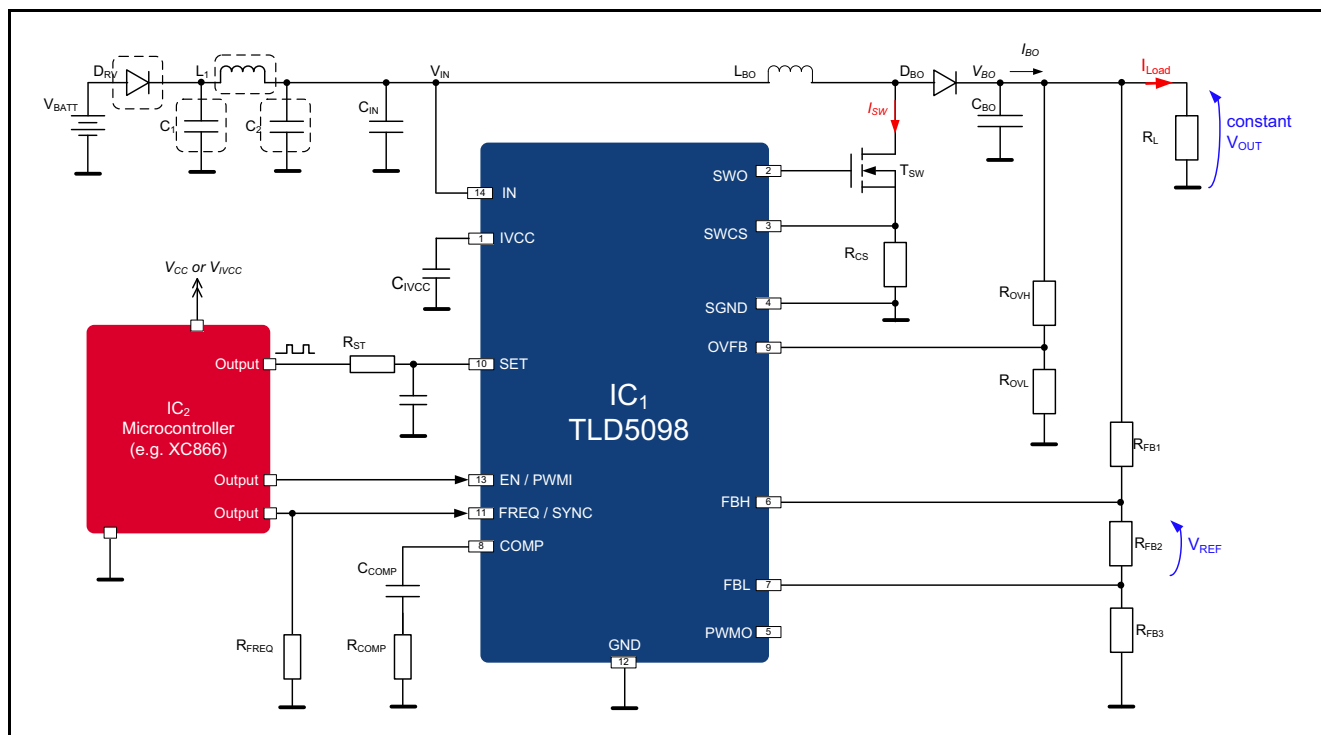


Figure 30 Boost voltage application circuit

| Reference Designator | Value | Manufacturer | Part Number | Type | Quantity |
|-------------------------------------|-----------------------------------|--------------|-----------------|------------|----------|
| D ₁₋₁₀ | White | Osram | LW W5AP | Diode | 10 |
| D _{BO} | Schottky, 3 A, 100 V _R | Vishay | SS3H10 | Diode | 1 |
| C _{BO} | 100 uF, 80V | Panasonic | EEVFK1K101Q | Capacitor | 1 |
| C _{IN} | 100 uF, 50V | Panasonic | EEEFK1H101GP | Capacitor | 1 |
| C _{COMP} | 10 nF, 16V | EPCOS | X7R | Capacitor | 1 |
| C _{IVCC} | 1 uF, 6.3V | Panasonic | X7R | Capacitor | 1 |
| IC ₁ | -- | Infineon | TLD5098 | IC | 1 |
| IC ₂ | -- | Infineon | XC866 | IC | 1 |
| L _{BO} | 100 uH | Coilcraft | MSS1278T-104ML_ | Inductor | 1 |
| R _{COMP} | 10 kohms, 1% | Panasonic | ERJ3EKF 1002V | Resistor | 1 |
| R _{FB1} , R _{FB3} | 51 kohms, 1% | Panasonic | ERJ3EKF 5102V | Resistor | 1 |
| R _{FB2} | 1 kohms, 1% | Panasonic | ERJ3EKF 1001V | Resistor | 1 |
| R _{FREQ} , R _{ST} | 20 kohms, 1% | Panasonic | ERJ3EKF 2002V | Resistor | 2 |
| R _{OVH} | 33.2 kohms, 1% | Panasonic | ERJ3EKF 3322V | Resistor | 1 |
| R _{OVL} | 1 kohms, 1% | Panasonic | ERJ3EKF 1001V | Resistor | 1 |
| R _{CS} | 50 mohms, 1% | Panasonic | ERJB1CFR05U | Resistor | 1 |
| T _{SW} | N-ch, OptiMOS-T2 100V | Infineon | IPD35N10S3L-26 | Transistor | 1 |

Figure 31 Bill of Materials for Boost voltage application circuit

Note: The application drawings and corresponding bill of materials are simplified examples. Optimization of the external components must be done accordingly to specific application requirements.

Application information

11.1 Further application information

- For further information you may contact <http://www.infineon.com/>
- Application Note: TLD509x DC-DC Multitopology Controller IC “Dimensioning and Stability Guideline - Theory and Practice”

12 Package outlines

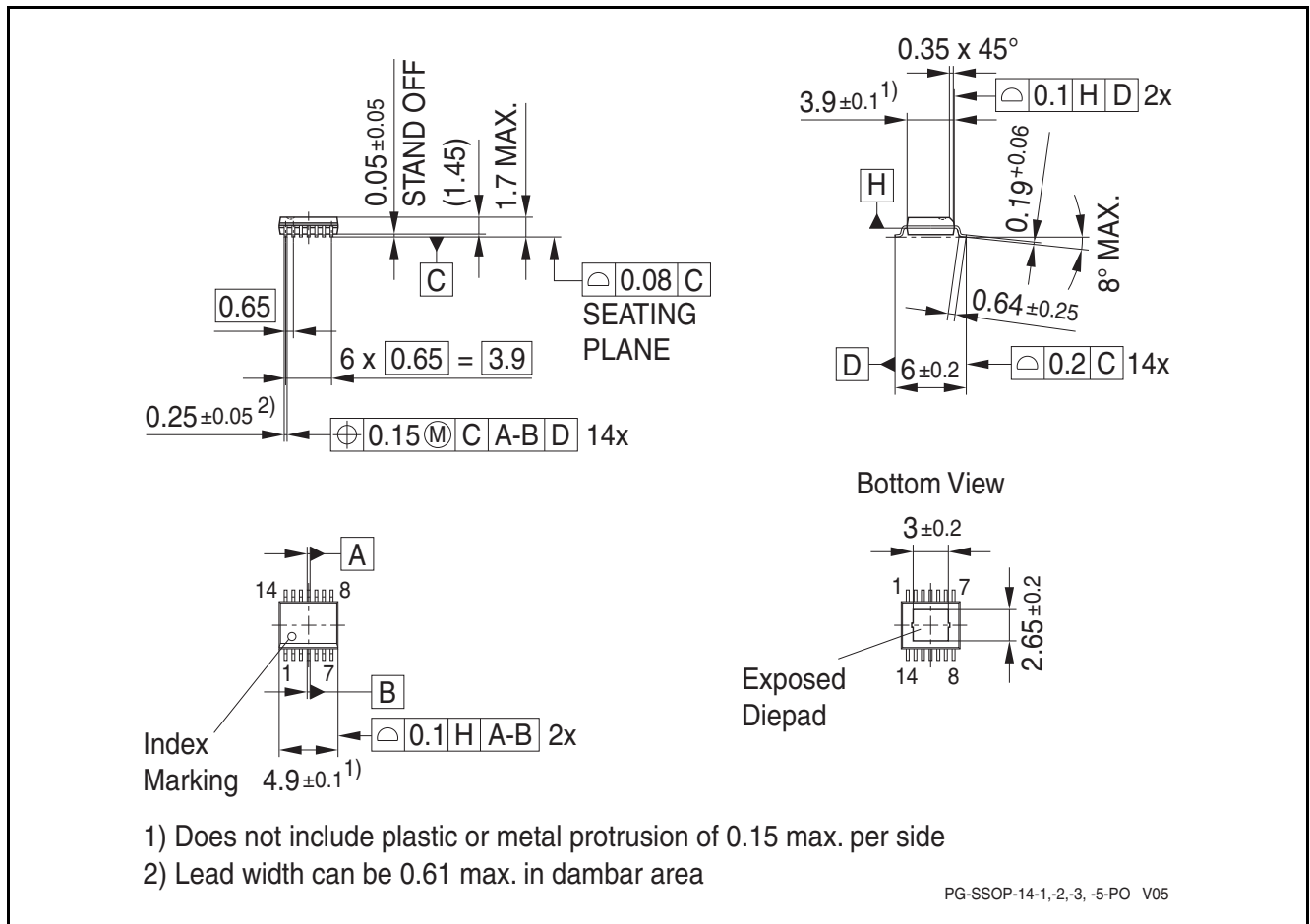


Figure 32 Outline PG-SSOP-14-3

Green product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

Further information on packages

<https://www.infineon.com/packages>

Revision history

13 Revision history

| Revision | Date | Changes |
|----------|------------|--|
| 1.3 | 2018-10-08 | Template update P_4.1.3 → added footnote P_4.3.2 to P_4.3.4 → added footnote |
| 1.2 | 2015-02-12 | Brand name change to LITIX™ Power |

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