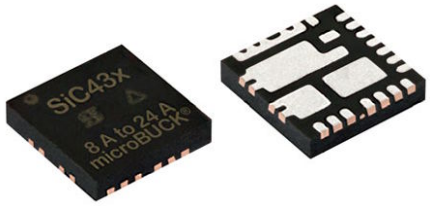
3 V to 24 V Input, 24 A microBUCK® DC/DC Converter



DESCRIPTION

The SiC431 is a synchronous buck regulator with integrated high side and low side power MOSFETs. Its power stage is capable of supplying 24 A continuous current at up to 1 MHz switching frequency. This regulator produces an adjustable output voltage down to 0.6 V from 3 V to 24 V input rail to accommodate a variety of applications, including computing, consumer electronics, telecom, and industrial.

SiC431's architecture supports ultrafast transient response with minimum output capacitance and tight ripple regulation at very light load. The device is internally compensated and no external ESR network is required for loop stability purposes. The device also incorporates a power saving scheme that significantly increases light load efficiency.

The regulator integrates a full protection feature set, including output over voltage protection (OVP), cycle by cycle over current protection (OCP) short circuit protection (SCP) and thermal shutdown (OTP). It also has UVLO and a user programmable soft start.

The SiC431 is available in lead (Pb)-free power enhanced MLP44-24L package in 4 mm x 4 mm dimension.

APPLICATIONS

- 5 V, 12 V, and 24 V input rail POLs
- Desktop, notebooks, server, and industrial computing
- Industrial and automation
- consumer electronics

FEATURES

RoHS COMPLIANT
HALOGEN FREE

- Versatile
  - Operation from 3 V to 24 V input voltage
  - Adjustable output voltage down to 0.6 V
  - Scalable solution 8 A (SiC438), 12 A (SiC437), and 24 A (SiC431)
  - Output voltage tracking and sequencing with pre-bias start up
  - ± 1 % output voltage accuracy from -40 °C to +125 °C
- Highly efficient
  - 97 % peak efficiency
  - 1 µA supply current at shutdown
  - 50 µA operating current, not switching
- Highly configurable
  - Four programmable switching frequencies available: 300 kHz, 500 kHz, 750 kHz, and 1 MHz
  - Adjustable soft start and adjustable current limit
  - Three modes of operation: forced continuous conduction, power save (SiC431B, SiC431D), or ultrasonic (SiC431A, SiC431C)
- Robust and reliable
  - Cycle-by-cycle current limit
  - Output overvoltage protection
  - Output undervoltage / short circuit protection with auto retry
  - Power good flag and over temperature protection
- Design tools
  - Supported by Vishay PowerCAD Online Design Simulation (www.vishay.com/power-ics/powercad-list/)
  - Design Support Kit (www.vishay.com/ppg?74589)
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

TYPICAL APPLICATION CIRCUIT AND PACKAGE OPTIONS

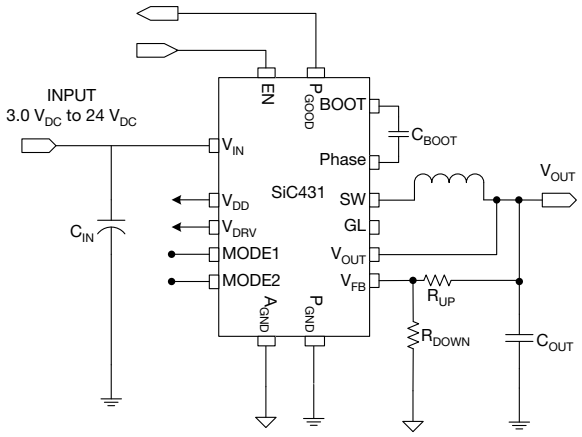


Fig. 1 - Typical Application Circuit for SiC431

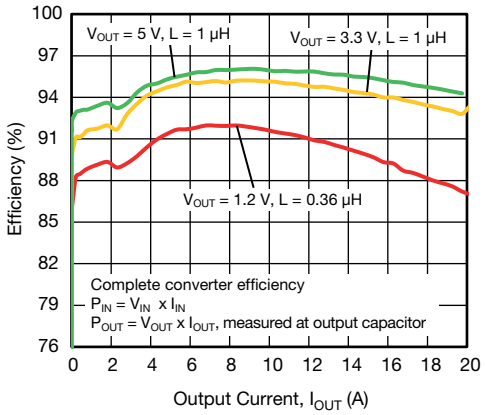


Fig. 2 - Efficiency vs. Output Current (V_{IN} = 12 V, f_{sw} = 500 kHz, Full Load)

PIN CONFIGURATION

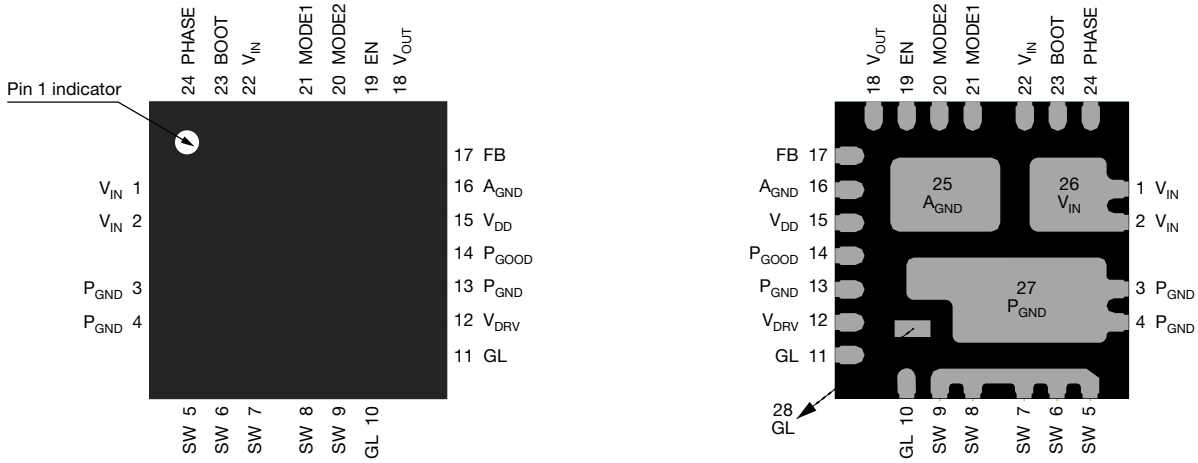


Fig. 3 - SiC431 Pin Configuration

PIN DESCRIPTION		
PIN NUMBER	**SYMBOL**	**DESCRIPTION**
1, 2, 22, 26	V_{IN}	Input voltage
3, 4, 13, 27	P_{GND}	Power signal return ground
5 to 9	SW	Switching node signal; output inductor connection point
10, 11, 28	GL	Low side power MOSFET gate signal
12	V_{DRV}	Supply voltage for internal gate driver. Connect a 2.2 µF decoupling capacitor to P_{GND}
14	P_{GOOD}	Power good signal output; open drain
15	V_{DD}	Supply voltage for internal logic. Connect a 1 µF decoupling capacitor to A_{GND}
16, 25	A_{GND}	Analog signal return ground
17	FB	Output voltage feedback pin; connect to V_{OUT} through a resistor divider network.
18	V_{OUT}	Output voltage sense pin
19	EN	Enable pin
20	MODE2	Soft start and current limit selection; connect a resistor to V_{DD} or A_{GND} per Table 2
21	MODE1	Operating mode and switching frequency selection; connect a resistor to V_{DD} or A_{GND} per Table 1
23	BOOT	Bootstrap pin; connect a capacitor to PHASE pin for HS power MOSFET gate voltage supply
24	PHASE	Switching node signal for bootstrap return path

ORDERING INFORMATION

PART NUMBER	PART MARKING	MAXIMUM CURRENT	V_{DD}, V_{DRV}	LIGHT LOAD MODE	OPERATING JUNCTION TEMPERATURE	PACKAGE
SiC431AED-T1-GE3	SiC431A	24 A	Internal	Ultrasonic	-40 °C to +125 °C	PowerPAK® MLP44-24L
SiC431BED-T1-GE3	SiC431B			Power saving		
SiC431CED-T1-GE3	SiC431C		External	Ultrasonic		
SiC431DED-T1-GE3	SiC431D			Power saving		

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)			
ELECTRICAL PARAMETER	**CONDITIONS**	**LIMITS**	**UNIT**
V_{IN}	Reference to P_{GND}	-0.3 to +25	V
V_{OUT}	Reference to P_{GND}	-0.3 to +22	
V_{DD} / V_{DRV}	Reference to P_{GND}	-0.3 to +6	
SW / PHASE	Reference to P_{GND}	-0.3 to +25	
SW / PHASE (AC)	100 ns; reference to P_{GND}	-8 to +30	
BOOT	Reference to P_{GND}	-0.3 to +31	
BOOT to SW		-0.3 to +6	
A_{GND} to P_{GND}		-0.3 to +0.3	
EN	Reference to A_{GND}	-0.3 to +25	
All other pins	Reference to A_{GND}	-0.3 to +6	
Temperature			
Junction temperature	T_J	-40 to +150	°C
Storage temperature	T_{STG}	-65 to +150	
Power Dissipation			
Junction-to-ambient thermal impedance ($R_{\theta JA}$)		16	°C/W
Junction-to-case thermal impedance ($R_{\theta JC}$)		2	
Maximum power dissipation	Ambient temperature = 25 °C	7.75	W
ESD Protection			
Electrostatic discharge protection	Human body model	4000	V
	Charged device model	1000	

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating/conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (all voltages referenced to A_{GND}, P_{GND} = 0 V)				
PARAMETER	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Input voltage (V_{IN}) (SiC431A, SiC431B)	4.5	-	24	V
Input voltage (V_{IN}) (SiC431C, SiC431D)	3	-	24	
Logic supply voltage, gate driver supply voltage (V_{DD}, V_{DRV}) (SiC431C, SiC431D)	4.5	5	5.5	
Enable (EN)	0	-	24	
Output voltage (V_{OUT})	0.6	-	0.9 x V_{IN} and < 20 V	
Temperature				
Recommended ambient temperature	-40 to +105			°C
Operating junction temperature	-40 to +125			

ELECTRICAL SPECIFICATIONS (V_{IN} = 12 V, V_{EN} = 5 V, T_J = -40 °C to +125 °C, unless otherwise stated)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Power Supplies						
V_{DD} supply	V_{DD}	V_{IN} = 6 V to 24 V (SiC431A, SiC431B)	4.75	5	5.25	V
V_{DD} UVLO threshold, rising	V_{DD_UVLO}		3.3	3.6	3.9	
V_{DD} UVLO hysteresis	$V_{DD\_UVLO\_HYST}$		-	300	-	mV
Maximum V_{DD} current	I_{DD}	V_{IN} = 6 V to 24 V	3	-	-	mA
V_{DRV} supply	V_{DRV}	V_{IN} = 6 V to 24 V (SiC431A, SiC431B)	4.75	5	5.25	V
Maximum V_{DRV} current	I_{DRV}	V_{IN} = 6 V to 24 V	50	-	-	mA
Input current	I_{IN}	Non-switching, V_{FB} > 0.6 V	-	50	120	µA
Shutdown current	I_{IN_SHDN}	V_{EN} = 0 V	-	0.5	3	
Controller and Timing						
Feedback voltage	V_{FB}	T_J = 25 °C	597	600	603	m/V
		T_J = -40 °C to +125 °C (1)	594	600	606	
V_{FB} input bias current	I_{FB}		-	2	-	nA
Minimum on-time	$t_{ON\_MIN.}$		-	50	65	ns
t_{ON} accuracy	$t_{ON\_ACCURACY}$		-10	-	10	%
On-time range	t_{ON_RANGE}		65	-	2250	ns
Minimum frequency, skip mode	$f_{SW\_MIN.}$	Ultrasonic version (SiC431A, SiC431C)	20	-	30	kHz
		Power save version (SiC431B, SiC431D)	0	-	-	
Minimum off-time	$t_{OFF\_MIN.}$		205	250	305	ns
Power MOSFETs						
High side on resistance	R_{ON_HS}	V_{DRV} = 5 V, T_A = 25 °C	-	6	-	mΩ
Low side on resistance	R_{ON_LS}		-	2	-	
Fault Protections						
Over current protection (inductor valley current)	I_{OCP}	T_J = -10 °C to +125 °C	-20	-	20	%
Output OVP threshold	V_{OVP}	V_{FB} with respect to 0.6 V reference	-	20	-	
Output UVP threshold	V_{UVP}		-	-80	-	
Over temperature protection	T_{OTP_RISING}	Rising temperature	-	150	-	°C
	T_{OTP_HYST}	Hysteresis	-	25	-	
Power Good						
Power good output threshold	$V_{FB\_RISING\_VTH\_OV}$	V_{FB} rising above 0.6 V reference	-	20	-	%
	$V_{FB\_FALLING\_VTH\_UV}$	V_{FB} falling below 0.6 V reference	-	-10	-	
Power good hysteresis	V_{FB_HYST}		-	40	-	mV
Power good on resistance	R_{ON_PGOOD}		-	7.5	15	Ω
Power good delay time	t_{DLY_PGOOD}		15	25	35	µs
EN / MODE / Ultrasonic Threshold						
EN logic high level	V_{EN_H}		1.6	-	-	V
EN logic low level	V_{EN_L}		-	-	0.4	
EN pull down resistance	R_{EN}		-	5	-	MΩ
Switching Frequency						
MODE1 (switching frequency)	R_{MODE1}	f_{SW} = 300 kHz	-	51	55	kΩ
		f_{SW} = 500 kHz	90	100	110	
		f_{SW} = 750 kHz	180	200	220	
		f_{SW} = 1000 kHz	450	499	-	
Soft Start						
Soft start time	t_{ss}	Connect R_{MODE2} between MODE2 and A_{GND}	1.8	3	4.2	ms
		Connect R_{MODE2} between MODE2 and V_{DD}	3.6	6	8.4	
Over Current Protection						
MODE2 (over current protection)	R_{MODE2}	I_{OCP} = 32 A	450	499	-	kΩ
		I_{OCP} = 24.8 A	180	200	220	
		I_{OCP} = 17.3 A	90	100	110	
		I_{OCP} = 9.6 A	-	51	55	

Note
(1) Guaranteed by design

FUNCTIONAL BLOCK DIAGRAM

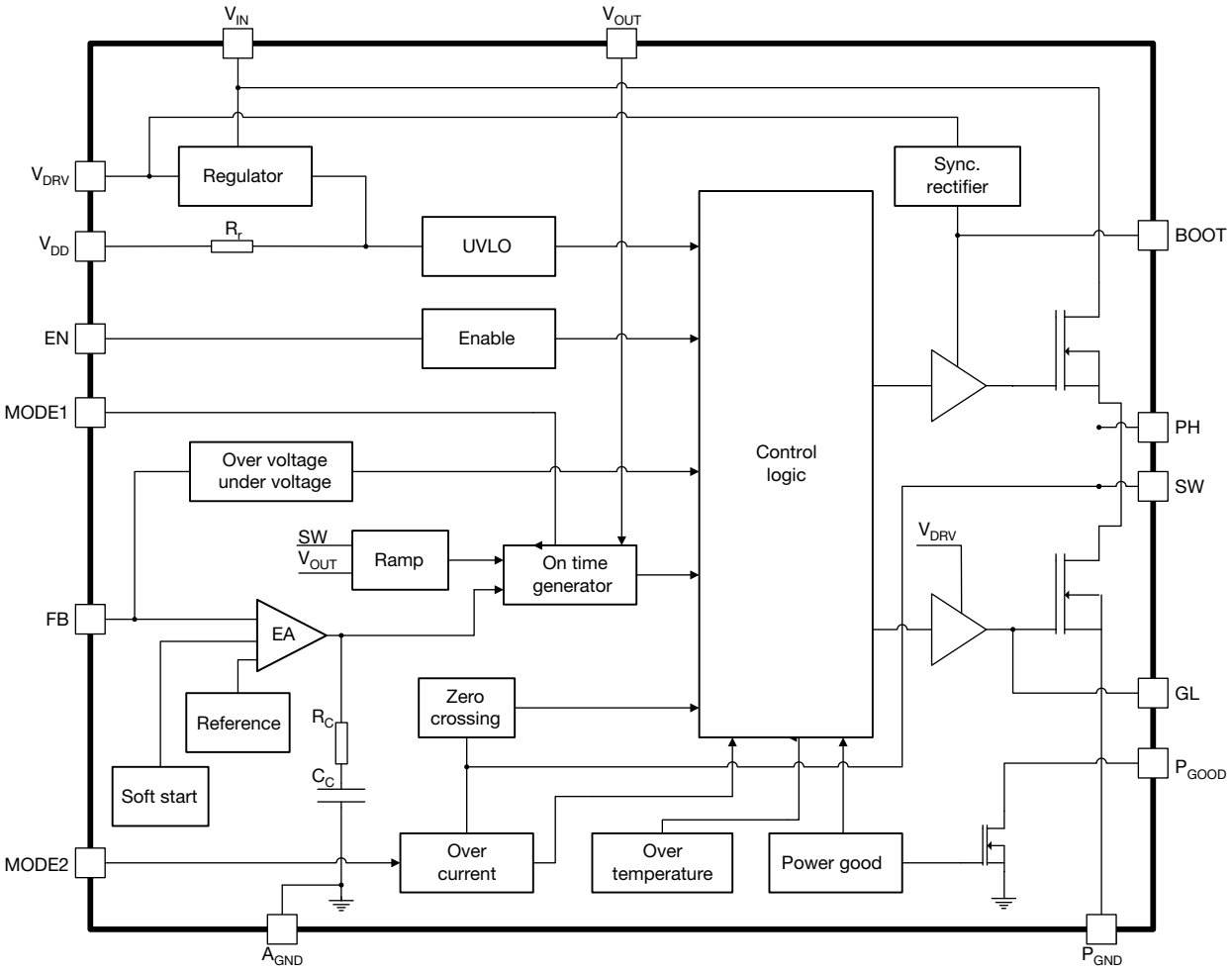


Fig. 4 - SiC431 Functional Block Diagram

OPERATIONAL DESCRIPTION

Device Overview

SiC431 is a high efficiency synchronous buck regulator capable of delivering up to 24 A continuous current. The device has user programmable switching frequency of 300 kHz, 500 kHz, 750 kHz, and 1 MHz. The control scheme delivers fast transient response and minimizes the number of external components. Thanks to the internal ramp information, no high ESR output bulk or virtual ESR network is required for the loop stability. This device also incorporates a power saving feature that enables diode emulation mode and frequency fold back as the load decreases.

SiC431 has a full set of protection and monitoring features:

- Over current protection in pulse-by-pulse mode
- Output over voltage protection
- Output under voltage protection with device latch
- Over temperature protection with hysteresis
- Dedicated enable pin for easy power sequencing
- Power good open drain output

This device is available in MLP44-24L package to deliver high power density and minimize PCB area.

Power Stage

SiC431 integrates a high performance power stage with a 2 mΩ n-channel low side MOSFET and a 6 mΩ n-channel high side MOSFET. The MOSFETs are optimized to achieve up to 97 % efficiency.

The input voltage (V_{IN}) can go up to 24 V and down to as low as 3 V for power conversion. For input voltages (V_{IN}) below 4.5 V an external V_{DD} and V_{DRV} supply is required (SiC431C, SiC431D). For input voltages (V_{IN}) above 4.5 V only a single input supply is required (SiC431A, SiC431B).

Control Mechanism

SiC431 employs an advanced voltage - mode COT control mechanism. During steady-state operation, feedback voltage (V_{FB}) is compared with internal reference (0.6 V typ.) and the amplified error signal (V_{COMP}) is generated at the internal comp node. An internally generated ramp signal and V_{COMP} feed into a comparator. Once V_{RAMP} crosses V_{COMP}, an on-time pulse is generated for a fixed time. During the on-time pulse, the high side MOSFET will be turned on. Once the on-time pulse expires, the low side MOSFET will be turned on after a dead time period. The low side MOSFET will stay on for a minimum duration equal to the minimum off-time ($t_{OFF\_MIN.}$) and remains on until V_{RAMP} crosses V_{COMP}. The cycle is then repeated.

Fig. 5 illustrates the basic block diagram for VM-COT architecture. In this architecture the following is achieved:

- The reference of a basic ripple control regulator is replaced with a high again error amplifier loop
- This establishes two parallel voltage regulating feedback paths, a fast and slow path
- Fast path is the ripple injection which ensures rapid correction of the transient perturbation
- Slow path is the error amplifier loop which ensures the DC component of the output voltage follows the internal accurate reference voltage

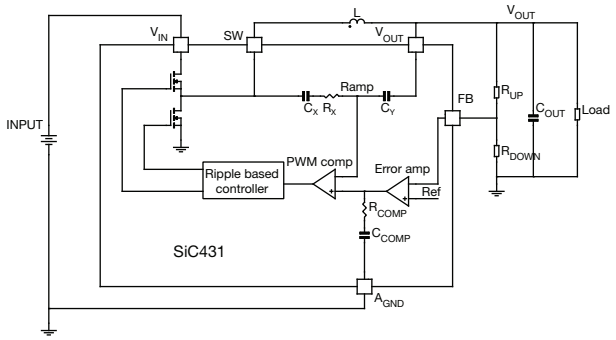


Fig. 5 - VM-COT Block Diagram

All components for RAMP signal generation and error amplifier compensation required for the control loop are internal to the IC, see Fig. 5. In order for the device to cover a wide range of V_{OUT} operation, the internal RAMP signal components (R_X, C_X, C_Y) are automatically selected depending on the V_{OUT} voltage and switching frequency. This method allows the RAMP amplitude to remain constant throughout the V_{OUT} voltage range, achieving low jitter and fast transient Response. The error amplifier internal compensation consists of a resistor in series with a capacitor (R_{COMP}, C_{COMP}).

Fig. 6 demonstrates the basic operational waveforms:

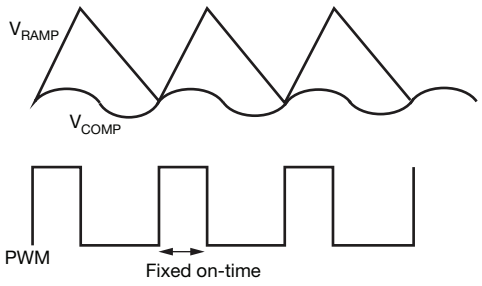


Fig. 6 - VM-COT Operational Principle

Light Load Condition

To improve efficiency at light-load condition, SiC431 provides a set of innovative implementations to eliminate LS recirculating current and switching losses. The internal zero crossing detector monitors SW node voltage to determine when inductor current starts to flow negatively. In power saving mode, as soon as inductor valley current crosses zero, the device deploys diode emulation mode by turning off low side MOSFET. If load further decreases, switching frequency is reduced proportional to load condition to save switching losses while keeping output ripple within tolerance. The switching frequency is set by the controller to maintain regulation. In the standard power save mode, there is no minimum switching frequency (SiC431B, SiC431D).

For SiC431A, SiC431C, the minimum switching frequency that the regulator will reduce to is < 20 kHz as the part avoids switching frequencies in the audible range. This light load mode implementation is called ultrasonic mode.

Mode Setting, Over Current Protection, Switching Frequency, and Soft Start Selection

The SiC431 has a low pin count, minimal external components, and offers the user flexibility to choose soft start times, current limit settings, switching frequencies and to enable or disable the light load mode. Two MODE pins, MODE1 and MODE2, are user programmable by connecting a resistor from MODEx to V_{DD} or A_{GND}, allowing the user to choose various operating modes. This is best explained in the tables below.

TABLE 1 - MODE1 CONFIGURATION SETTINGS

OPERATION	CONNECTION	f_{SWITCH} (kHZ)	R_{MODE1} (kΩ)
Skip	To A_{GND}	300	51
		500	100
		750	200
		1000	499
Forced CCM	To V_{DD}	300	51
		500	100
		750	200
		1000	499

TABLE 2 - MODE2 CONFIGURATION SETTINGS

SOFT-START TIME	CONNECTION	I_{LIMIT} (%)	R_{MODE2} (kΩ)
3 ms	To A_{GND}	30	51
		54	100
		78	200
		100 (32 A)	499
6 ms	To V_{DD}	30	51
		54	100
		78	200
		100 (32 A)	499

OUTPUT MONITORING AND PROTECTION FEATURES

Output Over Current Protection (OCP)

SiC431 has pulse-by-pulse over current limit control. The inductor current is monitored during low side MOSFET conduction time through $R_{DS(on)}$ sensing. After a pre-defined blanking time, the inductor current is compared with an internal OCP threshold. If inductor current is higher than OCP threshold, high side MOSFET is kept off until the inductor current falls below OCP threshold.

OCP is enabled immediately after V_{DD} passes UVLO rising threshold.

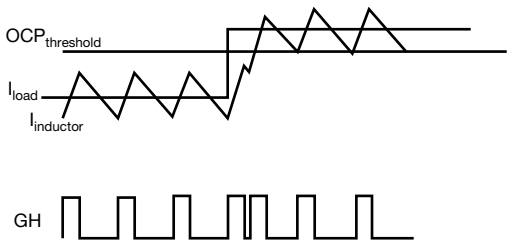


Fig. 7 - Over-Current Protection Illustration

Output Undervoltage Protection (UVP)

UVP is implemented by monitoring the FB pin. If the voltage level at FB drops below 0.12 V for more than 25 µs, a UVP event is recognized and both high side and low side MOSFETs are turned off. After a duration equivalent to 20 soft start periods, the IC attempts to re-start. If the fault condition still exists, the above cycle will be repeated.

UVP is active after the completion of soft start sequence.

Output Overvoltage Protection (OVP)

OVP is implemented by monitoring the FB pin. If the voltage level at FB rising above 0.72 V, a OVP event is recognized and both high side and low side MOSFETs are turned off. Normal operation is resumed once FB voltage drop below 0.68 V.

OVP is active after V_{DD} passes UVLO rising threshold.

Over-Temperature Protection (OTP)

OTP is implemented by monitoring the junction temperature. If the junction temperature rises above 150 °C, a OTP event is recognized and both high side and low MOSFETs are turned off. After the junction temperature falls below 115 °C (35 °C hysteresis), the device restarts by initiating a soft start sequence.

Sequencing of Input / Output Supplies

SiC431 has no sequencing requirements on its supplies or enables (V_{IN}, V_{DD}, V_{DRV}, EN).

Enable

The SiC431 has an enable pin to turn the part on and off. Driving the pin high enables the device, while driving the pin low disables the device.

The EN pin is internally pulled to A_{GND} by a 5 MΩ resistor to prevent unwanted turn on due to a floating GPIO.

Pre-Bias Start-Up

In case of pre-bias startup, output is monitored through FB pin. If the sensed voltage on FB is higher than the internal reference ramp value, control logic prevents high side and low side MOSFETs from switching to avoid negative output voltage spike and excessive current sinking through low side MOSFET.

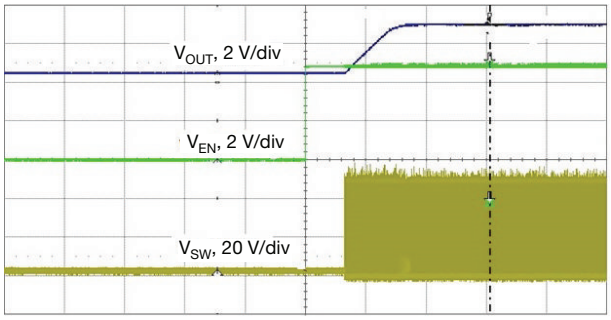


Fig. 8 - Pre-Bias Start-Up

Power Good

SiC431's power good is an open-drain output. Pull P_{GOOD} pin high through a > 10K resistor to use this signal. Power good window is shown in the below diagram. If voltage on FB pin is out of this window, P_{GOOD} signal is de-asserted by pulling down to A_{GND}. To prevent false triggering during transient events, P_{GOOD} has a 25 µs blanking time.

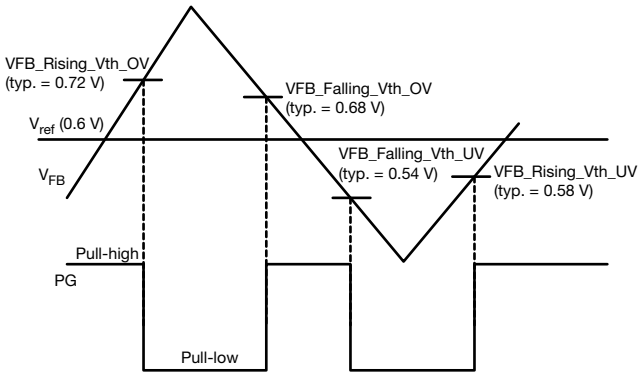


Fig. 9 - P_{GOOD} Window Diagram

ELECTRICAL CHARACTERISTICS

(V_{IN} = 12 V, V_{OUT} = 1.2 V, f_{sw} = 500 kHz, C_{OUT} = 47 µF x 13, C_{IN} = 10 µF x 6, unless otherwise noted)

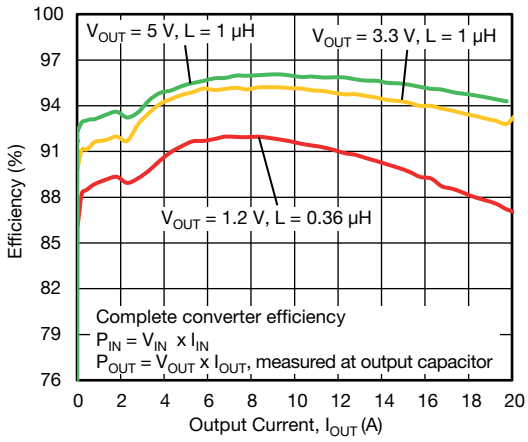


Fig. 10 - Efficiency vs. Output Current (V_{IN} = 12 V, f_{sw} = 500 kHz, Full Load)

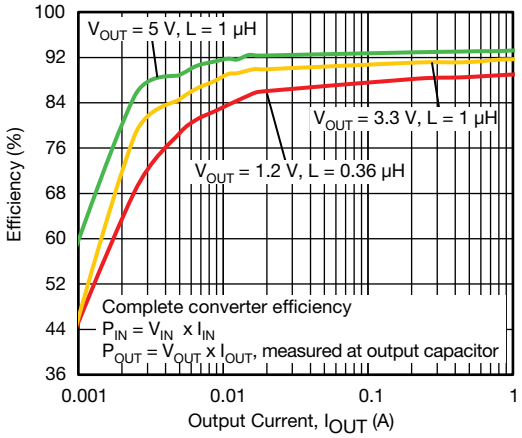


Fig. 13 - Efficiency vs. Output Current (V_{IN} = 12 V, f_{sw} = 500 kHz, Light Load)

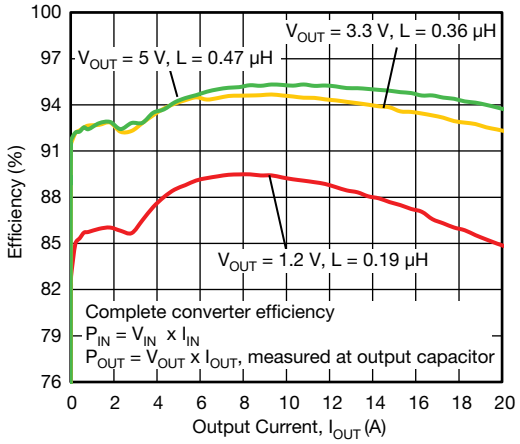


Fig. 11 - Efficiency vs. Output Current (V_{IN} = 12 V, f_{sw} = 1000 kHz, Full Load)

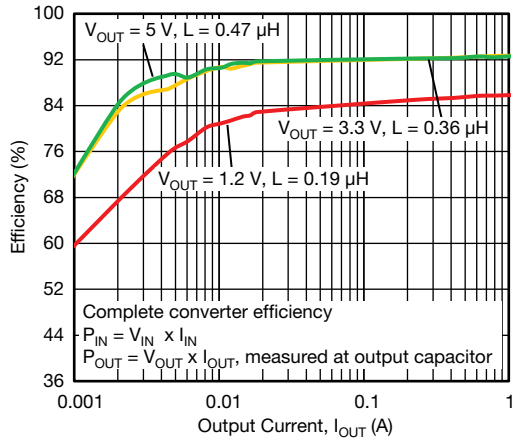


Fig. 14 - Efficiency vs. Output Current (V_{IN} = 12 V, f_{sw} = 1000 kHz, Light Load)

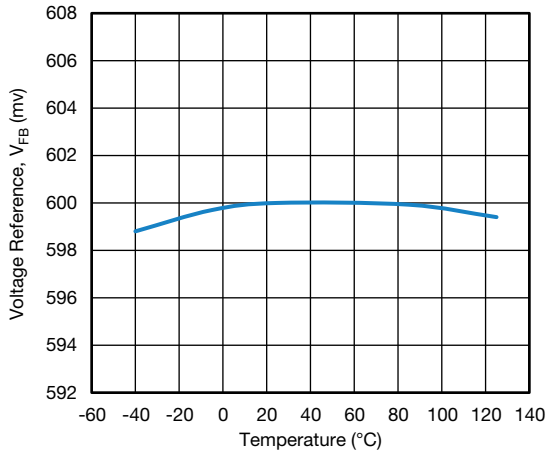


Fig. 12 - Voltage Reference vs. Junction Temperature

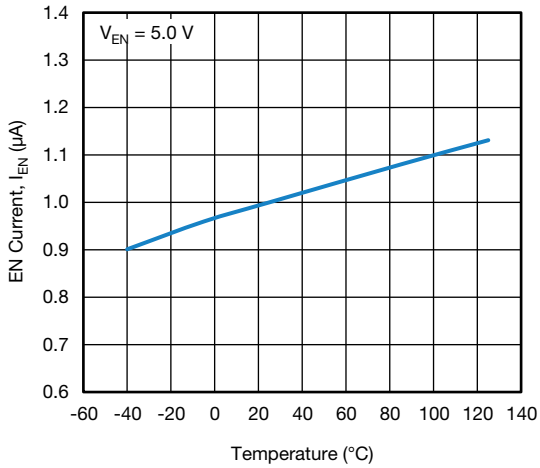


Fig. 15 - EN Current vs. Junction Temperature

ELECTRICAL CHARACTERISTICS

(V_{IN} = 12 V, V_{OUT} = 1.2 V, f_{sw} = 500 kHz, C_{OUT} = 47 µF x 13, C_{IN} = 10 µF x 6, unless otherwise noted)

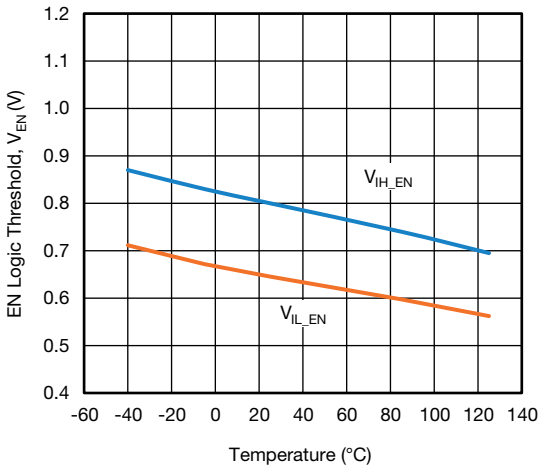


Fig. 16 - EN Logic Threshold vs. Junction Temperature

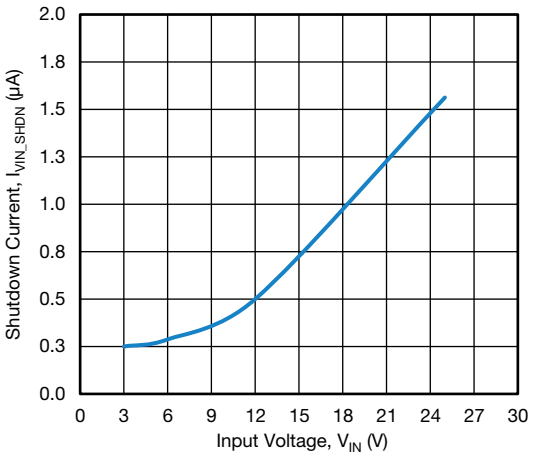


Fig. 19 - Shutdown Current vs. Input Voltage

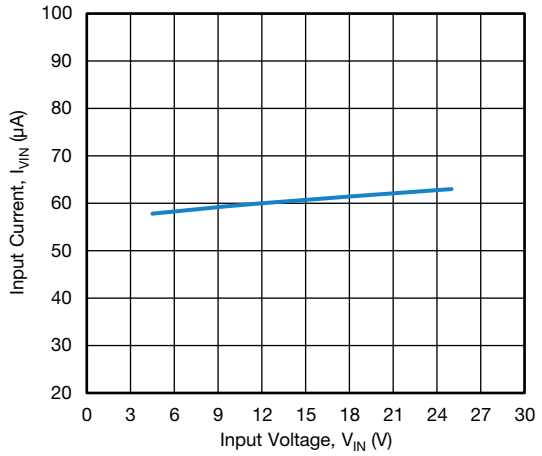


Fig. 17 - Input Current vs. Input Voltage

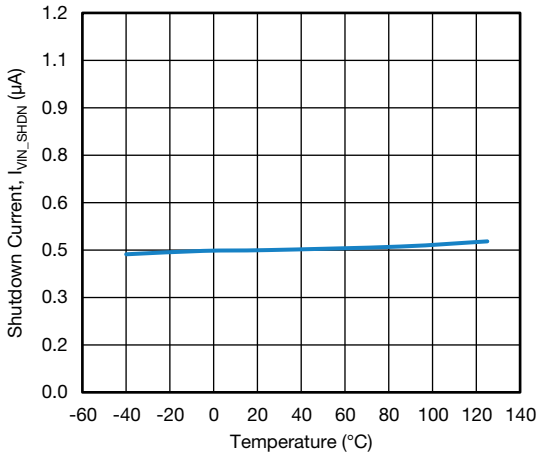


Fig. 20 - Shutdown Current vs. Junction Temperature

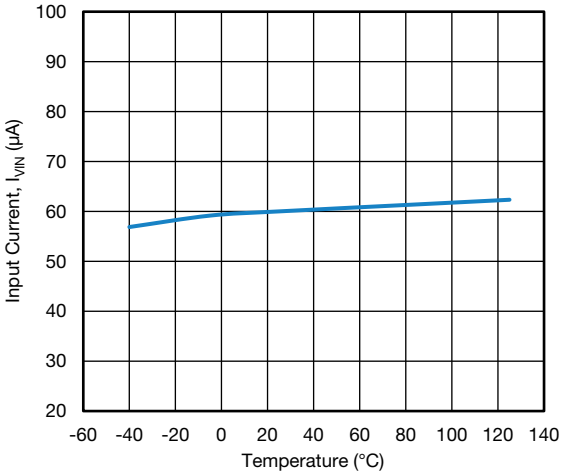


Fig. 18 - Input Current vs. Junction Temperature

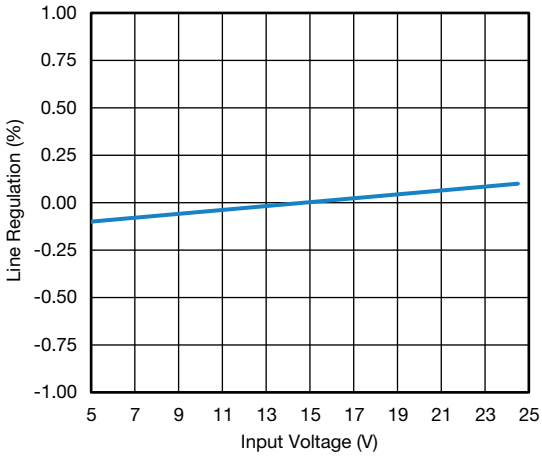


Fig. 21 - Line Regulation vs. Input Voltage

ELECTRICAL CHARACTERISTICS

(V_{IN} = 12 V, V_{OUT} = 1.2 V, f_{sw} = 500 kHz, C_{OUT} = 47 µF x 13, C_{IN} = 10 µF x 6, unless otherwise noted)

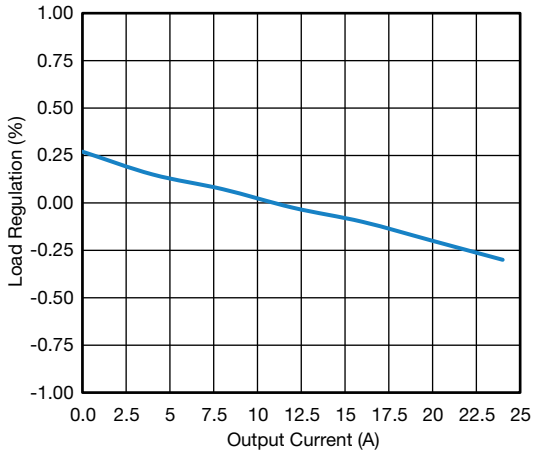


Fig. 22 - Load Regulation vs. Output Current

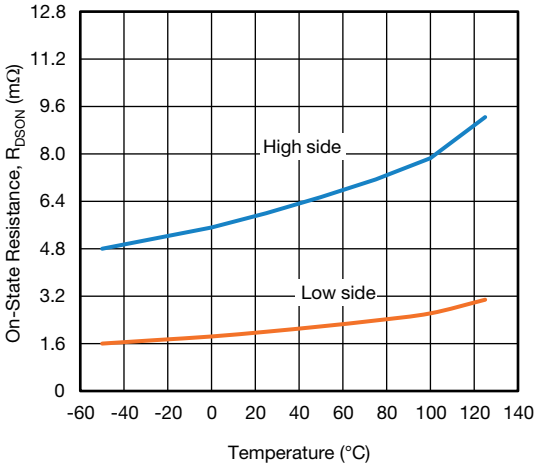


Fig. 23 - On Resistance vs. Junction Temperature

ELECTRICAL CHARACTERISTICS

(V_{IN} = 12 V, V_{OUT} = 1.2 V, f_{sw} = 500 kHz, C_{OUT} = 47 µF x 13, C_{IN} = 10 µF x 6, unless otherwise noted)

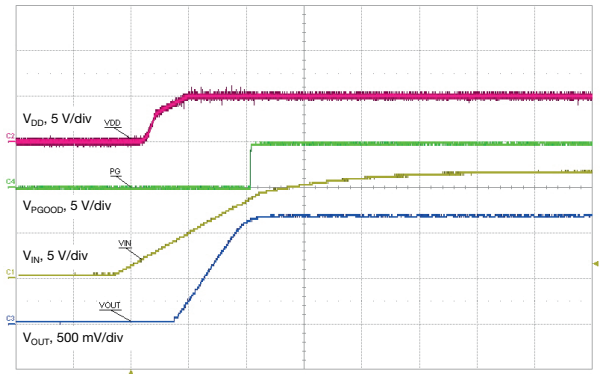


Fig. 24 - Startup with V_{IN}, t = 2 ms/div

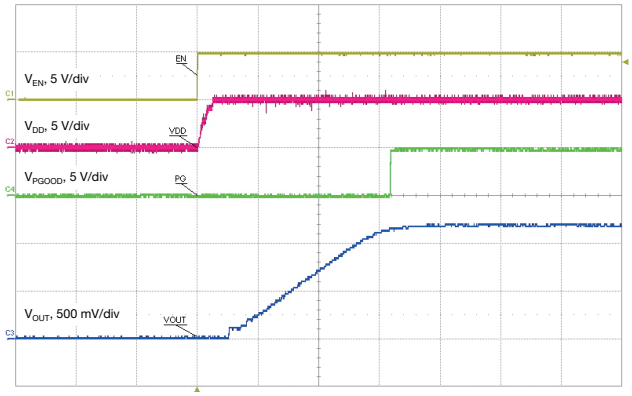


Fig. 27 - Startup with EN, t = 1 ms/div

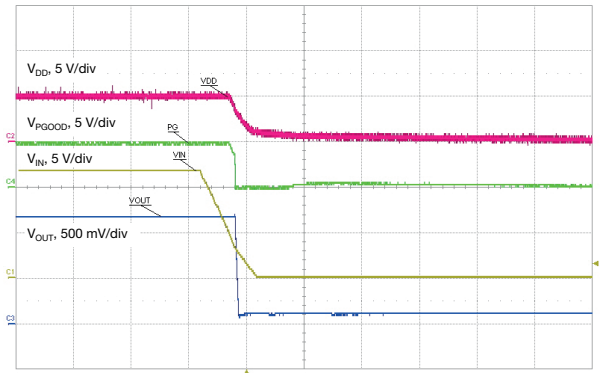


Fig. 25 - Shut down with V_{IN}, t = 100 ms/div

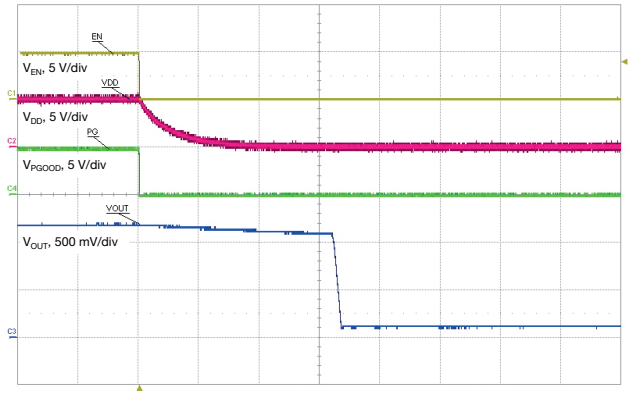


Fig. 28 - Shut down with EN, t = 200 ms/div

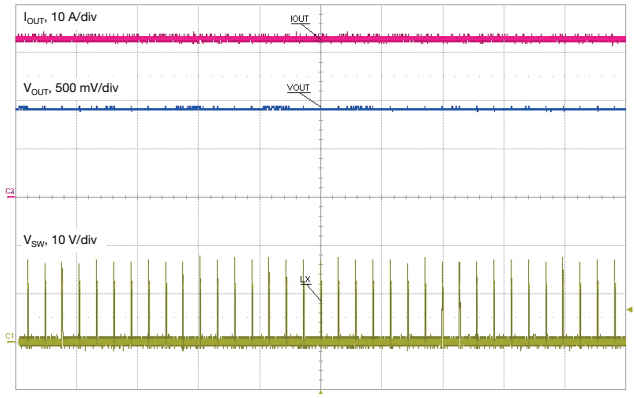


Fig. 26 - Overcurrent Protection Behavior, t = 5 µs/div

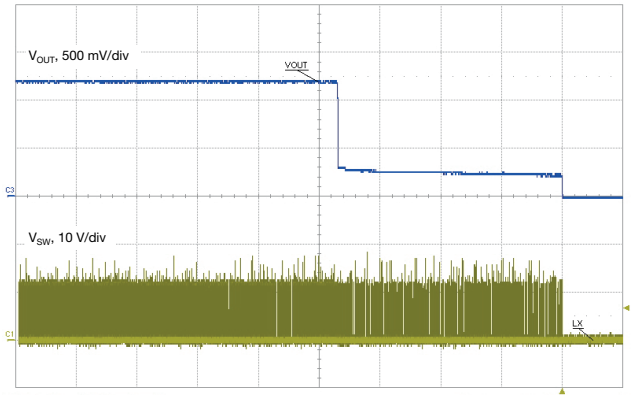


Fig. 29 - Output Undervoltage Protection Behavior, t = 50 ms/div

ELECTRICAL CHARACTERISTICS

(V_{IN} = 12 V, V_{OUT} = 1.2 V, f_{sw} = 500 kHz, C_{OUT} = 47 µF x 13, C_{IN} = 10 µF x 6, unless otherwise noted)

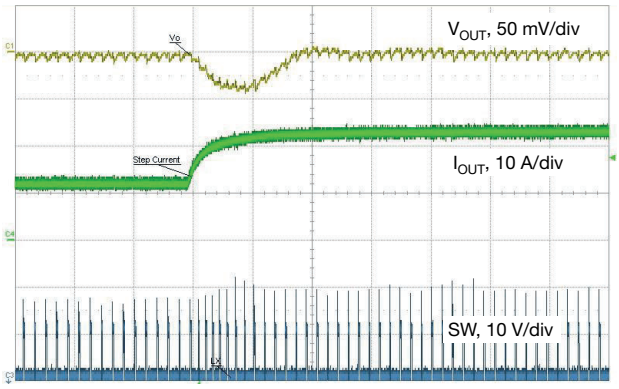


Fig. 30 - Load Step, 12 A to 24 A, 1 A/µs, t = 10 µs/div

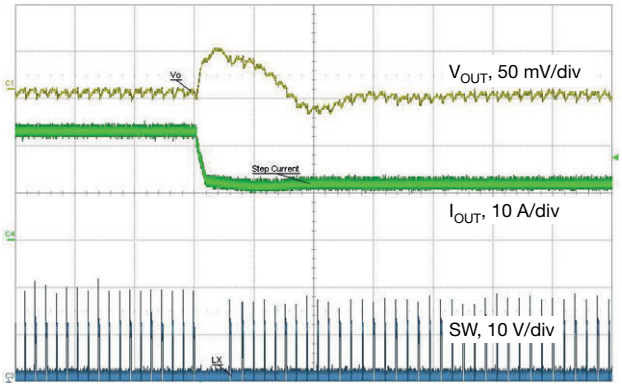


Fig. 33 - Load Release, 24 A to 12 A, 1 A/µs, t = 10 µs/div

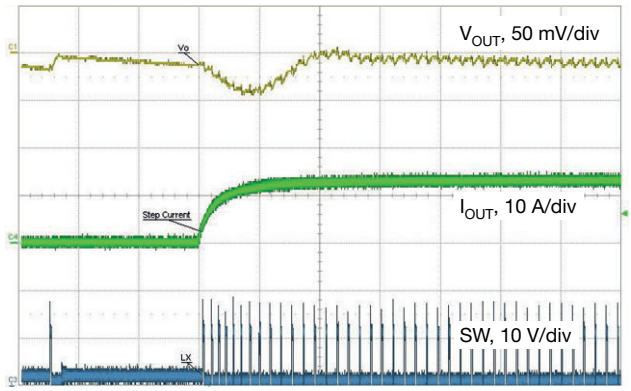


Fig. 31 - Load Step, 0.1 A to 12 A, 1 A/µs, t = 10 µs/div
Skip Mode Enabled

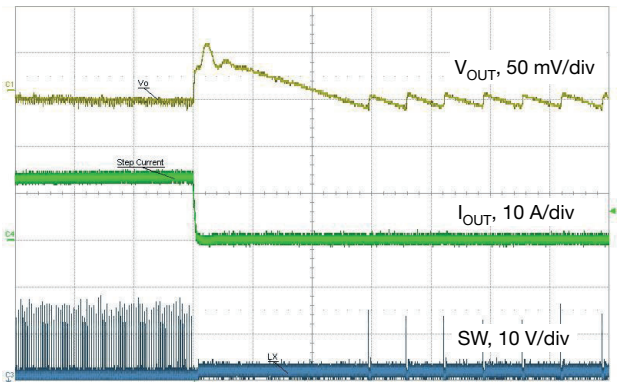


Fig. 34 - Load Release, 12 A to 0.1 A, 1 A/µs, t = 50 µs/div
Skip Mode Enabled

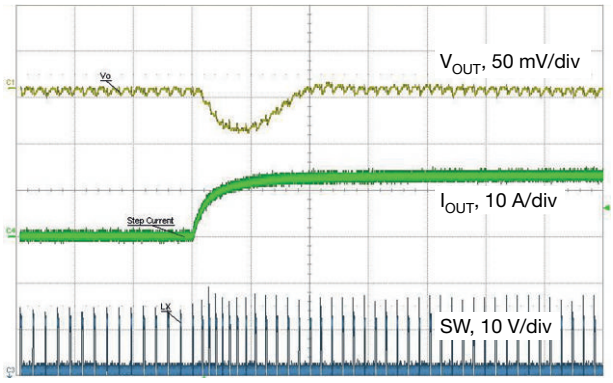


Fig. 32 - Load Step, 0.1 A to 12 A, 1 A/µs, t = 10 µs/div
Forced Continuous Conduction Mode

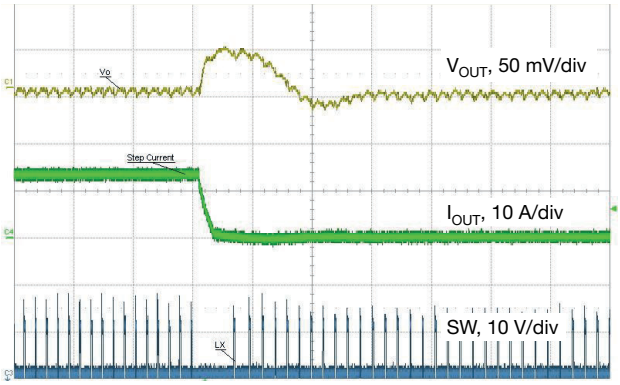


Fig. 35 - Load Release, 12 A to 0.1 A, 1 A/µs, t = 20 µs/div
Forced Continuous Conduction Mode

ELECTRICAL CHARACTERISTICS

(V_{IN} = 12 V, V_{OUT} = 1.2 V, f_{sw} = 500 kHz, C_{OUT} = 47 µF x 13, C_{IN} = 10 µF x 6, unless otherwise noted)

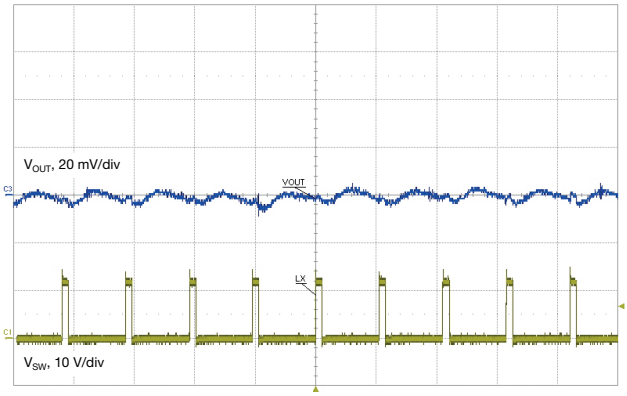


Fig. 36 - Output Ripple, 0.1 A, t = 2 µs/div
Forced Continuous Conduction Mode

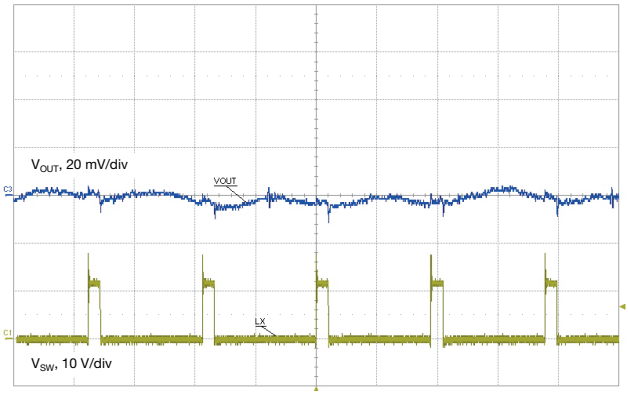


Fig. 38 - Output Ripple, 12 A, t = 1 µs/div
Forced Continuous Conduction Mode

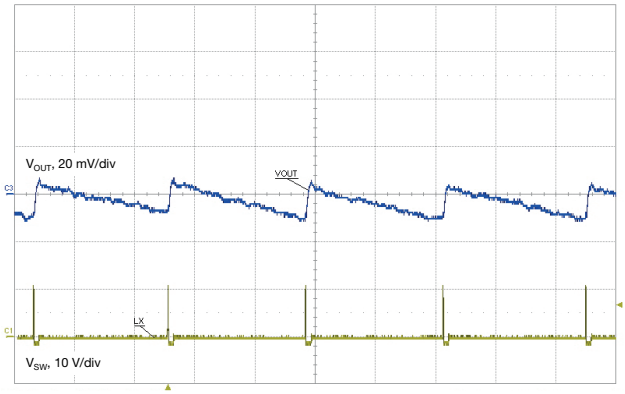


Fig. 37 - Output Ripple, 0.1 A, t = 20 µs/div
Skip Mode Enabled

EXAMPLE SCHEMATIC FOR SiC431

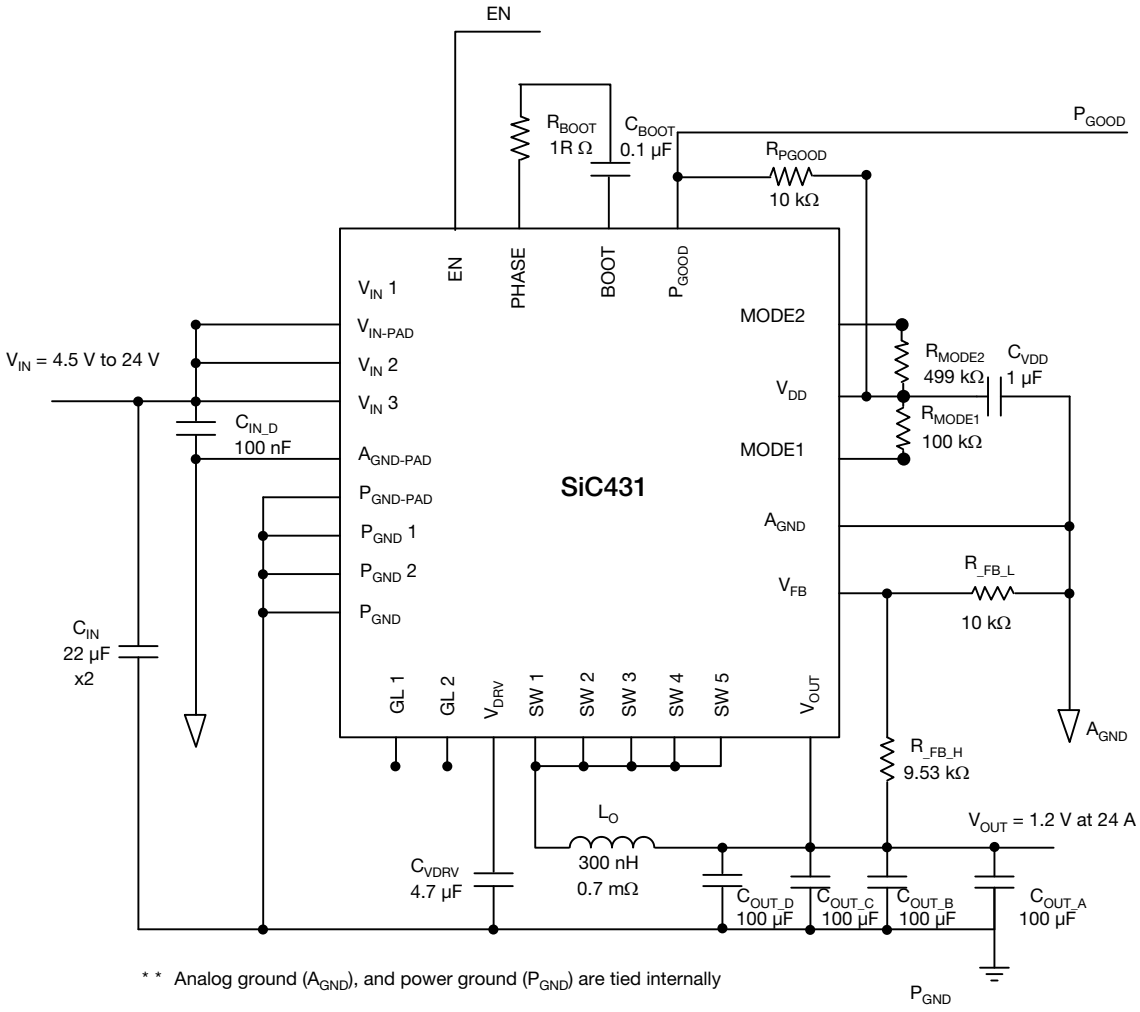


Fig. 39 - Schematic

EXTERNAL COMPONENT SELECTION FOR THE SiC43X

This section explains external component selection for the SiC43x family of regulators. Component reference designators in any equation refer to the schematic shown in Fig. 36.
See PowerCAD online design center to simplify external component calculations.

Output Voltage Adjustment

If a different output voltage is needed, simply change the value of V_{OUT} and solve for $R_{\_FB\_H}$ based on the following formula:

$$R_{\_FB\_H} = \frac{R_{\_FB\_L}(V_{OUT} - V_{FB})}{V_{FB}}$$

Where V_{FB} is 0.6 V for the SiC43X. $R_{\_FB\_L}$ should be a maximum of 10 kΩ to prevent V_{OUT} from drifting at no load.

Inductor Selection

In order to determine the inductance, the ripple current must first be defined. Low inductor values allow for the use of smaller package sizes but create higher ripple current which can reduce efficiency. Higher inductor values will reduce the ripple current and, for a given DC resistance, are more efficient. However, larger inductance translates directly into larger packages and higher cost. Cost, size, output ripple, and efficiency are all used in the selection process.

The ripple current will also set the boundary for power save operation. The SiC431 will typically enter power save mode when the load current decreases to 1/2 of the ripple current. For example, if ripple current is 4 A, power save operation will be active for loads less than 2 A. If ripple current is set at 40 % of maximum load current, power save will typically start at a load which is 20 % of maximum current.

The inductor value is typically selected to provide ripple current of 25 % to 50 % of the maximum load current. This provides an optimal trade-off between cost, efficiency, and transient performance. During the on-time, voltage across the inductor is (V_{IN} - V_{OUT}). The equation for determining inductance is shown below.

$$L_O = \frac{(V_{IN} - V_{OUT}) \times D}{K \times I_{OUT\_MAX.} \times f_{SW}}$$

where, K is the maximum percentage of ripple current, D is the duty cycle, $I_{OUT\_MAX.}$ is the maximum load current and f_{SW} is the switching frequency.

Capacitor Selection

The output capacitors are chosen based upon required ESR and capacitance. The maximum ESR requirement is controlled by the output ripple requirement and the DC tolerance. The output voltage has a DC value that is equal to the valley of the output ripple plus 1/2 of the peak-to-peak ripple. A change in the output ripple voltage will lead to a change in DC voltage at the output.

For instance, the design goal for output voltage ripple is 3 % (45 mV for V_{OUT} = 1.5 V) with ripple current of 4.43 A. The maximum ESR value allowed is shown by the following equation.

$$ESR_{MAX.} = \frac{V_{RIPPLE}}{I_{RIPPLE}} = \frac{45\ mV}{4.43\ A}$$

$$ESR_{MAX.} = 10.2\ m\Omega$$

The output capacitance is usually chosen to meet transient requirements. A worst-case load release (from maximum load to no load) at the moment of peak inductor current, determines the required capacitance. If the load release is instantaneous (maximum load to no load in less than 1 µs) the output capacitor must absorb all the inductor's stored energy. The output capacitor can be calculated according to the following equation.

$$C_{OUT\_MIN.} = \frac{L_O(I_{OUT} + 0.5 \times I_{RIPPLE_{MAX.}})^2}{V_{PK}^2 - V_{OUT}^2}$$

Where I_{OUT} is the output current, $I_{RIPPLE\_MAX.}$ is the maximum ripple current, V_{PK} is the peak V_{OUT} during load release, V_{OUT} is the output voltage.

The duration of the load release is determined by V_{OUT} and the inductor. During load release, the voltage across the inductor is approximately -V_{OUT}, causing a down-slope or falling di/dt in the inductor. If the di/dt of the load is not much larger than di/dt of the inductor, then the inductor current will tend to track the falling load current. This will reduce the excess inductive energy that must be absorbed by the output capacitor; therefore a smaller capacitance can be used.

Under this circumstance, the following equation can be used to calculate the needed capacitance for a given rate of load release (di_{LOAD}/dt).

$$C_{OUT} = \frac{\frac{L \times I_{PK}^2}{V_{OUT}} - (I_{PK} \times I_{RELEASE}) \times \frac{dT}{di_{LOAD}}}{2(V_{PK} - V_{OUT})}$$

$$I_{PK} = I_{RELEASE} + \left(\frac{1}{2} \times I_{RIPPLE_{MAX.}}\right)$$

Where I_{PK} is the peak inductor current, $I_{RIPPLE\_MAX.}$ is the maximum peak to peak inductor current, $I_{RELEASE}$ is the maximum load release current, V_{PK} is the peak V_{OUT} during load release, dI_{LOAD} /dt is the rate of load release.

If the load step does not meet the requirement, increasing the crossover frequency can help by adding feed forward capacitor (C_{FF}) in parallel to the upper feedback resistor to generate another zero and pole. Placing the geometrical mean of this pole and zero around the crossover frequency will result in faster transient response. f_Z and f_P are the generated zero and pole, see equations below.

$$f_Z = \frac{1}{2\pi \times R_{FB1} \times C_{FF}}$$

$$f_P = \frac{1}{2\pi \times (R_{FB1} // R_{FB2}) \times C_{FF}}$$

Where R_{FB1} is the upper feedback resistor, R_{FB2} is the lower feedback resistor C_{FF} is the feed forward capacitor, f_Z is the zero from feed forward capacitor, f_P is the pole frequency generated from the feed forward capacitor.

A calculator is available to assist user to obtain the value of the feed forward capacitance value.

From the calculator, obtain the crossover frequency (f_C). Use the equation below for the calculation of the feed forward capacitance value.

$$f_C = \sqrt{(f_Z \times f_P)}$$

$$C_{FF} = \frac{1}{2\pi \times (f_C \times \sqrt{(R_{FB1} \times (R_{FB1} // R_{FB2}))})}$$

As the internal RC compensation of the SiC431 works with a wide range of output LC filters, the SiC431 offers stable operation for a wide range of output capacitance, making the product versatile and usable in a wide range of applications.

Input Capacitance

In order to determine the minimum capacitance the input voltage ripple needs to be specified; $V_{CINPKPK} \leq 500$ mV is a suitable starting point. This magnitude is determined by the final application specification. The input current needs to be determined for the lowest operating input voltage,

$$I_{CIN(RMS)} = I_O \times \sqrt{D \times (1-D) + \frac{1}{12} \times \left(\frac{V_{OUT}}{L \times f_{sw} \times I_{OUT}}\right)^2 \times (1-D)^2 \times D}$$

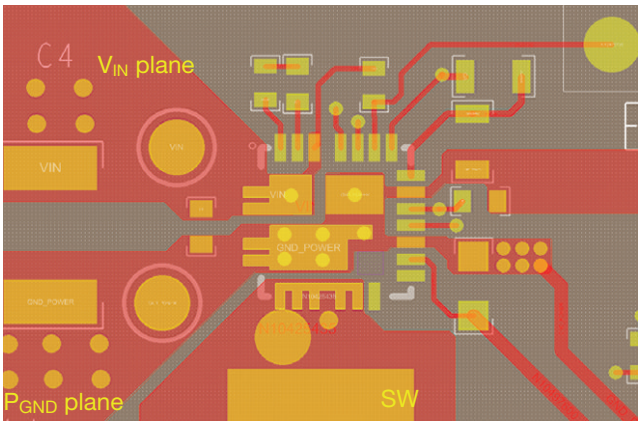
The minimum input capacitance can then be found,

$$C_{IN\_min.} = I_{OUT} \times \frac{D \times (1 - D)}{V_{CINPKPK} \times f_{sw}}$$

If high ESR capacitors are used, it is good practice to also add low ESR ceramic capacitance. A 4.7 µF ceramic input capacitance is a suitable starting point.
Care must be taken to account for voltage derating of the capacitance when choosing an all ceramic input capacitance.

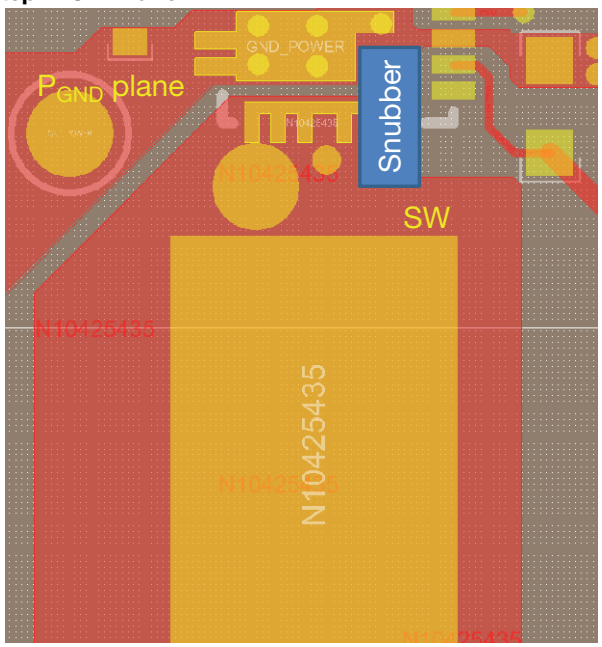
PCB LAYOUT RECOMMENDATIONS

Step 1: V_{IN}/GND Planes and Decoupling



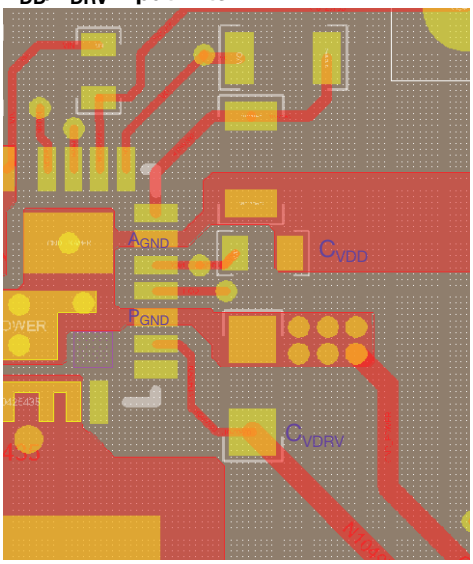
1. Layout V_{IN} and P_{GND} planes as shown above
2. Ceramic capacitors should be placed between V_{IN} and P_{GND}, and very close to the device for best decoupling effect
3. Various ceramic capacitor values and package sizes should be used to cover entire decoupling spectrum e.g. 1210 and 0603
4. Smaller capacitance values, closer to V_{IN} pin(s), provide better high frequency response

Step 2: SW Plane



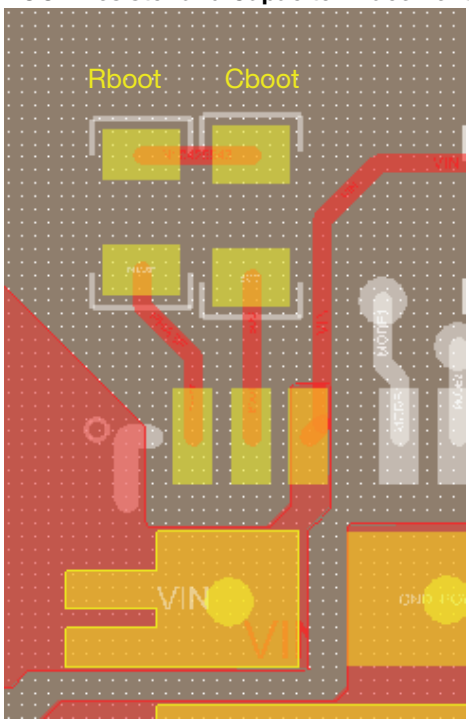
1. Connect output inductor to device with large plane to lower resistance
2. If a snubber network is required, place the components on the bottom layer as shown above

Step 3: V_{DD}/V_{DRV} Input Filter



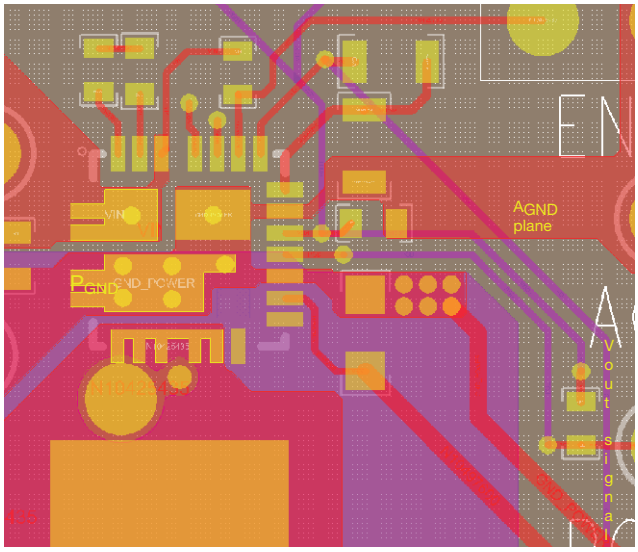
1. C_{VDD} cap should be placed between V_{DD} and A_{GND} to achieve best noise filtering
2. C_{VDRV} cap should be placed close to V_{DRV} and P_{GND} pins to reduce effects of trace impedance and provide maximum instantaneous driver current for low side MOSFET during switching cycle

Step 4: BOOT Resistor and Capacitor Placement



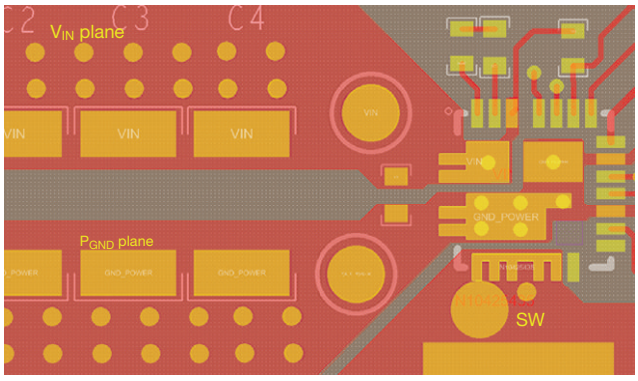
1. C_{BOOT} and R_{BOOT} need to be placed very close to the device, between PHASE and BOOT pins
2. In order to reduce parasitic inductance, it is recommended to use 0402 chip size for the resistor and the capacitor

Step 5: Signal Routing



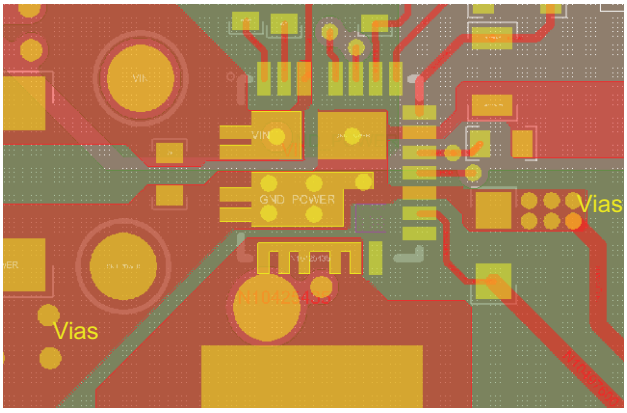
1. Separate the small analog signal from high current path. As shown above, the high paths with high dv/dt, di/dt are placed on the left side of the IC, while the small control signals are placed on the right side of the IC. All the components for small analog signal should be placed closer to IC with minimum trace length
2. IC analog ground (A_{GND}), pin 16, should have a single connection to P_{GND}. The A_{GND} ground plane connected to pin16 helps to keep A_{GND} quiet and improves noise immunity
3. The output signal can be routed through inner layers. Make sure this signal is far away from SW node and shielded by an inner ground layer

Step 6: Thermal Management



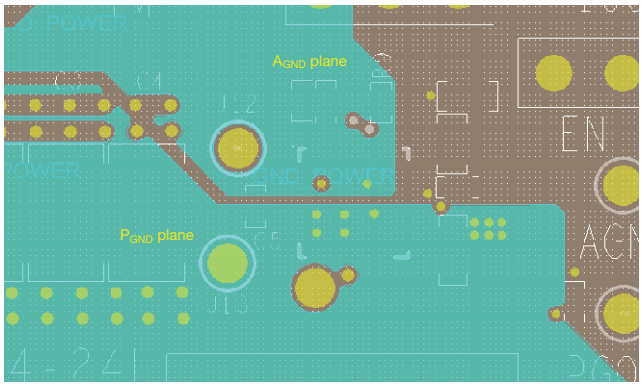
1. Thermal relief vias can be added to the V_{IN} and P_{GND} pads to utilize inner layers for high current and thermal dissipation
2. To achieve better thermal performance, additional vias can be placed on V_{IN} and P_{GND} planes. It is also necessary to duplicate the V_{IN} and ground plane at bottom layer to maximize the power dissipation capability of the PCB
3. SW pad is a noise source and it is not recommended to place vias on this pad
4. 8 mil vias on pads and 10 mil vias on planes are ideal via sizes. The vias on pad may drain solder during assembly and cause assembly issues. Please consult with the assembly house for guideline

Step 7: Ground Connection



1. In order to minimize the ground voltage drop due to high current, it is recommended to place vias on the P_{GND} planes. Make use of the inner ground layers to lower the impedance

Step 7: Ground Layer

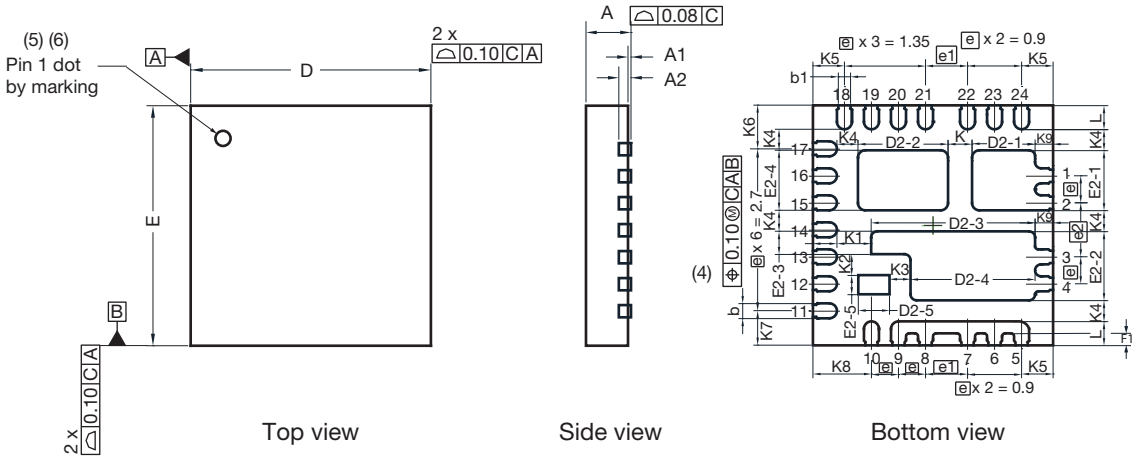


1. It is recommended to make the whole inner 1 layer (next to top layer) ground plane
2. This ground plane provides shielding between noise source on top layer and signal trace within inner layer
3. The ground plane can be broken into two section, P_{GND} and A_{GND}

PRODUCT SUMMARY				
Part number	SiC431A	SiC431B	SiC431C	SiC431D
Description	24 A, 4.5 V to 24 V input, 300 kHz, 500 kHz, 750 kHz, 1 MHz, synchronous buck regulator with ultrasonic mode and internal 5 V bias	24 A, 4.5 V to 24 V input, 300 kHz, 500 kHz, 750 kHz, 1 MHz, synchronous buck regulator with power save mode and internal 5 V bias	24 A, 3 V to 24 V input, 300 kHz, 500 kHz, 750 kHz, 1 MHz, synchronous buck regulator with ultrasonic mode (external 5 V bias)	24 A, 3 V to 24 V input, 300 kHz, 500 kHz, 750 kHz, 1 MHz, synchronous buck regulator with power save mode (external 5 V bias)
Input voltage min. (V)	4.5	4.5	3.0	3.0
Input voltage max. (V)	24	24	24	24
Output voltage min. (V)	0.6	0.6	0.6	0.6
Output voltage max. (V)	0.90 x V_{IN}	0.90 x V_{IN}	0.90 x V_{IN}	0.90 x V_{IN}
Continuous current (A)	24	24	24	24
Switch frequency min. (kHz)	300	300	300	300
Switch frequency max. (kHz)	1000	1000	1000	1000
Pre-bias operation (yes / no)	Y	Y	Y	Y
Internal bias reg. (yes / no)	Y	Y	N	N
Compensation	Internal	Internal	Internal	Internal
Enable (yes / no)	Y	Y	Y	Y
P_{GOOD} (yes / no)	Y	Y	Y	Y
Over current protection	Y	Y	Y	Y
Protection	OVP, OCP, UVP/SCP, OTP, UVLO	OVP, OCP, UVP/SCP, OTP, UVLO	OVP, OCP, UVP/SCP, OTP, UVLO	OVP, OCP, UVP/SCP, OTP, UVLO
Light load mode	Selectable ultrasonic	Selectable powersave	Selectable ultrasonic	Selectable powersave
Peak efficiency (%)	97	97	97	97
Package type	PowerPAK MLP 44-24L	PowerPAK MLP 44-24L	PowerPAK MLP 44-24L	PowerPAK MLP 44-24L
Package size (W, L, H) (mm)	4 x 4 x 0.75	4 x 4 x 0.75	4 x 4 x 0.75	4 x 4 x 0.75
Status code	1	1	1	1
Product type	microBUCK (step down regulator)	microBUCK (step down regulator)	microBUCK (step down regulator)	microBUCK (step down regulator)
Applications	Computers, consumer, industrial, healthcare, networking	Computers, consumer, industrial, healthcare, networking	Computers, consumer, industrial, healthcare, networking	Computers, consumer, industrial, healthcare, networking

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?74589.

PowerPAK® MLP24-44 Case Outline

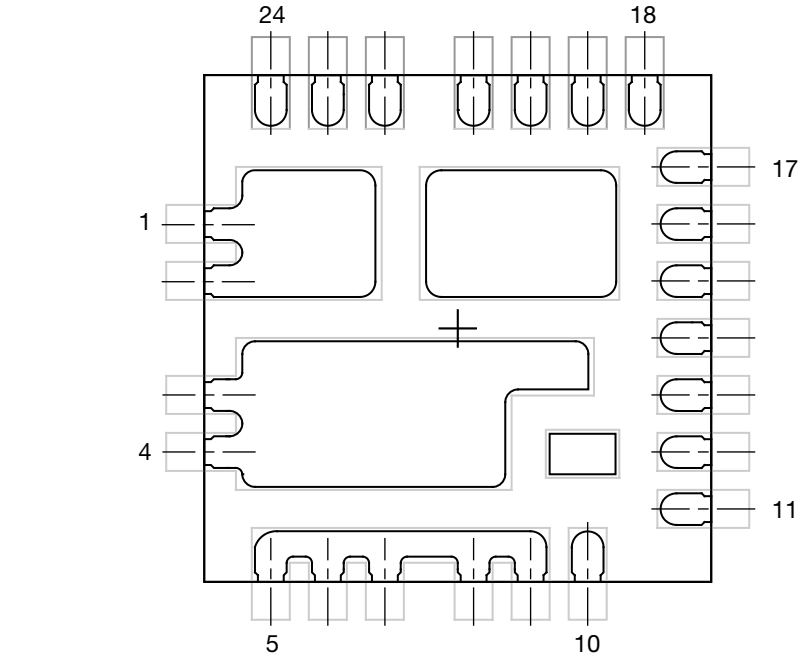


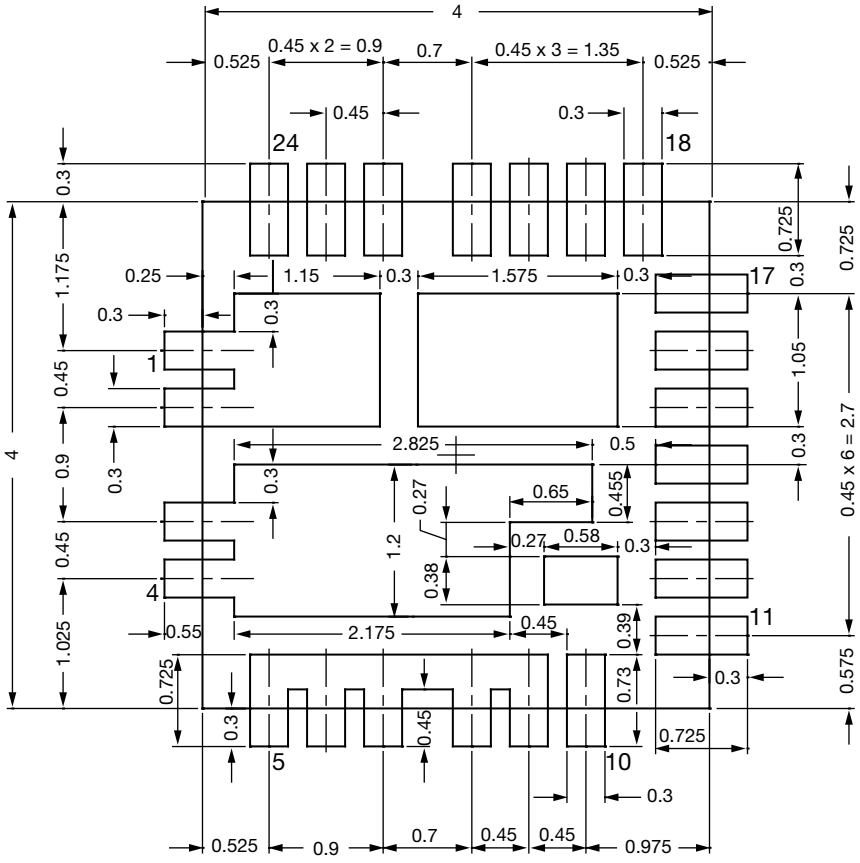
DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A [8]	0.70	0.75	0.80	0.027	0.029	0.031
A1	0.00	-	0.05	0.000	-	0.002
A2		0.20 ref.			0.008 ref.	
b [4]	0.20	0.25	0.30	0.008	0.010	0.012
b1	0.15	0.20	0.25	0.006	0.008	0.010
D	3.90	4.00	4.10	0.154	0.157	0.161
e		0.45 BSC			0.018 BSC	
e1		0.70 BSC			0.028 BSC	
e2		0.90 BSC			0.035 BSC	
E	3.90	4.00	4.10	0.154	0.157	0.161
F1		0.20 ref.			0.008 ref.	
L	0.35	0.40	0.45	0.014	0.016	0.018
N [3]		24			24	
D2-1	1.00	1.05	1.10	0.039	0.041	0.043
D2-2	1.45	1.50	1.55	0.057	0.059	0.061
D2-3	2.68	2.73	2.78	0.106	0.108	0.110
D2-4	2.02	2.07	2.12	0.079	0.081	0.083
D2-5	0.47	0.52	0.57	0.018	0.020	0.022
E2-1	0.95	1.00	1.05	0.037	0.039	0.041
E2-2	1.10	1.15	1.20	0.043	0.045	0.047
E2-3	0.33	0.38	0.43	0.013	0.015	0.017
E2-4	0.95	1.00	1.05	0.037	0.039	0.041
E2-5	0.27	0.32	0.37	0.011	0.013	0.015
K		0.40 ref.			0.016 ref.	
K1		0.57 ref.			0.022 ref.	
K2		0.35 ref.			0.014 ref.	
K3		0.35 ref.			0.014 ref.	
K4		0.35 ref.			0.014 ref.	
K5		0.525 ref.			0.021 ref.	
K6		0.725 ref.			0.029 ref.	
K7		0.575 ref.			0.023 ref.	
K8		0.975 ref.			0.038 ref.	
K9		0.30 ref.			0.012 ref.	
ECN: T22-0442-Rev. C, 10-Oct-2022 DWG: 6055						

Notes

(1) Use millimeters as the primary measurement
(2) Dimensioning and tolerances conform to ASME Y14.5M. - 1994
(3) N is the number of terminals
(4) Dimension b applies to plated terminal and is measured between 0.20 mm and 0.25 mm from terminal tip
(5) The pin #1 identifier must be existed on the top surface of the package by using indentation mark or other feature of package body
(6) Exact shape and size of this feature is optional
(7) Package warpage max. 0.08 mm
(8) Applied only for terminals

Recommended Land Pattern PowerPAK® MLP44-24L





All dimensions are in millimeters

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