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MC44605

High Safety, Latched Mode, GreenLine™ PWM Controller for (Multi) Synchronized Applications

The MC44605 is a high performance current mode controller that is specifically designed for off−line converters. This circuit has several distinguishing features that make it particularly suitable for multisynchronized monitor applications.

The MC44605 synchronization arrangement enables operation from 16 kHz up to 130 kHz. This product was optimized to operate with universal mains voltage, i.e., from 80 V to 280 V, and its high current totem pole output makes it ideally suited for driving a power MOSFET.

The MC44605 protections enable a well−controlled and safe power management. Four major faults while detected, activate the analogic counter of a disabling block designed to perform a latched circuit output inhibition.

Features

- This is a Pb−Free Device*

Current Mode Controller

- Current Mode Operation up to 250 kHz Output Switching Frequency
- Inherent Feed Forward Compensation
- Latching PWM for Cycle−by−Cycle Current Limiting
- Oscillator with Precise Frequency Control
- Externally Programmable Reference Current
- Secondary or Primary Sensing (Availability of Error Amplifier Output)
- Synchronization Facility
- High Current Totem Pole Output
- V_{cc} Undervoltage Lockout with Hysteresis
- Low Output dV/dT for Low EMI Radiations
- Low Startup and Operating Current

Safety/Protection Features

- Soft−Start Feature
- Demagnetization (Zero Current Detection) Protection
- Overvoltage Protection Facility against Open Loop
- EHT Overvoltage Protection (E.H.T.OVP): Detection of too High Synchronization Pulses
- Winding Short Circuit Detection (W.S.C.D.)
- Limitation of the Maximum Input Power (M.P.L.): Calculation of Input Power for Overload Protection
- Overheating Detection (O.H.D.): to Prevent the Power Switch from an Excessive Heating

Latched Disabling Mode

- When one of the following faults is detected: EHT overvoltage, Winding Short Circuit (WSCD), a too high input power (M.P.L.), power switch overheating (O.H.D.), an analogic counter is activated
- If the counter is activated for a time that is long enough, the circuit gets definitively disabled. The latch can only be reset by making decrease the V_{cc} down to about 3.0 V, i.e., practically by unplugging or turning off the SMPS.

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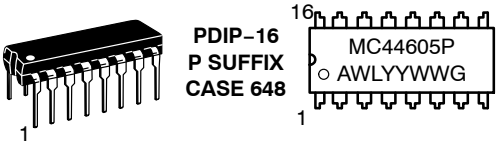
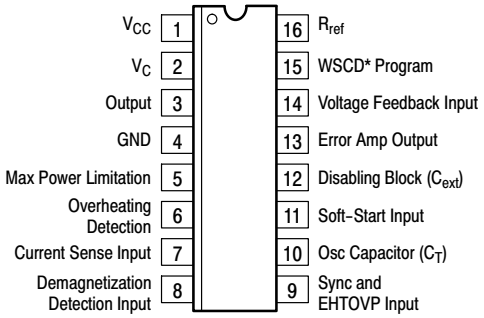
MARKING DIAGRAM



PDIP−16
P SUFFIX
CASE 648

A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G	= Pb−Free Package

PIN CONNECTIONS



(Top View)

*Winding Short Circuit Detection

ORDERING INFORMATION

Device	Package	Shipping
MC44605PG	PDIP−16 (Pb−Free)	25 Units/Rail

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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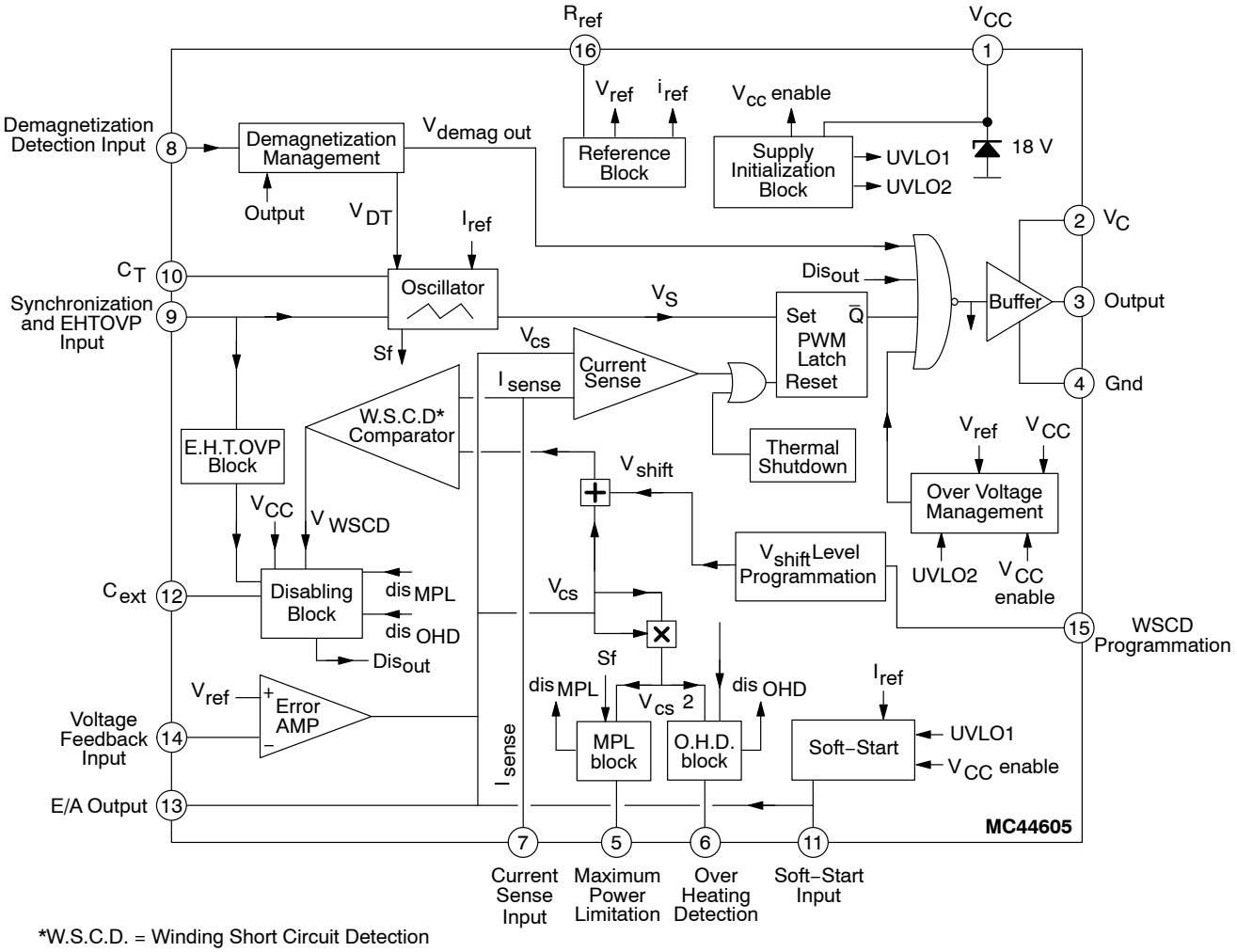
Block Diagram



*W.S.C.D. = Winding Short Circuit Detection

MAXIMUM RATINGS

Rating	Pin #	Symbol	Value	Unit
Total Power Supply and Zener Current		$(I_{CC} + I_Z)$	40	mA
Output Supply Voltage with Respect to Ground	2 1	V_C V_{CC}	18	V
Output Current Source Sink	3	 $I_{O(Source)}$ $I_{O(Sink)}$	 −750 750	mA
Output Energy (Capacitive Load per Cycle)		W	5.0	μJ
Soft−Start		V_{SS}	−0.3 to 2.2 V	V
Current Sense, Voltage Feedback, E/A Output, C_T, R_{ref}, MPL, OHD, C_{ext}, WSCD		V_{in}	−0.3 to 5.5 V	V
E.H.T.OVP, Sync Input Current Source Sink	 9 6 9 6	 $I_{sync\ (Source)}$ $I_{EHT\ (Source)}$ $I_{sync\ (Sink)}$ $I_{EHT\ (Sink)}$	 −4.0 10	mA
Demagnetization Detection Input Current Source Sink	8	 $I_{demag-ib\ (Source)}$ $I_{demag-ib\ (Sink)}$	 −4.0 10	mA
Error Amplifier Output Sink Current	13	$I_{E/A\ (Sink)}$	20	mA
Power Dissipation and Thermal Characteristics Maximum Power Dissipation at T_A = 85°C Thermal Resistance, Junction−to−Air		 P_D $R_{\theta JA}$	 0.6 100	 W °C/W
Operating Junction Temperature		T_J	150	°C
Operating Ambient Temperature		T_A	−25 to +85	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} and V_C = 12 V, R_{ref} = 10 kΩ, C_T = 2.2 nF, for typical values T_A = 25°C, for min/max values T_A = −25° to +85°C unless otherwise noted.) (Note 1)

Characteristic	Pin #	Symbol	Min	Typ	Max	Unit
OUTPUT SECTION (Note 2)						
Output Voltage (Note 3) Low Level Drop Voltage (I_{Sink} = 100 mA) (I_{Sink} = 500 mA) High Level Drop Voltage (I_{Source} = 200 mA) (I_{Source} = 500 mA)	3	 V_{OL} V_{OH} 	 – – – –	 1.0 1.4 1.5 2.0	 1.2 2.0 2.0 2.7	V
Output Voltage During Initialization Phase V_{CC} − 0 to 1.0 V, I_{Sink} = 10 μA V_{CC} − 1.0 to 5.0 V, I_{Sink} = 100 μA V_{CC} − 5.0 to 13 V, I_{Sink} = 1.0 μA	3	V_{OL}	 – – –	 – 0.1 0.1	 1.0 1.0 1.0	V
Output Voltage Rising Edge Slew−Rate (C_L = 1.0 nF, T_J = 25°C)		dVo/dT	–	300	–	V/μs
Output Voltage Falling Edge Slew−Rate (C_L = 1.0 nF, T_J = 25°C)		dVo/dT	–	−300	–	V/μs

1. Adjust V_{CC} above the startup threshold before setting to 12 V. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
2. No output signal when the Error Amplifier output is in Low State, i.e., when for instance, V_{FB} = 2.7 V.
3. V_C must be greater than 5.0 V.

ELECTRICAL CHARACTERISTICS (V_{CC} and V_C = 12 V, R_{ref} = 10 kΩ, C_T = 2.2 nF, for typical values T_A = 25°C, for min/max values T_A = −25° to +85°C unless otherwise noted.) (Note 4)

Characteristic	Pin #	Symbol	Min	Typ	Max	Unit
ERROR AMPLIFIER SECTION						
Voltage Feedback Input ($V_{E/A\ out}$ = 2.5 V)	14	V_{FB}	2.4	2.5	2.6	V
Input Bias Current (V_{FB} = 2.5 V)	14	I_{FB-ib}	−2.0	−0.6	–	μA
Open Loop Voltage Gain ($V_{E/A\ out}$ = 2.0 V to 4.0 V)		A_{VOL}	65	70	–	dB
Unity Gain Bandwidth T_J = 25°C T_A = −25° to +85°C		BW	 – –	 – –	 – 5.5	MHz
Voltage Feedback Input Line Regulation (V_{CC} = 10 V to 15 V)		$V_{FBline-reg}$	−10	–	10	mV
Output Current Sink ($V_{E/A\ out}$ = 1.5 V, V_{FB} = 2.7 V) T_A = −25° to +85°C Source ($V_{E/A\ out}$ = 5.0 V, V_{FB} = 2.3 V) T_A = −25° to +85°C	13	 I_{Sink} I_{Source}	 2.0 −2.0	 12 –	 – −0.2	mA
Output Voltage Swing High State ($I_{E/A\ out\ (source)}$ = 0.5 mA, V_{FB} = 2.3 V) Low State ($I_{E/A\ out\ (sink)}$ = 0.33 mA, V_{FB} = 2.7 V)	13	 V_{OH} V_{OL}	 5.5 –	 6.5 1.0	 7.5 1.1	V
CURRENT SENSE SECTION						
Maximum Current Sense Input Threshold ($V_{Feedback\ (pin14)}$ = 2.3 V and $V_{Soft-Start\ (pin11)}$ = 1.2 V)	7	V_{cs-th}	0.96	1.0	1.04	V
Input Bias Current	7	I_{cs-ib}	−10	−2.0	–	μA
Propagation Delay (Current Sense Input to Output at V_{TH} of MOS transistor = 3.0 V)		$t_{PLH(In/Out)}$	–	120	200	ns
OSCILLATOR AND SYNCHRONIZATION SECTION						
Frequency (T_A = −25° to +85°C)		F_{OSC}	16	–	20	kHz
Frequency Change with Voltage (V_{CC} = 10 V to 15 V)		$\Delta F_{OSC}/\Delta V$	–	0.05	–	%/V
Frequency Change with Temperature (T_A = −25° to +85°C)		$\Delta F_{OSC}/\Delta T$	–	0.05	–	%/°C
Ratio Charge Current/Reference Current (T_A = −25° to +85°C)		I_{charge}/I_{ref}	0.39	–	0.48	–
Free Mode Oscillator Ratio = $I_{discharge}/(I_{discharge} + I_{charge})$		D	72	75	78	%
Synchronization Input Threshold Voltage	9	V_{syncth}	−250	−200	−150	mV
Negative Clamp Level ($I_{syncth-in}$ = 2.0 mA)		NEG−SYNC	−0.65	−0.5	−0.34	V
UNDERVOLTAGE LOCKOUT SECTION						
Startup Threshold	1	$V_{stup-th}$	13.6	14.5	15.4	V
Disable Voltage After Threshold Turn−On (UVLO 1) (T_A = −25° to +85°C)	1	$V_{disable1}$	8.3	–	9.6	V
Disable Voltage After Threshold Turn−On (UVLO 2) (T_A = −25° to +85°C)	1	$V_{disable2}$	7.0	7.5	8.0	V

4. Adjust V_{CC} above the startup threshold before setting to 12 V. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.

ELECTRICAL CHARACTERISTICS (V_{CC} and V_C = 12 V, R_{ref} = 10 kΩ, C_T = 2.2 nF, for typical values T_A = 25°C, for min/max values T_A = −25° to +85°C unless otherwise noted.) (Note 5)

Characteristic	Pin #	Symbol	Min	Typ	Max	Unit
REFERENCE SECTION						
Reference Output Voltage (V_{CC} = 10 V to 15 V)	16	V_{ref}	2.4	2.5	2.6	V
Reference Current Range (I_{ref} = V_{ref}/R_{ref}, R = 5.0 k to 25 kΩ)	16	I_{ref}	−500	–	−100	μA
Reference Voltage Over I_{ref} Range		ΔV_{ref}	−40	–	40	mV
DEMAGNETIZATION DETECTION SECTION (Note 6)						
Demagnetization Detect Input Demagnetization Comparator Threshold (V_{pin9} Decreasing) Propagation Delay (Input to Output, Low to High) Input Bias Current (V_{demag} = 65 mV)	8	 $V_{demag-th}$ $t_{PLH(In/Out)}$ $I_{demag-Ib}$	 50 – −0.5	 65 0.5 –	 80 – –	 mV μs μA
Minimum Off−Time when the pin 8 is grounded		$T_{DEM-GND}$	1.5	3.0	4.5	μs
Negative Clamp Level (I_{demag} = −2.0 mA)		CLVL−neg	−0.50	−0.38	−0.25	V
Positive Clamp Level (I_{demag} = +2.0 mA)		CLVL−pos	0.50	0.72	0.85	V
SOFT−START SECTION (Note 7)						
Ratio Charge Current/I_{ref} (T_A = −25° to +85°C)		I_{ss-ch}/I_{ref}	0.37	–	0.43	–
Discharge Current ($V_{soft-start}$ = 1.0 V)		$I_{discharge}$	1.5	5.0	–	mA
Clamp Level		$V_{SS-CLVL}$	2.2	2.4	2.6	V
Circuit Inhibition Threshold (Note 8)		V_{SSinhi}	30	–	150	mV
V_{CS} Soft−Start Clamp Level ($R_{soft-start}$ = 5 kΩ)		$V_{CSsoft-start}$	0.45	0.5	0.55	V
OVERVOLTAGE SECTION						
Propagation Delay (V_{CC} > 18.1 V to V_{out} Low)		$T_{PHL(In/Out)}$	1.0	–	4.0	μs
Protection Level on V_{CC} (T_A = −25° to +85°C)		$V_{CC\ prot}$	15.9	–	18.1	V
EHT OVP SECTION (Note 9)						
Negative Clamp Level ($I_{synch-in}$ = −2.0 mA)		NEG−SYNC	−0.65	−0.5	−0.35	V
EHT OVP Input Threshold		V_{ref}	7.0	7.4	7.8	V
EHT OVP Input Bias Current ($V_{EHT\ OVP(pin\ 9)}$ = 0 V)	9	I_{EHTOVP}	−5.0	–	0	μA
WINDING SHORT CIRCUIT DETECTION SECTION						
WSCD Threshold with I_{pin15} = 200 μA		Vshift	70	100	120	mV
MPL & OHD SECTION						
MPL Parameter (Note 10)		Γ_{MPL}	0.185	0.240	0.295	V^{-1}
MPL Comparator Threshold (Note 11)		V_{MPL-th}	2.4	2.5	2.6	V
OHD Parameter (Note 12)		Γ_{OHD}	1.15	1.50	1.85	V^{-1}
OHD Comparator Threshold (Note 13)		V_{OHD-th}	2.4	2.5	2.6	V

5. Adjust V_{CC} above the startup threshold before setting to 12 V. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
6. This function can be inhibited by connecting pin 8 to GND. In this case, there is a minimum off−time equal to $T_{DEM-GND}$.
7. The MC44605 can be shut down by connecting soft−start pin (pin 11) to GND.
8. The circuit is shutdown if the soft−start pin voltage is lower than this level.
9. This function can be inhibited by connecting pin 9 to GND. In this case, the synchronization block is inhibited too and the MC44605 works in free mode.
10. This parameter is defined in the MPL §. This parameter is obtained by measuring the MPL pin average current and dividing this result by the corresponding squared V_{CS}, the measured frequency value and the C_T value deducted from the measured frequency value.
    Measurement conditions: $V_{Feedback(pin\ 14)}$ = 2.3 V, $V_{soft-start(pin\ 11)}$ = 0.5 V and pins 7, 8, and 9 connected to GND (the working frequency is typically equal to 18 kHz − R_{ref} = 10 kΩ ±1%, C_T = 2.2 nF).
11. The MPL comparator output is Dis_{MPL}.
12. This parameter is defined in the OHD §. This parameter is obtained by measuring the OHD pin average current and dividing this result by the corresponding squared V_{CS} value and multiplying it by the R_{ref} value.
    Measurement conditions: $V_{Feedback(pin\ 14)}$ = 2.3 V, $V_{soft-start(pin\ 11)}$ = 0.5 V and pins 7, 8, and 9 connected to GND (the working frequency is typically equal to 18 kHz − R_{ref} = 10 kΩ ±1%, C_T = 2.2 nF).
13. The OHD comparator output is Dis_{OHD}.

ELECTRICAL CHARACTERISTICS (V_{CC} and V_C = 12 V, R_{ref} = 10 kΩ, C_T = 2.2 nF, for typical values T_A = 25°C, for min/max values T_A = −25° to +85°C unless otherwise noted.) (Note 14)

Characteristic	Pin #	Symbol	Min	Typ	Max	Unit
DISABLING BLOCK SECTION						
Delay Pulse Width		T_{WSCD}	–	4.0	–	μs
Ratio (EHTOVP and WSCD Disabling Capacitor Charge Current)I_{ref}		I_{Dis-H}/I_{ref}	90	100	110	%
Ratio (MPL and OHD Disabling Capacitor Charge Current)I_{ref}		I_{Dis-L}/I_{ref}	2.7	3.1	3.5	%
Minimum V_{CC} Value Enabling the Disabling Block Latch (Note 15)		V_{CCDis}	1.0	–	5.0	V
TOTAL DEVICE						
Power Supply Current		I_{CC}				mA
Startup−Up (V_{CC} = 5.0 V with V_{CC} increasing)			–	0.35	0.55	
Startup−Up (V_{CC} = 9.0 V with V_{CC} increasing)			–	0.35	0.55	
Startup−Up (V_{CC} = 12 V with V_{CC} increasing)			–	0.35	0.55	
Operating T_A = −25°C to +85°C (Note 16)			–	20	25	
Disabling Mode (V_{CC} = 6.0 V) (Note 17)			–	–	0.55	
Power Supply Zener Voltage (I_{CC} = 35 mA)		V_Z	18.5	–	–	V
Thermal Shutdown		–	–	155	–	°C

14. Adjust V_{CC} above the startup threshold before setting to 12 V. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
15. Once a fault detection activated it, the Disabling Block Latch gets reset when the V_{CC} becomes lower than this threshold.
16. Refer to Note 14.
17. This consumption is measured while the circuit is inhibited by the Definitive Latch.

Pin	Name	Pin Description
1	V_{CC}	This pin is the positive supply of the IC.
2	V_C	The output high state, V_{OH}, is set by the voltage applied to this pin. With a separate connection to the power source, it gives the possibility to set by means of an external resistor the output source current at a different value than the sink current.
3	Output	The output current capability is suited for driving a power MOSFET.
4	GND	The ground pin is a single return typically connected back to the power source. It is used as control and power ground.
5	Maximum Power Limitation	This block enables to estimate the input power. When this calculated power is detected as too high, a fault information is sent to the disabling block in order to definitively disable the circuit.
6	Over−Heating Detection	This block estimates the MOSFET heating. When this calculated heating is too high, the device gets definitively disabled (disabling block action).
7	Current Sense Input	A voltage proportional to the current flowing into the power switch is connected to this input. The PWM latch uses this information to terminate the conduction of the output buffer. A maximum level of 1 V allows to limit the inductor current.
8	Demagnetization Detection	A voltage delivered by an auxiliary transformer winding provides to the demagnetization pin an indication of the magnetization state of the flyback energy reservoir. A zero voltage detection corresponds to a complete core demagnetization. The demagnetization detection prevents the oscillator from a re−start and so the circuit from a new conduction phase, if the fly−back is not in a dead−time state. This function can be inhibited by connecting Pin 8 to GND but in this case, there is a minimum off−time typically equal to 3 μs.
9	Synchronization and E.H.T.OVP Input	Activating the synchronization input pin with a pulse higher or equal to the negative threshold (typically −200 mV) allows the next switching period to be reinitialized. The oscillator is free when connecting Pin 9 to GND. When the E.H.T.OVP pin receives a voltage that is greater than 7.5 V, the disabling block C_{ext} capacitor is charged so that the circuit gets definitively disabled if the C_{ext} voltage becomes higher than V_{ref}. This block is incorporated to detect and disable the device when the synchronization pulses are too high.
10	Oscillator Capacitor C_T	The free mode oscillator frequency is programmed by the capacitor C_T choice together with the R_{ref} resistance value. C_T, connected between pin 10 and GND, generates the oscillator sawtooth.
11	Soft−Start	A capacitor connected to this pin can temporary reduce the maximum inductor peak current. By this way, a soft−start can be performed. By connecting pin 11 to Ground, the MC44605 is shutdown.
12	C_{ext} (Disabling Block)	When a too high synchronization pulse voltage (E.H.T.OVP) or a winding short circuit (WSCD) is detected, the capacitor C_{ext} is charged using a current source I_{Dis-H}. In the case of a MPL or OHD fault detection, C_{ext} is charged using I_{Dis-L}. If the C_{ext} capacitor voltage gets higher than V_{ref}, the circuit is definitively disabled. Then, to re−start, the converter must be switched off in order to make V_{CC} decrease down to about 0 V.
13	E/A Output	The error amplifier output is made available for loop compensation.
14	Voltage Feedback	This is the inverting input of the Error Amplifier. It can be connected to the Switching Mode Power Supply output through an optical (or else) feedback loop or to the subdivided V_{CC} voltage in case of primary sensing technic.
15	Winding Short Circuit Detection Programmation	The W.S.C.D. block is incorporated to detect the transformer Winding Short Circuits. This function is performed by detecting the inductor overcurrents thanks to a comparator which threshold is programmable to be well adapted to any application.
16	R_{ref}	The R_{ref} value fixes the internal reference current that is particularly used to perform the precise oscillator waveform. The current range goes from 100 μA up to 500 μA.

Summary of the Main Design Equations

The following table consists of equations enabling to dimension a multisynchronized SMPS operating in discontinuous mode.

$Pin_{max} = \frac{Pout_{max}}{\eta}$	$Pout_{max}$ is the maximum power the load may draw in normal working. The maximum input power Pin_{max} is easily deducted by dividing $Pout_{max}$ by the efficiency (η). In this kind of application, the efficiency is generally taken equal to 80%.
$Lp_{max} = \frac{\left[\frac{\sqrt{2}\cdot Vac_{min} \times NVo}{\sqrt{2}\cdot Vac_{min} + NVo}\right]^2}{2 \times Pin_{max} \times fsync_{max}}$	The inductor value Lp must be chosen lower than Lp_{max} or ideally equal to this value (to optimize the application design−in). In effect, if Lp was higher than Lp_{max}, a synchronized and discontinuous working could not be guaranteed (in some cases, the demagnetization phase would not be finished while a new conduction phase should start to follow the synchronization).
$Ipk_{max} = \sqrt{\frac{2 \times Pin_{max}}{L \times fsync_{min}}}$	Ipk_{max} is the maximum inductor peak current. This current is obtained when the power to transfer is maximum at the minimum synchronization frequency (60 W output, 30 kHz in the proposed application).
$d_{max} = \frac{\sqrt{Pin_{max} \times Lp \times fsync_{max}}}{Vac_{min}}$	d_{max} is the maximum duty cycle. The duty cycle is maximum at the lowest input voltage when the power demand is maximum while the synchronization frequency also is maximum.
$Pon_{max} = \frac{1}{3} \times Rds_{on} \times Ipk_{max}^2 \times d_{max}$	Pon_{max} is the maximum MOSFET on−time losses that are proportional to Ipk_{max}, d_{max} and Rds_{on} (on−time MOSFET resistor). This conduction losses estimation enables to dimension the power MOSFET.
$(V_{DS})\,max = \left(\sqrt{2} \times Vac_{max}\right) + (N \times Vout)$	(V_{DS})max is the maximum voltage the power switch must be able to face. In fact, this calculation does not take into account the turnings off spikes. So, it is necessary to take a margin of at least about 50 V.
$(V_D)\,max = \left(\sqrt{2} \times \frac{Vac_{max}}{N}\right) + Vout$	(V_D)max is the maximum voltage the high voltage secondary diode must be able to face. Because of the turning off spikes, a margin must also be taken.
$(ni)_{max} = N \times n_{Vout} \times Ipk_{max}$	(A_L) and (ni) are the magnetic parameters. $(ni)_{max}$ must not exceed the ferrite (ni). Otherwise, the transformer may get saturated when the peak current is high.
$A_L = \frac{L_P}{(N \times n_{Vout})^2}$	(A_L) is the ferrite constant that links the primary inductor value to the squared number of primary turns: $Lp = A_L \times n_p^2$.

Error Amplifier

A fully compensated Error Amplifier with access to the inverting input and output is provided. It features a typical DC voltage gain of 70 dB. The non inverting input is internally biased at 2.5 V and is not pinned out. The converter output voltage is typically divided down and monitored by the inverting input. The maximum input bias current with the inverting input at 2.5 V is −2.0 μA. This can cause an output voltage error that is equal to the product of the input bias current and the equivalent input divider source resistance.

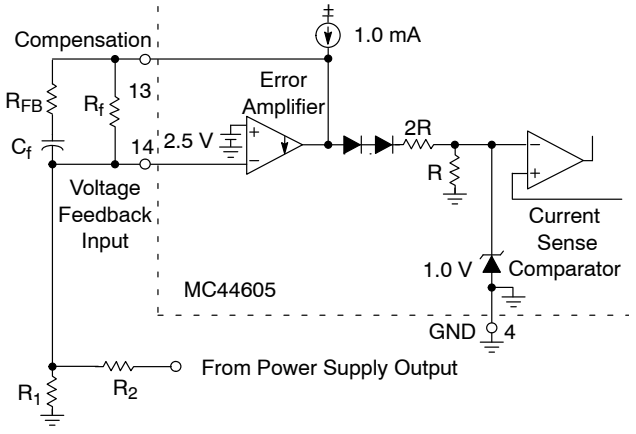


Figure 1. Error Amplifier Compensation

The Error Amp Output (Pin 13) is provided for external loop compensation. The output voltage is offset by two diodes drops (≈1.4 V) and divided by three before it connects to the inverting input of the Current Sense Comparator. This guarantees that no drive pulses appear at the Source Output (Pin 3) when Pin 13 is at its lowest state (V_{OL}). This occurs when the power supply is operating and the load is removed, or at the beginning of a soft−start interval. The Error Amp minimum feedback resistance is limited by the amplifier's minimum source current (0.2 mA) and the required output voltage (V_{OH}) to reach the current sense comparator's 1.0 V clamp level:

$$R1(min) = \frac{(3 \times 1\ V) + 1.4\ V}{0.2\ mA} = 22\ k\Omega$$

Current Sense Comparator and PWM Latch

The MC44605 operates as a current mode controller. The circuit uses a current sense comparator to compare the inductor current to the threshold level established by the Error Amplifier output (Pin 13). When the current reaches the threshold, the current sense comparator terminates the output switch conduction that has been initiated by the oscillator, by resetting the PWM Latch. Thus the error signal controls the peak inductor current on a cycle−by−cycle basis. This configuration ensures that only one single pulse appears at the Source Output during the appropriate oscillator cycle.

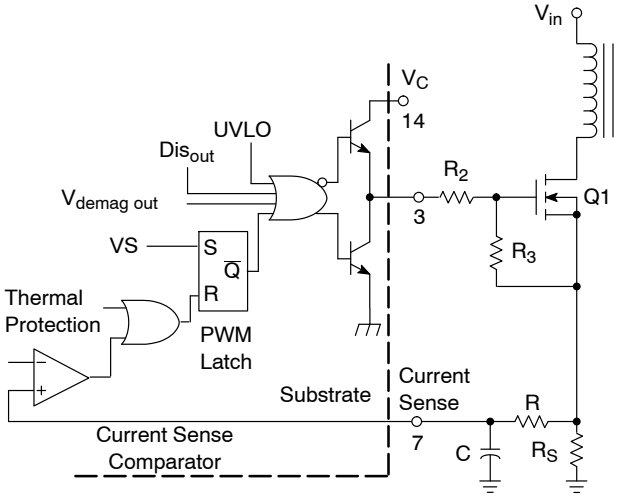


Figure 2. Output Totem Pole

The inductor current is converted to a voltage by inserting the ground referenced sense resistor R_S in series with the power switch Q1.

This voltage is monitored by the Current Sense Input (Pin 7) and compared to a level derived from the Error Amp output. The peak inductor current under normal operating conditions is controlled by the voltage at Pin 13 where:

$$I_{pk} \approx \frac{V_{(pin13)} - 1.4\ V}{3 \times R_S}$$

The Current Sense Comparator threshold is internally clamped to 1.0 V. Therefore the maximum peak switch current is:

$$I_{pk(max)} = \frac{1\ V}{R_S}$$

Undervoltage Lockout Section

As depicted in Figure 3, an undervoltage lockout has been incorporated to guarantee that the IC is fully functional before allowing the system working.

In effect, the V_{CC} is connected to the non inverting input of a comparator that has an upper threshold equal to 14.5 V (typical $V_{stup-th}$) and a lower one equal to 7.5 V (typical $V_{disable\ 2}$). This hysteresis comparator enables or disables the reference block that generates the voltage and current sources required by the system.

This block particularly, produces V_{ref} (pin 16 voltage) and I_{ref} that is determined by the resistor R_{ref} connected between pin 16 and the ground:

$$I_{ref} = \frac{V_{ref}}{R_{ref}} \text{ where } V_{ref} = 2.5\ V \text{ (typically)}$$

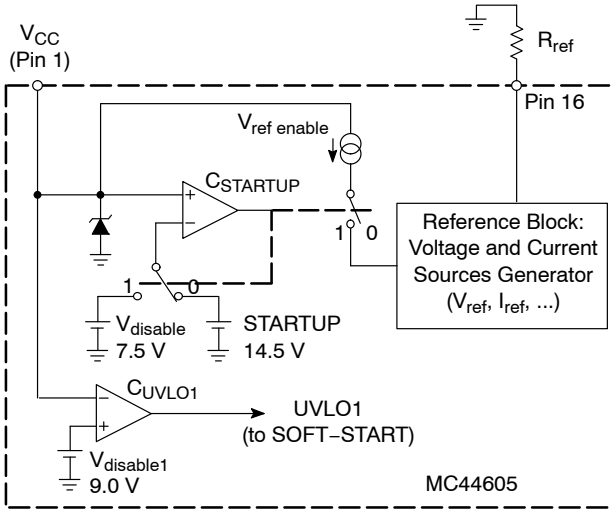


Figure 3. V_{CC} Management

In addition to this, V_{CC} is compared to a second threshold level that is nearly equal to 9.0 V ($V_{disable1}$) so that a signal UVLO1 is generated to reset the soft−start block and so, to disable the output stage (refer to the Soft−Start §) as soon as V_{CC} becomes lower than $V_{disable\ 1}$. In this way, the circuit is reset and made ready for a next startup, before the reference block is disabled (refer to Figure 3). Thus, finally the upper limit for the minimum normal operating voltage

is 9.4 V (maximum value of $V_{disable\ 1}$) and so the minimum hysteresis is 4.2 V. [$(V_{stup-th})_{min}$ = 13.6 V].

The large hysteresis and the low startup current of the MC44605 make it ideally suited for off−line converter applications where efficient bootstrap startup techniques are required.

Soft−Start Control Section

The V_{cs} value is clamped down to the pin 11 voltage.

So, if a capacitor is connected to this pin, its voltage increases slowly at the startup (the capacitor is charged by an internal current source 0.4 I_{ref}). So, V_{cs} is limited during the startup and then a soft−start is performed.

This pin can be used to inhibit the circuit by applying a voltage that is lower than V_{SSinhi} (refer to page 4). Particularly, the MC44605 can be shutdown by connecting the soft−start pin to ground.

As soon as V_{dis1} is detected (that is V_{cc} lower than $V_{disable1}$), a signal UVLO1 is generated until the V_{cc} falls down to V_{dis2} (refer to the undervoltage lockout section §). During the delay between the disable1 and the disable2, using a transistor controlled by UVLO1, the pin 11 voltage is made equal to zero in order to make the soft−start arrangement ready to work for the next re−start.

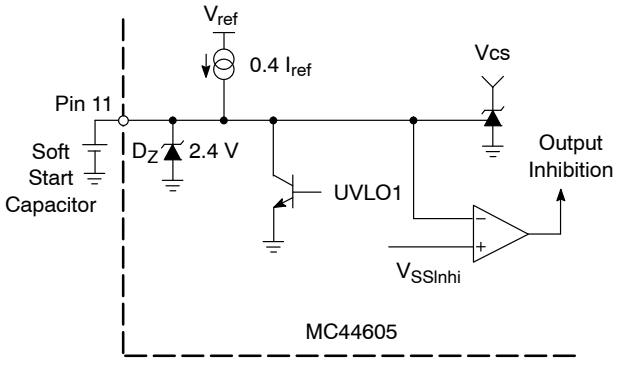


Figure 4. Soft−Start

Oscillator Section (Figures 5 & 5b)

The oscillator and synchronization behavior is represented in Figure 5b.

The MC44605 oscillator achieves four functions:

— it fixes the free mode frequency
— it takes into account the synchronization signal
— it does not allow a new power switch conduction if the flyback is not in a dead−time state when the circuit works in demagnetization mode (pin 8 connected)
— it builds the Sf pulse required by the MPL block

During the operating mode, the oscillator sawtooth can vary between a valley value (1.6 V typically) and a peak one (3.6 V typically) and presents three distinct phases:

— the C_T charge
— the C_T discharge
— the phase during which the oscillator voltage is maintained equal to its valley value. This happens at the end of a discharge cycle when the synchronization or demagnetization condition does not allow a new C_T charge phase. During this sequence, I_{REGUL} compensates the charge current I_{charge}.

The oscillator has two working modes:

— a free one when there is no synchronization
— a synchronized one.

In the free working, the oscillator grows up from its valley value to its peak one for the charge phase and when once the peak value is reached, a discharge sequence makes the C_T voltage decrease down to its valley value. When the decrease phase is finished, a new charge cycle occurs if the demagnetization condition is achieved (V_{DT} high). Otherwise there is a REGUL phase until V_{DT} gets high.

In the synchronized mode, the charge cycle is only allowed when the synchronization signal gets high while a dead time has been detected (V_{DT} high). This charge phase is stopped when the synchronization signal has got low and when the oscillator voltage is higher than V_{int}, the intermediary voltage level used to generate the calibrated pulse Sf by comparing the C_T voltage to this threshold. So, when these two conditions are performed, a discharge sequence is set until the oscillator voltage is equal to its valley value. Then, the C_T voltage is maintained constant thanks to the “REGUL” arrangement until the next synchronization pulse.

In both cases, during the charge phase, a signal V_S is generated. When Sf becomes high. V_S gets high and remains in this state until the PWN latch is set of Sf is low. Then, V_S keeps low until the next Sf high level. This oscillator behavior is obtained using the process described in Figure 5b.

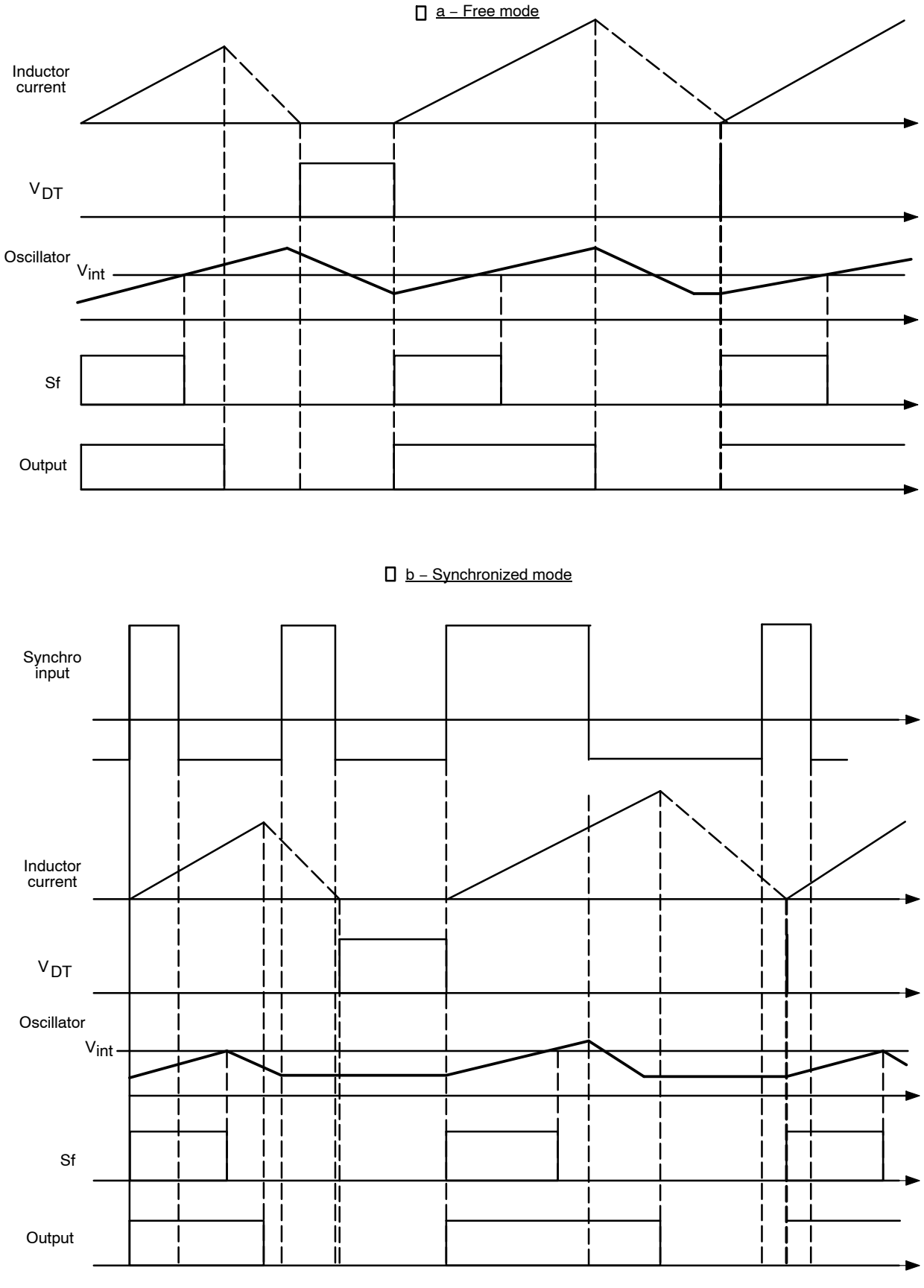


Figure 5b. Oscillator Behavior

In effect, the output of the latch L1 is:
— high during the oscillator capacitor charge and during the REGUL phase
— low for the oscillator capacitor discharge

Now, the latch L2 is set when the L1 output is high and the synchronization condition is performed (that is: sync = 1 − free mode or synchro signal high state) and during the dead−time (V_{DT} high). So, this latch is set for the C_T charge.

On the other hand, this latch is reset by the signal used to reset L1. Consequently, it is reset at the end of the charge phase.

So, in any case, Q_{L2} is:
— high during the C_T charge cycle
— low in the other cases

Thus, this latch enables to obtain a signal that is high for the charge phase and low in the other cases, whatever the mode (synchronized or free) and whatever the synchronization pulses width (higher than the delay necessary for the oscillator to reach its intermediary value or lower than this delay) in the synchronized mode.

That is why:
— the discharge current source must be connected to the oscillator capacitor when Q_{L1} is low. The condition (C_T voltage higher than the valley value) is added to stop the discharge phase as soon as the oscillator voltage is detected as lower than the valley value (without any delay due to the L1 latch propagation time).
— the REGUL current source must be connected when:
  - Q_{L1} is high (charge or REGUL phase)
  - Q_{L2} is low (the oscillator is not in a charge phase)

On the other hand, the oscillator charge is stopped when:
— the oscillator voltage reaches the peak value in the free mode
— the oscillator voltage is higher than the intermediary value (V_{int}) and the synchronization signal is negative, in the synchronized mode.

Consequently, in any case, Q_{L2} that is high during the oscillator charge phase, is high for the delay during which the oscillator voltage grows from the valley value up to the intermediary one. That is why the signal Sf (refer to the MPL block) that must be high when the oscillator voltage is between the valley value and the intermediary one during the charge phase (Q_{L2} high), is obtained using an AND gate with the following inputs:
— Q_{L2} (Q_{L2} high <=> charge phase)
— C_{OSCINT} (C_{OSCINT} high <=> the C_T voltage is lower than the intermediary value).

So, using the output of this AND gate, Sf is obtained.

This signal Sf is connected to a logic block consisting of two AND gates and an OR one. This block aims at supplying a signal VS that:
— gets high as soon as Sf becomes high if the PWM latch output is low
— gets low as soon as the PWM latch is set and then remains low until the next cycle.

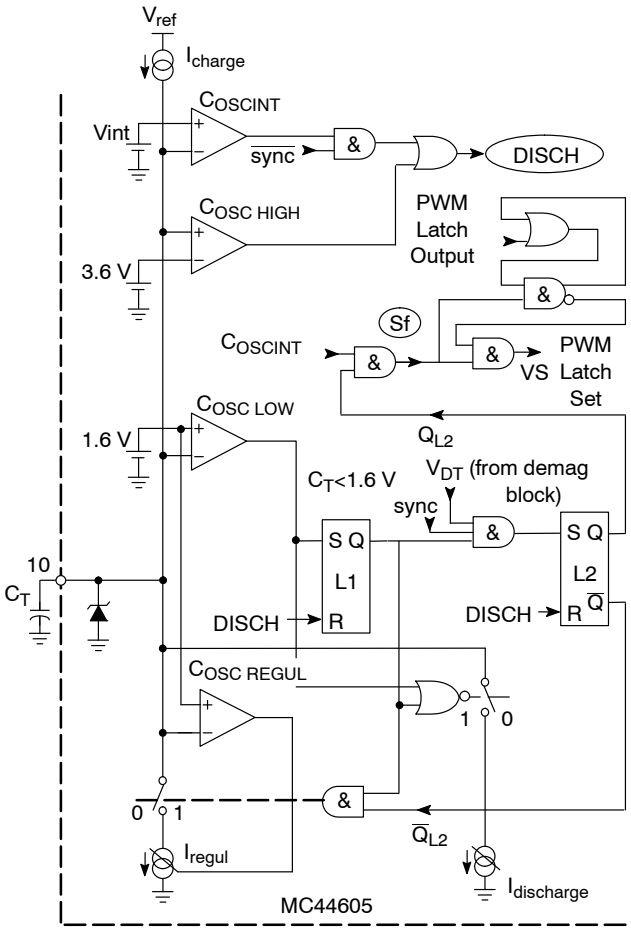


Figure 5. Oscillator

Synchronization Section (Note 1)

The synchronization block consists of a protection arrangement similar to the demagnetization block one (a diode + a negative active clamping system (Note 2)). In addition to this, a high value resistor (R − about 50 kΩ) is incorporated as the pin 9 input is also used by the EHTOVP section.

The signal obtained at the output of this protection arrangement, is compared to a negative threshold (−200 mV, typically) so that when the synchronization pulse applied to the pin 9 (through a resistor or a resistors divider to adapt this input to the EHTOVP function), is higher than this threshold, the system considers that the synchronization condition is performed (free mode or synchronization signal high level).

Note 1. The synchronization can be inhibited by connecting the pin 9 to the ground. By this means, a free mode is obtained.

Note 2. This negative active clamping system works even if the circuit is off. This feature is really useful as synchronization pulses may be applied while the product is off.

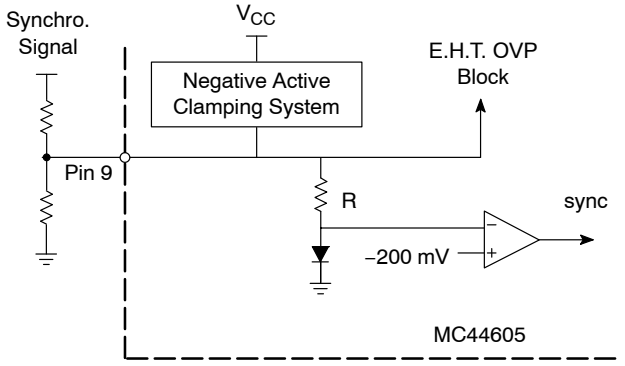


Figure 6. Synchronization

Demagnetization Section

This block is incorporated to detect the complete core demagnetization in order to prevent the power MOSFET from switching on if the converter is not in a dead time phase. That is why this block inhibits any oscillator re−start as long as the inductor current is not finished (from the beginning of the on−time to the end of the demagnetization phase).

In a fly−back, a good means to detect the demagnetization phase consists in using the V_{CC} winding voltage. In effect, this voltage is:

— negative during the on−time,
— positive during the off−time,
— equal to zero for the dead−time with generally a ringing (refer to Figure 7).

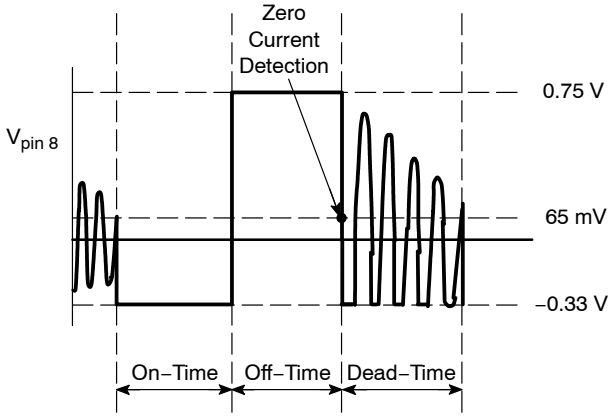


Figure 7. Demagnetization Detection

That is why, the MC44605 demagnetization detection consists of a comparator that compares the V_{CC} winding voltage to a reference that is typically equal to 65 mV.

A diode D is incorporated to clamp the positive applied voltages while an active clamping system limit the negative voltages to typically −0.33 V. This negative clamp level is high enough to avoid the substrate diode switching on.

A latch system is incorporated to keep the demagnetization block output level low as soon as a voltage lower than 65 mV is detected and as long as a new restart is produced (high level on the output (refer to Figure 8). This process avoids that any ringing on the signal used on the pin 8, disrupts the demagnetization detection (refer to Figure 7). Finally, this method results in a very accurate demagnetization phase detection, and the signal V_{DT} drawn from this block is high only for the dead time. Therefore, an oscillator re−start and so, a new power switch conduction is only allowed during the dead−time.

For a higher safety, the $V_{demagout}$ output of the demagnetization block is also directly connected to the output, to disable it during the demagnetization phase (refer to the block diagram).

The demagnetization detection can be inhibited by connecting pin 8 to the ground but in this case, a timer (about 3 μs) that is incorporated to set the latch when it can not be set by $V_{demagout}$, results in a minimum off−time (refer to Figure 8).

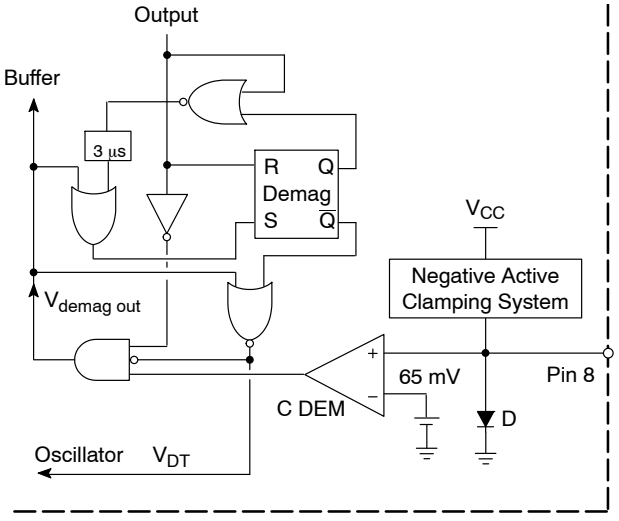


Figure 8. Demagnetization Block

Overvoltage Protection Section

The overvoltage arrangement compares a portion V_{cc} to V_{ref} (2.5 V) (refer to Figure 9). In fact, this threshold corresponds to a V_{CC} equal to to 17 V. When the V_{cc} is higher than this level, the output is latched off until a new circuit re−start.

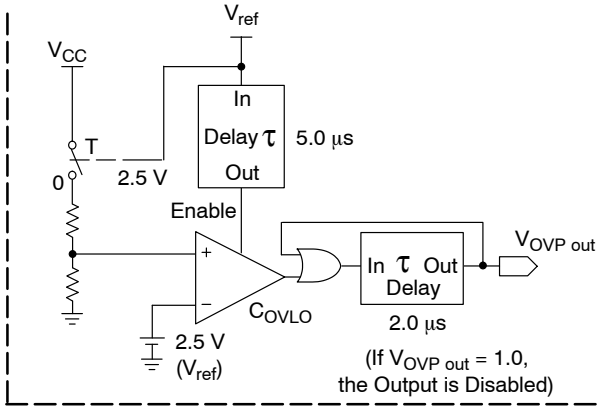


Figure 9. Overvoltage Protection

A delay (2 μs) is incorporated in order to avoid any activation due to interferences by only taking into account the overvoltages that last at least 2 μs.

The V_{CC} is connected when once the circuit has started−up in order to limit the circuit startup consumption (T is switched on when once V_{ref} has been generated).

The overvoltage section is enabled 5 μs after the regulator has started to allow the reference V_{ref} to stabilize.

E.H.T. Overvoltage Protection Section

This block uses the synchronization input as this section is incorporated to detect too high synchronization pulses and then to activate the device definitive latch in this case.

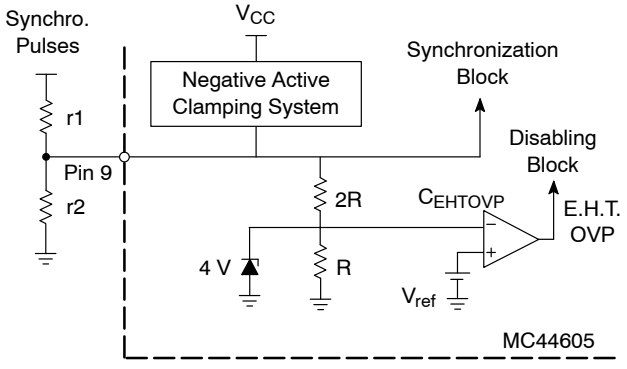


Figure 10. E.H.T. OVP

This block consists of a high impedance resistors bridge (R is nearly equal to 50 kΩ − refer to Figure 10) so that the EHTovp threshold is 7.5 V. So, using an external resistors bridge (r1, r2 <<R), the synchronization pulse level above which the working must be considered as wrong, can be adjusted.

For instance, if this threshold value is required to be equal to 30 V, V_{pin9} must be equal to 7.5 V when the synchronization pulse value is 30 V.

So, in this case:

$$30 \times \frac{r2}{r1 + r2} = 7.5$$

Then, the ratio (r1/r2) can be deducted:

$$\frac{r1}{r2} = 3$$

So, as r1 and r2 must be negligible in relation to R (about 50 kΩ), the couple of resistors can be chosen as follows:

$$r1 = 3\ k\Omega$$

and:

$$r2 = 1\ k\Omega$$

Winding Short Circuit Detection Section (WSCD)

The MC44605 being designed to control a Fly−Back SMPS, this block is incorporated to detect a short circuit on a transformer winding or on an output diode (refer to Figure 11).

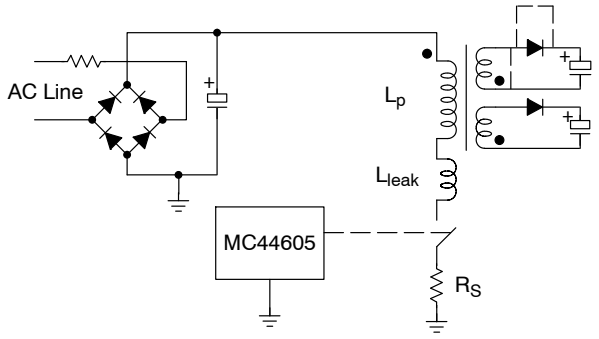


Figure 11. Winding Short Circuit Fault

In the case of a Winding Short Circuit, the primary inductor L_p is short circuited and then the current increase is only controlled by the leakage inductor L_{leak}.

In current mode, the power switch conduction is stopped when the inductor current is detected as high enough, by the controller. In fact, when the current sense resistor (R_s) voltage gets equal to V_{cs}, the current sense comparator switches to reset the output.

Now, the circuit has a propagation delay and the power switch needs some time to turn off. Consequently, there is a delay Δt between the moment at which the R_s voltage gets equal to V_{cs} and the actual current increase stop. So, this results in an overcurrent (refer to Figure 12).

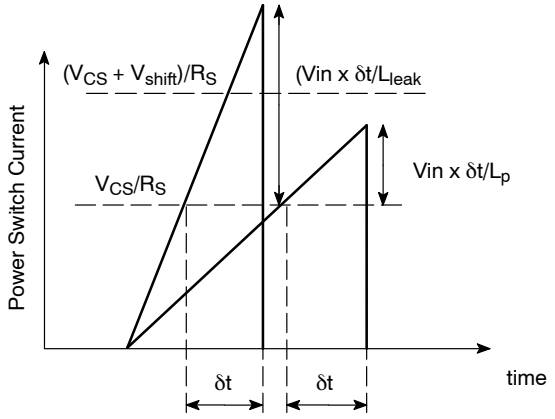


Figure 12. Overcurrent in a WSCD Case

Now, in normal working, this overcurrent ΔIpk is equal to:

$$\Delta Ipk = \frac{Vin \times \delta t}{L_P}$$

where: V_{in} is the input voltage (rectified a.c. line)

While in a WSCD case:

$$(\Delta Ipk)_{WSCD} = \frac{Vin \times \delta t}{L_{Leak}}$$

Consequently, as the leakage inductor value is generally much lower than the primary one (less than 5% generally), the overcurrent is much higher in the WSCD case. That is why this fault can be detected by detecting the high overcurrents.

So, the WSCD block consists of comparing the sensed current to a reference equal to: (V_{cs} + V_{shift}), where V_{shift} is a voltage proportional to the current injected in the pin 15 (refer to Figure 13).

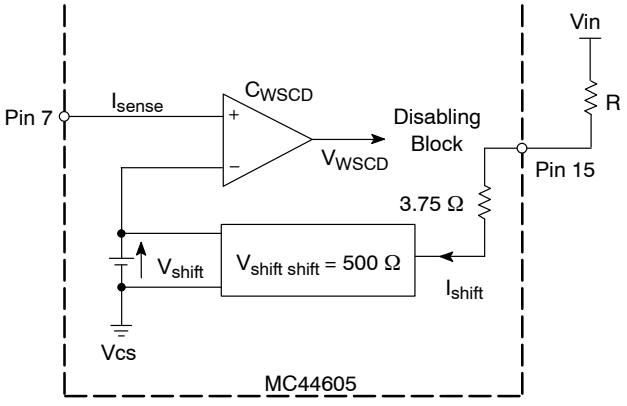


Figure 13. WSCD

Now, as the overcurrent level depends on the input voltage V_{in}, it is preferable to use a V_{shift} proportional to this input voltage instead of a constant V_{shift}. So, the WSCD pin must be connected to V_{in} through a resistor that fixes V_{shift} by adjusting the current injected in this pin 15.

Finally, when there is a winding short circuit, an overcurrent is detected by the WSCD comparator. The output of this comparator, V_{WSCD}, is connected to the disabling block (refer to the disabling block §).

Maximum Power Limitation Section (MPL)

The MPL block is designed to calculate this input power using the following equation:

$$Pin = \frac{1}{2} \times L_P \times Ipk^2 \times f$$

where: Lp is the inductor value
Ipk is the inductor peak current
f is the switching frequency

As V_{cs} is proportional to the inductor peak current ($V_{cs} = R_s$ x Ipk), the squared Ipk value is estimated by building a current source proportional to V_{cs}^2. This current is chopped by a calibrated pulse Sf, generated at each new oscillator cycle (refer to Figure 14).

Finally, using an external resistor and capacitor network (R_{MPL}, C_{MPL}) on the MPL pin, a voltage V_{MPL}, proportional to the input power can be obtained.

In effect,

$$V_{MPL} = R_{MPL} \times k_{MPL} \times Vcs^2 \times \frac{(Sf)}{T}$$

where: k_{MPL} is the multiplier gain
(Sf) is the width of the calibrated pulse
T is the switching (oscillator) period

Now, as Sf is built comparing the oscillator to a constant level, (Sf) is proportional to R_{ref} and C_T:

$$(Sf) = k1 \times R_{ref} \times C_T$$

where: k1 is a constant

On the other hand, k_{MPL} that is depending on the reference current source I_{ref}, is proportional to $1/R_{ref}$:

$$k_{MPL} = k2 \times \frac{1}{R_{ref}}$$

where: k2 is a constant

So:

$$V_{MPL} = R_{MPL} \times k1 \times k2 \times Vcs^2 \times f \times C_T$$

where: C_T is the oscillator capacitor

Finally:

$$V_{MPL} = R_{MPL} \times \Gamma_{MPL} \times Vcs^2 \times f \times C_T$$

where: Γ_{MPL} is the MPL parameter as defined in the specification. This is a constant equal to the product (k1 x k2).

Now, as:

$$Pin = \frac{1}{2} \times L_P \times Ipk^2 \times f$$

and:

$$Vcs = R_S \times Ipk$$

So:

$$V_{MPL} = \frac{2 \times R_{MPL} \times \Gamma_{MPL} \times C_T \times R_S^2}{L_P} \times Pin$$

A comparator is used to compare V_{MPL} to V_{ref}, the output of which, Dis_{MPL}, is connected to the "definitive inhibition latch" of the disabling block. So, when the calculated power is higher than the threshold, the circuit is definitively disabled (the system considers that there is an overload condition).

Finally, replacing V_{MPL} by 2.5 V (the threshold value), the R_{MPL} value to be used, can be deducted:

$$R_{MPL} = \frac{1.25 \times L_P}{\Gamma_{MPL} \times C_T \times R_S^2 \times (Pin)_{max}}$$

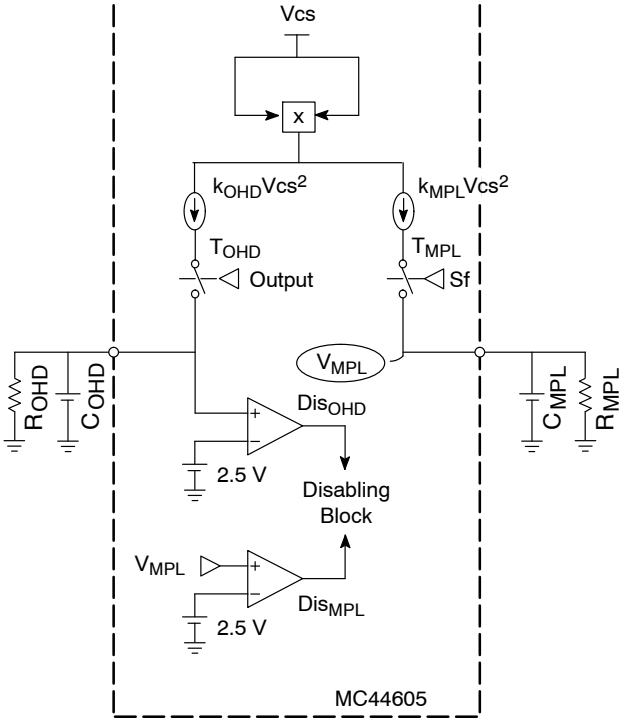


Figure 14. OHD and MPL

Overheating Detection Section (O.H.D.)

In the MPL block, the converter input power is calculated. In the O.H.D. block, that is the power MOSFET heating which is calculated, using the following equation:

$$p_{on} = \frac{1}{3} \times R_{dson} \times Ipk^2 \times d$$

where: p_{on} are the power switch on−time losses
R_{dson} is the conduction MOSFET resistor
d is the duty cycle

As in the MPL section, the squared Ipk term is estimated by building a current source proportional to Vcs^2.

The duty cycle is taken into account thanks to the action on this current source of a "chopper" controlled by the circuit output. By this means, the pin 6 average current is proportional to the squared peak current multiplied to the duty cycle (refer to Figure 14).

So, using an external resistor and capacitor network (R_{OHD}, C_{OHD}) on this pin, a voltage V_{OHD}, proportional to the conduction losses can be obtained.

Like in the MPL block, this voltage V_{OHD}, is compared to 2.5 V. If V_{OHD} gets higher than this threshold, the disabling block is activated by Dis_{OHD} (output of the comparator).

The external resistor R_{OHD} choice enables to obtain a calculated V_{OHD} equal to 2.5 V when the conduction losses are equal to their maximum value.

In effect,

$$V_{OHD} = R_{OHD} \times k_{OHD} \times Vcs^2 \times d$$

where: k_{OHD} is the multiplier gain

Now, as k_{OHD} that is depending on the reference current source I_{ref}, is proportional to $1/R_{ref}$:

$$k_{OHD} = k2 \times \frac{1}{R_{ref}}$$

where: k2 is a constant

So:

$$V_{OHD} = R_{OHD} \times k2 \times \frac{Vcs^2}{R_{ref}} \times d$$

Finally:

$$V_{OHD} = \frac{R_{OHD} \times \Gamma_{OHD} \times Vcs^2 \times d}{R_{ref}}$$

where: Γ_{OHD} is the OHD parameter as defined in the specification. This is a constant equal to k2.

Now, as:

$$Vcs = R_S \times Ipk$$

So, replacing Vcs and using the p_{on} equation:

$$V_{OHD} = \frac{3 \times R_{OHD} \times \Gamma_{OHD} \times R_S^2}{R_{ref} \times R_{dson}} \times p_{on}$$

So, by choosing the value of R_{OHD}, the heating corresponding to V_{ref} is determined. If the MOSFET dissipation is such that the heating is higher than this threshold, the "definitive inhibition latch" of the Disabling Block is activated and so, the output gets definitively disabled.

Consequently, by replacing V_{OHD} by 2.5 V (threshold value) in the last equation, the value R_{OHD} to use, can be deducted:

$$R_{OHD} = \frac{2.5 \times R_{ref} \times R_{dson}}{3 \times \Gamma_{OHD} \times R_S^2 \times (p_{on})_{max}}$$

where: $(p_{on})_{max}$ are the maximum on time losses that are acceptable.

Disabling Block Section

This section consists of a “definitive inhibition latch” (directly supplied by the V_{cc}) that disables the output (the output is forced to zero).

In effect, this block aims at definitively disabling the circuit when one of the following faults is detected:

— a Winding Short Circuit
— too high synchronization pulses
— a too high input power
— a too high power switch (MOSFET) heating

The signals corresponding to these faults are high when a fault is detected (for instance, when the input power is detected as too high, Dis_{MPL} is high).

When one (or several) of these four faults is detected, a current source charges C_{ext} (with a certain duty cycle) and when its voltage becomes higher than V_{ref}, the definitive inhibition latch is activated. Thus, the circuit gets definitively disabled after a delay depending on C_{ext}.

According to the detected fault, the current that charges C_{ext} is not the same:

The typical values are:

— 260 μA for EHTOVP and WSCD
— 8.5 μA for OHD and MPL

when R_{ref} is equal to 10 kΩ.

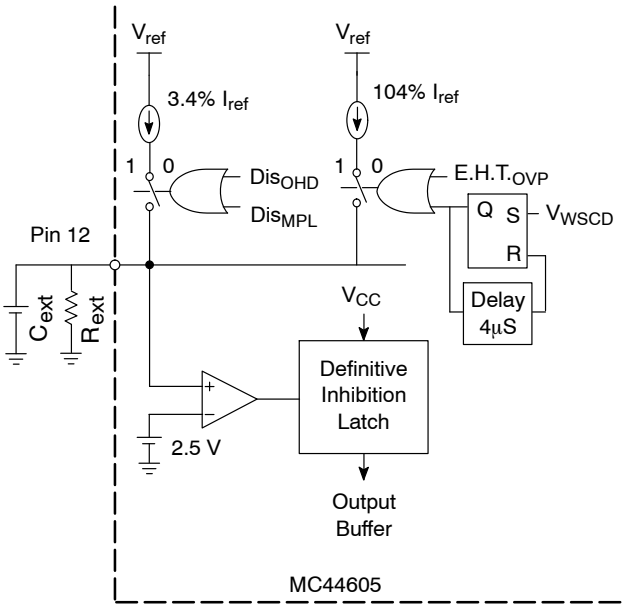


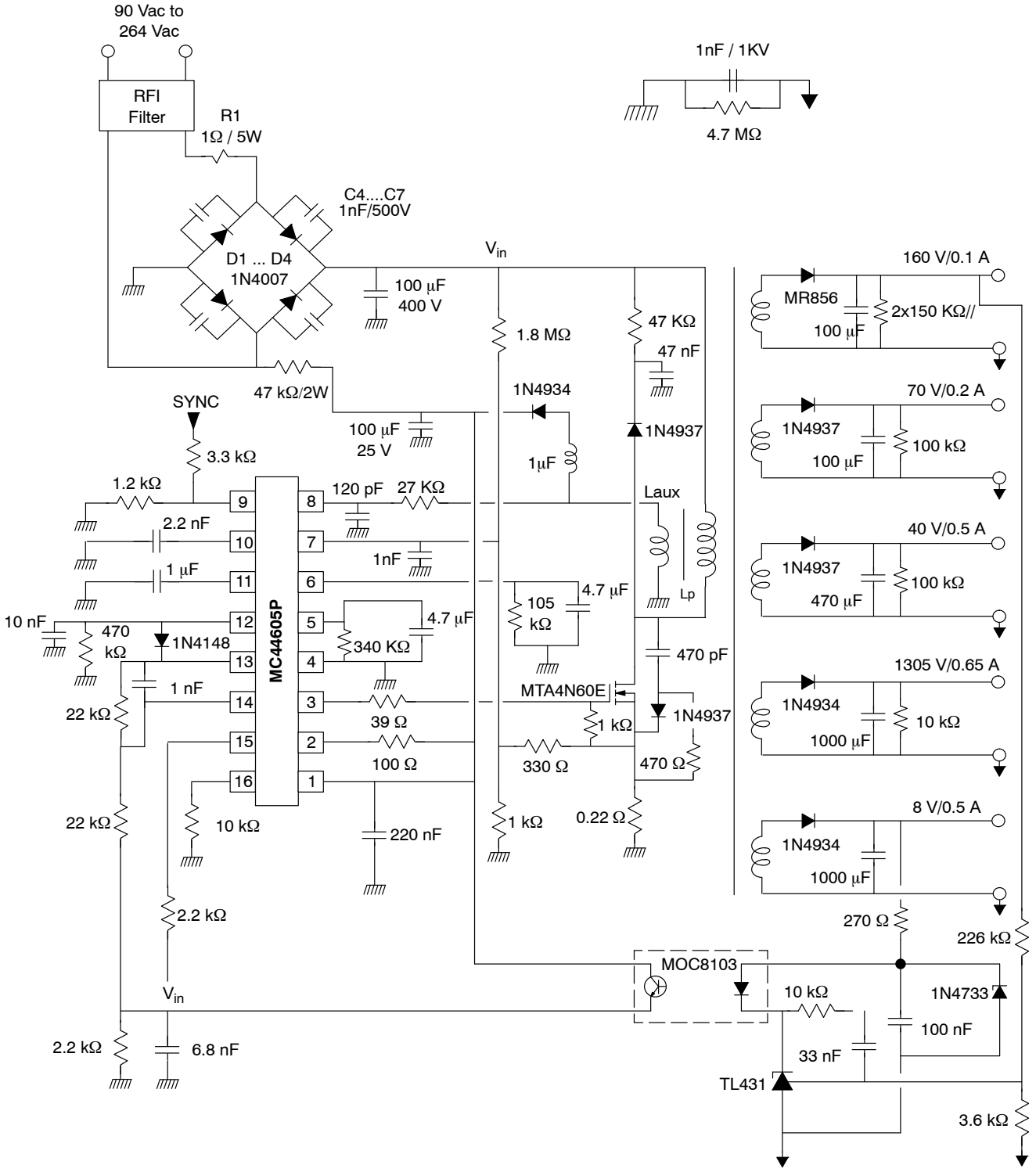
Figure 15. Disabling Block

This latch is reset when the V_{cc} falls down to about 3.0 V. In this case, if a new startup is performed, the circuit will work normally (until this fault or another one is detected).

Practically, to re−start after a fault has shutdown the circuit, the converter must be turned off for a time long enough to enable the V_{cc} capacitor discharge (repair time...).

Note: As V_{WSCD} is generally a really narrow pulse, it is necessary to add a latch and a delay to build a 4 μs width pulse when V_{WSCD} becomes high.

Application Schematic



65 W output SMPS controlled by the MC44605
Mains input range: 90 Vac <–> 264 Vac
Synchronization range: 30 kHz <–> 100 kHz

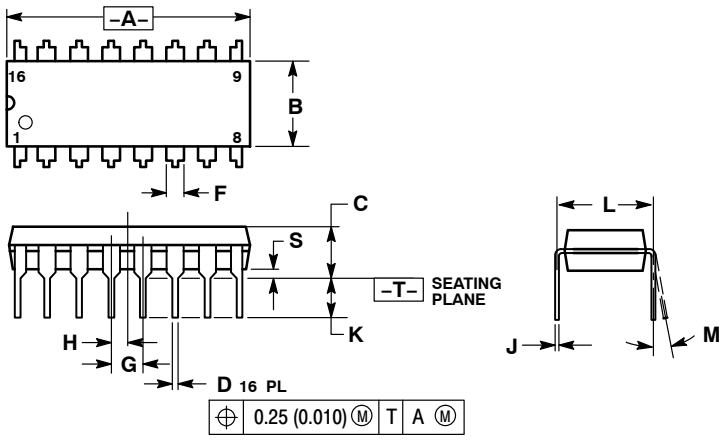
Orega Transformer ref. G5984–00
(Lp = 195 µH)

Performances

Input Voltage	90−260 Vac		
Synchronization Range	30 to 100 kHz		
Outputs	160 V	100 mA	
	70 V	200 mA	
	40 V	500 mA	
	13.5 V	650 mA	
	8.0 V	500 mA	
Measured Efficiency (Pout = 64 W)	30 kHz	110 Vac (Input)	80%
		220 Vac	83%
	60 kHz	110 Vac	81%
		220 Vac	82%
	100 kHz	110 Vac	80%
		220 Vac	80%
Standby Losses (No Load − Pout = 0)	110 Vac	2.0 W	
	220 Vac	3.2 W	
EHTovp Threshold	28 V		
Maximum Power Limitation	30 kHz	110 Vac (Input)	86 W (Input)
		220 Vac	87 W
	60 kHz	110 Vac	90 W
		220 Vac	95 W
	100 kHz	110 Vac	94 W
		220 Vac	110 W
Overheating Detection (Pout = 64 W): The input rms levels at which the circuit detects an OHD case.	30 kHz	85 V	
	60 kHz	76 V	
	100 kHz	76 V	
Winding Short Circuit Detection	Fully Functional (Tested by short circuiting one output diode or one transformer winding)		

PACKAGE DIMENSIONS

PDIP−16
CASE 648−08
ISSUE T



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0 °	10 °	0 °	10 °
S	0.020	0.040	0.51	1.01

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