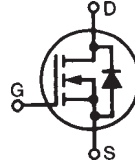


High Voltage Power MOSFET

IXTU05N100 IXTY05N100

$V_{DSS} = 1000V$
 $I_{D25} = 750mA$
 $R_{DS(on)} \leq 17\Omega$

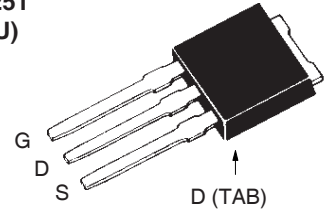
N-Channel Enhancement Mode
Avalanche Rated



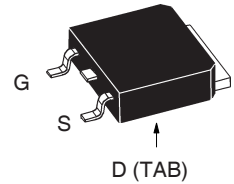
| Symbol | Test Conditions | Maximum Ratings | |
|------------|---|-----------------|------------|
| V_{DSS} | $T_J = 25^\circ C$ to $150^\circ C$ | 1000 | V |
| V_{DGR} | $T_J = 25^\circ C$ to $150^\circ C$, $R_{GS} = 1M\Omega$ | 1000 | V |
| V_{GSS} | Continuous | ± 30 | V |
| V_{GSM} | Transient | ± 40 | V |
| I_{D25} | $T_C = 25^\circ C$ | 750 | mA |
| I_{DM} | $T_C = 25^\circ C$, Pulse Width Limited by T_{JM} | 3 | A |
| I_A | $T_C = 25^\circ C$ | 1 | A |
| E_{AS} | $T_C = 25^\circ C$ | 100 | mJ |
| dv/dt | $I_S \leq I_{DM}$, $V_{DD} \leq V_{DSS}$, $T_J = 150^\circ C$ | 3 | V/ns |
| P_D | $T_C = 25^\circ C$ | 40 | W |
| T_J | | -55 ... +150 | $^\circ C$ |
| T_{JM} | | 150 | $^\circ C$ |
| T_{stg} | | -55 ... +150 | $^\circ C$ |
| T_L | Maximum Lead Temperature for Soldering | 300 | $^\circ C$ |
| T_{SOLD} | 1.6 mm (0.062in.) from Case for 10s | 260 | $^\circ C$ |
| F_C | Mounting force | 1.13 / 10 | Nm/lb.in. |
| Weight | TO-251 | 0.40 | g |
| | TO-252 | 0.35 | g |

| Symbol | Test Conditions ($T_J = 25^\circ C$, Unless Otherwise Specified) | Characteristic Values | | |
|--------------|---|-----------------------|------|---------------------------|
| | | Min. | Typ. | Max. |
| BV_{DSS} | $V_{GS} = 0V$, $I_D = 250\mu A$ | 1000 | | V |
| $V_{GS(th)}$ | $V_{DS} = V_{GS}$, $I_D = 250\mu A$ | 2.5 | | 4.5 V |
| I_{GSS} | $V_{GS} = \pm 30V$, $V_{DS} = 0V$ | | | ± 100 nA |
| I_{DSS} | $V_{DS} = V_{DSS}$, $V_{GS} = 0V$ $T_J = 125^\circ C$ | | | 25 μA 500 μA |
| $R_{DS(on)}$ | $V_{GS} = 10V$, $I_D = 375mA$, Note 1 | | | 17 Ω |

TO-251
(IXTU)



TO-252
(IXTY)



G = Gate D = Drain
 S = Source TAB = Drain

Features

- International Standard Packages
- Fast Switching Times
- Avalanche Rated
- $R_{ds(on)}$ HDMOS™ Process
- Rugged Polysilicon Gate Cell structure
- Extended FBSOA

Advantages

- High Power Density
- Space Savings

Applications

- Switch-Mode and Resonant-Mode Power Supplies
- Flyback Inverters
- DC Choppers

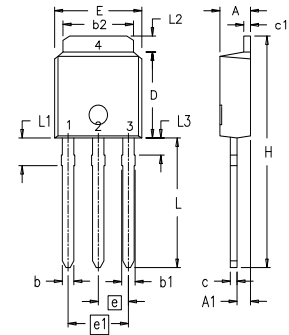
| Symbol | Test Conditions ($T_J = 25^\circ\text{C}$, Unless Otherwise Specified) | Characteristic Values | | |
|--------------|---|-----------------------|------|------------------------|
| | | Min. | Typ. | Max. |
| g_{fs} | $V_{DS} = 20\text{V}$, $I_D = 500\text{mA}$, Note 1 | 0.55 | 0.93 | S |
| C_{iss} | $V_{GS} = 0\text{V}$, $V_{DS} = 25\text{V}$, $f = 1\text{MHz}$ | | 260 | pF |
| C_{oss} | | | 22 | pF |
| C_{rss} | | | 8 | pF |
| $t_{d(on)}$ | Resistive Switching Times $V_{GS} = 10\text{V}$, $V_{DS} = 0.5 \cdot V_{DSS}$, $I_D = 1\text{A}$ $R_G = 47\Omega$ (External) | | 11 | ns |
| t_r | | | 19 | ns |
| $t_{d(off)}$ | | | 40 | ns |
| t_f | | | 28 | ns |
| $Q_{g(on)}$ | $V_{GS} = 10\text{V}$, $V_{DS} = 0.5 \cdot V_{DSS}$, $I_D = 1\text{A}$ | | 7.8 | nC |
| Q_{gs} | | | 1.4 | nC |
| Q_{gd} | | | 4.1 | nC |
| R_{thJC} | | | | 3.1 $^\circ\text{C/W}$ |

Source-Drain Diode

| Symbol | Test Conditions ($T_J = 25^\circ\text{C}$, Unless Otherwise Specified) | Characteristic Values | | |
|----------|--|-----------------------|------|--------|
| | | Min. | Typ. | Max. |
| I_S | $V_{GS} = 0\text{V}$ | | | 750 mA |
| I_{SM} | Repetitive, Pulse Width Limited by T_{JM} | | | 3 A |
| V_{SD} | $I_F = I_S$, $V_{GS} = 0\text{V}$, Note 1 | | | 1.5 V |
| t_{rr} | $I_F = I_S$, $-di/dt = 100\text{A}/\mu\text{s}$ $V_R = 100\text{V}$, $V_{GS} = 0\text{V}$ | | 710 | ns |

Note 1: Pulse test, $t \leq 300\mu\text{s}$, duty cycle, $d \leq 2\%$.

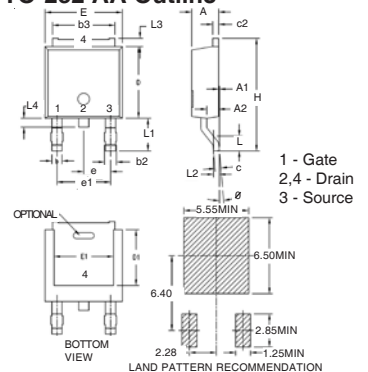
TO-251 Outline



1. Gate 2. Drain
3. Source 4. Drain

| Dim. | Millimeter | | Inches | |
|------|------------|-------|--------|------|
| | Min. | Max. | Min. | Max. |
| A | 2.19 | 2.38 | .086 | .094 |
| A1 | 0.89 | 1.14 | 0.35 | .045 |
| b | 0.64 | 0.89 | .025 | .035 |
| b1 | 0.76 | 1.14 | .030 | .045 |
| b2 | 5.21 | 5.46 | .205 | .215 |
| c | 0.46 | 0.58 | .018 | .023 |
| c1 | 0.46 | 0.58 | .018 | .023 |
| D | 5.97 | 6.22 | .235 | .245 |
| E | 6.35 | 6.73 | .250 | .265 |
| e | 2.28 | BSC | .090 | BSC |
| e1 | 4.57 | BSC | .180 | BSC |
| H | 17.02 | 17.78 | .670 | .700 |
| L | 9.89 | 9.65 | .350 | .380 |
| L1 | 1.91 | 2.28 | .075 | .090 |
| L2 | 0.89 | 1.27 | .035 | .050 |

TO-252 AA Outline



- 1 - Gate
2, 4 - Drain
3 - Source

| SYM | INCHES | | MILLIMETERS | |
|-------|----------|------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | .086 | .094 | 2.19 | 2.38 |
| A1 | 0 | .005 | 0 | 0.12 |
| A2 | .038 | .046 | 0.97 | 1.17 |
| b | .025 | .035 | 0.64 | 0.89 |
| b2 | .030 | .045 | 0.76 | 1.14 |
| b3 | .200 | .215 | 5.08 | 5.46 |
| c | .018 | .024 | 0.46 | 0.61 |
| c2 | .018 | .023 | 0.46 | 0.58 |
| D | .235 | .245 | 5.97 | 6.22 |
| D1 | .180 | .205 | 4.57 | 5.21 |
| E | .250 | .265 | 6.35 | 6.73 |
| E1 | .170 | .205 | 4.32 | 5.21 |
| e | .090 BSC | | 2.28 BSC | |
| e1 | .180 BSC | | 4.57 BSC | |
| H | .370 | .410 | 9.40 | 10.42 |
| L | .055 | .070 | 1.40 | 1.78 |
| L1 | .100 | .115 | 2.54 | 2.92 |
| L2 | .020 BSC | | 0.50 BSC | |
| L3 | .025 | .040 | 0.64 | 1.02 |
| L4 | .025 | .040 | 0.64 | 1.02 |
| theta | 0° | 10° | 0° | 10° |

IXYS Reserves the Right to Change Limits, Test Conditions, and Dimensions.

| | | | | | | | | | | |
|--|-----------|-----------|-----------|-----------|--------------|--------------|--------------|--------------|--------------|-------------|
| IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents: | 4,835,592 | 4,931,844 | 5,049,961 | 5,237,481 | 6,162,665 | 6,404,065 B1 | 6,683,344 | 6,727,585 | 7,005,734 B2 | 7,157,338B2 |
| | 4,860,072 | 5,017,508 | 5,063,307 | 5,381,025 | 6,259,123 B1 | 6,534,343 | 6,710,405 B2 | 6,759,692 | 7,063,975 B2 | |
| | 4,881,106 | 5,034,796 | 5,187,117 | 5,486,715 | 6,306,728 B1 | 6,583,505 | 6,710,463 | 6,771,478 B2 | 7,071,537 | |

Fig. 1. Output Characteristics @ $T_J = 25^\circ\text{C}$

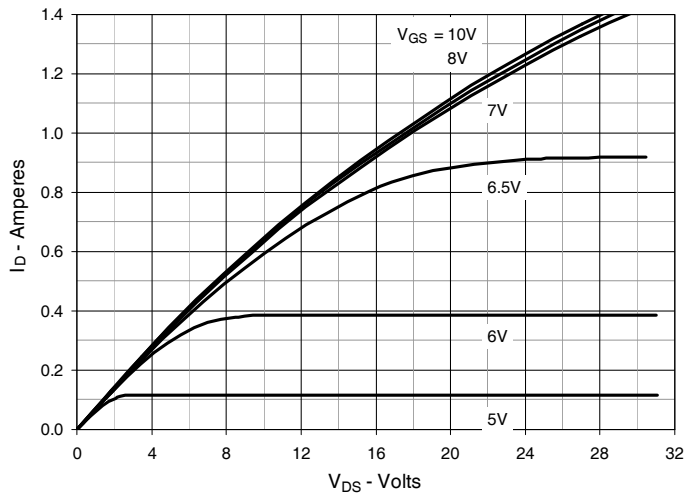


Fig. 2. Output Characteristics @ $T_J = 125^\circ\text{C}$

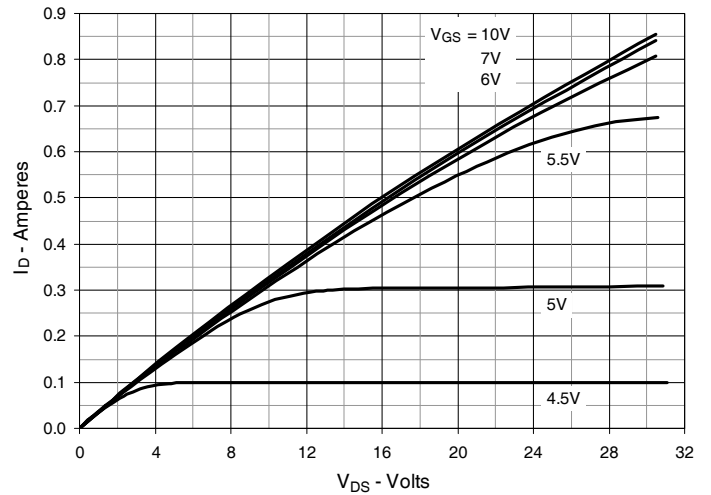


Fig. 3. $R_{DS(on)}$ Normalized to $I_D = 0.35\text{A}$ Value vs. Junction Temperature

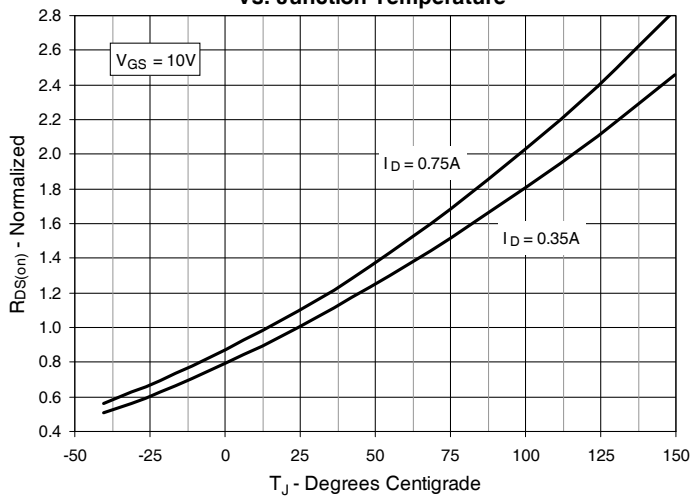


Fig. 4. $R_{DS(on)}$ Normalized to $I_D = 0.35\text{A}$ Value vs. Drain Current

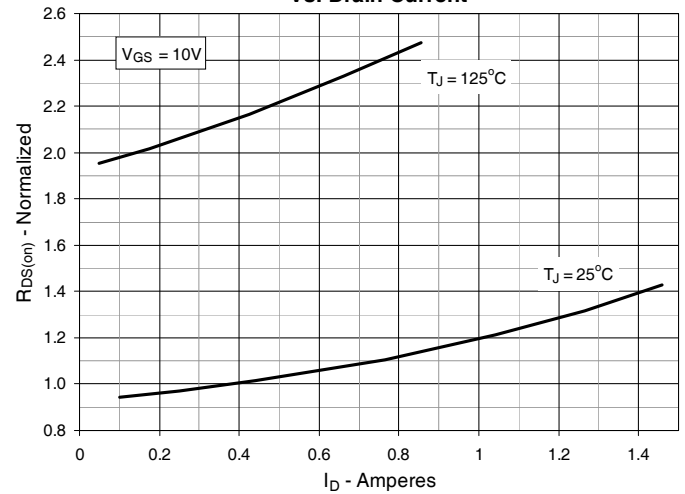


Fig. 5. Maximum Drain Current vs. Case Temperature

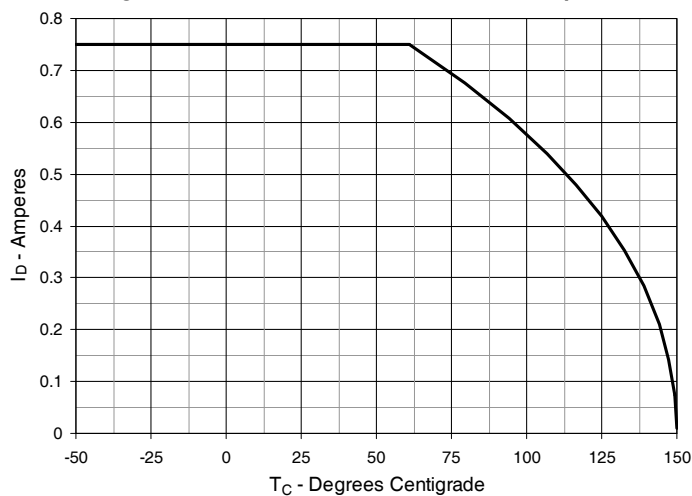


Fig. 6. Input Admittance

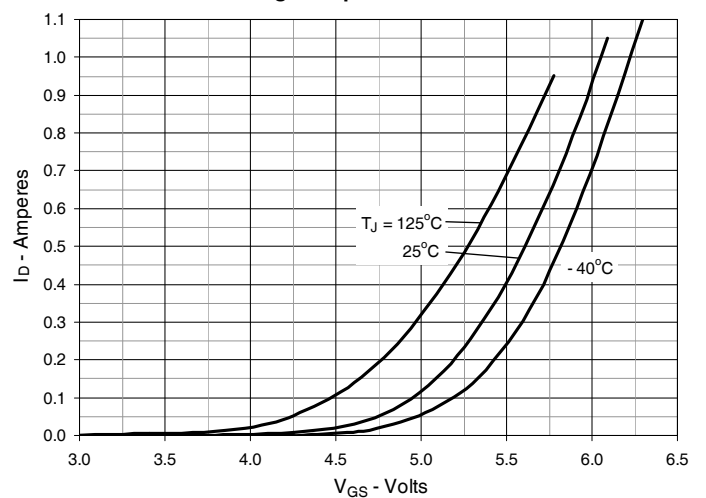


Fig. 7. Transconductance

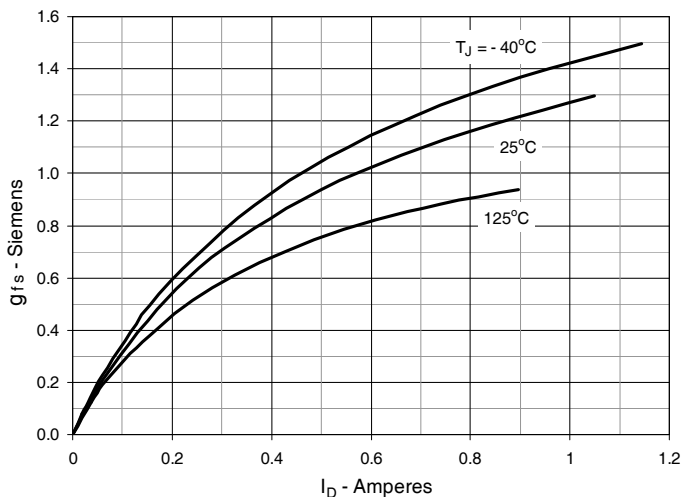


Fig. 8. Forward Voltage Drop of Intrinsic Diode

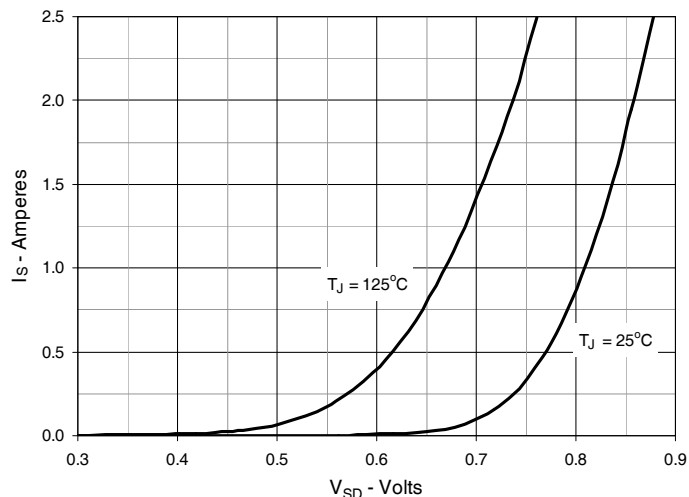


Fig. 9. Gate Charge

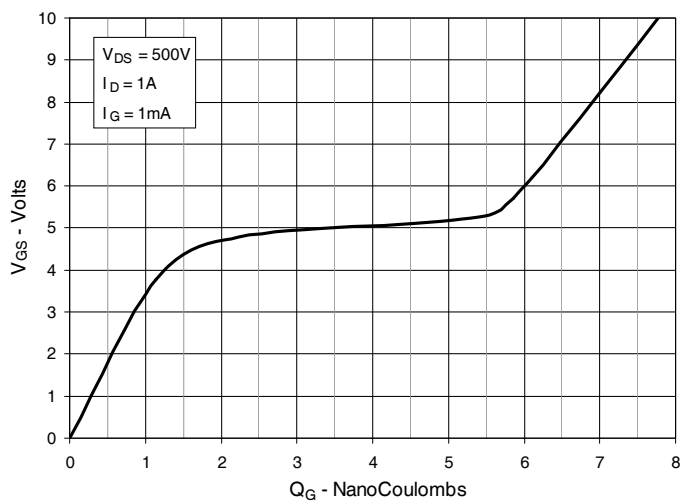


Fig. 10. Capacitance

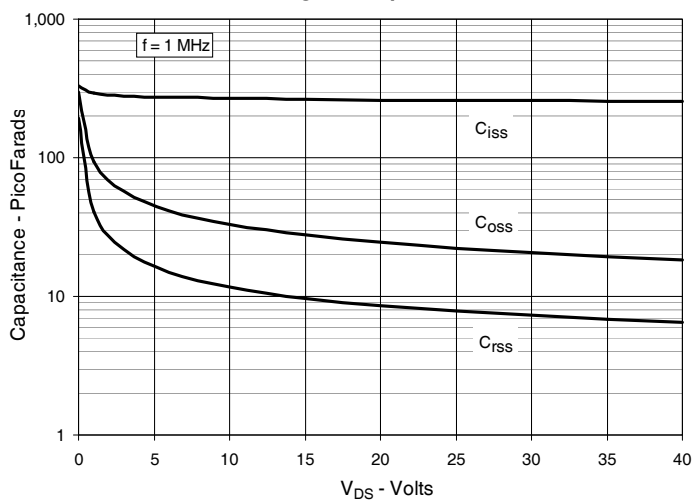


Fig. 11. Forward-Bias Safe Operating Area @ $T_C = 25^\circ\text{C}$

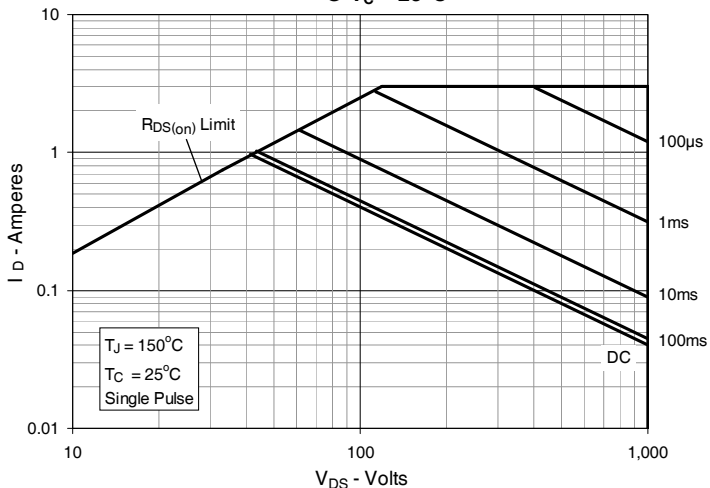


Fig. 12. Forward-Bias Safe Operating Area @ $T_C = 75^\circ\text{C}$

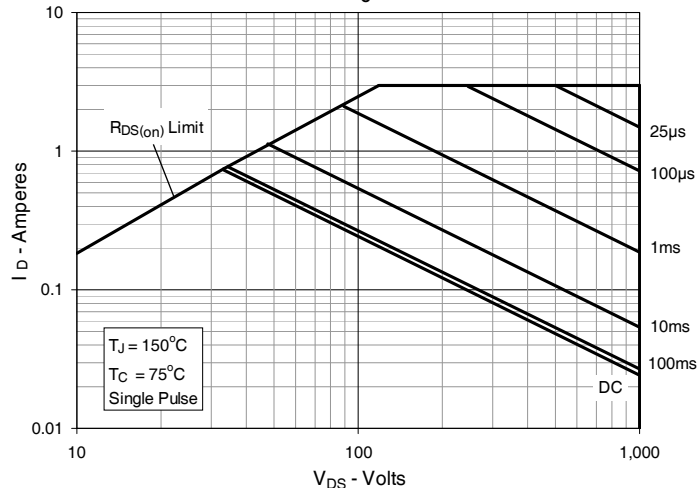
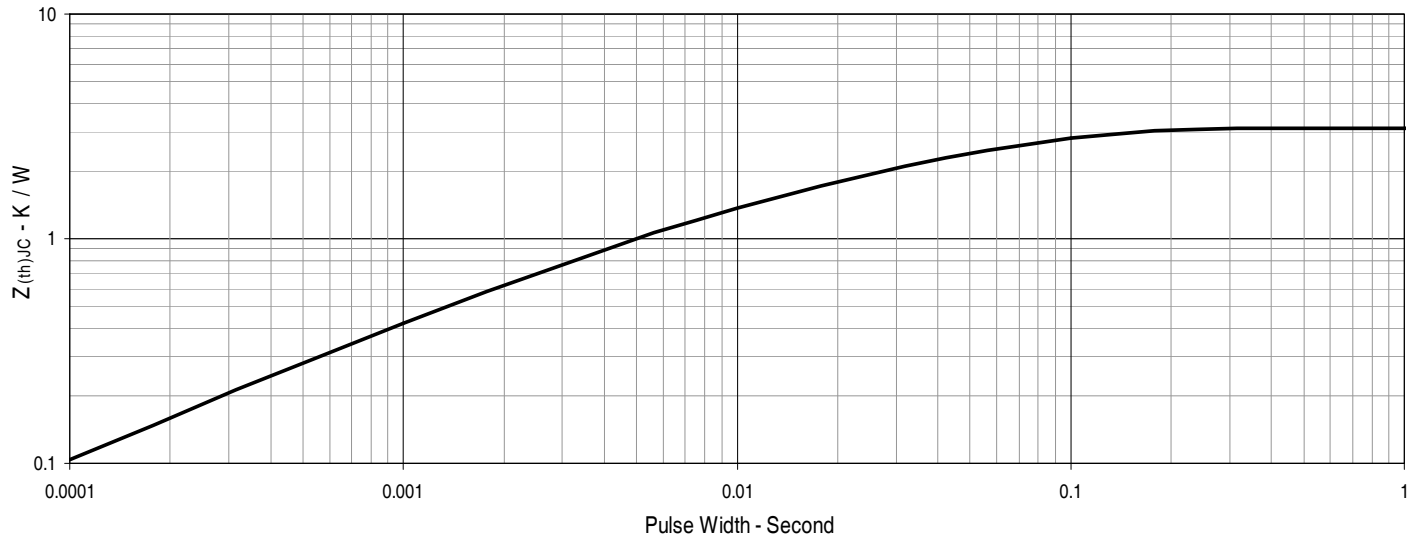


Fig. 13. Maximum Transient Thermal Impedance





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