NCP1237

Fixed Frequency Current Mode Controller for Flyback Converters

The NCP1237 is a new generation of the NCP12xx fixed−frequency current−mode controllers featuring Dynamic Self−Supply (DSS), pin−to−pin compatible with the previous generation.

The DSS function greatly simplifies the design of the auxiliary supply and the V_{CC} capacitor by activating the internal startup current source to supply the controller during transients.

Due to its proprietary Soft−Skip™ mode combined with frequency foldback, the controller exhibits excellent efficiency in light load condition while still achieving very low standby power consumption. This Soft−Skip feature also dramatically reduces the risk of acoustic noise, which enables the use of inexpensive transformers and capacitors in the clamping network.

The NCP1237 features a dual−level timer−based fault detection that controls the amount of transient peak power that the controller can deliver for a limited time.

Internal frequency jittering, ramp compensation, and a versatile latch input make this controller an excellent candidate for converters where ruggedness and components cost are the key constraints.

In addition, the controller includes a new high voltage circuitry that combines a startup current source and a brown−out / line OVP detector able to sense the input voltage either from the rectified ac line or the dc filtered bulk voltage.

Finally, due to a careful design, the precision of critical parameters is well controlled over the entire temperature range (−40°C to +125°C), enabling easier design and increased safety (e.g. ±5% for the peak current limit, ±7% for the oscillator).

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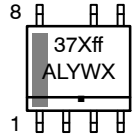
MARKING DIAGRAM

SOIC−7
CASE 751U



37Xff = Specific Device Code
X = A or B
ff = 65, 00, or 33
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 40 of this data sheet.

Features

- Timer−Based Transient Power and Overload Protections with Auto−Recovery (Option B) or Latched (Option A) Operation
- High−Voltage Current Source with DSS with Built−in Brown−out and Line Overvoltage Protections
- Fixed−Frequency Current−Mode Operation with Built−in Ramp Compensation
- Frequency Jittering for a Reduced EMI Signature
- Adjustable Overpower Compensation
- Latch−off Input for Severe Fault Conditions, with Direct Connection of an NTC for Overtemperature Protection (OTP)
- Protection Against Winding Short−Circuit
- Frequency Foldback transitioning into Soft−Skip for Improved Performance in Standby
- 65 kHz Oscillator (100 kHz and 133 kHz Versions Available Upon Request)
- V_{CC} Operation up to 28 V
- Increased Precision on Critical Parameters
- ±1.0 A Peak Drive Capability
- 4.0 ms Soft−Start
- Internal Thermal Shutdown with Hysteresis
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant*

Typical Applications

- ac−dc Adapters for Notebooks, LCD, and Printers
- Offline Battery Chargers
- Consumer Electronic Power Supplies
- Auxiliary/Housekeeping Power Supplies

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

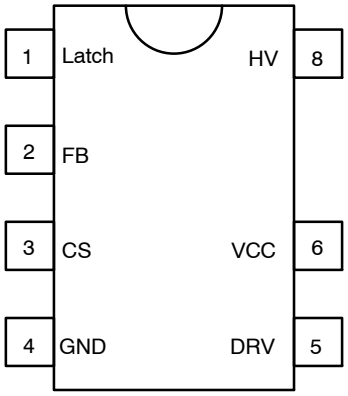


Figure 1. Pinout

TYPICAL APPLICATION EXAMPLE

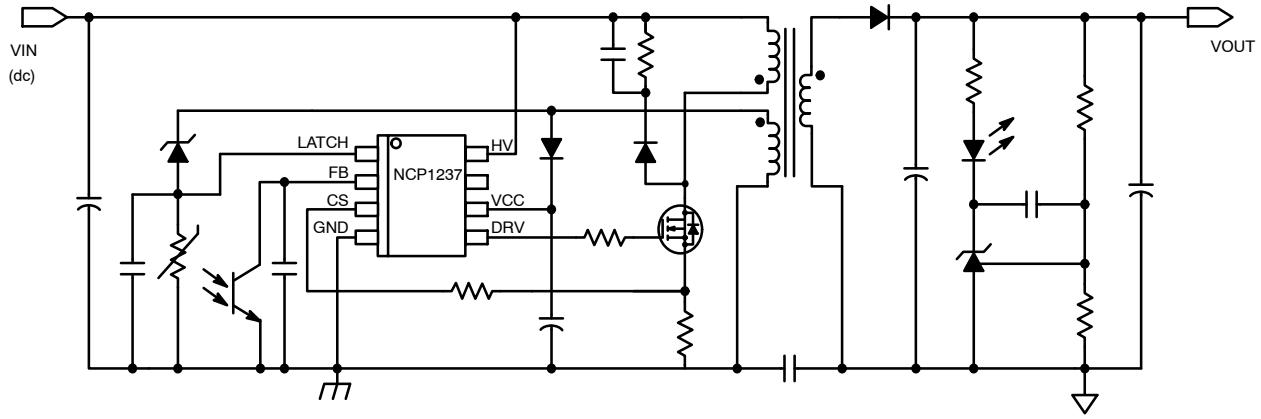


Figure 2. Typical Application

PIN FUNCTION DESCRIPTION

Pin No	Pin Name	Function	Pin Description
1	LATCH	Latch−off Input	Pull the pin up or down to latch−off the controller. An internal current source allows the direct connection of an NTC for over temperature detection
2	FB	Feedback	A pull−down optocoupler controls the output regulation.
3	CS	Current Sense	Senses the primary current for current−mode operation, and provides a mean for overpower compensation adjustment.
4	GND	−	IC ground
5	DRV	Drive Output	Drives an external MOSFET
6	V_{CC}	V_{CC} Input	This supply pin accepts up to 28 Vdc
8	HV	High−Voltage Pin	Connects to the bulk capacitor or the rectified AC line to perform the functions of Dynamic Self−Supply and brown−out / line overvoltage detections

SIMPLIFIED INTERNAL BLOCK SCHEMATIC

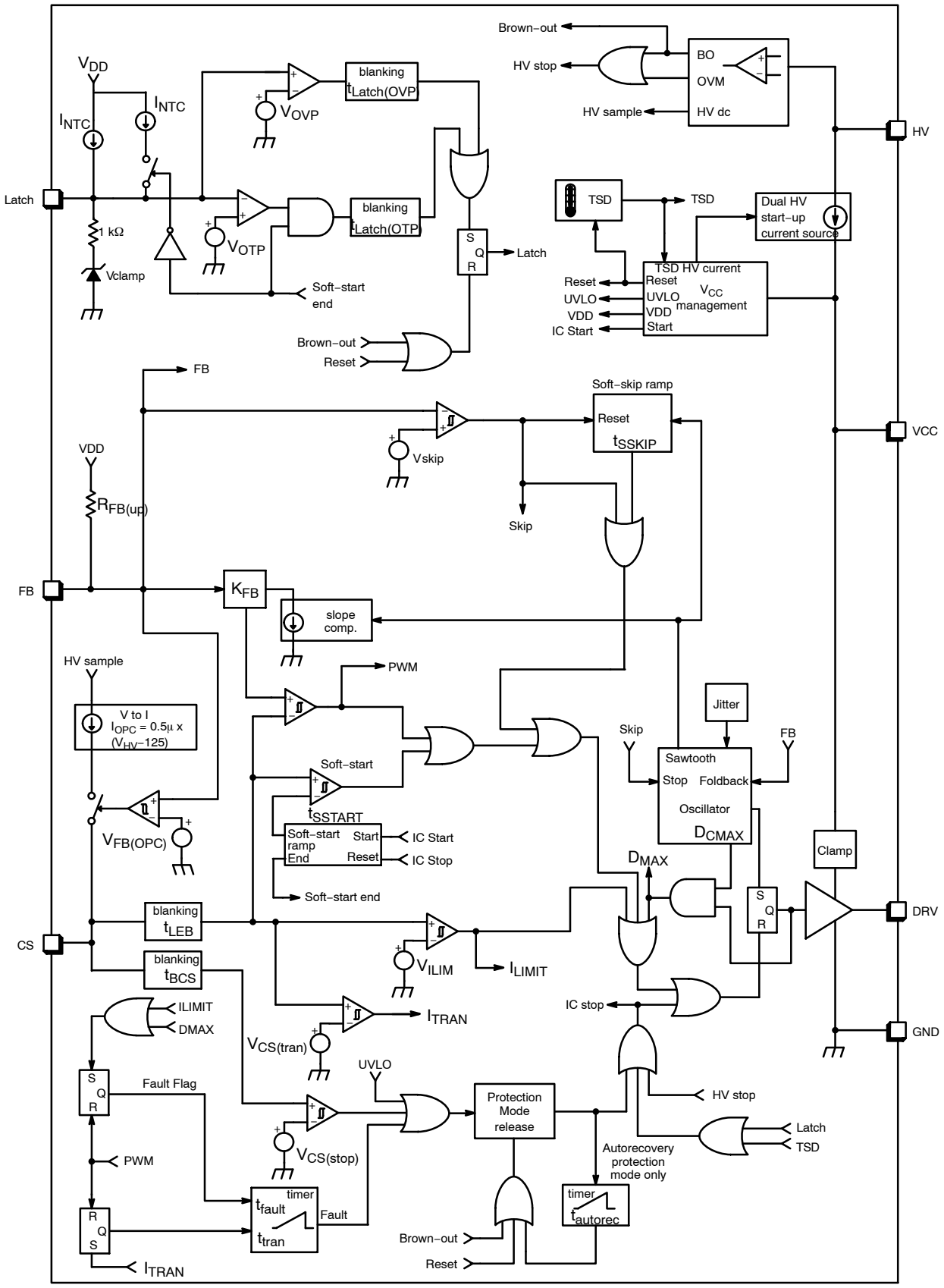


Figure 3. Simplified Internal Block Schematic

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Pin (pin 6) (Note 1) Voltage range Current range	 V_{CCMAX} I_{CCMAX}	 −0.3 to 28 ±30	 V mA
High Voltage Pin (pin 8) (Note 1) Voltage range Current range	 V_{HVMAX} I_{HVMAX}	 −0.3 to 500 ±20	 V mA
Driver Pin (pin 5) (Note 1) Voltage range Current range	 V_{DRVMAX} I_{DRVMAX}	 −0.3 to 20 ±1500	 V mA
All other pins (Note 1) Voltage range Current range	 V_{MAX} I_{MAX}	 −0.3 to 10 ±10	 V mA
Thermal Resistance SOIC−7 Junction−to−Air, low conductivity PCB (Note 2) Junction−to−Air, medium conductivity PCB (Note 3) Junction−to−Air, high conductivity PCB (Note 4)	$R_{\theta JA}$	 162 147 125	°C/W
Temperature Range Operating Junction Temperature Storage Temperature Range	 T_{JMAX} $T_{STRGMAX}$	 −40 to +150 −60 to +150	°C
ESD Capability Human Body Model (HBM) per JEDEC standard JESD22, Method A114E (All pins except HV) Machine Model (MM) per JEDEC standard JESD22, Method A115A		 2000 200	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. This device contains latch−up protection and exceeds 100 mA per JEDEC Standard JESD78
2. As mounted on a 80 x 100 x 1.5 mm FR4 substrate with a single layer of 100 mm^2 of 1 oz copper traces and heat spreading area. As specified for a JEDEC 51−1 conductivity test PCB. Test conditions were under natural convection or zero air flow.
3. As mounted on a 80 x 100 x 1.5 mm FR4 substrate with a single layer of 100 mm^2 of 2 oz copper traces and heat spreading area. As specified for a JEDEC 51−2 conductivity test PCB. Test conditions were under natural convection or zero air flow.
4. As mounted on a 80 x 100 x 1.5 mm FR4 substrate with a single layer of 650 mm^2 of 1 oz copper traces and heat spreading area. As specified for a JEDEC 51−3 conductivity test PCB. Test conditions were under natural convection or zero air flow.

ELECTRICAL CHARACTERISTICS (For typical values T_J = 25°C, for min/max values T_J = −40°C to +125°C, V_{HV} = 120 V, V_{CC} = 11 V unless otherwise noted)

Characteristics	Test Condition	Symbol	Min	Typ	Max	Unit
HIGH VOLTAGE CURRENT SOURCE						
Minimum voltage for current source operation		$V_{HV(min)}$	–	–	60	V
Current flowing out of V_{CC} pin @ V_{HV} = 60 V	V_{CC} = 0 V V_{CC} = $V_{CC(on)}$ − 0.5 V	I_{start1} I_{start2}	0.2 4	0.5 8	0.8 12	mA
Off−state leakage current	V_{HV} = 500 V	$I_{start(off)}$	–	25	50	μA
SUPPLY						
Turn−on threshold level, V_{CC} going up HV current source stop threshold		$V_{CC(on)}$	11.0	12.0	13.0	V
HV current source restart threshold		$V_{CC(min)}$	9.5	10.5	11.5	V
Turn−off threshold level		$V_{CC(off)}$	8.5	9.5	10.5	V
Blanking duration on $V_{CC(min)}$ and $V_{CC(off)}$ detection	Guaranteed by design	$t_{UVLO(blank)}$	7	10	13	μs
V_{CC} decreasing level at which the internal logic resets		$V_{CC(reset)}$	4.0	5.2	6.5	V
V_{CC} level for I_{START1} to I_{START2} transition		$V_{CC(inhibit)}$	0.4	0.65	0.9	V
Internal current consumption (Note 5)	DRV open, V_{FB} = 3 V C_{drv} = 1 nF, V_{FB} = 3 V Off mode (skip or before startup) Fault mode (fault or latch)	ICC1 ICC2 ICC3 ICC4	2.0 2.3 0.9 0.4	2.5 3.3 1.2 0.7	3.0 4.3 1.5 1.0	mA
BROWN−OUT AND LINE OVERVOLTAGE						
Brown−out threshold voltage	V_{HV} going up V_{HV} going down	$V_{HV(start)}$ $V_{HV(stop)}$	104 97	112 105	120 113	V
Timer duration for line cycle drop−out		t_{HV}	43	61	79	ms
Overvoltage threshold	V_{HV} going up V_{HV} going down	$V_{HV(OV1)}$ $V_{HV(OV2)}$	400 395	430 425	460 455	V
Blanking duration on line overvoltage detection		$t_{OV(blank)}$	–	250	–	μs
OSCILLATOR						
Oscillator frequency		f_{OSC}	60	65	70	kHz
Maximum duty ratio		D_{MAX}	75	80	85	%
Frequency jittering amplitude, in percentage of F_{OSC}	Guaranteed by design	A_{jitter}	±4	±6	±8	%
Frequency jittering modulation frequency	Guaranteed by design	F_{jitter}	85	125	165	Hz
OUTPUT DRIVER						
Rise time, 10% to 90% of V_{CC}	V_{CC} = $V_{CC(min)}$ + 0.2 V, C_{DRV} = 1 nF	t_{rise}	–	22	34	ns
Fall time, 90% to 10% of V_{CC}	V_{CC} = $V_{CC(min)}$ + 0.2 V, C_{DRV} = 1 nF	t_{fall}	–	22	34	ns
Current capability	V_{CC} = $V_{CC(min)}$ + 0.2 V, C_{DRV} = 1 nF DRV high, V_{DRV} = 0 V DRV low, V_{DRV} = V_{CC}	 $I_{DRV(source)}$ $I_{DRV(sink)}$	 – –	 1000 1000	 – –	mA
Clamping voltage (maximum gate voltage)	V_{CC} = V_{CCmax} − 0.2 V, DRV high	$V_{DRV(clamp)}$	11	13.5	16	V
High−state voltage drop	V_{CC} = $V_{CC(min)}$ + 0.2 V, R_{DRV} = 33 kΩ, DRV high	$V_{DRV(drop)}$	–	–	1	V

5. Internal supply current only, current in FB pin not included (current flowing through GND pin only).

ELECTRICAL CHARACTERISTICS (For typical values T_J = 25°C, for min/max values T_J = −40°C to +125°C, V_{HV} = 120 V, V_{CC} = 11 V unless otherwise noted)

Characteristics	Test Condition	Symbol	Min	Typ	Max	Unit
CURRENT SENSE						
Input Bias Current	V_{CS} = 0.7 V	I_{bias}	–	0.02	–	μA
Maximum internal current setpoint	V_{FB} > 3.5 V	V_{ILIM}	0.665	0.7	0.735	V
Threshold for immediate fault protection activation		$V_{CS(stop)}$	0.95	1.05	1.15	V
Propagation delay from V_{ILIM} detection to DRV off	V_{CS} = V_{ILIM}	t_{delay}	50	80	110	ns
Leading Edge Blanking Duration for V_{ILIM}		t_{LEB}	190	250	310	ns
Leading Edge Blanking Duration for $V_{CS(stop)}$		t_{BCS}	90	120	150	ns
Slope of the compensation ramp		$S_{comp(65kHz)}$	–	–32.5	–	mV / μs
Soft−start duration	From 1st pulse to V_{CS} = V_{ILIM}	t_{SSTART}	2.8	4.0	5.2	ms
OVERPOWER COMPENSATION						
V_{HV} to I_{OPC} conversion ratio		K_{OPC}	–	0.5	–	μA / V
Current flowing out of CS pin	V_{HV} = 125 V V_{HV} = 162 V V_{HV} = 325 V V_{HV} = $V_{HV(OV2)}$ − 5 V	$I_{OPC(125)}$ $I_{OPC(162)}$ $I_{OPC(325)}$ $I_{OPC(max)}$	– – – 102	0 52 104 120	– – – 138	μA
FB voltage above which I_{OPC} is applied		$V_{FB(OPC)}$	1.50	1.65	1.80	V
FB voltage below which I_{OPC} = 0		$V_{FB(OPCE)}$	–	1.25	–	V
Refresh operation for dc operation		t_{WD}	25	35	45	ms
FEEDBACK						
Internal pull−up resistor	T_J = 25°C	$R_{FB(up)}$	15	20	25	kΩ
V_{FB} to internal current setpoint division ratio		K_{FB}	4.7	5.0	5.3	–
Internal pull−up voltage on the FB pin		$V_{FB(ref)}$	4.3	5.0	5.7	V
OVERCURRENT PROTECTION						
Fault timer duration	From CS reaching V_{ILIMIT} to DRV stop	t_{fault}	64	78	98	ms
Autorecovery mode latch−off time duration		$t_{autorec}$	1.0	1.4	1.8	s
CS threshold for transient peak timer activation		$V_{CS(tran)}$	0.47	0.5	0.53	V
Transient peak power timer duration	$V_{CS(peak)}$ = V_{ILIM} − 5% From 1st time V_{CS} > $V_{CS(tran)}$ to DRV stop	t_{tran}	117	156	195	ms
FREQUENCY FOLDBACK						
Feedback voltage threshold below which frequency foldback starts		$V_{FB(fold)}$	1.3	1.4	1.5	V
Minimum switching frequency	V_{FB} = $V_{skip(in)}$ + 0.2 V	$f_{OSC(min)}$	21	27	31	kHz
Threshold below which the frequency foldback is finished and the controller switches at $f_{OSC(min)}$		$V_{FB(endfold)}$	–	1.0	–	V
SKIP CYCLE MODE						
Feedback voltage thresholds for skip mode	V_{FB} going down V_{FB} going up	$V_{skip(in)}$ $V_{skip(out)}$	0.63 0.72	0.7 0.80	0.77 0.88	V
Soft−skip duration	From 1st pulse to V_{CS} = $V_{FB(fold)}$ / K_{FB}	t_{SSKIP}	–	100	–	μs

5. Internal supply current only, current in FB pin not included (current flowing through GND pin only).

ELECTRICAL CHARACTERISTICS (For typical values T_J = 25°C, for min/max values T_J = −40°C to +125°C, V_{HV} = 120 V, V_{CC} = 11 V unless otherwise noted)

Characteristics	Test Condition	Symbol	Min	Typ	Max	Unit
LATCH−OFF INPUT						
High threshold	V_{Latch} going up	V_{OVP}	2.37	2.5	2.63	V
Low threshold	V_{Latch} going down	V_{OTP}	0.76	0.8	0.84	V
Current source for direct NTC connection During normal operation During soft−start	V_{Latch} = 0 V	 I_{NTC} $I_{NTC(SSTART)}$	 78 156	 91 182	 104 208	µA
Blanking duration on high latch detection		$t_{Latch(OVP)}$	40	55	70	µs
Blanking duration on low latch detection		$t_{Latch(OTP)}$	–	400	–	µs
Clamping voltage	I_{Latch} = 0 mA I_{Latch} = 1 mA	$V_{clamp0(Latch)}$ $V_{clamp1(Latch)}$	1.0 1.8	1.2 2.3	1.4 2.8	V
TEMPERATURE SHUTDOWN						
Temperature shutdown	T_J going up	T_{TSD}	135	150	165	°C
Temperature shutdown hysteresis	T_J going down	$T_{TSD(HYS)}$	20	30	40	°C

5. Internal supply current only, current in FB pin not included (current flowing through GND pin only).

TYPICAL PERFORMANCE CHARACTERISTICS

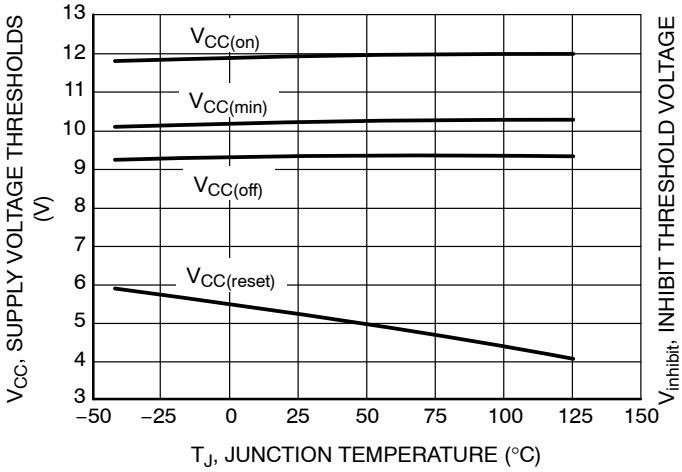


Figure 4. Supply Voltage Thresholds vs. Junction Temperature

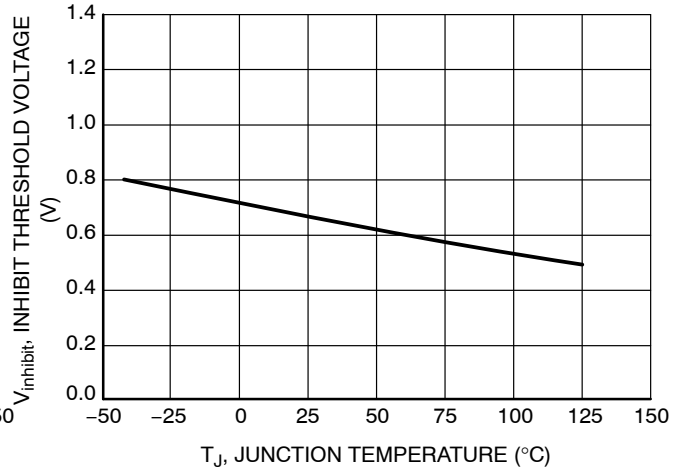


Figure 5. Inhibit Threshold Voltage vs. Junction Temperature

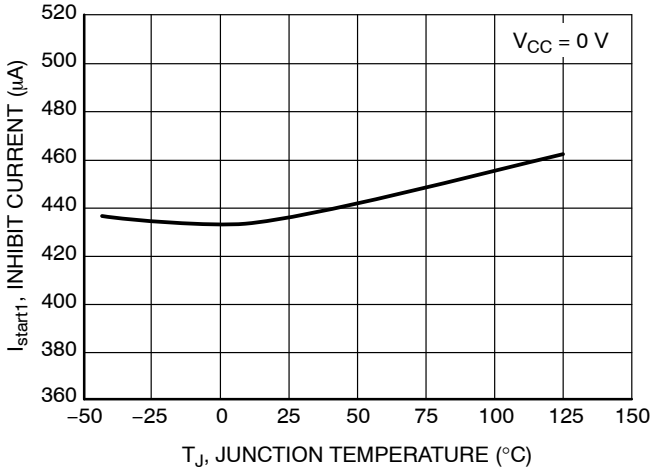


Figure 6. Inhibit Current vs. Junction Temperature

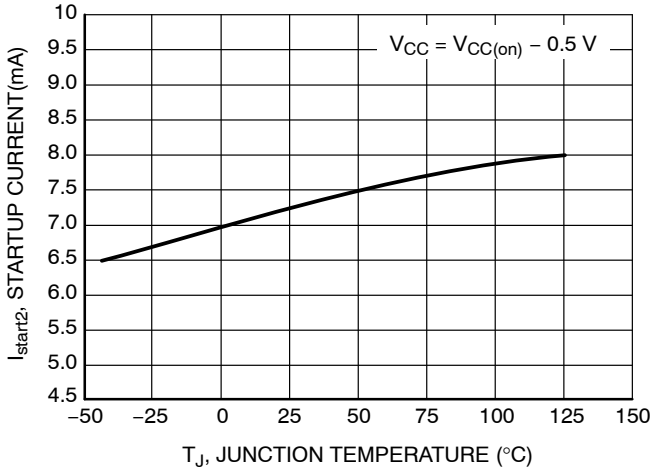


Figure 7. Startup Current vs. Junction Temperature

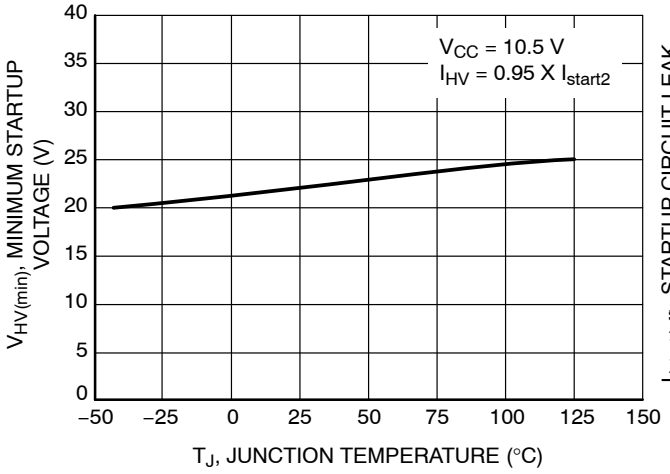


Figure 8. Minimum Startup Voltage vs. Junction Temperature

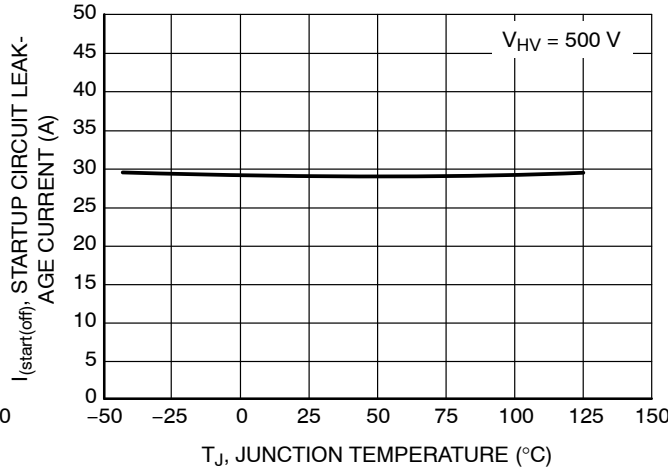


Figure 9. Startup Circuit Leakage Current vs. Junction Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

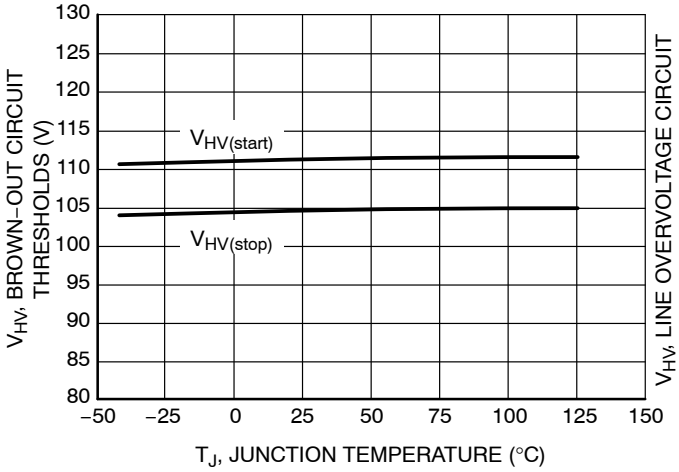


Figure 10. Brown−Out Circuit Thresholds vs. Junction Temperature

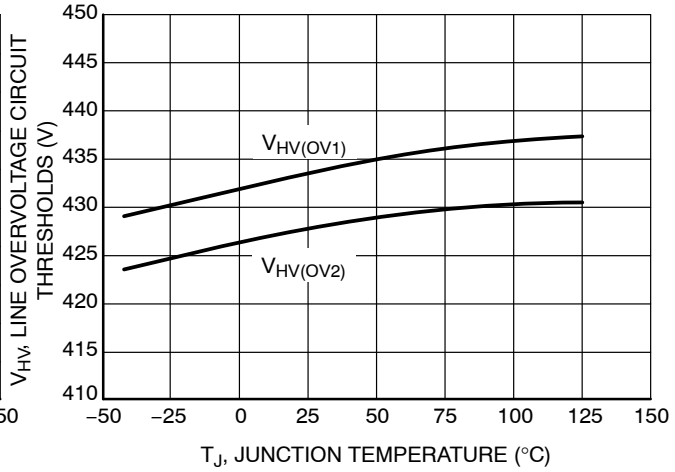


Figure 11. Line Overvoltage Circuit Thresholds vs. Junction Temperature

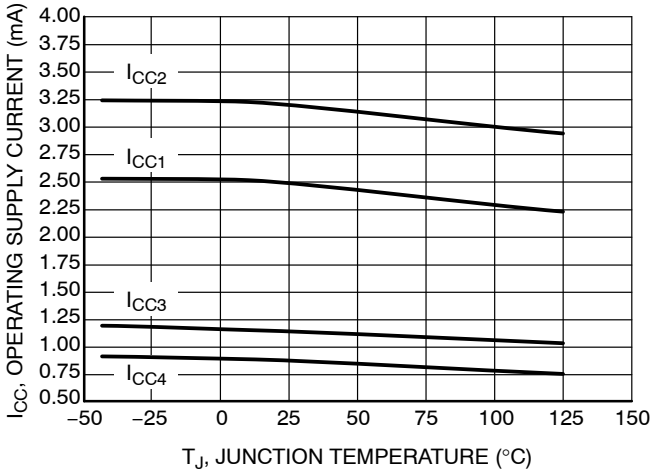


Figure 12. I_{CC} Supply Currents vs. Junction Temperature

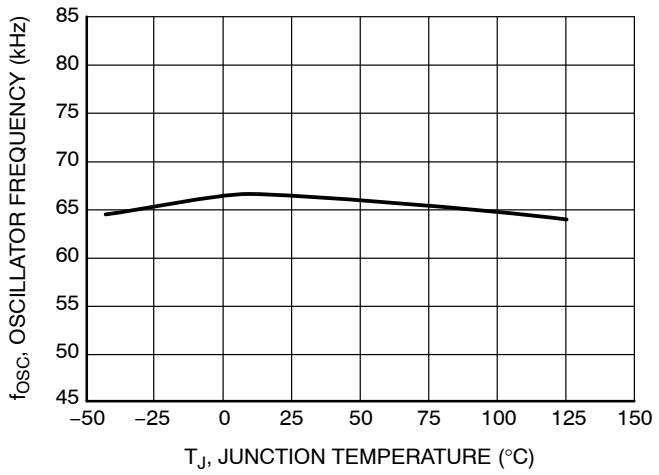


Figure 13. Oscillator Frequency vs. Junction Temperature

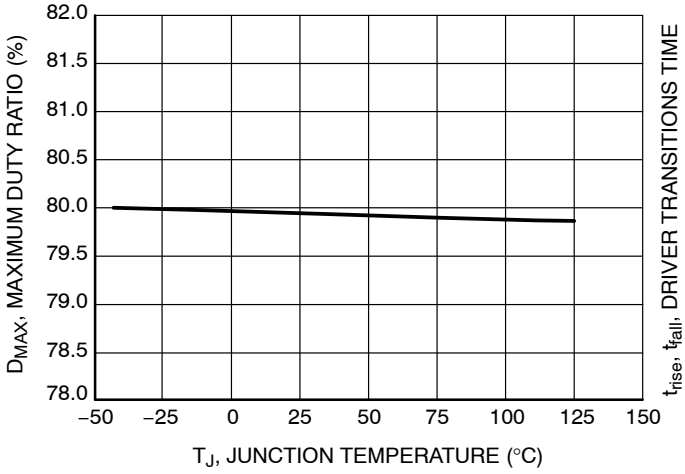


Figure 14. Maximum Duty Ratio vs. Junction Temperature

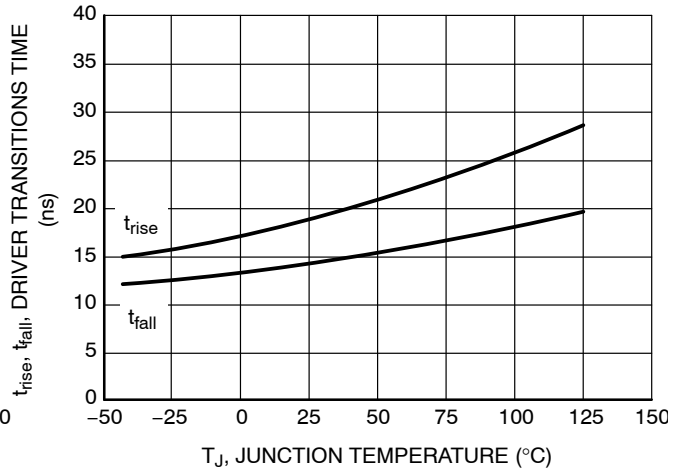


Figure 15. Driver Transitions Time vs. Junction Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

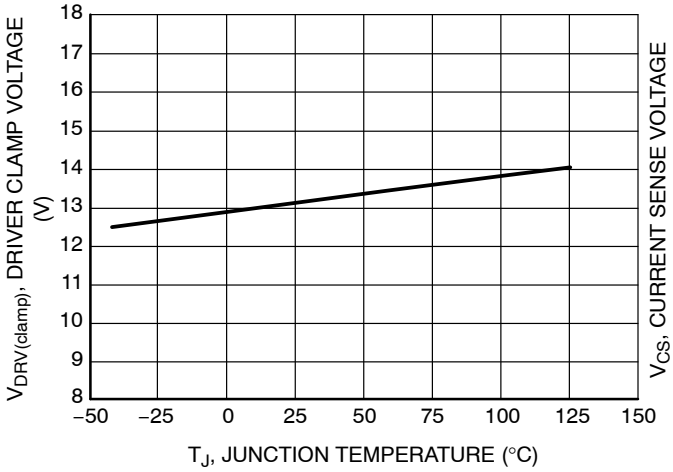


Figure 16. Driver Clamp Voltage vs. Junction Temperature

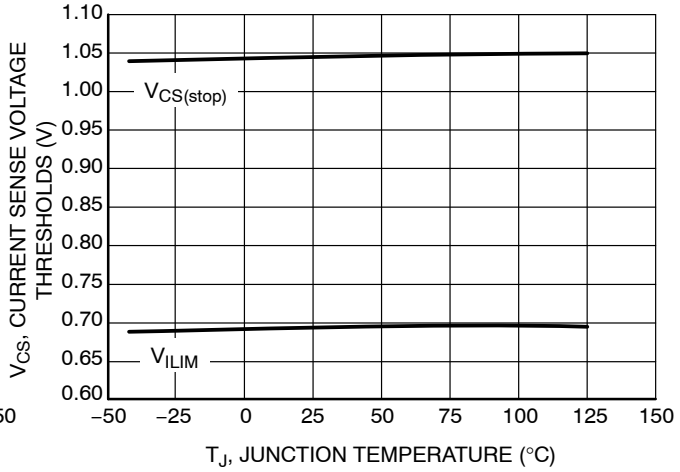


Figure 17. Current Sense Voltage Thresholds vs. Junction Temperature

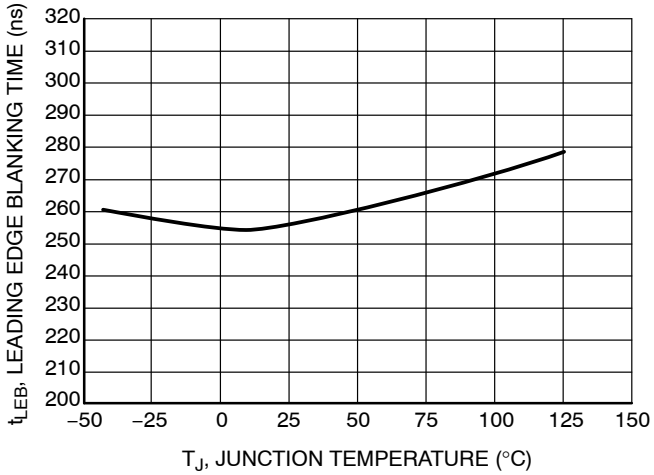


Figure 18. Leading Edge Blanking Time vs. Junction Temperature

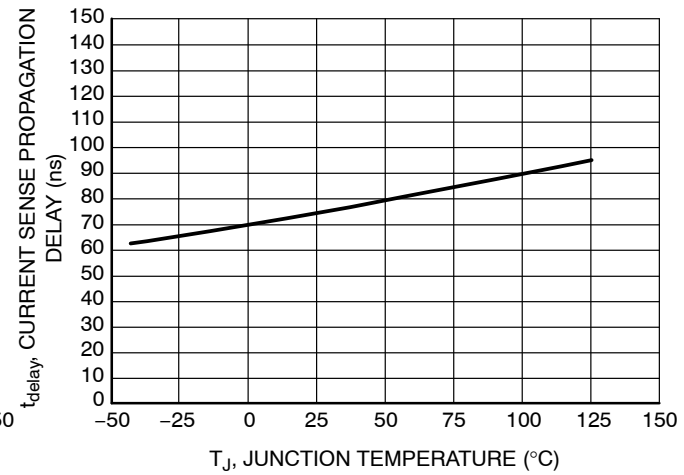


Figure 19. Current Sense Propagation Delay vs. Junction Temperature

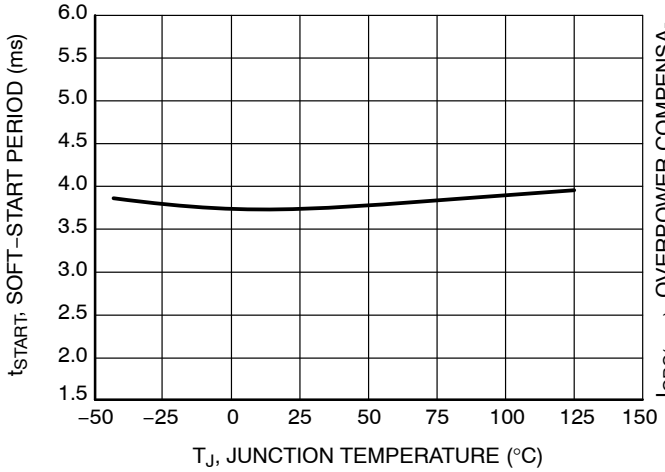


Figure 20. Soft−Start Period vs. Junction Temperature

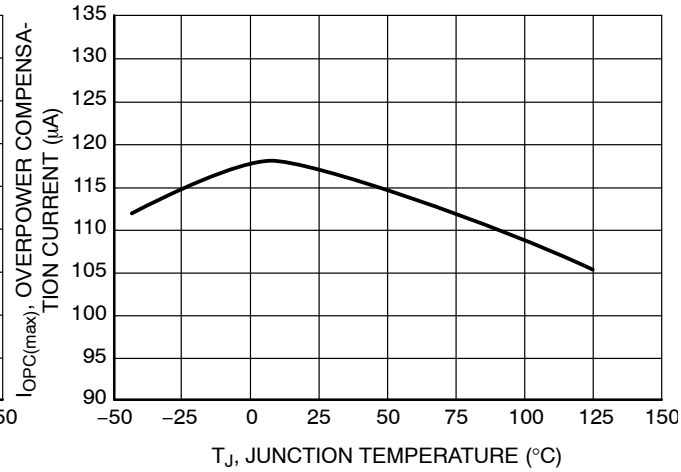


Figure 21. Overpower Compensation Current vs. Junction Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

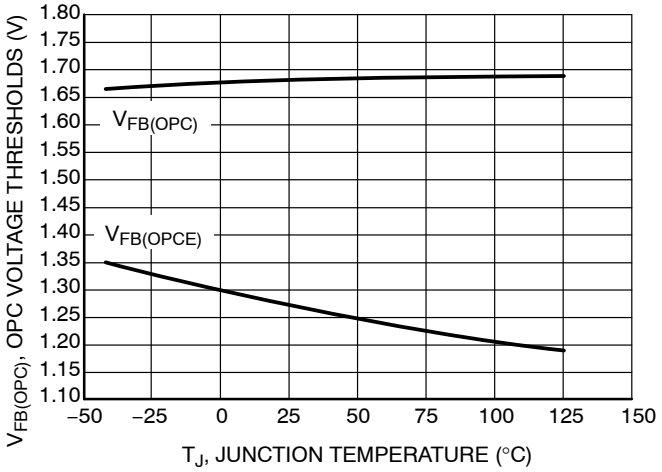


Figure 22. OPC FB Thresholds vs. Junction Temperature

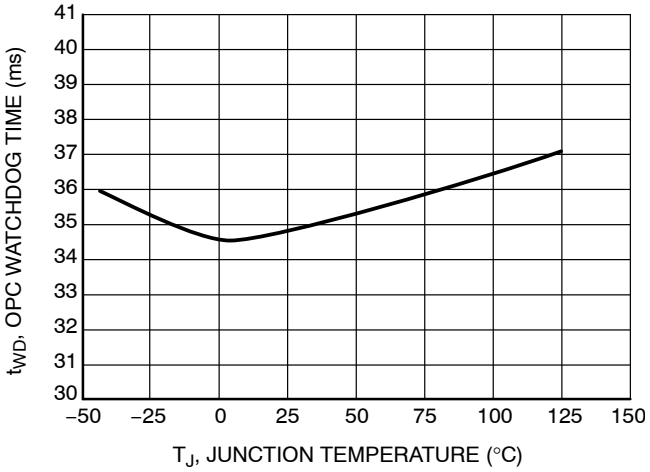


Figure 23. OPC Watchdog Time Thresholds vs. Junction Temperature

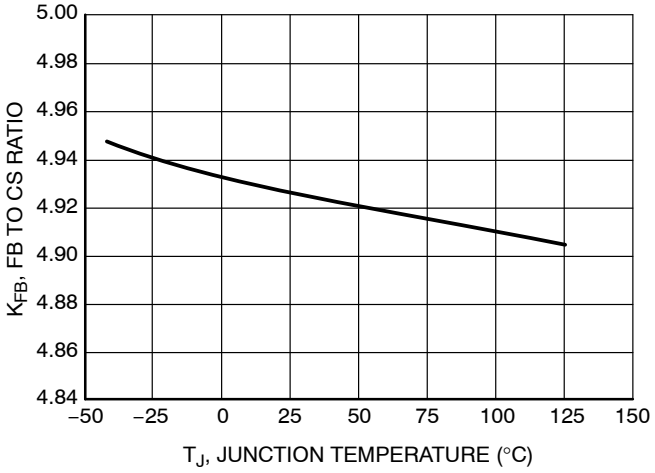


Figure 24. FB to CS Ratio vs. Junction Temperature

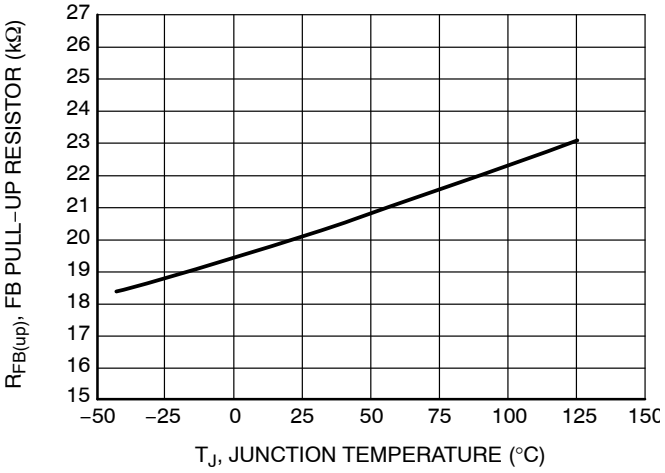


Figure 25. FB Pull−up Resistor vs. Junction Temperature

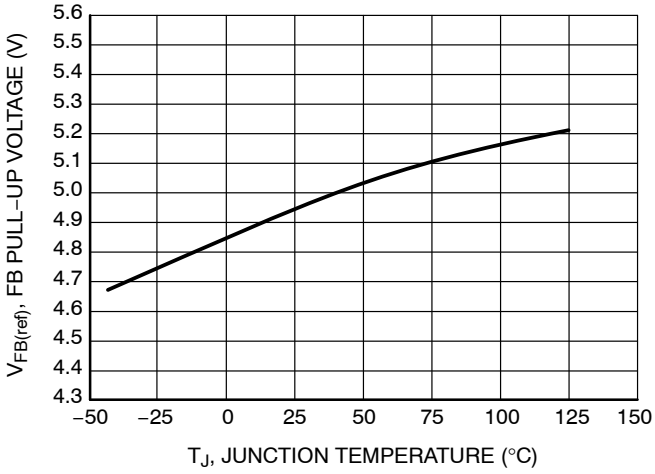


Figure 26. FB Pull−up Voltage vs. Junction Temperature

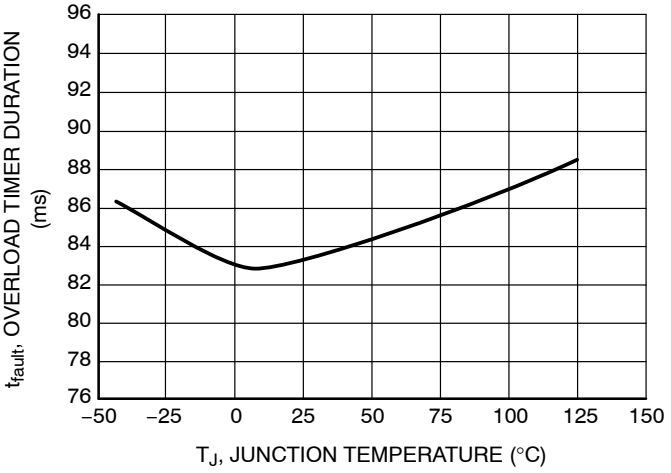


Figure 27. Overload Timer Duration vs. Junction Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

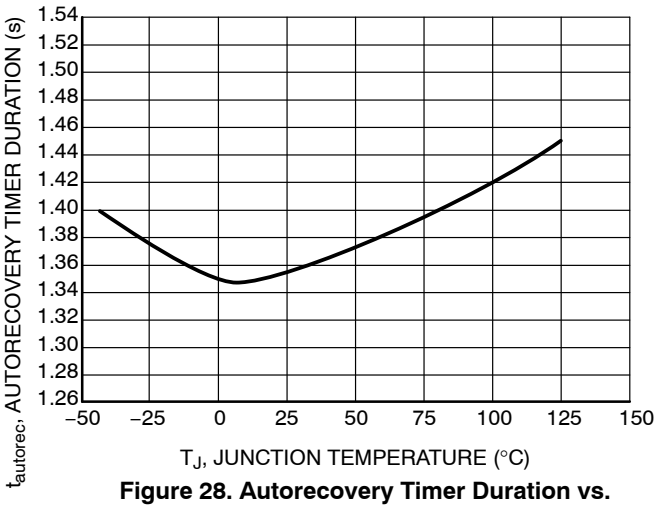


Figure 28. Autorecovery Timer Duration vs. Junction Temperature

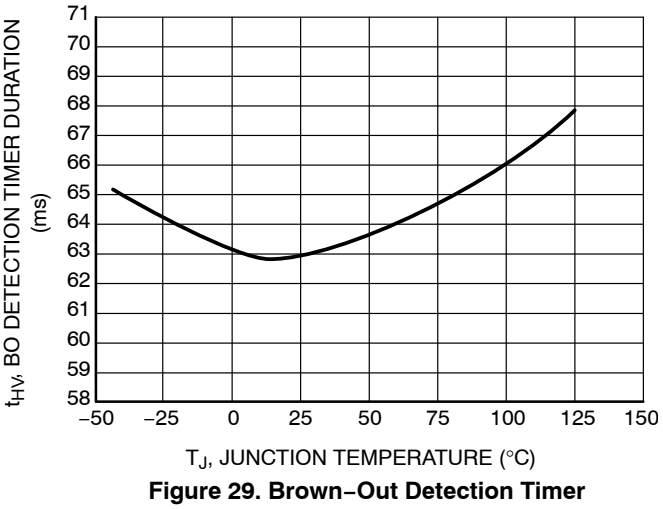


Figure 29. Brown−Out Detection Timer Duration vs. Junction Temperature

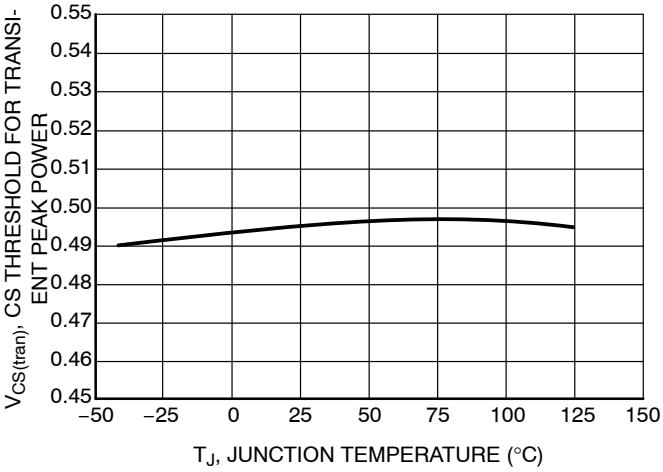


Figure 30. CS Threshold for Transient Peak Power vs. Junction Temperature

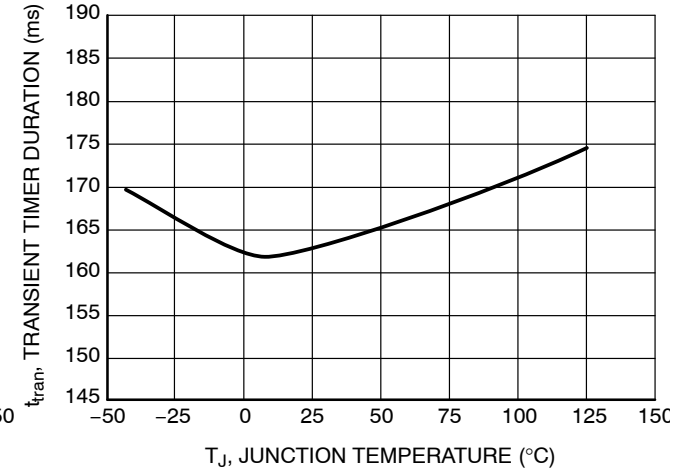


Figure 31. Transient Timer Duration vs. Junction Temperature

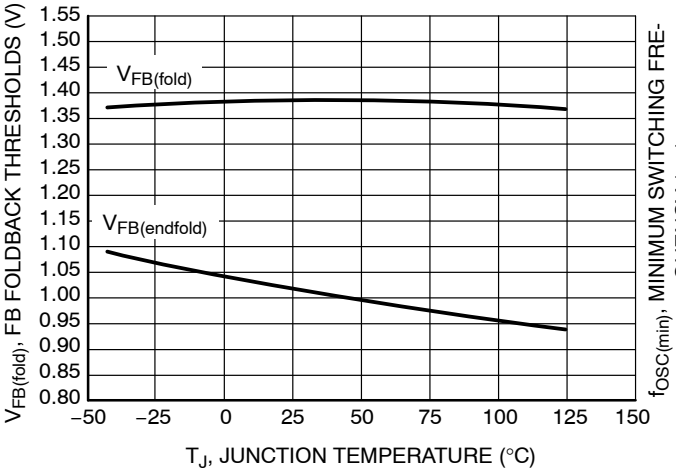


Figure 32. FB Thresholds for Frequency Foldback vs. Junction Temperature

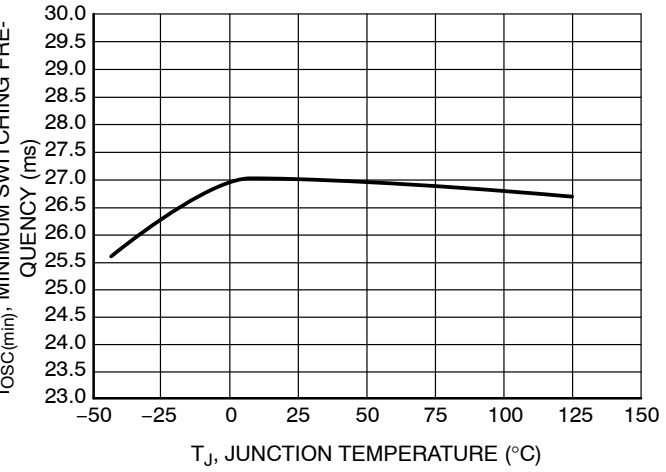


Figure 33. Minimum Switching Frequency vs. Junction Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

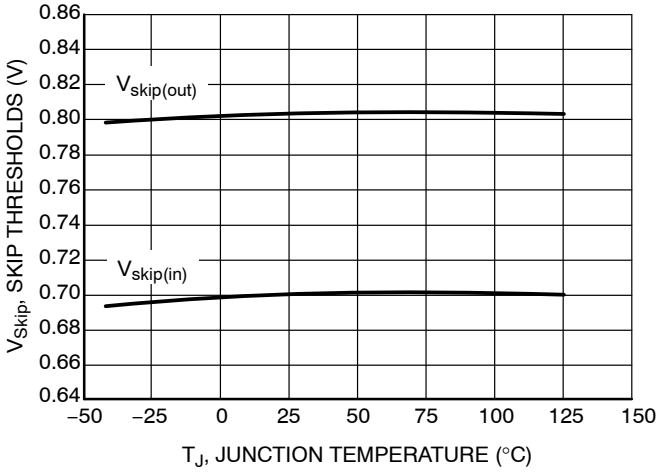


Figure 34. Skip Thresholds vs. Junction Temperature

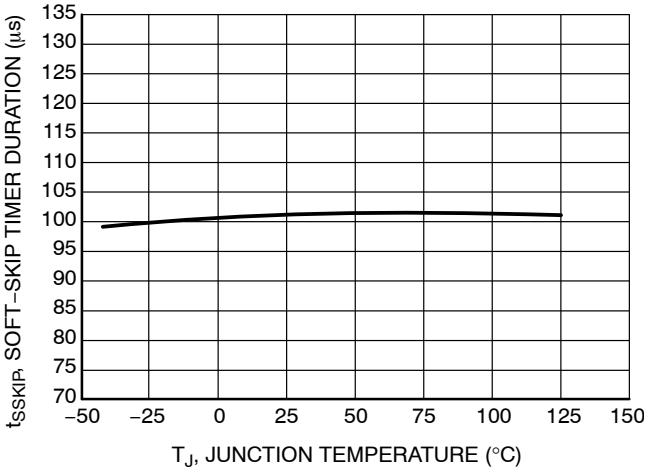


Figure 35. Soft−Skip Timer Duration vs. Junction Temperature

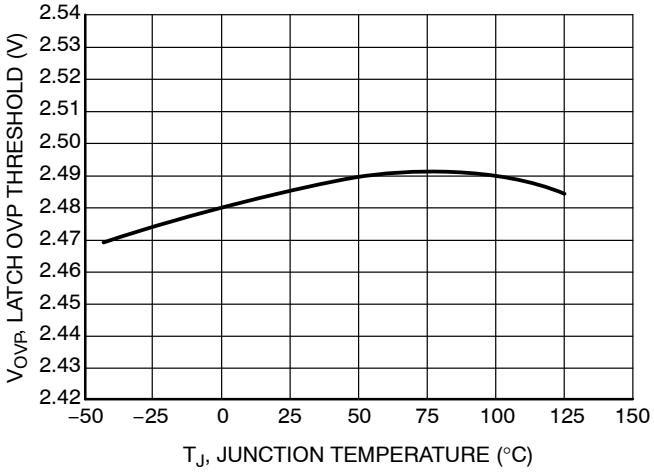


Figure 36. Latch OVP Threshold vs. Junction Temperature

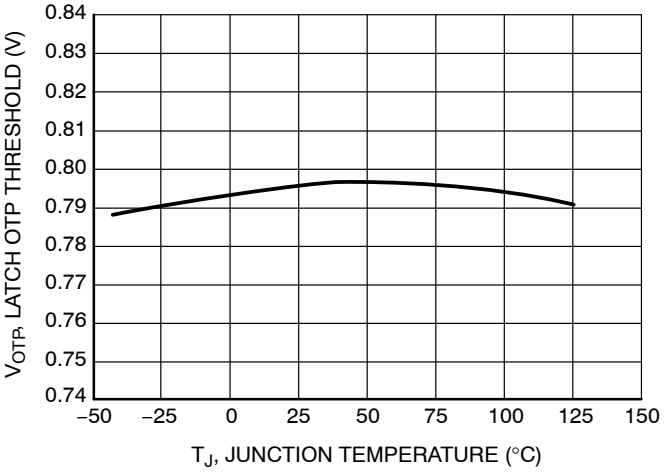


Figure 37. Latch OTP Threshold vs. Junction Temperature

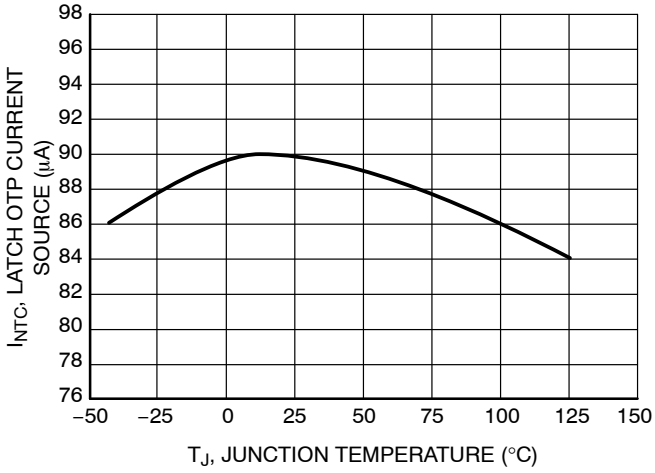


Figure 38. Latch OTP Current Source vs. Junction Temperature

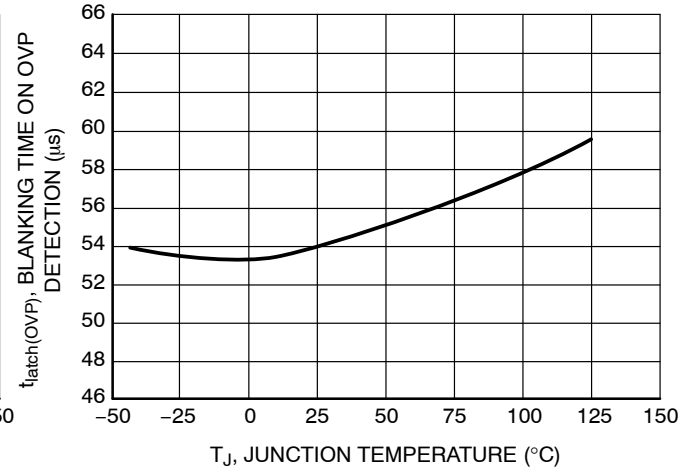


Figure 39. Blanking Time on OVP Detection vs. Junction Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

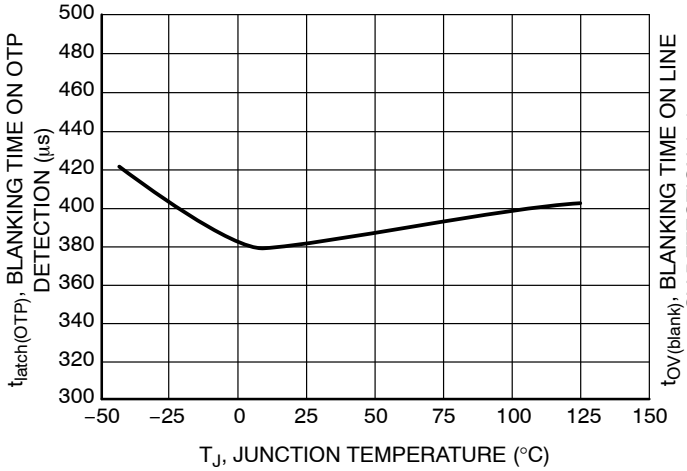


Figure 40. Blanking Time on OTP Detection vs. Junction Temperature

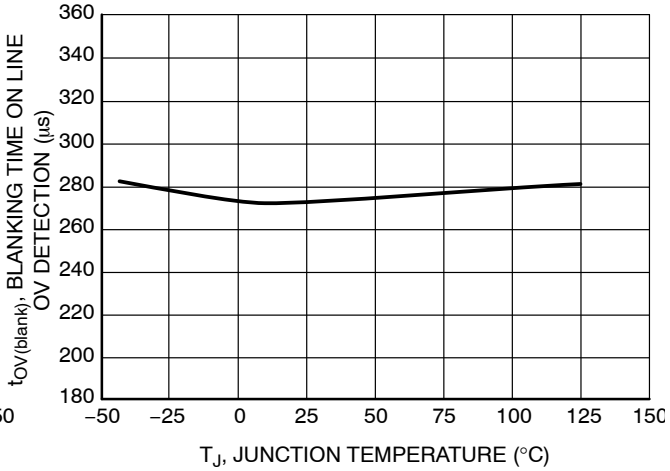


Figure 41. Blanking Time on Line OV Detection vs. Junction Temperature

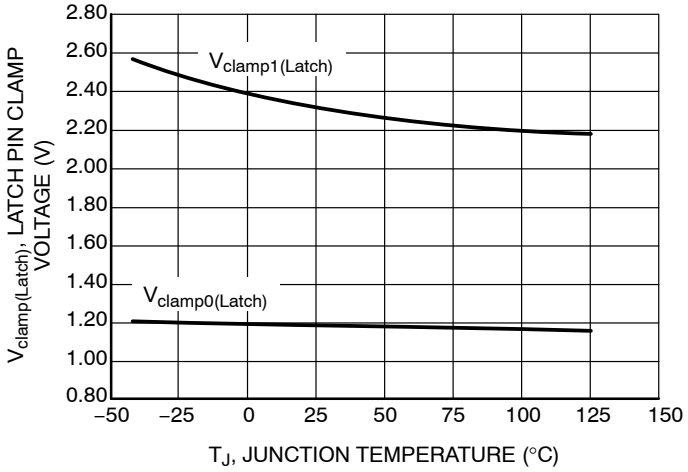


Figure 42. Latch Pin Clamp Voltage vs. Junction Temperature

APPLICATION INFORMATION

Introduction

The NCP1237 includes all of the necessary features to build a safe and efficient power supply based on a fixed−frequency flyback converter. It is particularly well suited for applications where low part count is a key parameter, without sacrificing safety.

- **Current−Mode Operation with slope compensation**: The primary peak current is permanently controlled by the FB voltage, ensuring maximum safety: the DRV turn−off event is dictated by the peak current setpoint. It also ensures that the frequency response of the system remains a first order if in DCM, which eases the design of the feedback loop. The controller can also be used in CCM with a wide input voltage range due to its fixed ramp compensation that prevents the appearance of sub−harmonic oscillations in most of the applications.
- **Fixed−Frequency Oscillator with Jittering**: The NCP1237 is available in various frequency options to fit any application. The internal oscillator features a low−frequency jittering that helps to pass the EMI requirements by spreading out the energy content of frequency peaks in quasi−peak and average mode.
- **Latched / Autorecovery Timer−Based dual−level Overcurrent Protection**: The overcurrent protection has 2 different levels. At the low level the controller can still regulate but starts a long timer. The high level corresponds to the loss of regulation and starts the usual overload timer. This allows a power supply to transiently deliver a higher power for a limited time. The overcurrent protection depends only on the FB signal, enabling it to work with any transformer, even with very poor coupling or high leakage inductance. Both protections are fully latched on the A version (the power supply has to be unplugged then restarted in order to resume operation, even if the overload condition disappears), and autorecovery on the B version. The timers' durations are fixed. The controller also enters the same protection mode if the voltage on the CS pin reaches 1.5 times the maximum internal setpoint, which enables to detect winding short circuits.
- **High Voltage Startup Current Source with Brown−Out and Line Overvoltage Detections**: Due to On Semiconductor's Very High Voltage technology, the NCP1237 can directly be connected to the high input voltage. The startup current source ensures a clean startup while ensuring low losses when it is off, and the Dynamic Self−Supply (DSS) restarts the startup current source to supply the controller if the V_{CC} supply transiently drops. The high voltage pin also features a high−voltage sensing circuitry, which is able to turn the controller off if the input voltage is too low (brown−out condition) or too high (line overvoltage). This protection works either with a DC input voltage or a rectified AC input voltage, and is independent of the high voltage ripple. It uses a peak detector synchronized with line frequency, or with the internal watchdog timer if the HV pin is tied to a dc voltage.
- **Adjustable Overpower Compensation**: The high voltage sensed on the HV pin is converted into a current to add to the current sense voltage an offset proportional to the input voltage. By choosing the value of the resistor in series with the CS pin, the amount of compensation can be adjusted to the application.
- **Frequency foldback then Soft−Skip mode for light load operation**: In order to ensure a high efficiency in all load conditions, the NCP1237 implements a frequency foldback (the switching frequency is lowered to reduce switching losses) for light load condition; and a Soft−Skip (disabled in case of fast load transients) for extremely low load condition.
- **Extended V_{CC} range**: The NCP1237 accepts a supply voltage as high as 28 V, making the design of the power supply easier.
- **Clamped Driver Stage**: Despite the high supply voltage, the voltage on DRV pin is safely clamped below 16 V; allowing the use of any standard MOSFET, and reducing the current consumption of the controller.
- **Dual Latch−off Input**: The NCP1237 can be latched off by an increasing voltage applied to its Latch pin (typically an overvoltage) or by a decreasing one, and an NTC can be directly connected to the latch pin thanks to the precise internal current source.
- **Soft−Start**: At every startup the peak current is gradually increased during 4 ms to minimize the stress on power components.
- **Temperature Shutdown**: The NCP1237 is internally protected against self−heating: if the die temperature is too high, the controller shuts all circuitries down (including the HV startup current source), allowing the silicon to cool down before attempting to restart. This ensures a safe behavior in case of failure.

Typical Operation

- **Startup**: The HV startup current source ensures the charging of the V_{CC} capacitor up to the startup threshold $V_{CC(on)}$, until the input voltage is high enough (above $V_{HV(start)}$) to enable the switching. The controller then delivers pulses, starting with a soft−start period t_{SSTART} during which the peak current linearly increases before the current−mode control takes over. During the soft−start period, the low level latch is ignored, and the latch current is double, to ensure a fast pre−charge of the decoupling capacitor on the Latch pin.

- **Normal operation**: As long as the feedback voltage is within the regulation range, the NCP1237 runs at a fixed frequency (with jittering) in current−mode control, where the peak current (sensed on the CS pin) is set by the voltage on the FB pin. A fixed ramp compensation is applied internally to prevent sub−harmonic oscillations from occurring. The V_{CC} must be supplied by an external source (such as an auxiliary winding), as the startup current source cannot permanently supply the controller without overheating.
- **Light load operation**: When the FB voltage decreases below $V_{FB(fold)}$, typically corresponding to a load of 20% (DCM design only) to 30% (CCM / DCM design) of the maximum load, the switching frequency starts to decrease down to $f_{OSC(min)}$. By lowering the switching losses, this feature helps to improve the efficiency in light load conditions. The frequency jittering is disabled in light load operation.
- **No load operation**: When the FB voltage decreases below $V_{skip(in)}$, typically corresponding to a load of 1% of the maximum load, the controller enters Skip mode. By completely stopping the switching while the feedback voltage is below $V_{skip(out)}$, the losses are further reduced, allowing to minimize the power dissipation under extremely low load conditions. In order to avoid audible noise, the peak current is gradually increased during the t_{SSKIP} duration while exiting the skip mode (Soft−Skip function). In case of abrupt load increase during Soft−Skip mode, the soft−skip portion is bypassed and the peak current needed for regulation is directly applied. V_{CC} can be maintained between $V_{CC(on)}$ and $V_{CC(min)}$ by the DSS.
- **Overload**: The NCP1237 features a timer−based dual−level overload detection, solely dependent on the feedback information: as soon as the internal peak current setpoint goes above the $V_{CS(tran)}$ threshold, a first internal timer starts to count, but the controller is still able to regulate up to V_{ILIM}. Once it reaches the V_{ILIM} clamp, the internal overload timer starts to count. When either timer times out, the controller stops and enters the protection mode, autorecovery for the B version (the controller initiates a new start−up after $t_{autorec}$ elapses), or latched for the A version (the latch is released if a brown−out event occurs or V_{CC} is reset).
- **Brown−out**: The NCP1237 features on its HV pin a true AC line monitoring circuitry which includes a minimum startup threshold, brown−out protection, and overvoltage protection. All of these circuits are autorecovery and operate independently of any ripple on the input voltage. They can even work with an unfiltered, rectified AC input. All thresholds are fixed, but they are designed to fit most of the standard ac−dc conversion applications.
- **Latch−off**: When the Latch input is pulled up (typically by an overvoltage condition), or pulled low (typically by an overtemperature condition, using the provided current source with an NTC), the controller latches off. The latch is released when a brown−out condition occurs, or when V_{CC} decreases below $V_{CC(reset)}$.

DETAILED DESCRIPTION

High−Voltage Current Source (Dynamic Self−Supply) with Built−in Brown−out Detection

The NCP1237 HV pin can be connected either to the rectified bulk voltage, or to the ac line through a rectifier.

Startup

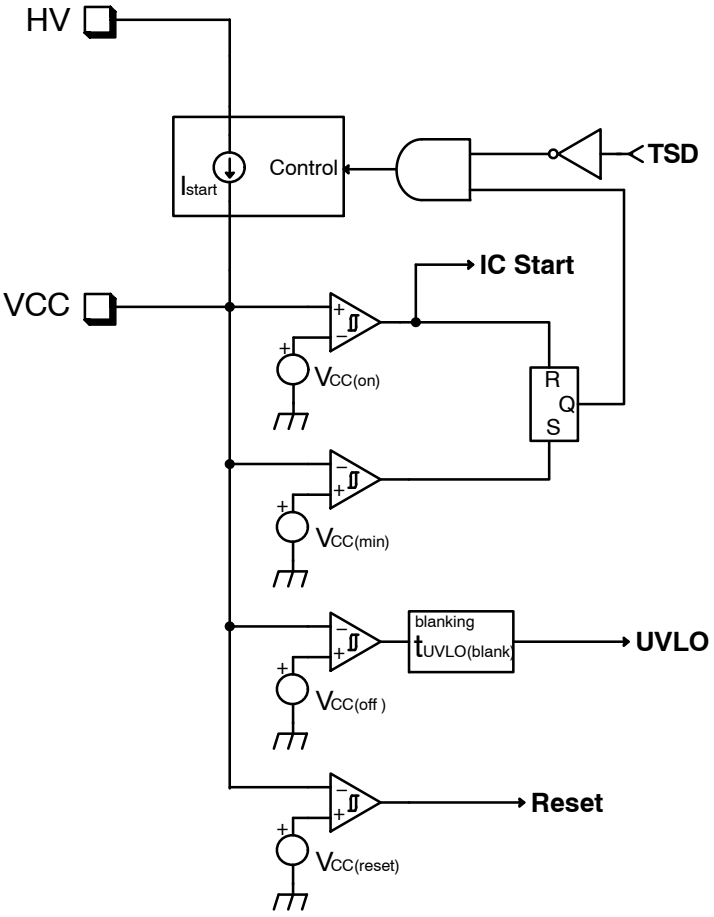


Figure 43. HV Startup Current Source Functional Schematic

At startup, the current source turns on when the voltage on the HV pin is higher than $V_{HV(min)}$, and turns off when V_{CC} reaches $V_{CC(on)}$. It turns on again when V_{CC} reaches $V_{CC(min)}$. This sequence repeats until the input voltage is high enough to ensure a proper startup, i.e. when V_{HV} reaches $V_{HV(start)}$. The switching actually starts the next time V_{CC} reaches $V_{CC(on)}$, as shown in Figure 5.

Even though the DSS is able to maintain the V_{CC} voltage between $V_{CC(on)}$ and $V_{CC(min)}$ by turning the HV startup current source on and off, it can only be used in light load conditions, otherwise the power dissipation on the die would be too high. As a result, an auxiliary voltage source is needed to supply V_{CC} during normal operation.

The DSS is useful to keep the controller alive when no switching pulses are delivered, e.g. in a brown−out condition, or to prevent the controller from stopping during load transients when the V_{CC} might drop below $V_{CC(off)}$.

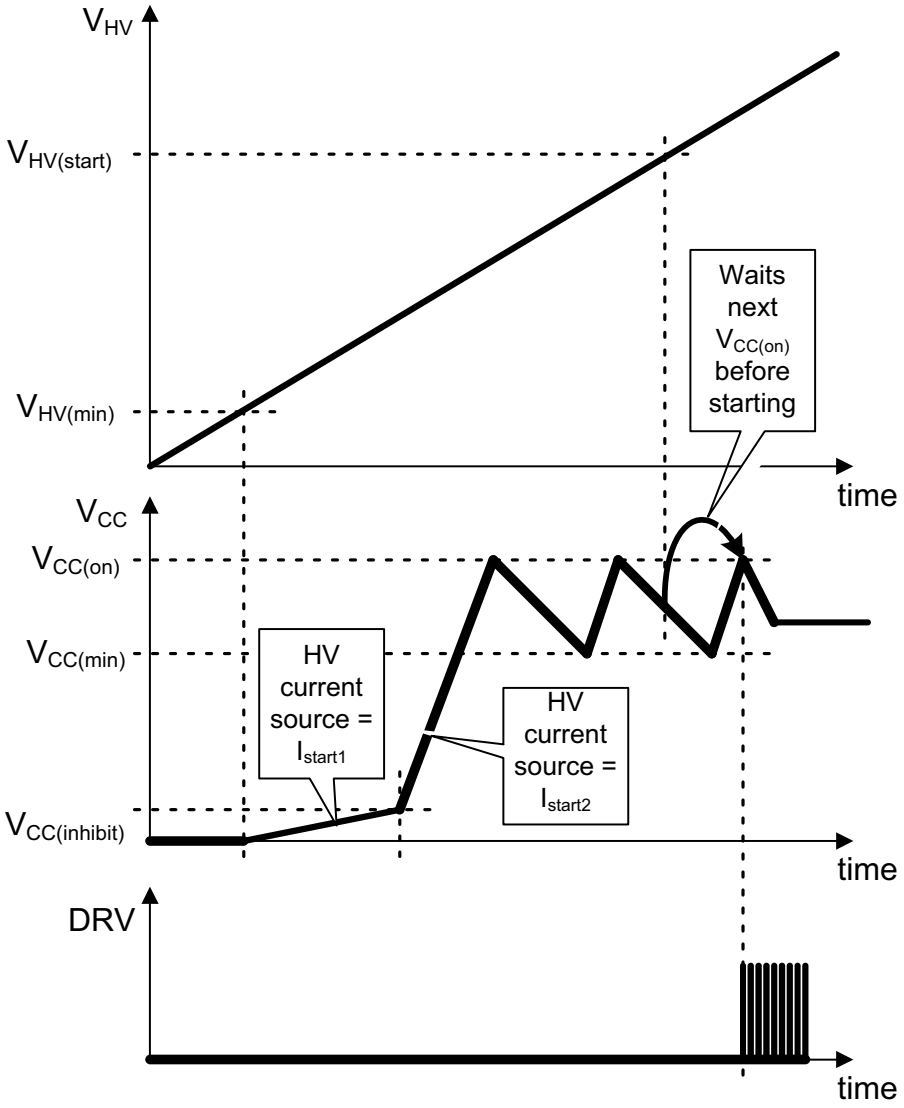


Figure 44. Startup Timing Diagram

To reduce the power dissipation in case the V_{CC} pin is shorted to GND (in case of V_{CC} capacitor failure, or external pulldown on V_{CC} to disable the controller), the startup current is lowered when V_{CC} is below $V_{CC(inhibit)}$.

There are only two conditions for which the current source doesn't turn on when V_{CC} reaches $V_{CC(min)}$: the voltage on HV pin is too low (below $V_{HV(min)}$), or a thermal shutdown condition (TSD) has been detected. In all other conditions, the HV current source always turns on and off to maintain V_{CC} between $V_{CC(min)}$ and $V_{CC(on)}$.

Brown−out and Line Overvoltage

When the input voltage goes below $V_{HV(stop)}$, a brown−out condition is detected, and the controller stops. The HV current source alternatively turns on and off to maintain V_{CC} between $V_{CC(on)}$ and $V_{CC(min)}$ until the input voltage is back above $V_{HV(start)}$.

The same situation occurs when an overvoltage is detected on the ac line, i.e. when the input voltage goes above $V_{HV(OV)}$: the controller stops, and resumes normal operation when the overvoltage condition has gone.

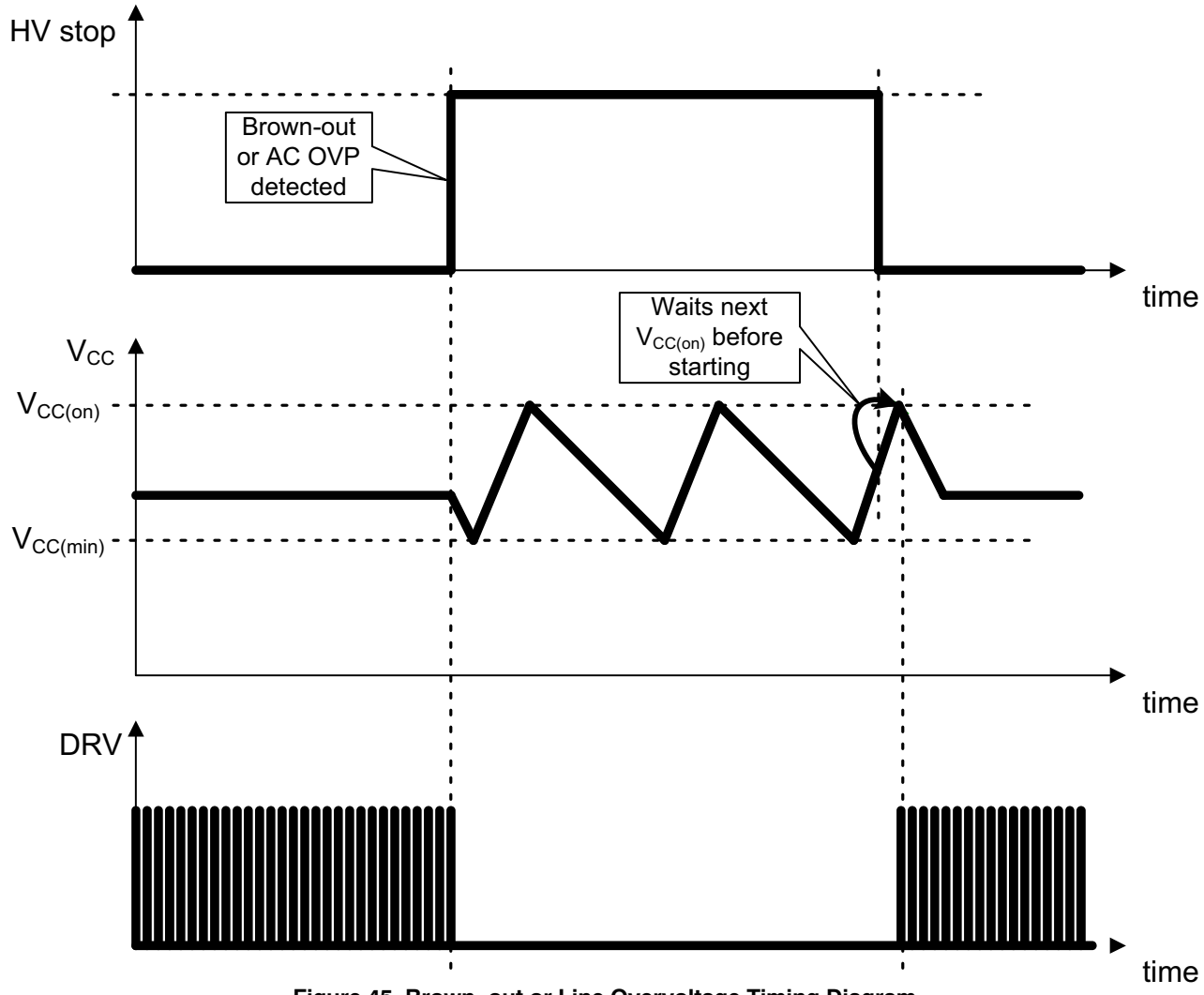


Figure 45. Brown−out or Line Overvoltage Timing Diagram

When V_{HV} crosses the $V_{HV(start)}$ threshold, the controller can start immediately. When it crosses $V_{HV(stop)}$, it triggers a timer of duration t_{HV}: this ensures that the controller doesn't stop in case of line cycle drop−out.

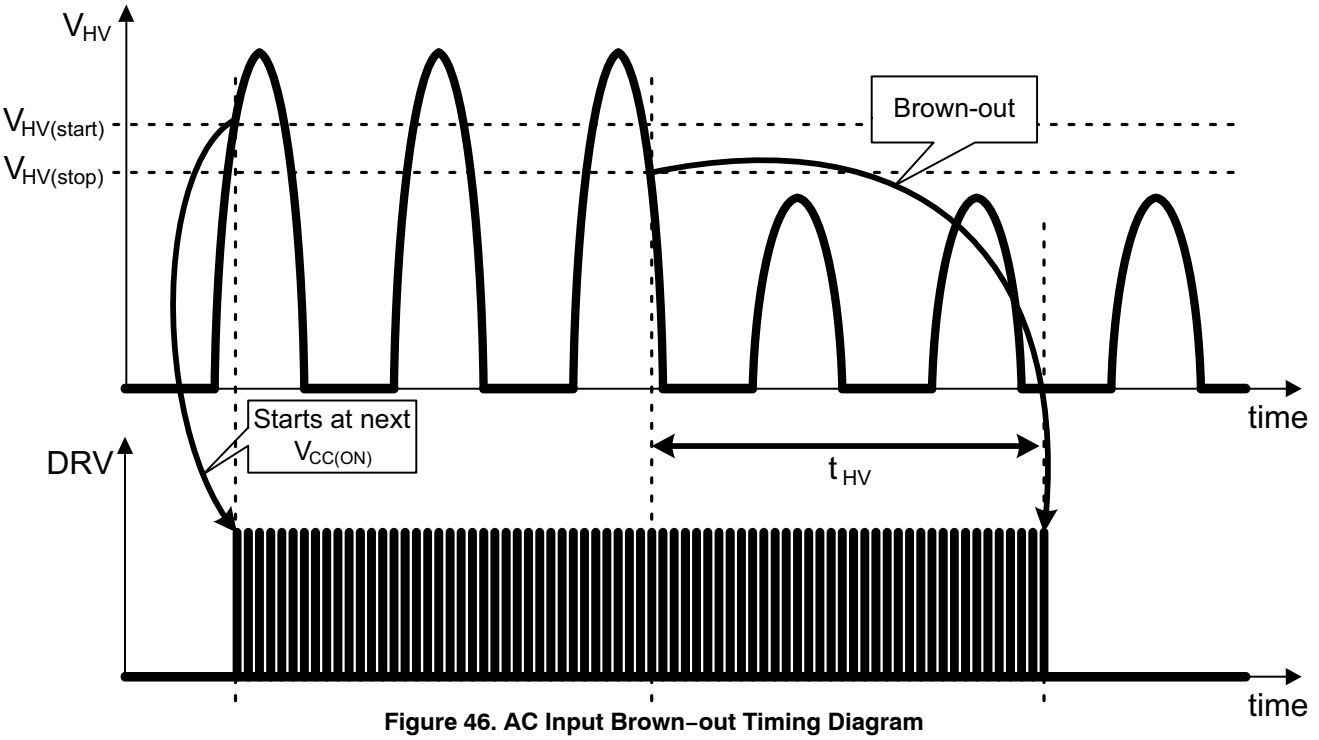


Figure 46. AC Input Brown−out Timing Diagram

The same scheme is used for the Line OVP, except that this time the controller must not stop instantaneously when the input voltage goes above $V_{HV(OV1)}$. In order to be insensitive to spikes and voltage surges a blanking circuit is inserted after the output of the comparator, with a duration of $t_{OV(blank)}$.

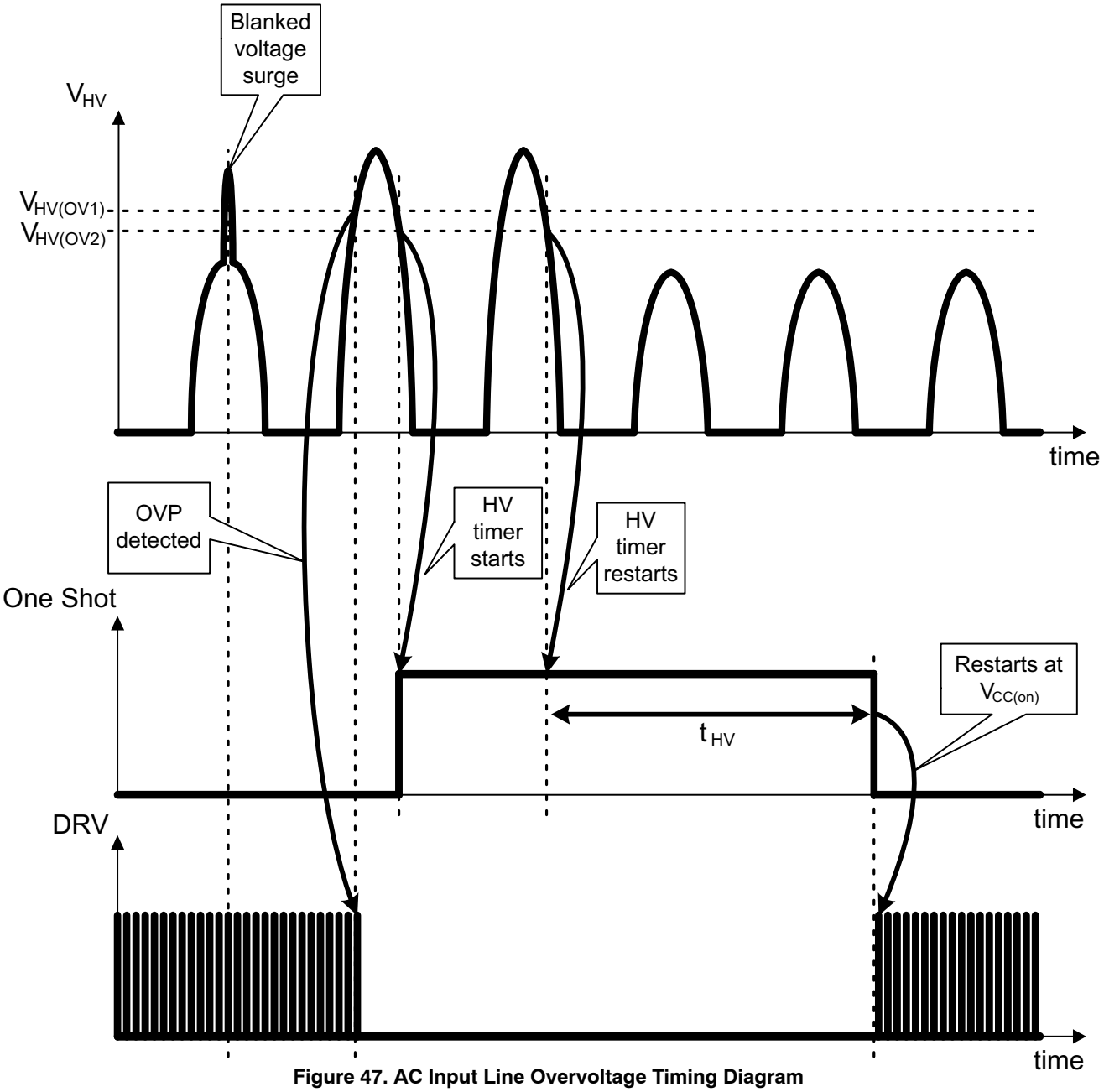


Figure 47. AC Input Line Overvoltage Timing Diagram

Oscillator with Maximum Duty Ratio and Frequency Jittering

The NCP1237 includes an oscillator that sets the switching frequency with an accuracy of ±7%. The maximum duty ratio of the DRV pin is 80% (typical), with an accuracy of ±7%.

In order to improve the EMI signature, the switching frequency jitters around its nominal value, with a triangle−wave shape.

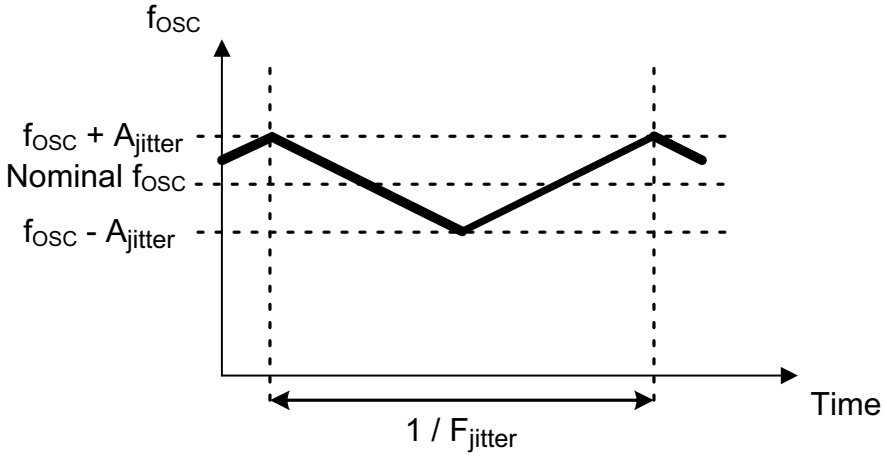


Figure 48. Frequency Jittering

Clamped Driver

The supply voltage for the NCP1237 can be as high as 28 V, but most of the MOSFETs that will be connected to the DRV pin cannot tolerate a gate−to−source voltage greater than 20 V on their gate. The driver pin is therefore clamped safely below 16 V.

This driver has a typical current capability of ±1.0 A.

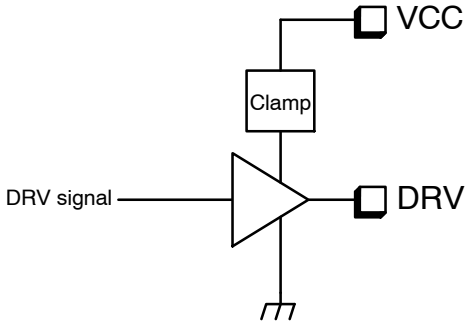


Figure 49. Clamped Driver

CURRENT−MODE CONTROL WITH OVERPOWER COMPENSATION AND SOFT−START

Current Sensing

NCP1237 is a current−mode controller, which means that the FB voltage sets the peak current flowing in the inductance and the MOSFET. This is done through a PWM comparator: the current is sensed across a resistor and the resulting voltage is applied to the CS pin. V_{CS} is applied to one input of the PWM comparator through the LEB block. On the other input the FB voltage divided by K_{FB} sets the threshold: when V_{CS} reaches this threshold, the output driver is turned off.

The maximum value for the peak current, V_{ILIM}, is set by a dedicated comparator.

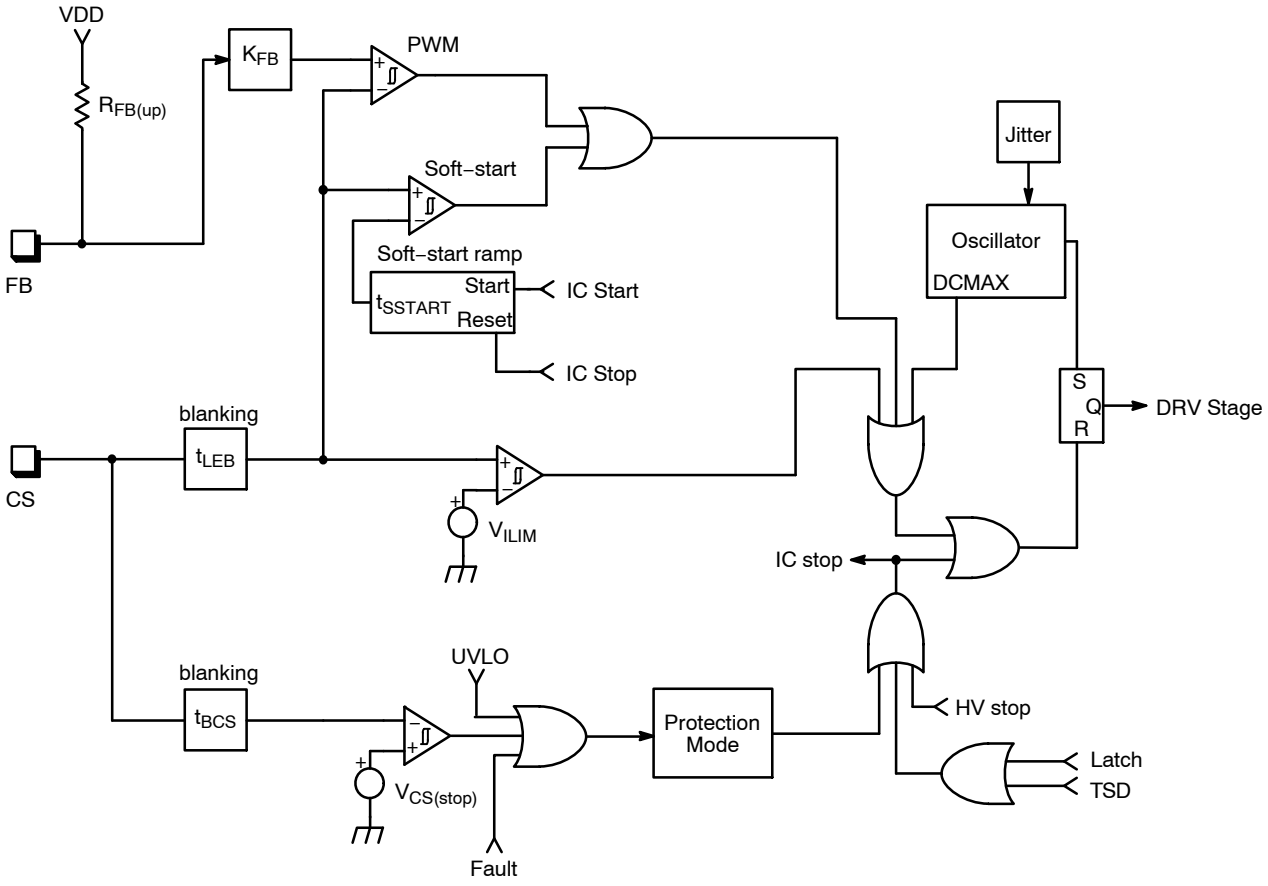


Figure 50. Current Sense Block Schematic

Each time the controller is starting (i.e. the controller was off and starts, or restarts, when V_{CC} reaches $V_{CC(on)}$), a soft−start is applied: the current sense setpoint is linearly increased from 0 (the minimum level can be higher than 0 because of the LEB and propagation delay) until it reaches V_{ILIM} (after a duration of t_{SSTART}), or until the FB loop imposes a setpoint lower than the one imposed by the soft−start (the 2 comparators outputs are OR'ed).

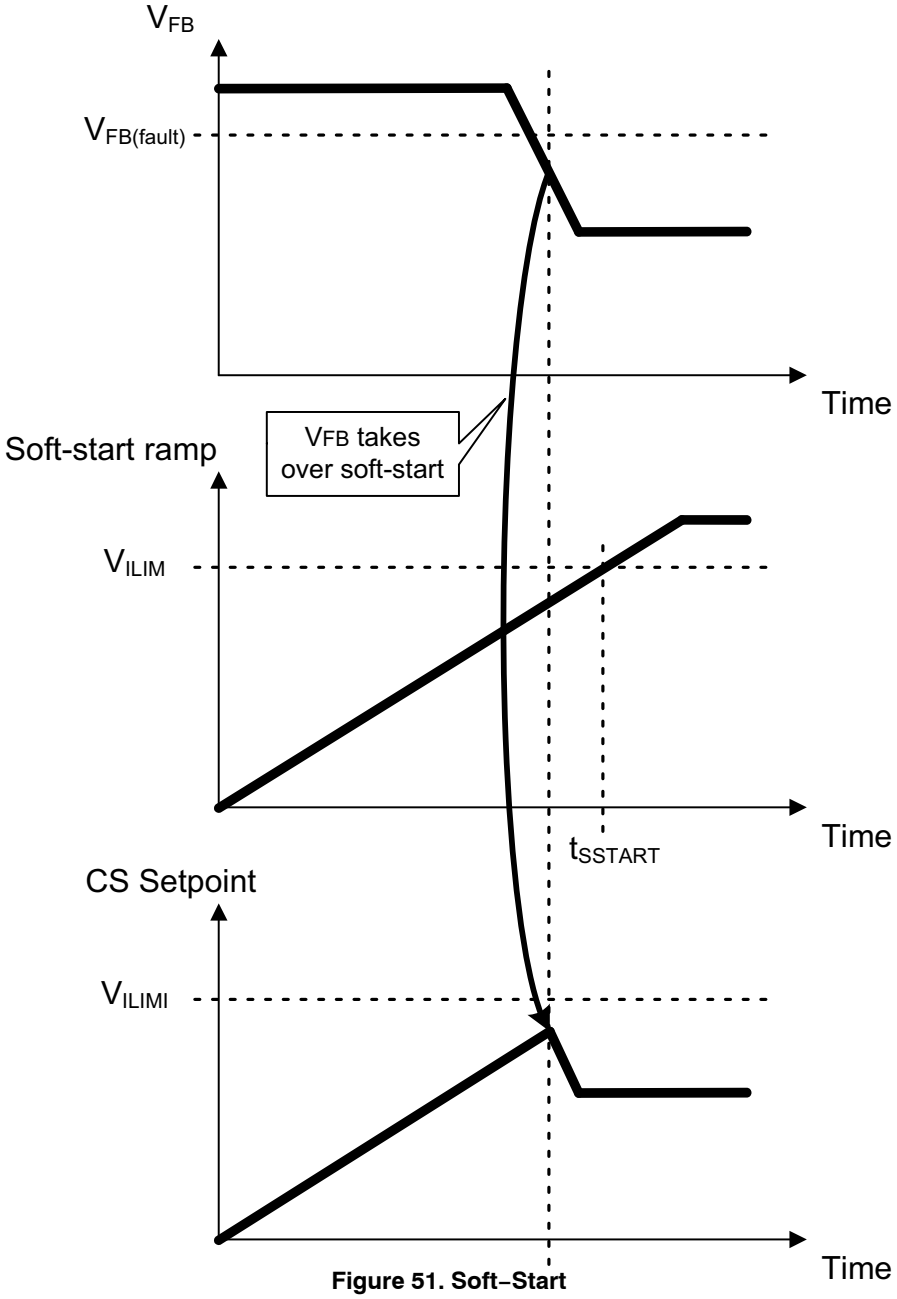


Figure 51. Soft−Start

Under some conditions, like a winding short−circuit for instance, not all the energy stored during the *on* time is transferred to the output during the *off* time, even if the on time duration is at its minimum (imposed by the propagation delay of the detector added to the LEB duration). As a result, the current sense voltage keeps on increasing above V_{ILIM}, because the controller is blind during the LEB blanking time. Dangerously high current can grow in the system if nothing is done to stop the controller. In order to protect against this, an additional comparator is included, that senses when V_{CS} reaches $V_{CS(stop)}$ (= 1.5 x V_{ILIM}). As soon as this comparator toggles, the controller immediately enters the protection mode (latched or autorecovery according to the chosen option).

Compensation for Overpower Detection

The power delivered by a flyback power supply is proportional to the square of the peak current:

$$P_{OUT} = \frac{1}{2} \cdot \eta \cdot L_P \cdot F_{SW} \cdot I_P{}^2 \qquad \text{(eq. 1)}$$

(in discontinuous conduction mode).

Unfortunately, due to the inherent propagation delay of the logic, the actual peak current is higher at high input voltage than at low input voltage, as shown in Figure 52. This leads to a significant difference in the maximum output power delivered by the power supply.

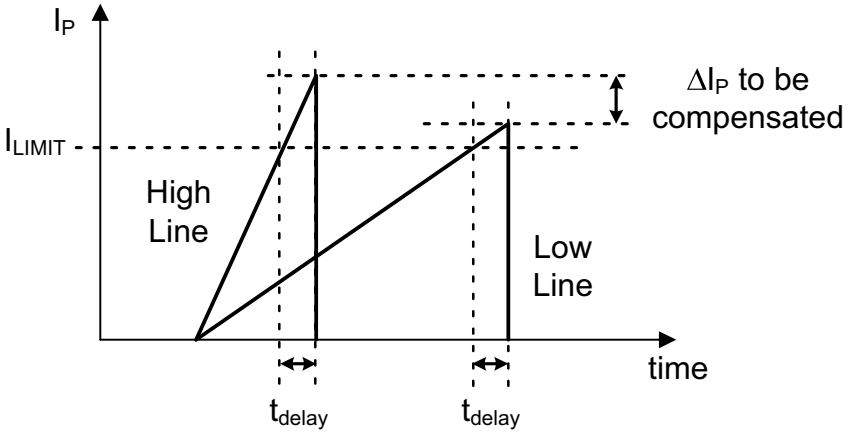


Figure 52. Line Compensation for True Overpower Protection

To compensate this and have an accurate overpower protection, an offset proportional to the input voltage is added to the CS signal by turning on an internal current source (I_{OPC}): by adding an external resistor (R_{OPC}) in series between the sense resistor and the CS pin, a voltage offset is created across it by the current. The compensation can be adjusted by changing the value of the R_{OPC} resistor.

Since in light load conditions this offset is in the same order of magnitude as the current sense signal, it must be removed. Therefore the compensation current is only added when the FB voltage is higher than $V_{FB(OPC)}$, as shown in Figure 54.

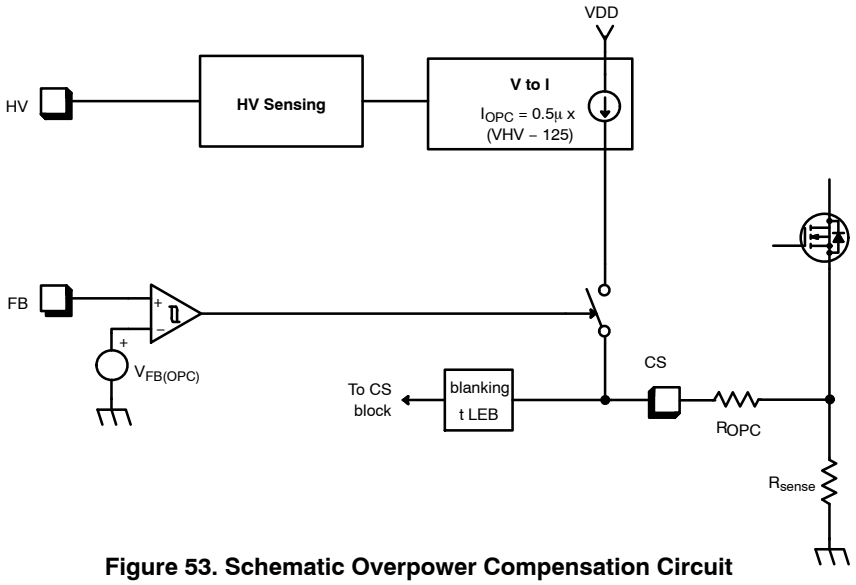


Figure 53. Schematic Overpower Compensation Circuit

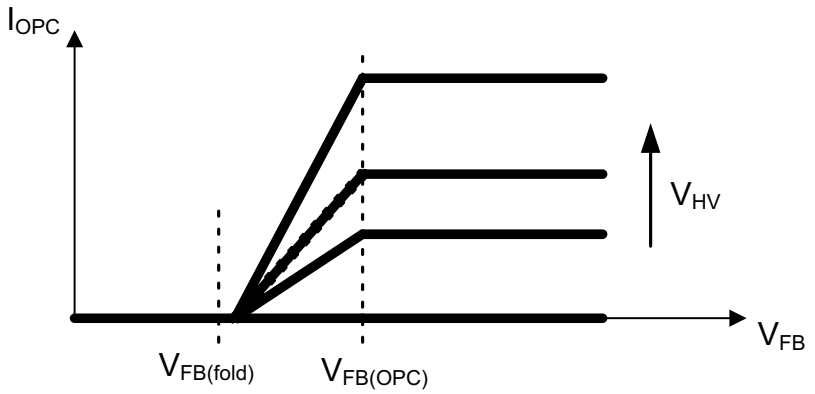


Figure 54. Overpower Compensation Current Relation to Feedback Voltage and Input Voltage

A peak detector continuously senses the ac input, and its output is periodically sampled and reset, in order to follow closely the input voltage variations. The sample and reset events are controlled by the brown-out comparator when the HV pin is connected to the AC line input (as shown in Figure 55). In the case the HV pin is connected to the DC-link capacitor, its voltage never crosses the brown-out threshold, and the watchdog timer t_{WD} is used to generate the sampling and reset events (Figure 56). Note that depending on the relative speeds at which the HV and VCC voltages appear at start-up, the correct overpower compensation current may be delayed by one cycle.

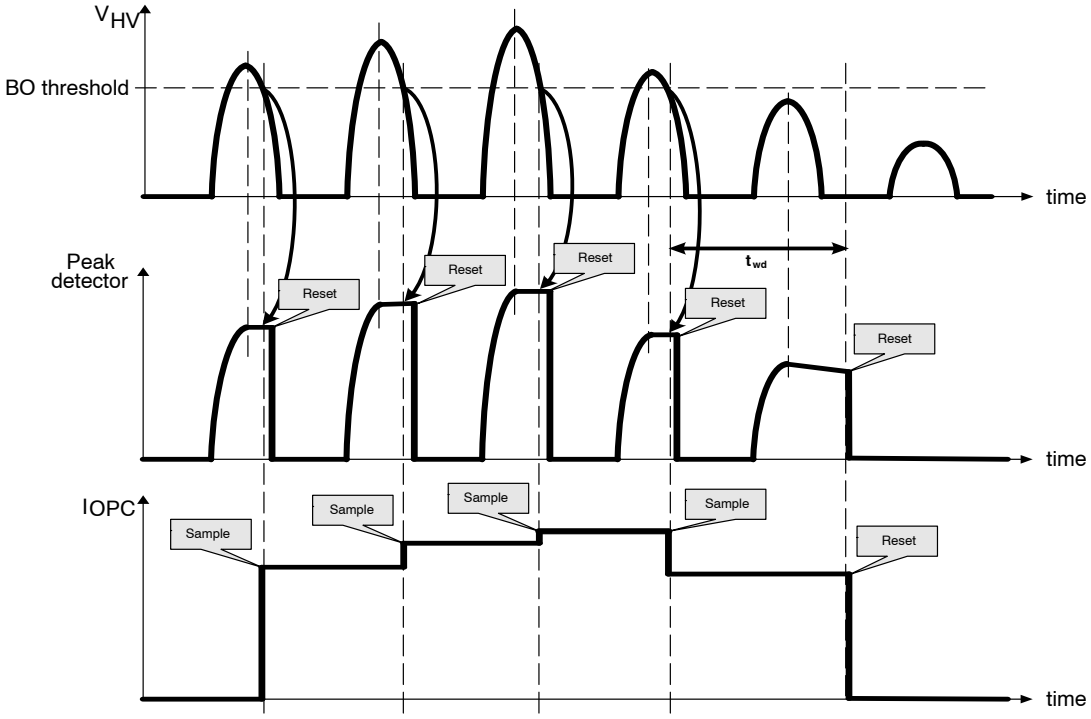


Figure 55. Overpower Compensation Current with the HV pin connected to an ac voltage

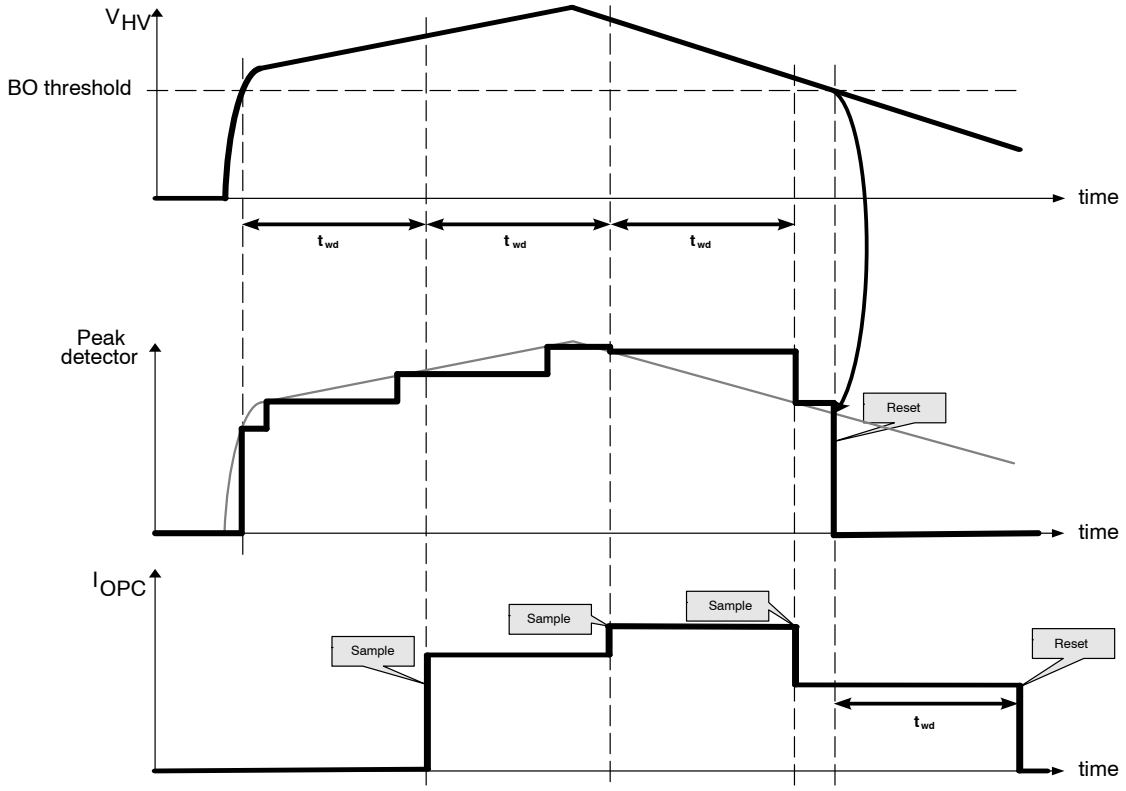


Figure 56. Overpower Compensation Current with the HV pin connected to a dc voltage

Feedback with Slope Compensation

The ratio from the FB voltage to the current sense setpoint is typically 5. This means that the FB voltage corresponding to V_{ILIM} is 3.5 V. There is a pullup resistor of 20 kΩ (typical) from FB pin to the internal reference $V_{FB(ref)}$.

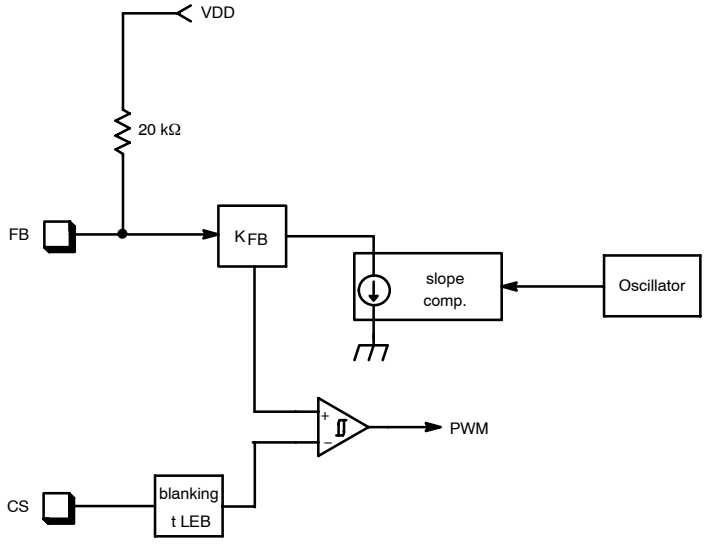


Figure 57. FB Circuitry

In order to allow the NCP1237 to operate in CCM with a duty cycle above 50%, a fixed slope compensation is internally applied to the current−mode control. The slope appearing on the internal voltage setpoint for the PWM comparator is −32.5 mV/μs typical for the 65 kHz version (and respectively −50 mV/μs and −67 mV/μs for the 100 kHz and 133 kHz versions).

OVERCURRENT PROTECTION WITH FAULT TIMER

Classical Overcurrent Protection

When an overcurrent occurs on the output of the power supply, the feedback loop asks for more power than the controller can deliver, and the CS setpoint reaches V_{ILIM}. When this event occurs, an internal t_{fault} timer is started: once the timer times out, DRV pulses are stopped and the controller is either latched off (latched protection, Version A), or it enters an autorecovery mode (Version B). The timer is reset when the CS setpoint goes back below V_{ILIM} before the timer elapses. The fault timer is also started if the driver signal is reset by the max duty ratio.

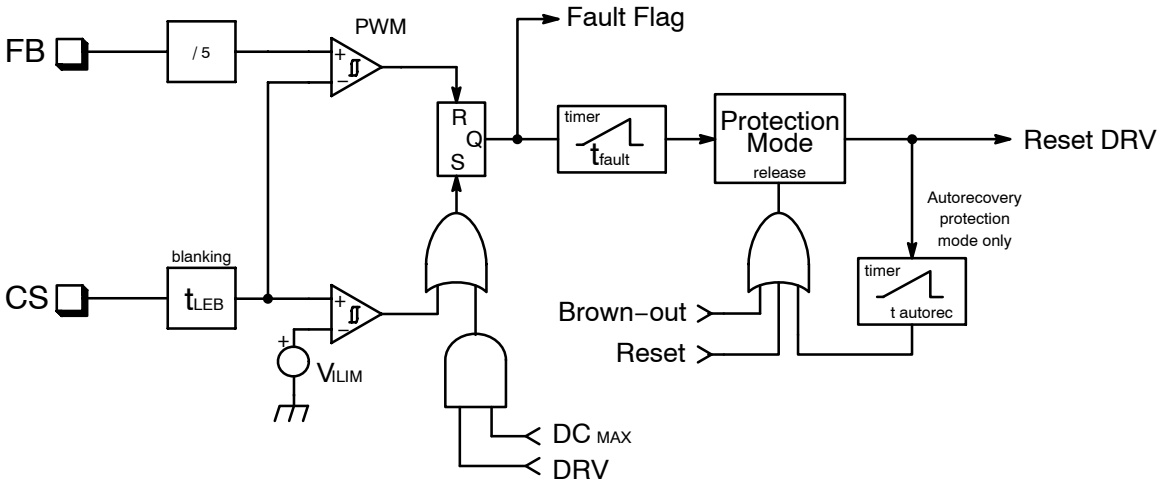


Figure 58. Timer−Based Overcurrent Protection

In autorecovery mode, the controller tries to restart after $t_{autorec}$. If the fault has gone, the supply resumes operation; if not, the system starts a new burst cycle (see Figure 59).

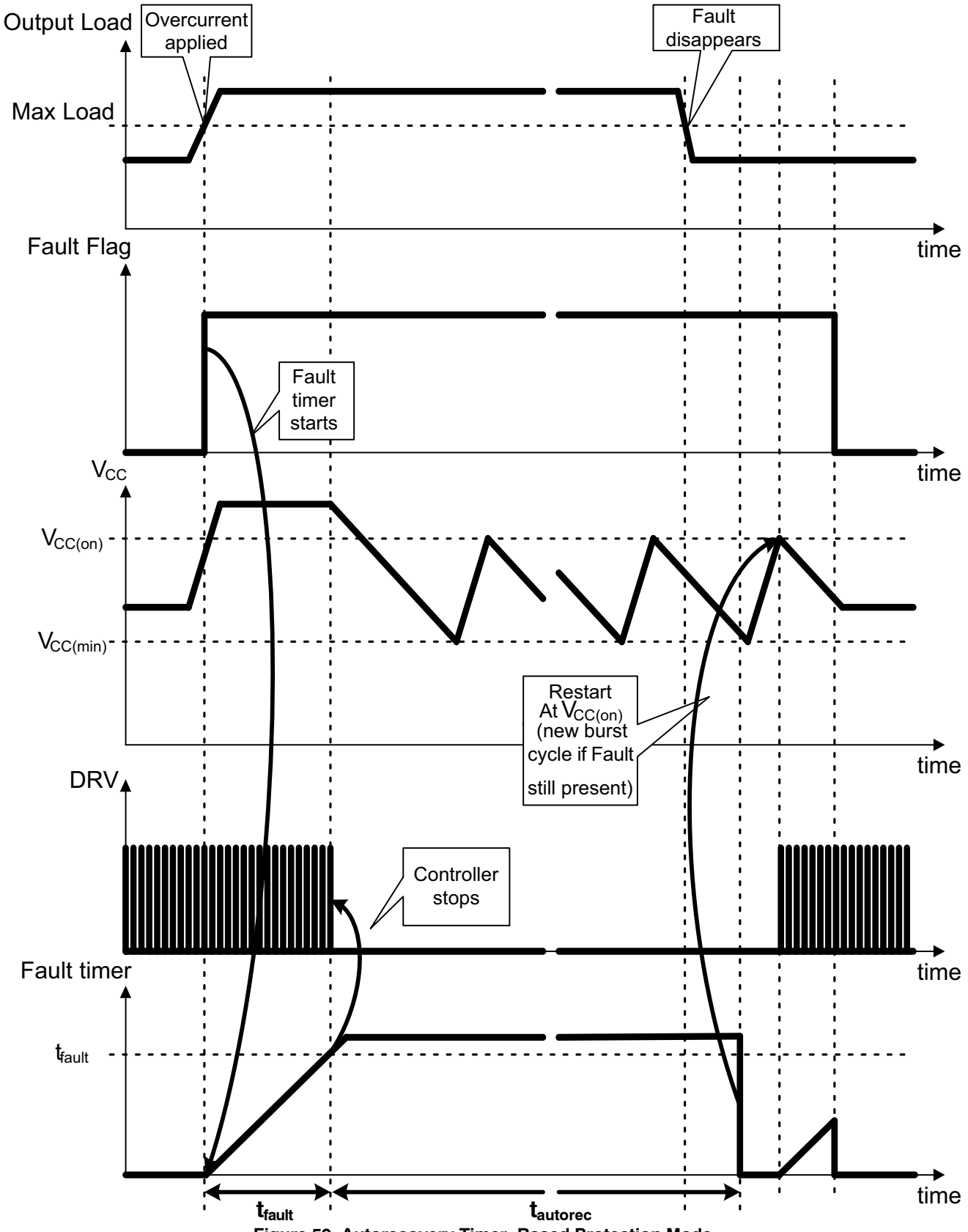


Figure 59. Autorecovery Timer−Based Protection Mode

In the latched version (Figure 60), the controller can restart only if a brown−out or a V_{CC} reset occurs. In a real application this can only happen if the power supply is unplugged from the mains line.

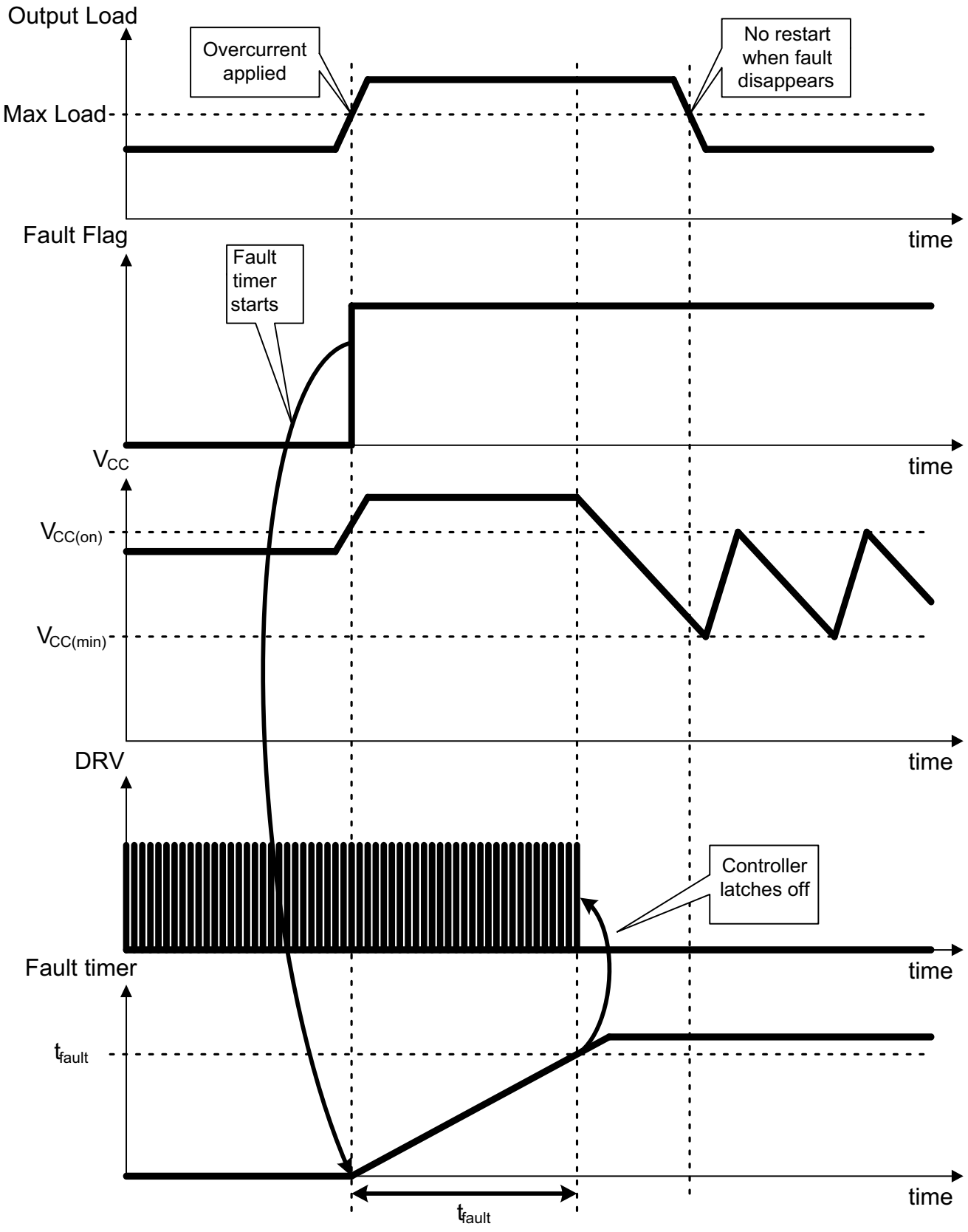


Figure 60. Latched Timer−Based Overcurrent Protection

Dual−Level Overcurrent Protection

For some applications (e.g. printer adapters), it is necessary that the controller maintains regulation while it has detected a first level of overload. This is to authorize a transient peak power higher than the maximum continuous output power.

This is implemented by adding another comparator whose threshold is $V_{CS(tran)}$, a CS voltage level lower than V_{ILIM}, which starts the charging of another timer, with a duration t_{tran} longer than t_{fault} (168 ms typical). If the timer reaches its maximum duration, the controller enters protection mode (latched or autorecovery depending on the option).

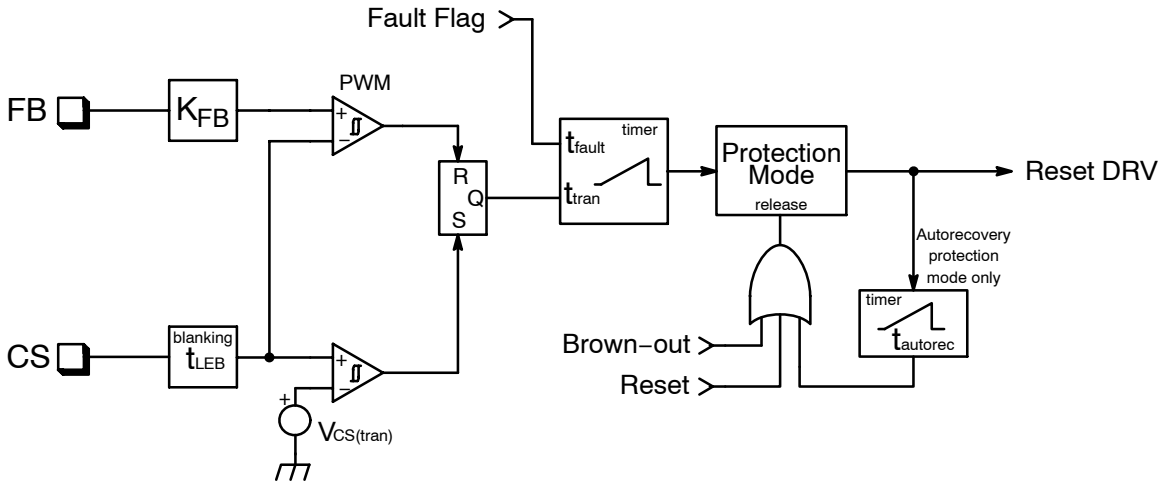


Figure 61. Dual−Level Timer−Based Overcurrent Protection

The typical level at which this transient peak timer starts is $V_{CS(tran)}$ = 0.5 V, which gives half the maximum output power in DCM.

The duration of the transient peak timer is t_{tran} (168 ms typical). Figures 62 and 63 show the operation of the transient peak timer in two different peak power conditions.

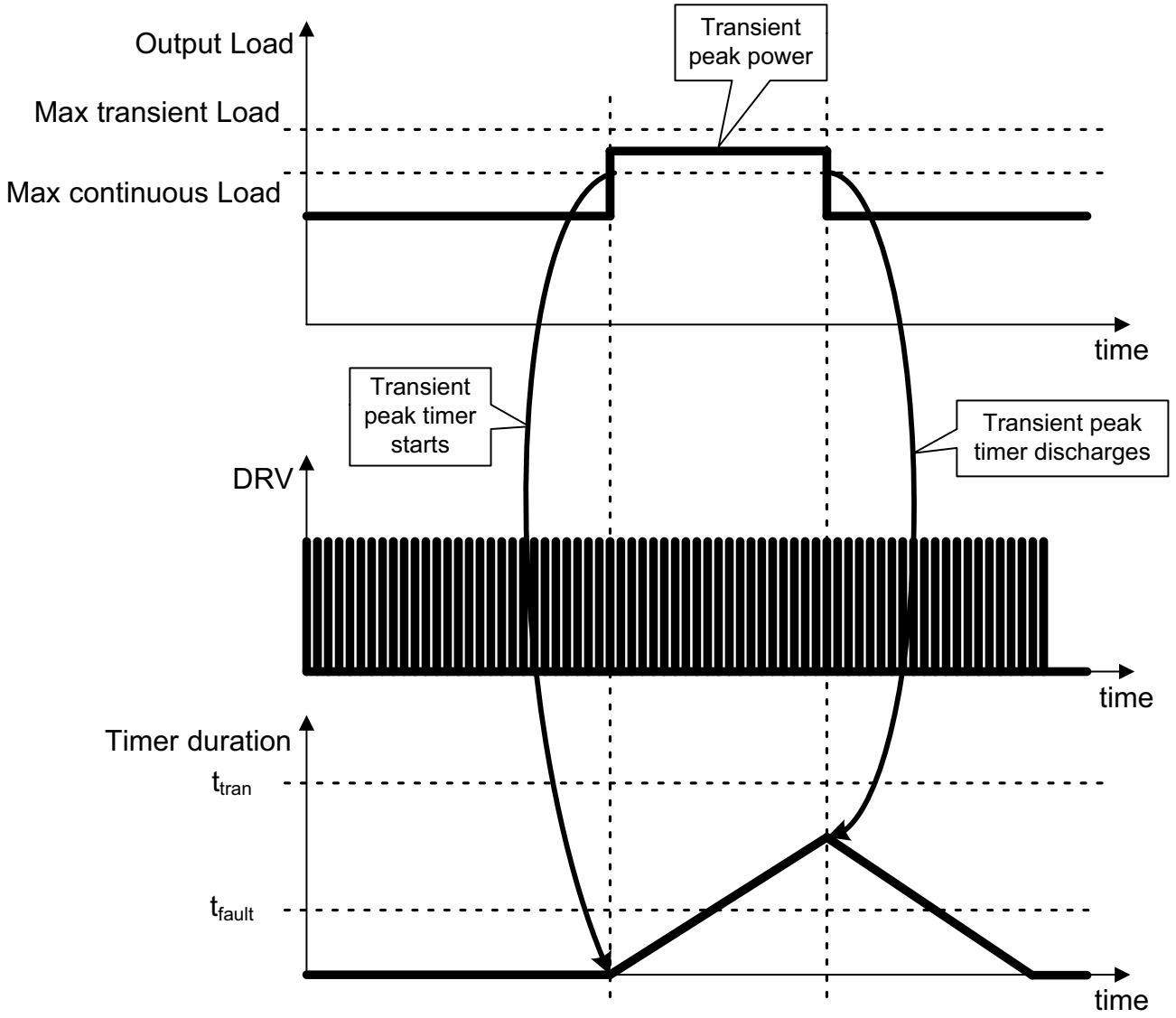


Figure 62. Transient Peak Power Delivery

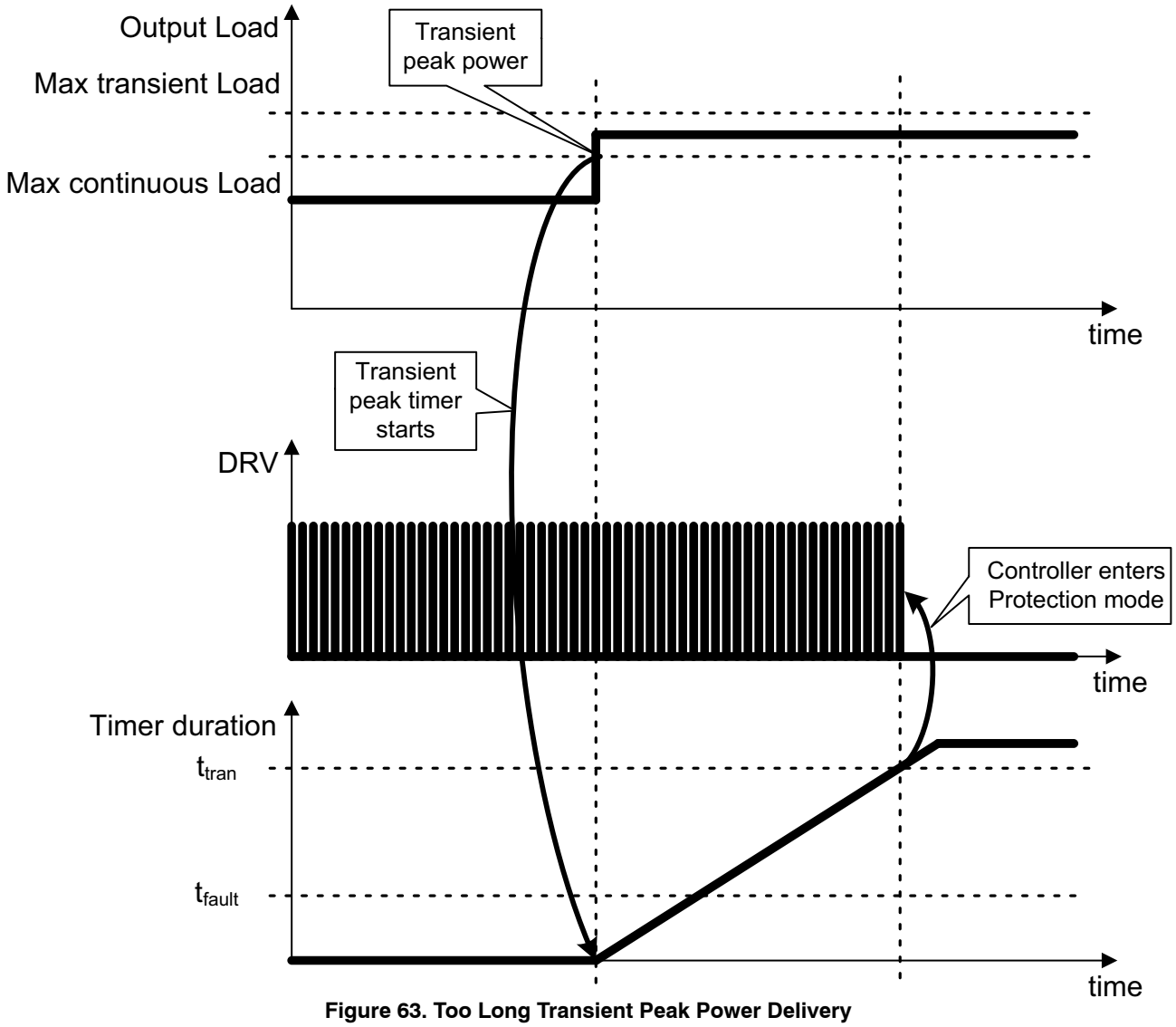


Figure 63. Too Long Transient Peak Power Delivery

LOW LOAD OPERATION

Frequency Foldback

In order to improve the efficiency in light load conditions, the frequency of the internal oscillator is linearly reduced from its nominal value down to $f_{OSC(min)}$. This frequency foldback starts when the voltage on FB pin V_{FB} goes below $V_{FB(fold)}$, and is complete before V_{FB} reaches $V_{skip(in)}$, whatever the nominal switching frequency option is. The current−mode control is still active while the oscillator frequency decreases, but the frequency jittering is off.

Note that the frequency foldback is disabled if the controller runs at its maximum duty cycle.

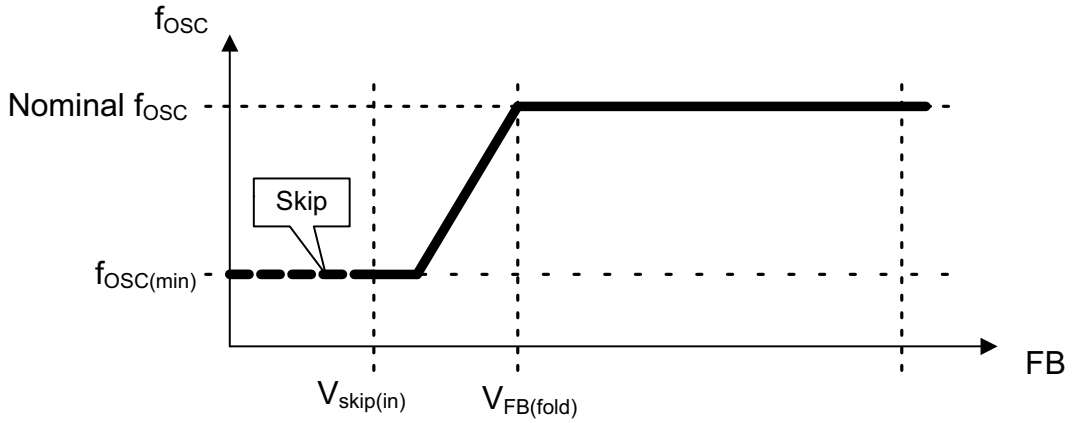


Figure 64. Frequency Foldback when the FB Voltage Decreases

Skip Cycle Mode with Soft−Skip

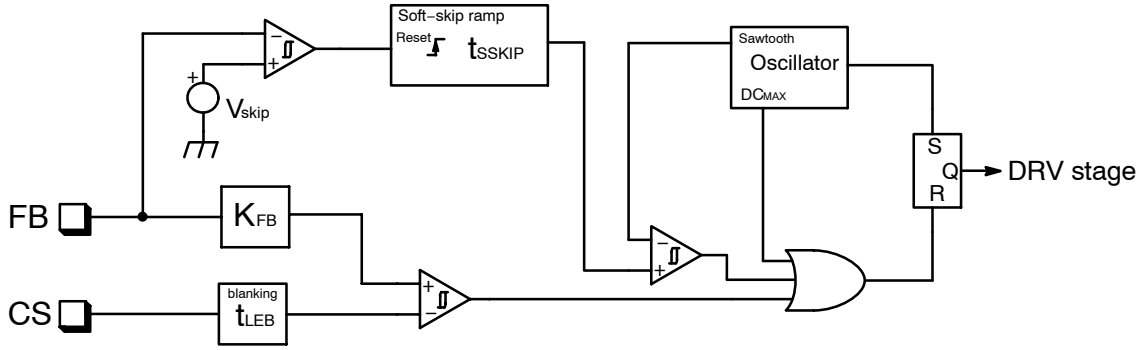


Figure 65. Skip Cycle with Soft−Skip Schematic

When V_{FB} reaches $V_{skip(in)}$ while decreasing, the skip mode is activated: the driver stops, and the internal consumption of the controller is decreased. While V_{FB} is below $V_{skip(out)}$, the controller remains in this state. When V_{FB} crosses $V_{skip(out)}$, the DRV pin starts to pulse again, and the controller restarts with a short Soft−Skip duration (t_{SSKIP}). The soft−skip imposes the peak current from nearly 0, in a voltage−mode manner: it doesn't have the same behavior as the startup soft−start which is current−mode driven.

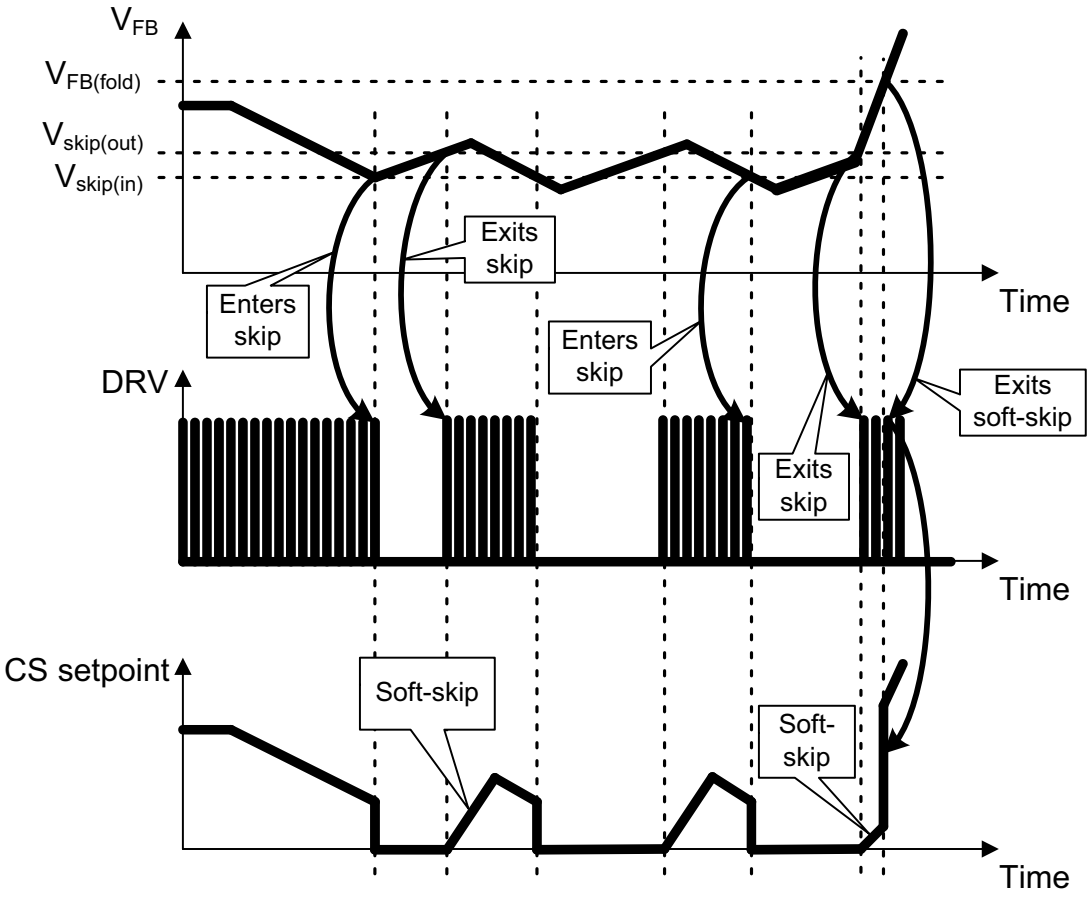


Figure 66. Skip Cycle with Soft−Skip Timing Diagram

If during the Soft−Skip duration the FB voltage goes above $V_{FB(fold)}$, the Soft−Skip ends instantaneously, and the peak current follows the setpoint imposed by the current−mode control. This transient load detection feature avoids large output voltage drops if a load transient occurs while the controller is in soft−skip mode.

Latch−off Input

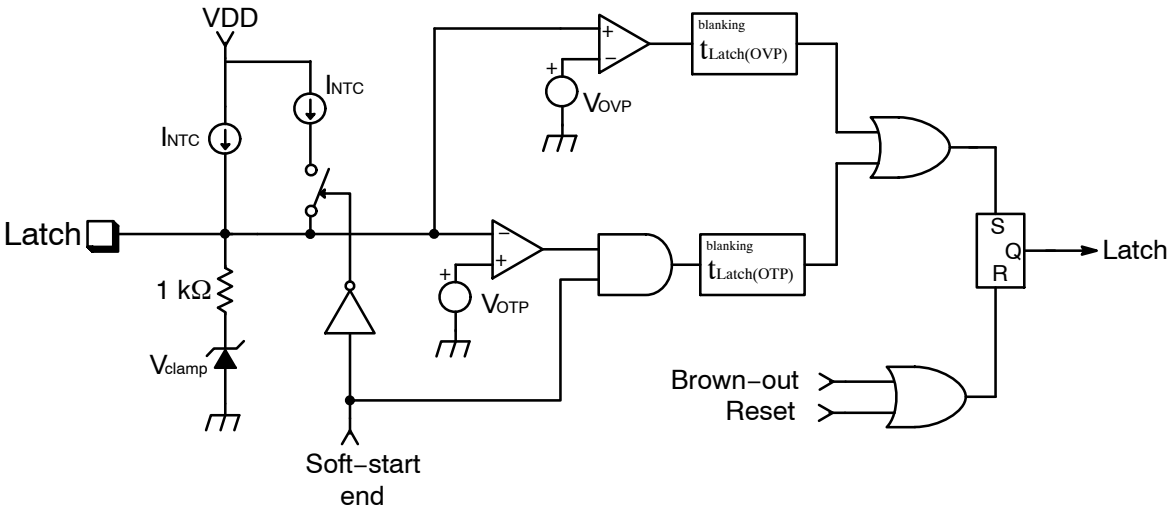


Figure 67. Latch Detection Schematic

The Latch pin is dedicated to the latch−off function. It includes two thresholds that define a working window, between a high latch and a low latch. Within these 2 thresholds; the controller is allowed to run; but as soon as either the low or the high threshold is crossed, the controller is latched off. The lower threshold is intended to be used with an NTC thermistor, with the internal current source I_{NTC} providing the necessary bias current.

An active clamp prevents the voltage from reaching the high threshold if it is only pulled up by the I_{Latch} current. To reach the high threshold, the pullup current has to be higher than the pulldown capability of the clamp (typically 1.5 mA at V_{OVP}).

To avoid any false triggering, noise spikes shorter than $t_{Latch(OVP)}$ or $t_{Latch(OTP)}$ respectively are blanked, and only longer events can actually latch the controller.

Reset occurs when a brown−out condition is detected or the V_{CC} is cycled down to a $V_{CC(reset)}$, which in a real application can only happen if the power supply is unplugged from the AC line.

Upon startup, the internal references take some time before reaching their nominal values; and one of the comparators could toggle inadvertantly. Therefore the internal logic ignores the latch signal before the controller is ready to start. Once V_{CC} reaches $V_{CC(on)}$, the latch pin High latch state is enabled and the DRV switching starts only if it is allowed; whereas the Low latch (typically sensing an overtemperature) is taken into account only after the soft−start is finished. In addition, the NTC current is doubled during the soft−start period, to speed up the charging of the Latch pin capacitor.

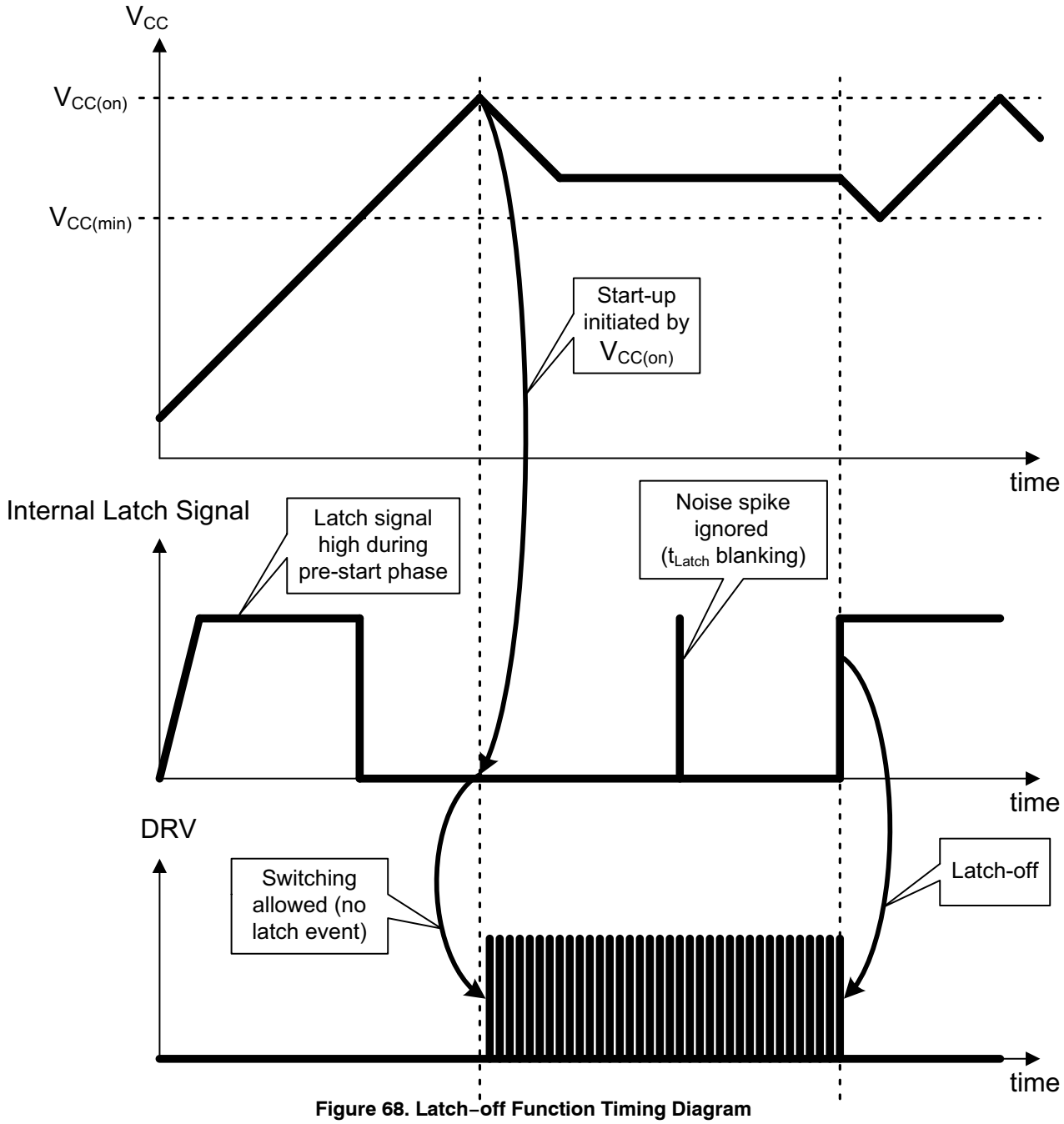


Figure 68. Latch−off Function Timing Diagram

Temperature shutdown

The die includes a temperature shutdown protection with a turn−off threshold guaranteed between 140°C and 160°C, and a typical hysteresis of 30°C. When the temperature rises above the high threshold, the controller stops switching instantaneously, the HV current source is turned off, and the internal logic state is reset.

When the temperature falls below the low threshold, the HV startup current source is enabled, and a regular startup sequence takes place.

STATE DIAGRAMS

HV Startup Current Source

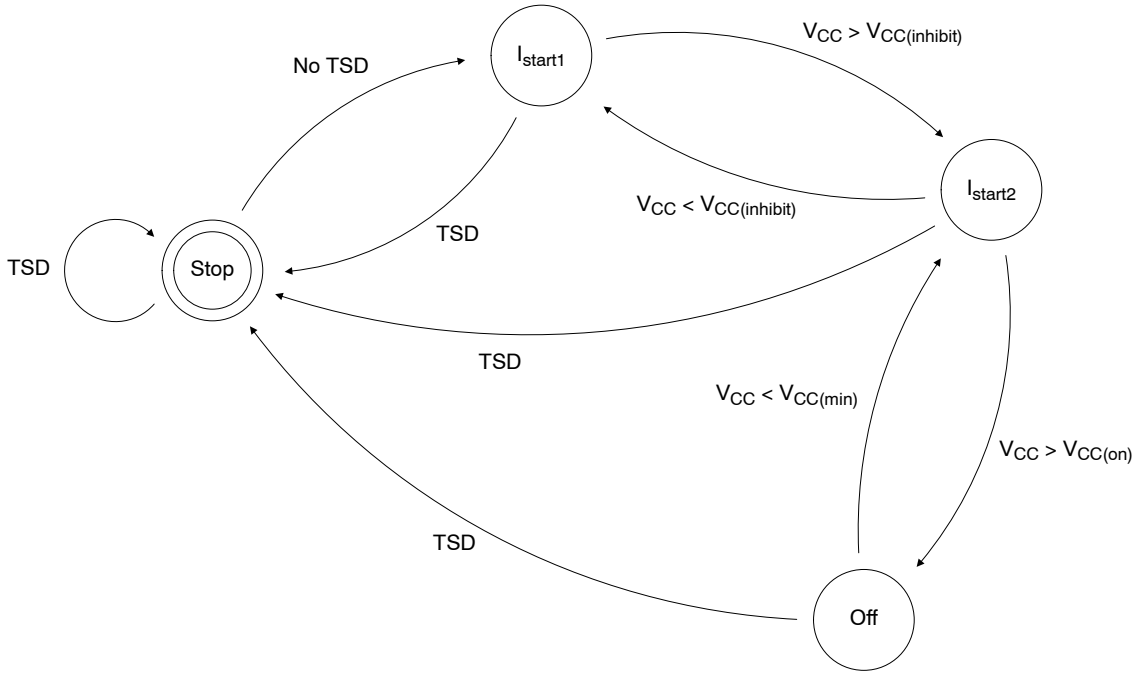


Figure 69. HV Startup Current Source State Diagram

Controller Operation (Latched Version: A Option)

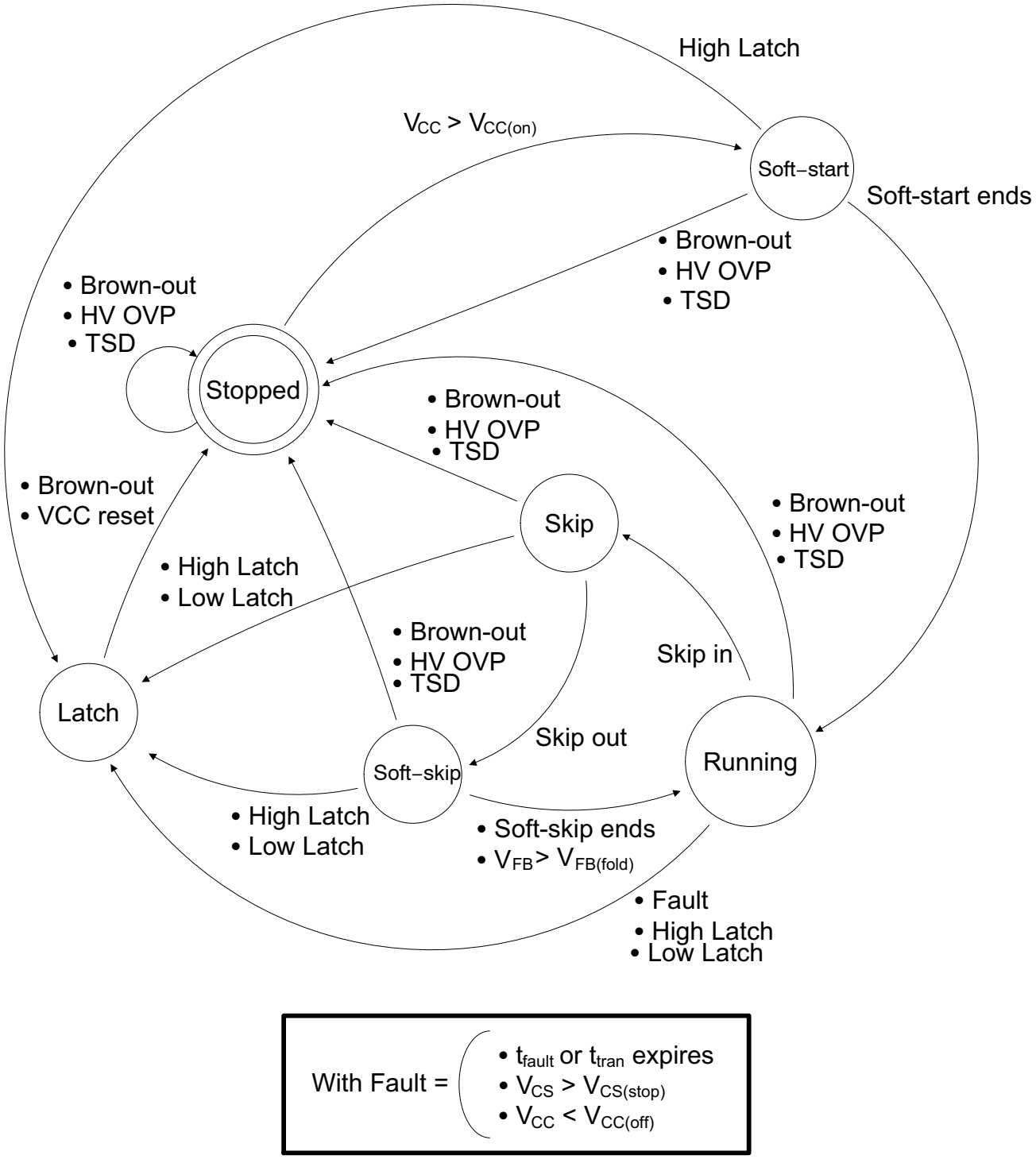


Figure 70. Controller Operation State Diagram (Latched Overload Protection)

Controller Operation (Autorecovery Version: B Option)

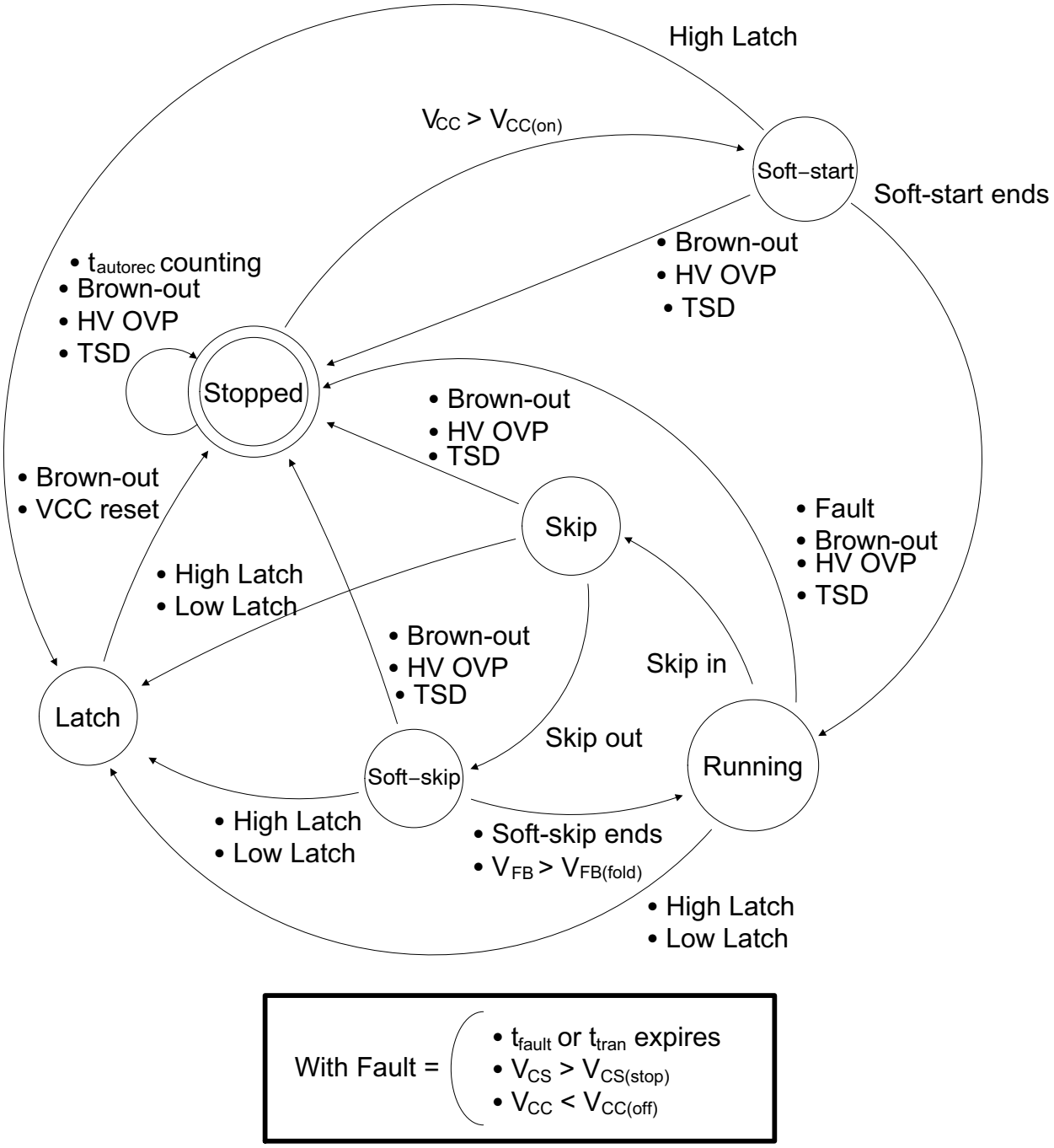


Figure 71. Controller Operation State Diagram (Autorecovery Overload Protection)

Table 1. ORDERING INFORMATION

Part No.	Overload Protection	Switching Frequency	Package	Shipping†
NCP1237AD65R2G	Latched	65 kHz	SOIC−7 (Pb−Free)	2500 / Tape & Reel
NCP1237BD65R2G	Autorecovery	65 kHz	SOIC−7 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Soft−Skip is a trademark of Semiconductor Components Industries, LLC (SCILLC).

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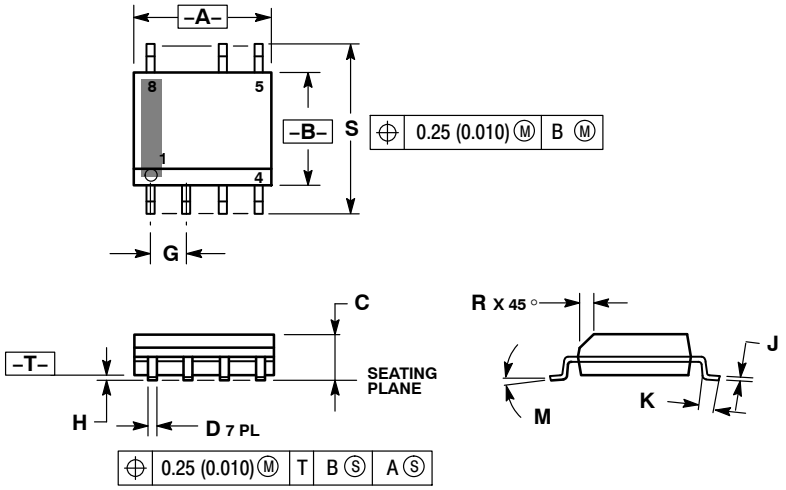
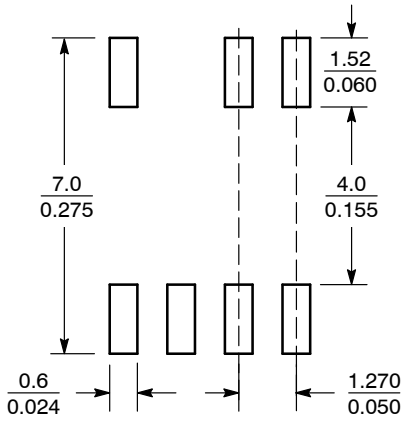
SCALE 1:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B ARE DATUMS AND T IS A DATUM SURFACE.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

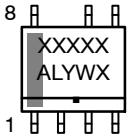
SOLDERING FOOTPRINT*



SCALE 6:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM



XXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb–Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, “G” or microdot “ ▪”, may or may not be present.

STYLES ON PAGE 2

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DATE 20 OCT 2009

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6.
7. NOT USED
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. NOT USED
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. NOT USED
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. NOT USED
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5.
6.
7. NOT USED
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6.
7. NOT USED
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. NOT USED
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR (DIE 1)
2. BASE (DIE 1)
3. BASE (DIE 2)
4. COLLECTOR (DIE 2)
5. COLLECTOR (DIE 2)
6. EMITTER (DIE 2)
7. NOT USED
8. COLLECTOR (DIE 1)

STYLE 9:
PIN 1. EMITTER (COMMON)
2. COLLECTOR (DIE 1)
3. COLLECTOR (DIE 2)
4. EMITTER (COMMON)
5. EMITTER (COMMON)
6. BASE (DIE 2)
7. NOT USED
8. EMITTER (COMMON)

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. NOT USED
8. GROUND

STYLE 11:
PIN 1. SOURCE (DIE 1)
2. GATE (DIE 1)
3. SOURCE (DIE 2)
4. GATE (DIE 2)
5. DRAIN (DIE 2)
6. DRAIN (DIE 2)
7. NOT USED
8. DRAIN (DIE 1)

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Email Requests to: orderlit@onsemi.com

ON Semiconductor Website: www.onsemi.com

TECHNICAL SUPPORT
North American Technical Support:
Voice Mail: 1 800−282−9855 Toll Free USA/Canada
Phone: 011 421 33 790 2910

Europe, Middle East and Africa Technical Support:
Phone: 00421 33 790 2910
For additional information, please contact your local Sales Representative

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